**Section II.A.Technical Motivation.Sharing the spectrum**

Despite existing in the center of the federally-defined, 13,000 square-mile “National Radio Quiet Zone”, radio frequency interference (RFI) from a variety of sources (satellites, ground-based RADAR, wireless consumer devices, etc…) is a continual plague upon the data quality at the Green Bank Observatory (GBO) and other radio astronomy observatories around the world. Due to the expanding presence of wireless devices in our lives, and the inevitable pervasiveness of self-driving cars relying on RADAR or similar active-RF methods for guidance, as well as the increasing sensitivity and bandwidth of astronomy receiver systems (and thus the total number of RFI detections per-second), GBO is actively pursuing methods of staying at the forefront of real-time RFI-excision techniques.

Due to limitations with existing hardware (comparatively low number of on-board resources such as block random access memory (BRAM), digital signal processing (DSP) cores, logic cells, etc…, comparatively low bandwidth I/O transceivers, as well as the relative difficulty meeting timing closure on the Virtex-6 compared to the current generation’s technology), we are not able to implement and test/qualify many promising RFI-mitigation techniques (ex. Spectral Kurtosis, Machine Learning). If we were to have access to more resource-rich, faster field-programmable gate arrays (FPGAs) with greatly increased numbers and speed of the on-board resources listed above, implementing and testing these methods would become possible.

In addition to developments in the number and speed of FPGA resources, there has been great developments in FPGA toolflows and related hardware that fundamentally changes the paradigm of what is possible. This includes expected but substantial improvements in achieving timing closure (accelerates design & deployment of firmware), cross-language programming (lowers the knowledge barrier for FPGA design & allows faster prototyping of conceptual DSP techniques), as well as revolutionary hardware developments such as the upcoming Xilinx Versal series artificial intelligence (AI) accelerator chips.

Having access to these new hardware and software platforms outlined in this document will enable the GBO to maintain or increase its position as a world-leader in spectrum-sharing technologies and methods.

**Section II.B.New Hardware**

The acquisition of new hardware will allow the GBO to make tremendous strides towards becoming truly a world-leader in the next generation of digital backend systems. As these newest generations of technologies become available, many levels of testing and qualification will need to be done to prove the efficacy of new designs that will inevitably lead to achieving levels of performance by traditional metrics (signal bandwidth, time-resolution, dynamic range) that are simply not achievable under our current hardware regime.

The evaluations that we do on different aspects of the cutting-edge hardware will be widely applicable to other interested observatories (and research institutions) in the national and international community. A small subset of expected investigations is listed below:

**New communication protocols and methods:**  
As GBO moves from IF-over-fiber with equipment room sampling to receiver-room sampling (at ~quintuple the bit-rate of previous instruments) with 100 Gigabit Ethernet (GbE) fiber downlinks to the equipment room as the backbone of our signal sampling/transmission pipeline, we will need to develop solutions to mitigate a plethora of predictable problems.

For example, the AD9213 analog-to-digital converter’s (ADC) (single-channel, 12-bits, 10GSPS) power dissipation is 5.1W, compared to the 10W maximum power dissipation allowed per the VME International Trade Association (VITA) 57 specification for the “FPGA Mezzanine Card” (FMC/FMC+) daughter card specification. Since each VCU118 (our target receiver-room development platform) contains only a single VITA 57-compliant connector with high-speed transceivers, we will likely need to either develop power-mitigation methods that would allow us to safely contravene the standards (allowing multiple ADCs per VCU118), or we would need to develop robust methods of cross-board ADC clock synchronization (single ADC per VCU118) to ensure that our dual-polarized samples are coherent. We will also then have to develop custom ADC boards that complies with our preferred method.

Continuing with the AD9213 as an archetype of the upcoming generation of ADCs, its’ total maximum bit-rate will be 12bitsx10GSPS=120Gbps. That is more than a single 100GbE port is capable of handling. With the majority of new Xilinx FPGA boards having only 2x100GbE ports (the VCU118 is an outlier with 2x100GbE QSFP28 ports and 1x100GbE FireFly port), we are in an age of technological development where the ADC bit-rates are growing faster than the I/O bandwidth of FPGA boards. This will spur examinations of optimal network topologies (1 or 2 polarizations per receiver-room board? 1 or 2 polarizations per equipment room board), 100GbE duplex (how comparatively large is the duplex logic to single-direction logic?), and other related questions that will allow us to maximize our system’s throughput bandwidth while minimizing system cost and complexity.

A new trend among FPGA board designers is to include a PCIe edge-connector on the newest boards (while also eliminating the 1GbE port that we have used for FPGA-related monitor & control functions in previous designs). This trend will require us to integrate PCIe-based monitor and control functionality, and to measure how different bi-directional monitor & control data-rates between the host computer and the FPGA over the PCIe bus effect the main, uni-directional data-transfer rates from the FPGA to the host computer.

**RFI-shielding & Cooling:**   
As an inherent feature of transitioning toward receiver-room signal sampling, we will need to install (relatively) large, digitally noisy electronics in an environment that mandates minimal power consumption and a low-level of emitted radio-frequency emissions.

At the GBO, all installed electrical equipment in the receiver room is required to be ITU-R RA.769 compliant (protection criteria used for radio astronomical measurements), whereas equipment in typical commercial applications in the United States is only required to be 47 C.F.R. 15 Class A compliant. Functionally, this equates to GBO being responsible for providing an additional ~100dBm of isotropic radiated power suppression to any commercial-off-the-shelf (COTS) unintentional radiators that we wish to install close to the focal point of the GBT.

To meet these strict requirements (and limit unwanted perturbations of the yet-to-be sampled data), GBO will likely have to make considerable adjustments/shielding to the hardware of any COTS boards (such as the VCU118) that are placed there. This is something that the GBO has considerable expertise and experience designing and implementing. Suppression methods that we have used previously on COTS equipment include component-level shielding of ‘noisy’ components (chip cage) & equipment-level shielding (metal box, in-case RF absorbent foam). We also have considerable experience designing low-radiation electronics, and an excellent RF anechoic chamber to validate our modifications.

However, many RFI-shielding techniques (encasing boards within metal boxes) works to cross-purposes with effective cooling techniques. As such, GBO will also be developing efficient and simple cooling methods (air-cooling is given priority due to its’ simplicity, but water-cooling will be considered if necessary).

All RFI-shielding and cooling techniques used at GBO will be broadly applicable to any observatory interested in using the VCU118 or similar.

**Section II.B.Firmware Development**

In light of the variety of new hardware that GBO intends to base future digital backend systems on, a variety of new firmware ‘blocks’ (sets of low-level FPGA code abstracted to a higher level for easier use by firmware system designers) will need to be developed for interfacing with various FPGA-facing peripherals as well as for executing advanced DSP techniques. In addition, new firmware ‘tools’ may need to be developed to allow our CASPER-based designs to take advantage of the totality of hardware advancements that are provided by Xilinx Ultrascale+ and later technologies. Much of this new firmware development can be compartmented into functional blocks within Xilinx’s Embedded Developer’s Kit (EDK) architecture. ‘Basic EDK blocks’ are primarily blocks dedicated to data processing with no use of peripheral components (BRAM, transceivers, Microblaze access, etc…), whereas ‘CASPER EDK blocks’ interface with peripherals. Many of the CASPER EDK blocks exist for earlier generations of hardware, but considerable work is required to prepare them for the newest generations. A discussion of prospective developments is provided below:

To take advantage of the possibilities enabled by the newest generation of data-transmission technologies, GBO intends to create CASPER EDK blocks that interface with the 100GbE core (both single-direction and duplex flavors), PCIe (generations 3x16 and 4x8 – including monitor and control of the FPGA board over the PCIe), as well as a block to interface the FPGA with our custom ADC cards via the FMC/FMC+ slots on the VCU118. The 100GbE blocks and ADC card block can be considered improvements upon existing capabilities, while the PCIe interface (and especially the monitor and control aspect) will be groundbreaking in the CASPER community.

In addition to the new functional blocks listed above, GBO will create additional blocks (basic EDK) to improve our digital signal processing (DSP) capabilities. For example, we intend to develop blocks implementing new RFI-mitigation methods (discussed in more detail in the “Active RFI-Excision” section) that are too computationally expensive to run in real-time under our current hardware regime. These developments can largely be considered (with the exception of Machine Learning) translations of algorithmic implementations from python notebooks to hardware descriptive languages (HDL).

The two above paragraphs largely address what we must do to harvest the expected fruits of Moore’s law (higher-speed data transmission, higher-density FPGA chips), but Xilinx has also made great developments in some less obvious directions. In recent years, their focus has widened to include heterogeneous computing architectures such as the Manycore Processor System on Chip (MPSoC), Radio Frequency System on Chip (RFSoC), and the Adaptive Compute Acceleration Platform (ACAP).

While all of these advancements open up new, exciting horizons of system and DSP design, the most exciting possibilities are enabled by the Xilinx ACAP architecture (upcoming chip series is named Versal). These chips are heterogeneous devices, combining the generality and accessibility of CPUs, the vector processing power of GPUs/DSPs, the IO/memory bandwidth and adaptability of FPGAs, and integrated ADCs and digital-to-analog converters (DACs) suitable for commercial 5G applications. Subsets of these chips were developed with the deployment of real-time neural-network based machine learning (ML) as the targeted applications (upcoming native integration between the Xilinx chips and common ML suites such as Caffe or TensorFlow via an application overlay through Xilinx’s Vivado has been announced). A broader discussion of ML possibilities is provided in the “Active RFI-Excision” section.

With such a wide variety of advancements being exhibited in the Versal series, the depth and breadth of possible firmware developments required to take advantage of the full suite of improvements is quite large. CASPER EDK blocks could be developed to interface the scalar processing, vector processing and programmable logic portions of the chip – this will enable acceleration of our DSP algorithms and a faster and less intrusive monitor and control methodology for the board compared to the current CASPER standard of interfacing via a soft-core Microblaze processor.

Additionally, while the ADCs that are integrated with the ACAP may be too slow for the high-bandwidth, high time-resolution requirements of many upcoming radio astronomy instruments, possessing integrated, high-speed DACs (Xilinx’s integrated DACs have so far been significantly faster than their ADCs) will allow us to improve our ability to perform full-system tests – this would not only accelerate our design-to-deployment cycle, but would also allow more robust, realistic, and real-time evaluation of future algorithms. Thus, creating CASPER EDK blocks that would interface the ADCs/DACs with the toolflow would enable improved test methodologies, and the use of the ADCs (lowering the system-cost for systems where the speed is acceptable).

Finally, developing a methodology for tying together Xilinx’s upcoming ML application overlay with the CASPER toolflow will enable the implementation of real-time ML algorithms for applications such as transient detection and RFI-mitigation.

**Section II.B.Active RFI-Excision**

As mentioned in section II.A, the GBO is committed to continuing in its role as a world-leader in spectrum sharing. To that point, a survey of current RFI-excision/suppression techniques under development or consideration at the observatory is provided below.

**Impulsive RFI-Mitigation (Robust Recursive Power Estimator):**  
Initially conceived by Cedric Viou at Nancay Observatory as a method for detecting and eliminating interference from ground-based RADAR sources (but could be applicable to other RFI sources) – it functions by measuring the mean power level (in the frequency domain) and flags/replaces sets of samples that exceed a given threshold above the power level for a given amount of time (detection is based both on power and duration of the pulse). The GBO digital group has now implemented this functionality in firmware, and has implemented it in multiple backend systems currently being used on-site at Green Bank. Testing is currently underway, but our ability to validate its effectiveness (and to have it become accepted by the wider astronomy community at large) is severely hindered by a lack of formal validation plan like the one outlined above. To the best of our knowledge, GBO currently possesses the only CASPER-implemented real-time RFI-excision enabled backend systems.  
Source: https://arxiv.org/pdf/1703.00473.pdf

**Spectral Kurtosis:**Initially conceived by Gelu Nita at the Center for Solar-Terrestrial Research at New Jersey Institute of Technology as a robust statistical RFI-detector, the simple sum/sum-squared algorithm works by measuring the kurtosis of given sample sets. As kurtosis measurements are more affected by a few, extreme outliers rather than many, moderate outliers, we can assume that any high-kurtosis samples (above user-adjustable thresholds) are contaminated with RFI and are mitigated. Over the past year, a collaboration between the GBO digital engineering group and West Virginia University Physics department have created a python-based implementation of the “Generalized Spectral Kurtosis Estimator” (Source 1). Our current implementation is not real-time, and has been designed specifically to operate on archived (and extensively analyzed) Green Bank Ultimate Pulsar Procesing Instrument-RAW (GUPPI-RAW) data files (high time-resolution, world-class, CASPER-based pulsar backend system at Green Bank) – its overall effectiveness has been proven. However, none of our extant backend systems have enough logic/DSP cores/RAM resources available in the FPGA chips to allow an implementation of Spectral Kurtosis to co-exist with the existing channelization firmware that currently occupies ever-growing percentages of the available resources on our current hardware. Acquisition of newer FPGAs with 3x-5x more logic/DSP cores/RAM resources would enable us to create and test a real-time implementation of this method that could then be shared with the wider community.

Spectral Kurtosis has also been identified as a promising method for the detection and classification of extra-terrestrial transient signals (source 2). Given the currently high level of excitement surrounding Fast Radio Bursts (FRBs), and the GBT’s prowess at detecting them, harnessing the power of ever more subtle and effective transient-detection methods will likely prove to be the key to solving many astronomical mysteries.  
Source 1: <https://arxiv.org/pdf/1005.4371.pdf>  
Source 2: https://doi.org/10.1142/S2251171716410099

**Machine Learning:**Machine learning is subset of artificial intelligence who’s applicability and accessibility has increased dramatically in recent years. In response to industry trends, Xilinx has recently taken steps to optimize their hardware (see previous discussion of ACAP/Versal/AI integration) and software - to the point where ML algorithms can now be ran faster and developed much easier than in the recent past. The Xilinx ML-suite is also compatible with the Alveo-series chips, but the Versal series is advertised as being intentionally optimized for such applications.

While there have been some promising investigations into Machine Learning’s applications to the astronomical community in areas such as RFI-detection (Source 1), source classification (Source 2), and transient-detection (Source 3), a concerted effort to create a validated, real-time algorithm, or to even publish an open-source dataset for training and testing a model to our specifications has yet to come to fruition. As part of our goal to maintain our position as a world-leading observatory in spectrum sharing, GBO intends to utilize the new Xilinx’s new hardware and software advances in concert with the datasets outlined in the “Standardized Excision Validation Procedure” section below to bring real-time Machine Learning applications to life in the astronomical community.  
Source 1: <http://hdl.handle.net/10019.1/98464>  
Source 2: <https://arxiv.org/pdf/1705.03413.pdf>  
Source 3: http://blpd0.ssl.berkeley.edu/frb-machine/CNNFRB\_eprint.pdf

**Standardized Excision Validation Procedure:**

Such a methodology would likely include a list of types of observations (pulsar coherent de-dispersion, pulsar incoherent de-dispersion, transient searches, spectral line, etc…) – each with a set of detectable parameters of the observed source that are of interest for each observation type (pulsar period, dispersion measure, spectral line strength, polarization relationship, etc…). We would also have to generate a list of RFI characteristics (amplitude, bandwidth, duration, frequency sweep, etc…).

Once this list of observation types and parameters has been created, we could generate (or create, from previously observed data – or a mixture of the two) a series of canonically representative, RFI-free spectrograms (all RFI-mitigation strategies currently under investigation by GBO occur post-channelization) that encapsulate as broad of a representation of the possible combinations of the types of observations and detectable parameters as we can (depending on if we generate vs create, the number of spectrograms could range from hundreds of thousands to hundreds).

At this point, we will have the parameters to measure, and a set of RFI-free spectrograms, the next step would be to use our list of RFI characteristics to methodically inject various RFI patterns into the RFI-free spectrograms to create RFI-spectrograms. Each RFI-free spectrogram would need to be injected with multiple RFI patterns (both at once, and recursively) – this method could conceivably result in us generating significantly more RFI-spectrograms than RFI-free spectrograms.

Once we have generated a large set of both RFI-spectrograms and RFI-free spectrograms (there will be examples of both without any astronomical sources), we can send them all through the RFI-mitigation algorithms and measure not only the success/failure (especially false-positive) rate of detecting RFI, we can also use them to determine the extent to which the different mitigation techniques affect the underlying astronomical data.

This large dataset (and the mechanism behind producing it) could also obviously be used as a training/test set for training/testing Machine Learning implementations of RFI-mitigation.

The limits for acceptable amounts of non-detections, false-positives, and signal perturbations can either be determined by GBO before the commencement of the larger validation procedure, or can be determined after we have a better understanding of the nuanced effects of our mitigation methods. In either case, it is likely that these limits will be somewhat fluid – the limits could tighten when mitigation techniques improve or when high-sensitivity observations are taking place, and could loosen as the data rates from receivers improve and the RFI-conditions in the area of the GBO worsen.

Regardless of the difficulties that such a plan would entail, it is GBO’s view that such a plan is of paramount importance to ensure the integrity of our scientific products moving forward. All data generation methods, sample spectrograms, detection limits and, perturbation limits arrived at by GBO could then be made publicly available for the benefit of the wider community.

A similar methodology and dataset (or maybe a subset of the larger dataset mentioned above) could also be developed and used to evaluate transient-detection and classification algorithms and methods.