

3. Watch the video at <https://www.youtube.com/watch?v=dX9CGRZwD-w> and answer the following questions. This content creator is fabulous, and it is highly suggested to watch other videos as you get time! (a) (1/2 point) Within a CPU what are the metal wires called? (b) (1/2 point) How many layers of wires are in a CPU? (c) (1/2 point) How many CPU chips fit on a 300mm silicon wafer? (d) (1/2 point) What does FOUP stand for? (e) (1/2 point) How long does it take to manufacture a single chip? (f) (1/2 point) What factor is the pattern shrunk by in the photolithography machine? (g) (1/2 point) What is a purpose of metrology tools? (h) (1/2 point) How thick are the 300mm diameter wafers?

(a) Within a CPU what are the metal wires called? (½ point)

Answer: Interconnects

From the transcript: *"Zooming in even further, we see layers of metal wires, or interconnects, and at the very bottom are the transistors that form the basic logic gates."*

(b) How many layers of wires are in a CPU? (½ point)

Answer: 17 layers

From the transcript: *"In actuality there are a total of 17 metal layers of wires in the CPU, and each successive set of levels uses larger and larger interconnects."*

(c) How many CPU chips fit on a 300mm silicon wafer? (½ point)

Answer: 230 CPUs

From the transcript: *"This CPU is manufactured on a 300-millimeter silicon wafer which can fit 230 CPU chips."*

(d) What does FOUP stand for? (½ point)

Answer: Front Opening Universal Pod

From the transcript: *"These silicon wafers are carried in stacks of 25 using a container called a front opening universal pod, or foup."*

(e) How long does it take to manufacture a single chip? (½ point)

Answer: 3 months

From the transcript: *"Within this microchip factory, silicon wafers travel from machine to machine and undergo around a thousand processes over a 3-month period."*

Also confirmed: *"To build the entire chip composed of 80 different layers it takes 3 months of traveling from tool to tool where at each stop one of the 940 process steps is completed."*

(f) What factor is the pattern shrunk by in the photolithography machine? (½ point)

Answer: 4 (or 4x reduction/factor of 4)

From the transcript: *"After the light passes through the photomask, the UV light goes to more lenses in order to shrink down the pattern by a factor of 4 and print a single layer of the design onto the photoresist."*

(g) What is a purpose of metrology tools? (½ point)

Answer: To inspect for defects and ensure nanometer-level precision / To take pictures of the wafer surface and determine if there are defects

From the transcript: *"And finally, sixth are tools that inspect the transistors and metal layers for defects and are called metrology tools. A common metrology tool uses a scanning electron microscope with nanometer-level resolution to take pictures of the top surface of the wafer and determine if there are defects such as improperly patterned layers or particles on the surface."*

(h) How thick are the 300mm diameter wafers? (½ point)

Answer: Three-quarters of a millimeter (or 0.75 mm / ~775 micrometers)

From the transcript: *"For reference, these 300-millimeter wafers are around three-quarters of a millimeter thick, they have a barcode on the side and a small notch in them to indicate the direction of the crystal lattice."*

BELOW: AI transcription of video- <https://www.youtube.com/watch?v=dX9CGRZwD-w>
Via : <https://youtubetotranscript.com/transcript?v=dX9CGRZwD-w>

Inside this smartphone are 62 microchips containing a total of 90 billion transistors. These microchips are incredibly powerful and the cornerstone of all technology, but how are billions of nanoscopic transistors manufactured into a microchip the size of a tiny ant? Well, all these microchips were manufactured in a semiconductor fabrication plant like this one. Inside it is a clean room which spans the area of 8 football fields and is filled with hundreds of machines ranging in size from that of a van to that of a city bus and costing anywhere between a few million and 170 million dollars. Within this microchip factory, silicon wafers travel from machine to machine and undergo around a thousand processes over a 3-month period. And, by the end of production, each silicon wafer will be covered in hundreds of CPU chips each containing 26 billion transistors. When we zoom in we can see the nanoscopic transistors at the bottom and over a dozen layers of wires above. This integrated circuit is then cut out from the wafer, tested, and packaged so that it can be installed into your desktop computer. In this video we're going to explore the entire microchip manufacturing process and show you how billions of nanoscopic transistors and an impossibly complex 3D maze of wires are manufactured in one of the world's most technologically advanced microchip factories. It's an incredibly complicated process, so stick around and let's jump right in! A portion of this video is sponsored by Brilliant.org. There are two sides to understanding how microchip manufacturing works. The first is the sequence of steps and processes needed to build the nanoscopic transistors and the labyrinth of wires. Whereas the second is how the semiconductor fab and multimillion dollar equipment on the cleanroom floor work, and we'll be flipping between these two sides to get a complete picture. Let's start by opening up this desktop computer, focusing on the CPU and taking a look at what's inside. Here we have an integrated circuit, or die, which we'll refer to as a chip. This chip has 24 cores, a memory controller, a graphics processor, and many other sections. Within one of the cores, we can see its block diagram and the various elements. Zooming in on this multiply block, we find a layout of 44 thousand transistors that physically execute 32-bit multiplication and constitute just point zero zero zero one seven percent of the overall 26 billion transistors in the CPU. Zooming in even further, we see layers of metal wires, or interconnects, and at the very bottom are the transistors that form the basic logic gates. Note that these layers of metal interconnects aren't floating, but rather, the empty space that you see is filled with insulating materials, thus providing structure, and preventing the metal wire layers from touching. Furthermore, here we're only showing the transistors at the bottom and five layers of metal interconnects with vias traveling vertically between the layers. In actuality there are a total of 17 metal layers of wires in the CPU, and each successive set of levels uses larger and larger interconnects. At the bottom are local interconnects that move data around this 32 bit multiply circuit. In the middle are intermediate interconnects that move data around the core, and at the top are global interconnects that move data around the entire CPU. You might be wondering how small are these transistors? Zooming in again and past the interconnect layers we find FinFets, which are transistors whose channel dimensions are 36 by 6 by 52 nanometers with a transistor to transistor pitch of 57 nanometers. Clearly the transistors are incredibly small. Here's a mitochondria, a dust particle, and a human hair for size comparisons. Now that you have a sense of what the transistors and labyrinth of metal interconnects look like, let's explore how they're manufactured. We'll begin with an analogy. Imagine baking a cake that's 80 layers tall, with each layer cut to a unique shape. To make this cake there are 940 steps in the recipe, which takes 3 months to complete and includes hundreds of exotic ingredients. And, if any

measurement, baking time, or temperature is more than one percent off, then the cake is entirely ruined. That's kind of what it's like to make a microchip, but microchips are even more complicated. Let's look at a single layer of this integrated circuit and run through a simplified set of steps used to build it. To start, a layer of insulating silicon dioxide is deposited on top of the wafer and then a layer of light sensitive photoresist is spread across the top. Next, using UV Light and a stencil, a pattern is applied to the photoresist. Solvents then are used to remove the areas hit by the UV light, thus creating a patterned mask layer. Using the mask, the revealed silicon dioxide is etched away down to the previous layer. Next the mask layer is removed, and a layer of copper is added to cover the wafer and fill in the areas that were just etched away. Finally, the surface is ground down and leveled off to reveal the copper and insulator patterns. And thus, a single layer is completed. In order to build the next layer, which is a vertical set of metal vias, we repeat the same set of steps, but use a different pattern for the photomask. Since these layers are all built using the same set of steps it's more effective to visualize the steps as a circle like a clock. To build all the 80 layers of the die, this sequence is repeated over and over, resulting in 940 steps. One important note is that the FinFet transistors at the bottom are even more complicated than the metal wires, and thus additional steps are needed to fabricate them. Furthermore, cleaning the wafer to wash away dust particles that may have landed on the wafer, as well as inspecting the wafer to make sure everything is being built properly, happens frequently and these steps need to be added to the circle. A different tool is used to complete each of these process steps. . Now that we have an understanding of the steps, let's take a look at this semiconductor fabrication plant. This CPU is manufactured on a 300-millimeter silicon wafer which can fit 230 CPU chips. In contrast DRAM chips are considerably smaller and thus 952 of them can fit on a wafer. These silicon wafers are carried in stacks of 25 using a container called a front opening universal pod, or foup. This sealed plastic wafer carrier is transported around the cleanroom floor using an overhead transport system which lowers the foup onto the tool's landing pad. Inside the tool, robotic arms transport the wafer through vacuum load locks and to different process chambers where materials are added, removed, or processed in ways that we'll explore later. The wafers are then returned to the foup, resealed inside, lifted up to the overhead transport system, and carried to and dropped onto the next tool, where the next step in the process is completed. To build the entire chip composed of 80 different layers it takes 3 months of traveling from tool to tool where at each stop one of the 940 process steps is completed. In order to increase the microchip mass production capabilities of a semiconductor fabrication plant or fab, typically there are dozens of the same semiconductor tools organized in rows that perform the same process. On the cleanroom floor there are a total of 435 semiconductor tools resulting in the fab's production capacity of 50,000 wafers or 11.5 million CPUs a month. These tools have rather complicated names, so we'll start by categorizing them according to their functionality. There are 6 groups: making the mask layer, adding material, removing material, modifying the material, cleaning the wafer, and finally inspecting the wafer. We've color coded the different functional groups to the various tools and process steps to help you not get lost. Let's next look at each of these semiconductor tools and see how they process the wafer in various ways. We'll start with the ones that are used to make the mask layer or the nanoscopic stencil on the wafer. These tools include the photoresist spin coater, photolithography tool, developer and photoresist stripper. First the photoresist spin coater applies a light-sensitive layer to the surface of the wafer and sends it through a soft bake where

the wafer is heated in order to evaporate the solvent from the photoresist. Next the wafer goes to the lithography tool which shines UV light through a stencil, which is technically called a photomask. The light passes through the stencil and is then demagnified or shrunk down to produce a nanoscopic pattern on the wafer. Wherever the light from the stencil touches the wafer, the photoresist is weakened. The wafer then goes to the developer and the weakened photoresist is washed away, leaving only the patterned nanoscopic stencil on the wafer. The wafer is then sent through a hard bake to harden the remaining photoresist. Next the wafer travels to other tools to undergo processing, and once these processes are completed the wafer goes to a photoresist stripper which uses solvents to dissolve and remove the photoresist mask layer. And that's how a mask layer is formed and then removed. The photolithography tool is one of the most important, so let's take a look at it. Inside is a UV light source, a set of lenses to focus the light, a photomask which contains the stencil, or design of the layer to be patterned, and a wafer carrier. The photomask is 6 by 6 inches, and, based on the dimensions of the CPU, can fit 2 copies of a single layer of the CPU design. The purpose of using a photomask with these crazy optics is because it's a reliable way to copy and paste a design for billions of nanoscopic transistors and wires onto 230 identical CPUs on a single wafer in a few minutes. After the light passes through the photomask, the UV light goes to more lenses in order to shrink down the pattern by a factor of 4 and print a single layer of the design onto the photoresist. The wafer carrier steps from position to position, printing the photomask image at each stop, until all 230 chips are patterned. Let's clarify one detail. In our previous examples, we talked a lot about this CPU having 80 layers. Specifically, what we were referring to is the number of photomasks and mask layers used to create all the different layers of patterns on the wafer. Therefore, one complete CPU chip uses 80 different photomasks, each costing 300,000 dollars. With only one mask layer being patterned at a time, this CPU chip will undergo 80 separate visits to the lithography tool. We could spend another hour talking about photolithography but let's move onto the next category of tools. Deposition tools are used to add or deposit material onto the wafer. A lot of times we use the mask layer from the photolithography step to add materials to the areas uncovered by the mask layer, kind of like spray painting through a stencil. Due to the wide range of elements and compounds used to create the layers, deposition tools have a wide range of variations with complicated names and acronyms for each variant. But essentially there are 3 key groups of materials that are added or deposited onto the wafer: metals such as copper or tantalum, insulators which are typically called oxides, and crystalline layers of silicon. Each group of different materials uses different physics and chemistry principles to deposit the material on the wafer and therefore has a different technical name for the tool that deposits the material. Deposition tools typically have a central wafer handling chamber, with the various chambers attached to the edges, each one dedicated to adding just a single element or compound. The next category of machines do the opposite, which is to remove material. There are 2 key methods. The first is etching. Etchers use either corrosive chemicals or high energy plasmas to react with and remove materials from the surface of the wafer. They are typically used with the mask layer stencil in order to remove the material exposed by the mask, thus creating a hole that can be later filled by a deposition tool. The second method to remove material is CMP, which is chemical mechanical planarization. CMP applies slurry and uses abrasive pads to grind and polish away the top surface of the wafer, making it perfectly flat. CMP levels off the top layers of the wafer and is

typically used as the last step in a cycle of processes in order to prepare the wafer for another layer to be added. The fourth category are tools that modify the silicon and are called ion implanters. These tools use the photomask stencil to bombard the unmasked regions with phosphor, boron, or other elements in order to make the P and the N regions required to form the transistors themselves. Therefore, ion implanters are only used in the front end of line. You might think that this is adding material. However, ion implanters only add around one atom of phosphor or boron for every 10,000 atoms of silicon. Additionally, while other machines spray paint a layer on top of the wafer, ion implanters hurl atoms deep into the silicon lattice, kind of like a cannon launching a baseball 6 feet into a concrete wall. This process typically damages the silicon lattice, which is why the following step is to repair the silicon by heating the wafer using a separate tool called an annealer. The fifth category of tools are used to clean and remove any contaminants or particles from the wafer. These wafer washers use ultra-pure water to clean the wafer and then dry it with nitrogen or hot isopropyl alcohol. Cleaning the wafer happens rather frequently in order to remove any stray particles that may have fallen onto the wafer. And finally, sixth are tools that inspect the transistors and metal layers for defects and are called metrology tools. A common metrology tool uses a scanning electron microscope with nanometer-level resolution to take pictures of the top surface of the wafer and determine if there are defects such as improperly patterned layers or particles on the surface. When fabricating an integrated circuit that takes 3 months to complete, it's important to repeatedly monitor the progress and make sure that each of the processes is being executed with nanometer-level precision. Now that we've covered each of the categories, here are the color coded process steps along with the layout of the tools in the semiconductor fabrication plant. Let's run through the complete set of steps used to manufacture a single metal interconnect layer. First a layer of insulating silicon dioxide is deposited onto the wafer. Next photoresist is spread across the surface and the wafer is sent through a soft bake to remove the solvent. The wafer then travels to the photolithography tool where the design from the photomask is transferred to each of the chips on the wafer by weakening the areas of photoresist hit by the light. The wafer next goes to the developer to wash away the sections that were hit by the light from the lithography tool and then through a hard bake to harden the remaining photoresist. With the mask layer built, the wafer goes to an etching tool, where a plasma etcher removes a vertical column through the exposed silicon dioxide until it reaches the previous layer's metal vias. Next the wafer is sent to a photoresist stripper where the mask layer is removed. The wafer then travels to a physical vapor deposition tool where a sequence of metals fills in the exposed pattern and coats the wafer in metal. Finally the wafer is sent to a chemical mechanical planarization tool where the metal is ground down so that all that remains is a flat layer of insulating silicon dioxide and conductive copper interconnects that match the pattern from the photomask. A single metal layer is now completed, and the wafer is ready for the next cycle to begin where insulating silicon dioxide and the vias will be added. Note that cleaning and wafer metrology or inspection steps occur in between many of these other steps. Furthermore, the process steps to make the transistors are less straightforward and utilize the ion implanter, and thus we'll cover them in a separate video on transistor physics and design. These steps are for building the integrated circuit on the wafer, however, there are additional steps in manufacturing a microchip which we'll explore in a little bit. But before we get there, one important thing to note is that the semiconductor industry is incredibly secretive regarding the exact tool layout and the process

steps and recipes used to make the transistors. We wanted to make the best video on how microchips are made and it took us 180 hours of scouring the internet and textbooks for information and reference images and, using what we found, we spent 205 hours modeling each of these tools, the many layers of the integrated circuit, and the semiconductor fab. Furthermore, writing the script took about 100 hours, and then animating all these visuals took more than 825 hours. As a result, this video took over 1300 hours to make, and it's entirely free to watch. We want to make more videos like this one where we explore computer architecture and how transistors work, and we can't do it without your help. The best way you can help is by taking a few seconds to scroll down, write a comment below, like this video, subscribe if you haven't already and then share this video on social media or send it to a friend or colleague. Truly, just a few seconds of your time helps far more than you think. Additionally, we have a Patreon page where we'll be releasing behind the scenes footage of our work and updates for upcoming videos. If you find what we do useful, we would appreciate any support. Thank you.

So then, what are the additional steps in manufacturing a microchip? Before chip manufacturing at the fab, we first have to manufacture the silicon wafers by refining quartzite into pure silicon, and then growing a monocrystalline ingot and cutting it into wafers. For reference, these 300-millimeter wafers are around three-quarters of a millimeter thick, they have a barcode on the side and a small notch in them to indicate the direction of the crystal lattice. Furthermore, these wafers are incredibly delicate, and shatter into hundreds of shards when broken. A single wafer costs around a hundred dollars, but after being populated with CPUs it's worth closer to a hundred thousand dollars, making it quite literally ten times more valuable than its weight in gold. Moving onto the steps after chip manufacturing. The completed wafer is sent to a separate building where each of the CPUs undergoes rigorous testing to figure out if it works as intended. If a CPU works, that's great. But frequently a particle or photomask defect has damaged a section of the integrated circuit, rendering that section defective. These semi-functional circuits are then categorized, or binned, based on what still works. These Intel Thirteenth Gen processors are sold as an i9, i7, i5, or i3, depending on how many cores are functional with different product lines of CPUs whose on-board integrated graphics sections are defective. These wafers are transported to another building where the chips are cut out using a laser, flipped over, and placed on an interposer which distributes the connection points to a printed circuit board while a protective heat conductive cover is placed on the back side. The printed circuit board holds the landing grid array that interfaces with the motherboard as well as various electrical components. Next an integrated heat spreader is mounted on top, and the entire assembly is tested one last time before being packaged for sale. Finally, the CPU is now ready to be mounted onto the motherboard and installed into your desktop computer. It's important to understand that chip manufacturing requires an incredible amount of science and engineering and there's a free and easy way to learn the basic principles inside each of these complex tools and that's with this video's sponsor, Brilliant.org! Brilliant reimagines how courses are taught. Instead of boring hour-long lectures or textbooks that put you to sleep, Brilliant uses fun and interactive modules inside thousands of lessons from basics to advanced topics – and new lessons are added every month. Whatever your skill level, Brilliant customizes its content to fit your needs and allows you to learn at your own pace. We use Brilliant daily. We're working on videos on how AI and Chat GPT Works, and so each of our animators is progressing through their lessons on How Large Language Models work. Because you're watching this video, you

probably enjoy learning about how technology works, and fortunately for you, Brilliant just added a course on this very topic. In it they have lessons such as How GPS Works, How Computer Memory Works, and how Recommendation Algorithms such as those used by YouTube work. If you're looking to advance your career, Brilliant is the go-to resource for leveling up your skills and staying up-to-date on the latest concepts behind world-changing technology. For the viewers of this channel, Brilliant is offering a free 30-day trial with access to all their thousands of lessons. Additionally, Brilliant is offering 20% off an annual subscription. Just go to brilliant.org/branchededucation. The link is in the description below. Microchip Fabrication is a massive topic, and thus, we have two more equally complex videos that we're working on. The first will be an in-depth 3D animated factory tour and the second will explore transistor physics, FinFets, and the next generation of transistors. We're also working on a series of videos on GPUs and a separate one on CPU architecture so make sure to subscribe so you don't miss any of our videos. We're thankful to all our Patreon and YouTube Membership Sponsors for supporting our work. If you want to financially support our work, you can find the links in the description below. This is Branch Education, and we create 3D animations that dive deeply into the technology that drives our modern world. Watch another Branch video by clicking one of these cards or [click here](#) to subscribe. Thanks for watching to the end!