

Ryan Young
CSE 2300w Lab Report
D-flipflop Lab

Shift Registers

Objectives:

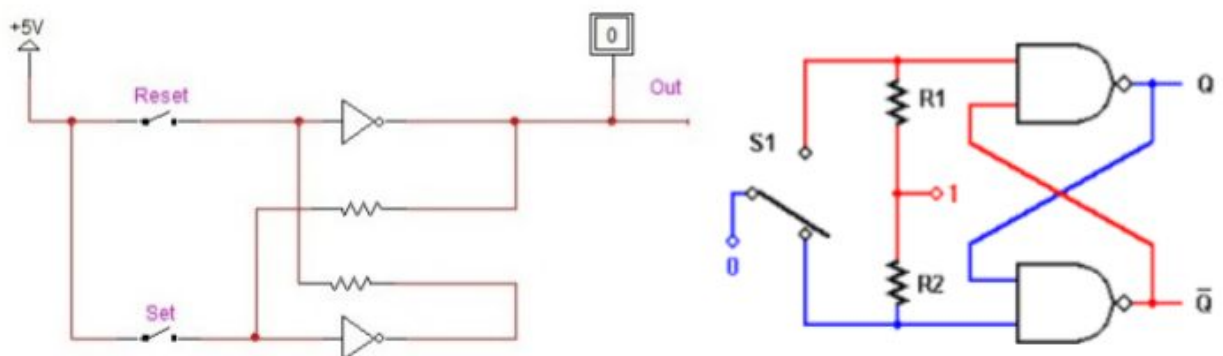
The objective for this lab was to use four D-flipflop to build a register to show that serial and parallel input and output can be achieved through the D preset and clear inputs. We also built a circuit specifically for the clock input.

Introduction:

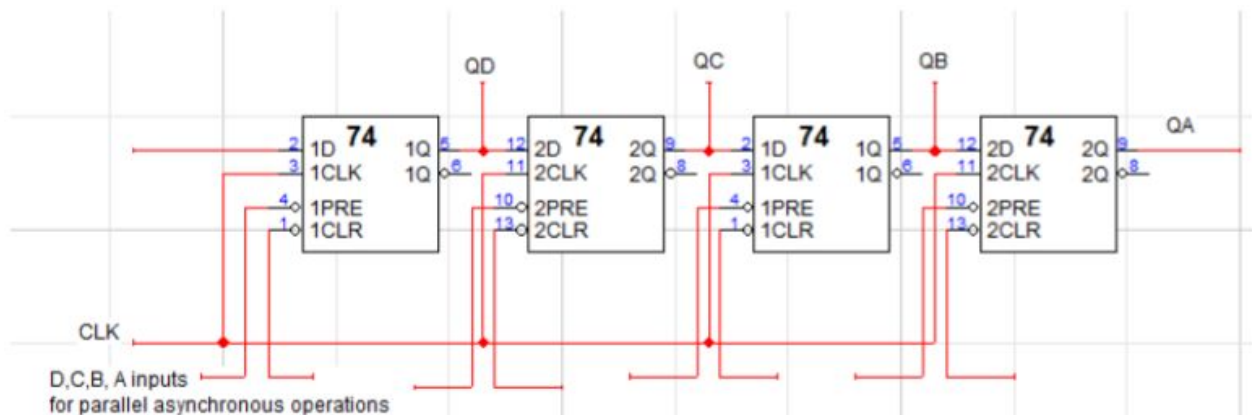
The theory behind this lab revolves around the concept of a shift register. A shift register is composed of two or more D-flipflops. These flipflops are connected by a common clock so that when the clock pulses data moves bit by bit through one D-flipflop. The physical chips we are using on our breadboard allow data to move on the rising edge of the clock cycle. This essentially means that data will only move when the clock cycles from a 0 to a 1 and will remain there until the next 0 to 1 cycle.

Procedure:

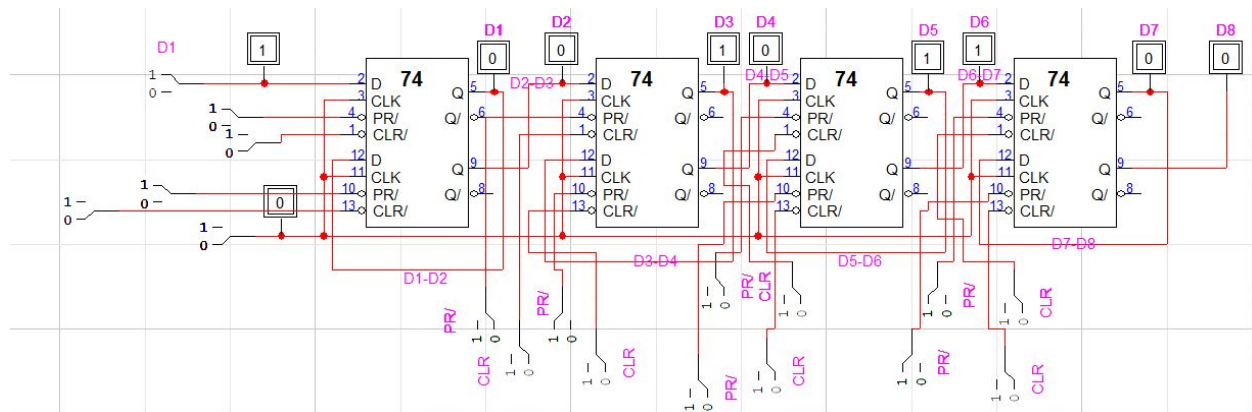
- 1.) Firstly we must read through the entire PDF and make sure we understand what the lab is asking.
- 2.) After that is completed then I created the debouncer circuit on the physical breadboard based off the schematic below. This allows us to maintain a solid 1 or 0 thus countering any noise produced by a switch.



- 3.) Next following the completion of the debouncer circuit I used the diagram showing the four connected D-flipflops (as seen below) and finished the rest of the circuit using two SN7494 physical chips.



- 4.) Finally I completed the lab report and made sure all my testing was correct.



Discussion:

Conclusions:

Questions:

- 1.) The main functional purpose of this register is to serially shift the values to the right by one each clock cycle. But in terms of use in a microprocessor they can be used for things such as I/O controls.
- 2.) Yes both are Dual D-flipflops that are positive edge driven that include an option to set and reset or clear each one.