

YURUN YUAN

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EDUCATION

University of Science and Technology of China (USTC)

September 2019 - Present

Major in Computer Science

GPA: 3.97/4.3 (ranking 6/252), Average score: 92.24/100

Core courses:

- | | | | |
|---------------------------------------|--------|-------------------------------------|--------|
| · Operating Systems (Honors) | 97/100 | · Computer Organization & Design | 94/100 |
| · Data Structures | 95/100 | · Introduction to Computing Systems | 95/100 |
| · Programming (Advanced) | 98/100 | · Graph Theory | 97/100 |

RESEARCH EXPERIENCE

Advanced Data Systems Laboratory, USTC

November 2021 - Present

Research Assistant, Advisor: Cheng Li

gitlab.com/hipress/hipress

- Researched on gradient compression algorithms used in DNN training, including TernGrad and 3-LC.
- Extended CompLL, a compiler that aims to help practitioners develop gradient compression algorithms by converting a DSL into highly-optimized CUDA C++ code, to support more language features, including loops, arrays, and an operator `prefix_sum`.
- Implemented algorithm 3-LC in the DSL and converted it into CUDA C++ code using the extended compiler.

Team LUNA, Big Data Laboratory, USTC

October 2021 - December 2021

Backend Developer

gitlab.com/ryanyuan-yyr/luna-ailab-api

- Studied the usage of MySQL, ORM and Flask.
- Built the backend for the API website, which manages users' data in MySQL databases and provides user authentication services.

SELECTED COURSE PROJECTS

A Compiler for cminusf, a C-like Programming Language

October 2021 - January 2022

Compilers Principles, prof.Cheng Li

github.com/ryanyuan-yyr/2021fall-compiler_cminus

- Used `lexer` and `bison` to implement the lexical and semantic analysis.
- Led a group of 3 to build the abstract syntax tree, translate `cminusf` source code into LLVM IR, and implement machine independent optimization(constant propagation, live-variable analysis and loop invariant hoist) with C++.
- Extended the syntax of `cminusf`, including structures, member functions, class templates and operator overloading.

A Primary 5-Stage-Pipelined RISC-V CPU with FPGA

May 2021 - June 2021

Computer Organization & Design, prof.Chao Wang

github.com/ryanyuan-yyr/COD-Labs

- Implemented a `pipelined` CPU in Verilog, supporting arithmetic instructions, `load/store instructions`, `memory mapped I/O`, `instruction ecall` and interrupts.
- Performed stimulation and synthesis on Vivado. Programmed on the FPGA development board.

Shell in Rust

May 2021

Operating Systems(Honors), prof.Kai Xing github.com/ryanyuan-yyr/OSH-2021-Labs/tree/main/lab2

- Learned about basic concepts and syntax of Rust.
- Implemented a shell in Rust, supporting pipe, SIGINT, and I/O redirection.

FAT16 in User Space

June 2021

Operating Systems, prof. Yongkun Li

github.com/ryanyuan-yyr/FAT-filessystem

- Used FUSE to implement a FAT16 filesystem on Ubuntu, supporting the creation and removal of files and directories.

MISCELLANEOUS

Language

TOEFL: 105/120. Reading 30, Listening 24, Speaking 22, Writing 29

Awards

Scholarship for Outstanding Students, 2020 - 2021 (Gold award, 15/172)

Programming skills

C, C++, Python, **Rust**, Verilog

Software skills

Vivado, L^AT_EX, Visual Studio Code

Volunteer work

Mathematics tutor for high school students