

# YURUN YUAN

Western Campus, University of Science and Technology of China ◊ Anhui, China

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## EDUCATION

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**University of Science and Technology of China (USTC)**

September 2019 - Present

Major in Computer Science

GPA: 3.97/4.3 (ranking 6/252), Average score: 92.24/100

Core courses:

· Operating Systems	97/100	· Computer Organization & Design	94/100
· Data Structures	95/100	· Introduction to Computing Systems	95/100
· Programming (Advanced)	98/100	· Graph Theory	97/100

## RESEARCH EXPERIENCE

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**Advanced Data Systems Laboratory, USTC**

November 2021 - Present

*Research Assistant, Advisor: Cheng Li*

[gitlab.com/hipress/hipress](https://gitlab.com/hipress/hipress)

- Researched on gradient compression algorithms used in DNN training, e.g., 3-LC, Terngrad, etc.
- Extended CompLL, a compiler for a DSL, which aims to help practitioners develop highly-optimized gradient compression algorithms, to support more language features.

**Team LUNA, Big Data Laboratory, USTC**

October 2021 - December 2021

*Backend Developer*

[gitlab.com/ryanyuan-yyr/luna-ailab-api](https://gitlab.com/ryanyuan-yyr/luna-ailab-api)

- Studied the usage of MySQL, ORM and Flask.
- Built the backend for the API website, which manages users' data in MySQL databases and provides user authentication services.

## SELECTED COURSE PROJECTS

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**A Compiler for cminusf, a C-like Programming Language**

October 2021 - January 2022

*Compilers Principles, prof. Cheng Li*

[github.com/ryanyuan-yyr/2021fall-compiler\\_cminus](https://github.com/ryanyuan-yyr/2021fall-compiler_cminus)

- Used **Lexer** and **Bison** to implement the lexical and semantic analysis.
- Led a group of 3 to build the abstract syntax tree, translate **cminusf** source code into LLVM IR, and implement several optimization passes with C++.
- Extended the syntax of **cminusf**, including classes, class templates and operator overloading.

**A Primary 5-Stage-Pipelined RISC-V CPU with FPGA**

May 2021 - June 2021

*Computer Organization & Design, prof. Chao Wang*

[github.com/ryanyuan-yyr/COD-Labs](https://github.com/ryanyuan-yyr/COD-Labs)

- Implemented the CPU in **Verilog**, supporting arithmetic instructions, IO instructions and interrupts.
- Performed stimulation and synthesis on Vivado. Programed on the FPGA development board.

## MISCELLANEOUS

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**Language**

TOEFL: 105/120. Reading 30, Listening 24, Speaking 22, Writing 29

**Awards**

Scholarship for Outstanding Students, 2020 - 2021 (Gold award, 15/172)

**Programming skills**

C, C++, Python, Verilog

**Software skills**

Vivado, L<sup>A</sup>T<sub>E</sub>X, Visual Studio Code

**Volunteer work**

Mathematics tutor for high school students