YURUN YUAN

Western Campus, University of Science and Technology of China ⋄ Anhui, China
(+86) 152 · 1221 · 6859 ⋄ yr_yuan@mail.ustc.edu.cn
ryanyuan-yyr.github.io ⋄ github.com/ryanyuan-yyr

EDUCATION

University of Science and Technology of China (USTC) September 2019 - Present
Major in Computer Science
GPA: 3.97/4.3 (ranking 6/252), Average score: 92.24/100
Core courses:

· Operating Systems	97/100	· Computer Organization & Design	94/100
· Data Structures	95/100	· Introduction to Computing Systems	95/100
· Programming (Advanced)	98/100	· Graph Theory	97/100

RESEARCH EXPERIENCE

Advanced Data Systems Laboratory, USTC November 2021 - Present
Research Assistant, Advisor: Cheng Li *gitlab.com/hipress/hipress*

- Researched on gradient compression algorithms used in DNN training, including TernGrad and 3-LC.
- Extended `CompLL`, a compiler that aims to help practitioners develop gradient compression algorithms by converting a DSL into highly-optimized CUDA C++ code, to support more language features, including loops, arrays and an operator `prefix_sum`.
- Implemented algorihtm 3-LC in the DSL and converted it into CUDA C++ code using the extended compiler.

Team LUNA, Big Data Laboratory, USTC October 2021 - December 2021
Backend Developer *gitlab.com/ryanyuan-yyr/luna-ailab-api*

- Studied the usage of MySQL, ORM and Flask.
- Built the backend for the API website, which manages users' data in MySQL databases and provides user authentication services.

SELECTED COURSE PROJECTS

A Compiler for `cminiusf`, a C-like Programming Language October 2021 - January 2022
Compilers Principles, prof. Cheng Li *github.com/ryanyuan-yyr/2021fall-compiler_cminus*

- Used `Lexer` and `Bison` to implement the lexical and semantic analysis.
- Led a group of 3 to build the abstract syntax tree, translate `cminusf` source code into LLVM IR, and implement constant propagation, live-variable analysis and loop invariant hoist with C++.
- Extended the syntax of `cminusf`, including structures, member functions, class templates and operator overloading.

A Primary 5-Stage-Pipelined RISC-V CPU with FPGA May 2021 - June 2021
Computer Organization & Design, prof. Chao Wang *github.com/ryanyuan-yyr/COD-Labs*

- Implemented a pipelined CPU in `Verilog`, supporting arithmetic instructions, load/store instructions, memory mapped I/O, instruction `ecall` and interrupts.
- Performed stimulation and synthesis on Vivado. Programmed on the FPGA development board.

MISCELLANEOUS

Language	TOEFL: 105/120. Reading 30, Listening 24, Speaking 22, Writing 29
Awards	Scholarship for Outstanding Students, 2020 - 2021 (Gold award, 15/172)
Programming skills	C, C++, Python, Verilog
Software skills	Vivado, LaTeX, Visual Studio Code
Volunteer work	Mathematics tutor for high school students