YuRun Yuan

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Education

University of Science and Technology of China (USTC) Hefei, China
B.S. in Computer Science with honors Sep 2019 – Jun 2023(expected)

- GPA: 3.97/4.3 (ranking 3/256)
- Core courses: Principles and Techniques of Compiler (100/100), Foundations of Algorithms (97/100), Operating Systems (Honors) (97/100), Computer Organization & Design (94/100), Data Structures (95/100)

Selected Research Projects

Manage Heterogeneous Memory Hierarchy with Java Runtime Feb 2022 - Present
Research Intern, Advisor: Prof. Jian Huang PlatformX Group, UIUC

- Identified a certain object access pattern in JVM to locate frequently accessed objects
- Proposed a new policy that leverages the semantic information in JVM to place objects with different access frequencies in different memories, taking advantage of low latency of fast memory and high capacity of slow memory

Extension of a DSL compiler for ML applications Nov 2021 - Jan 2022
Research Assistant, Advisor: Prof. Cheng Li Advanced Data Systems Laboratory, USTC

- Studied popular gradient compression algorithms used in DNN training, including TernGrad and 3-LC
- Extended `CompLL`, a compiler that translates C-like DSL code into highly-optimized CUDA C++ code, to support more language features, including loops, arrays, and a new operator `prefix_sum`
- Implemented the 3-LC algorithm in DSL with only 69 lines of code, which greatly reduces developers' burden

Selected Course Projects

A Compiler for `cminusf`, a C-like Programming Language Oct 2021 - Jan 2022
Principles of Compiler Design Project Link

- Extended the syntax of `cminusf` to support structures, class templates, member functions, and operator overloading
- Implemented the lexical and semantic analysis of the compiler with `lexer` and `bison`
- Led a group of 3 to build the abstract syntax tree, translate `cminusf` source code into intermediate representation, and implement machine-independent optimization(constant propagation, live-variable analysis, and loop invariant hoist) with LLVM

A Primary 5-Stage-Pipelined RISC-V CPU with FPGA May 2021 - Jun 2021
Computer Organization & Design Project Link

- Implemented a pipelined CPU in `Verilog`, supporting arithmetic instructions, load/store instructions, memory mapped I/O, instruction `ecall` and interrupts
- Evaluated the CPU performance in the Vivado simulator and on a real FPGA board

Skills & Techniques

- *TOEFL:* Reading 30, Listening 24, Speaking 22, Writing 29
- *GRE:* Verbal 152, Quantitative 170, Analytical Writing 4.0
- *Programming Skills:* C/C++, Python, Java, Rust, Verilog, SQL
- *Software Skills:* Vivado, gem5, LaTeX, Maxine JVM

Awards & Honors

- Shenzhen Stock Exchange Scholarship 2021
- Scholarship for Outstanding Students (Gold award, 15/172) 2021
- Hua Xia Talent Program First Prize Scholarship (12 / 254 students major in CS) 2020-2021