3EJ4 (Fall 2022):

Electronic Devices and Circuits

Lab #4

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**Part 1 Questions:**

Q.1:

The circuit will maintain a linear amplification behaviour for all inputs above 4V and all outputs above -4.7. When the output voltage is 0V, the input voltage is roughly .5V.

Q.2:

The simulated voltage gain is arbitrarily close to 1, yielding a voltage gain in dB of 0dB in theory. The measured circuit exhibits a voltage gain closer to .8dB .

**Part 2 Questions:**

Q.3:

When Iref is .1mA, Io is .104 mA. When Iref is 1mA, Io is .975mA. The design of the circuit would imply that it is impossible for the output current to be greater than the reference current while both BJTs are in forward active mode. This is due to the bases and emitters of the BJTs being shorted, coupling their theoretical collector current while attributing the combined base current to the reference current. Since the reference current is therefore equal to the output current with the addition of the base currents, the reference current must be exclusively greater than the output current. This rule is broken for the low current case above. I believe that this anomaly is due to the input/output impedances of the current mirror being non-ideal; ideal in this case being 0 at the input and infinite at the output. The current sink which defines the reference current has an arbitrarily high impedance, while the load resistor has a defined resistance far less than this. The non-ideal BJT on the output end of the current mirror is therefore unable to restrain the output current to the reference current due to the insufficient current load in combination with the realistic, non-ideal parameters of the BJT. At the higher current, the load resistance provides sufficient load with greater voltage drop, relieving the requirement on the mirror to restrain the output current.

Q.4:

The input resistance is 389.12 ohms. The current gain is 1.048 A/A. The output impedance is 1.58 Mohms.

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**Part 3 Questions:**

Q.5:

The voltage gain is 70.07 dB for the differential-mode signal. A 0.0039499 volt offset was needed to correct the difference between Q1 and Q2. The measured results demonstrated a much lower gain of 56.6 dB.

Q.6:

According to the simulated results, the 3-dB point is at 11kHz, when the angle is offset by 4.47E+1 or roughly 45 degrees and the voltage is reduced from 6.37V down by a factor of roughly .707 to 4.53V.

Q.7:

The 3-dB frequency of the circuit using the current mirror is 11kHz while that of the resistor-loaded circuit has a 3-dB frequency of 9.1MHz. The current mirror based amplifier has a simulated gain of 70.07VdB while the resistor based amplifier has a voltage gain of 19.63VdB. The current mirror design therefore sacrifices the 3-dB frequency characteristic in favour of the gain characteristic.

Q.8:

The 3-dB frequency of the mirror-loaded circuit of 11kHz yields a gain of 67.1 dB, making for a GBW of 738 kHz. The 3-dB frequency of the resistor-loaded circuit of 9.12MHz yields a gain of 16.6 dB, making for a GBW of 152MHz.