1 - Cover Sheet
2 - Connector+IO: HSEC connector and Device IO
3 - Power+Misc: LDO, optional SVS, optional XTAL, LEDs
4 - ADC: ADC interface circuitry
5 - Xds100v2_Emu: isolated xds100v2 emulator
6 - EmuInterface: isolation circuitry for emulator
7 - EVM Hardware and Silkscreen components

Note that all switches are displayed in the schematic as they are oriented in the layout.

Revision History

Rev	ECN #	Approved Date	Approved by	Notes
E1	N/A	15Dec2015	BL	First Draft
E2	N/A	20Sept2016	BL	Second Draft
A	N/A	06Jan2016	BL	Add CE Mark; Fix silkscreen issues
B	N/A	05Mar2018	BL	Replace F280049M with F280049C. Migrate to Vault. Update compliance logos. Replace Y1 crystal for long term availability.

Orderable: TMDSCNCD280049C	Designed for: Public Release	Mod. Date: 3/16/18
TID #: N/A	Project Title: F280049C controlCARD	
Number: MCU009 Rev: B	Sheet Title: Cover Sheet	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 1 of 7
Drawn By: Brett Larimore	File: MCU009B_CoverSheet.SchDoc	Size: B
Engineer: Brett Larimore	Contact: http://www.ti.com/support	

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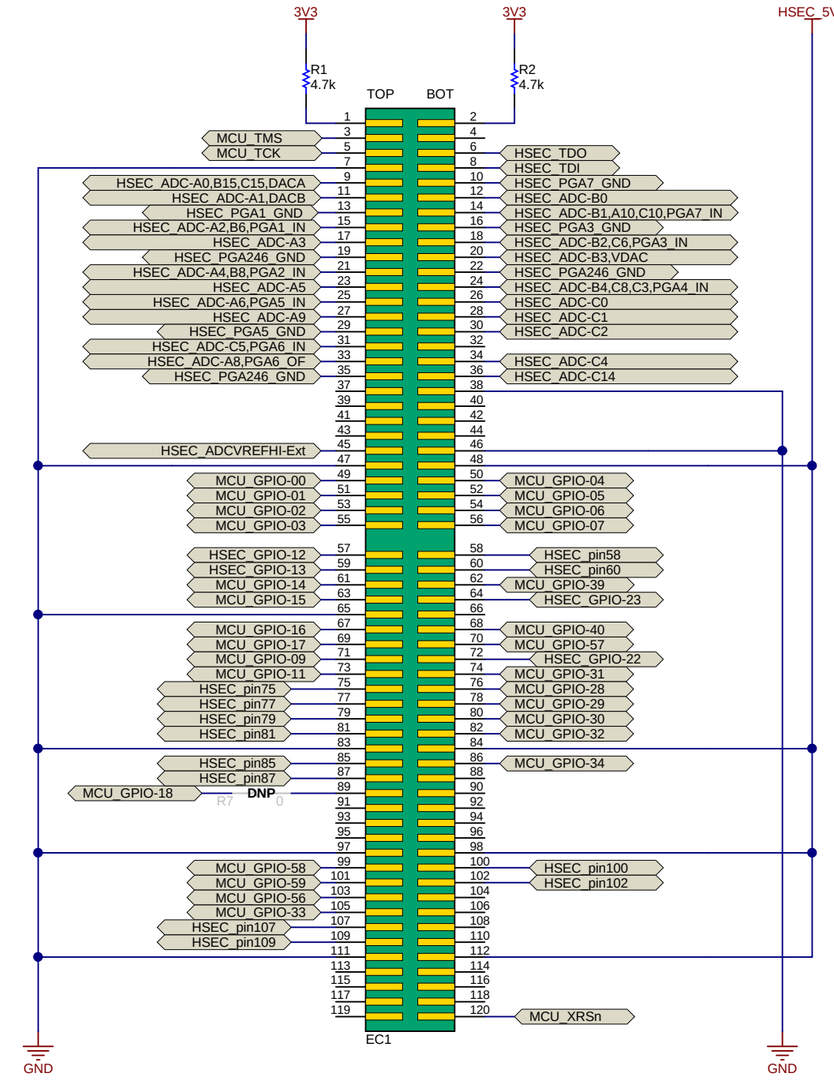

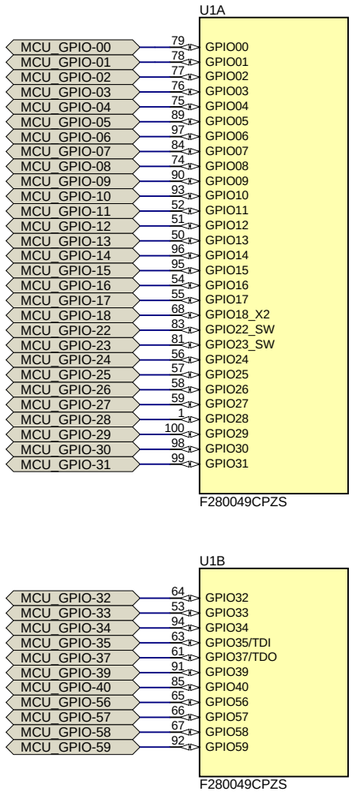

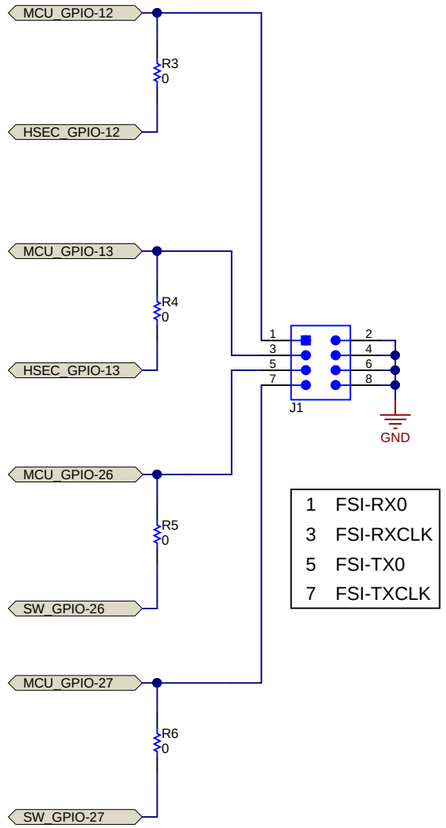

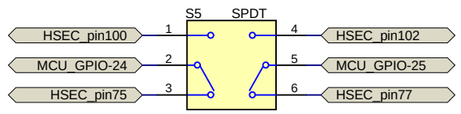

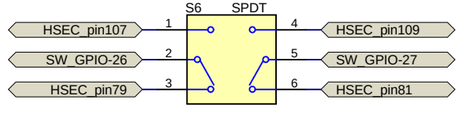

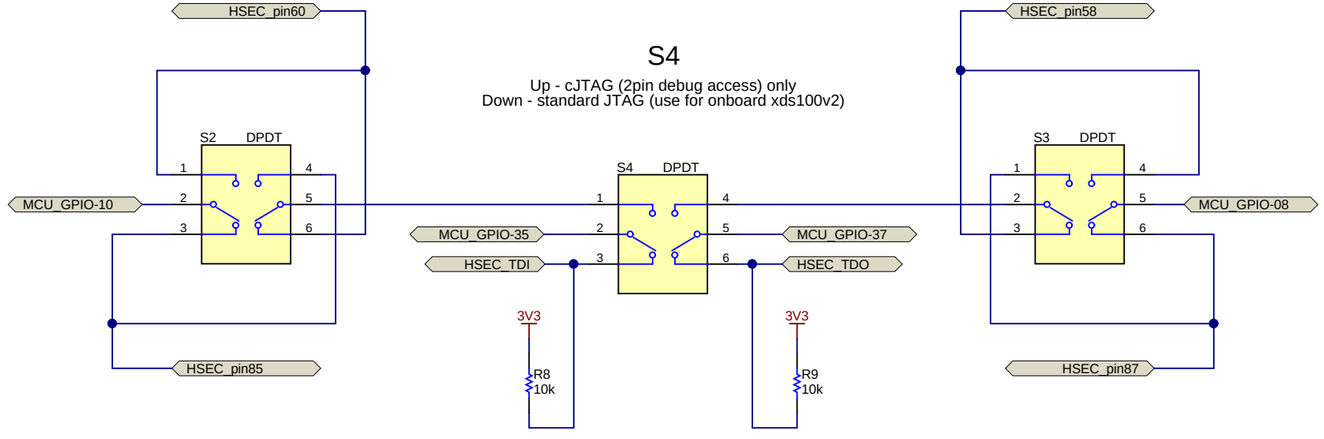

Orderable: TMDSCNCD280049C		Designed for: Public Release	Mod. Date: 3/16/18
TID #: N/A		Project Title: F280049C controlCARD	
Number: MCU009	Rev: B	Sheet Title: Connector+IO	
SVN Rev: Version control disabled		Assembly Variant: 001	Sheet: 2 of 7
Drawn By:		File: MCU009B_Connector+IO.SchDoc	Size: B
Engineer: Brett Larimore		Contact: http://www.ti.com/support	

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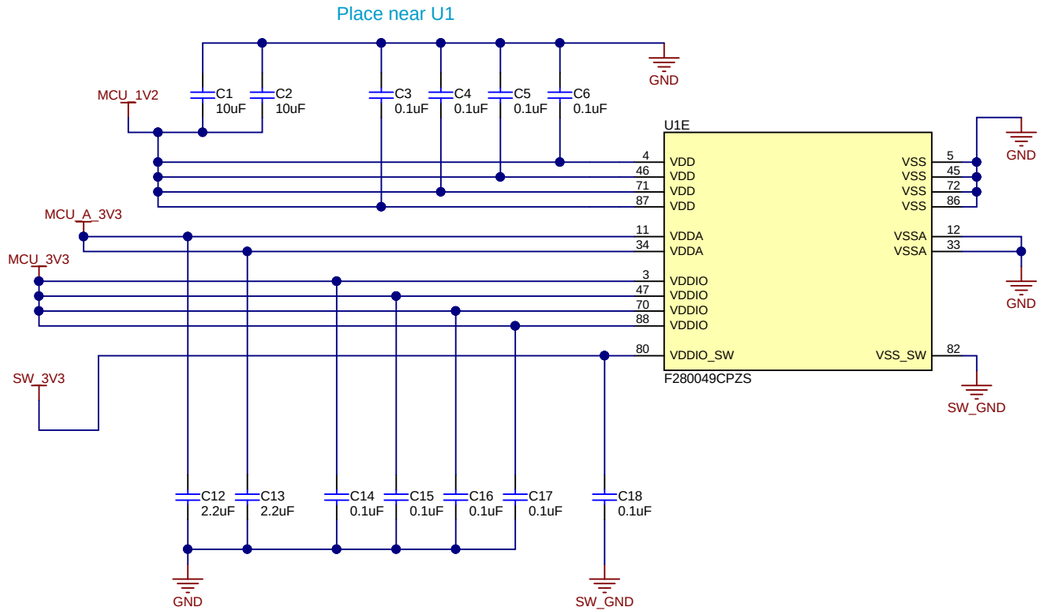

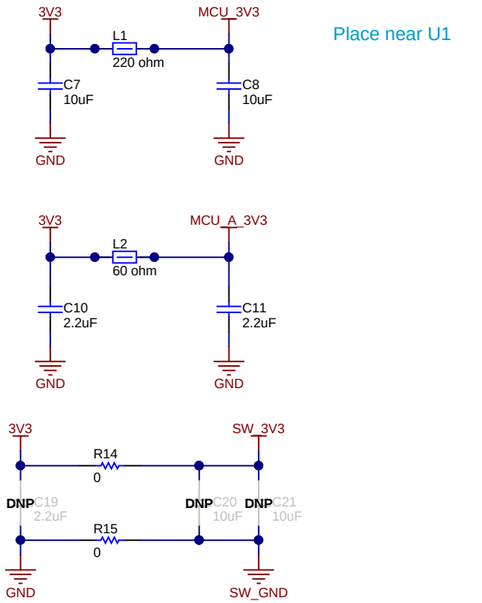

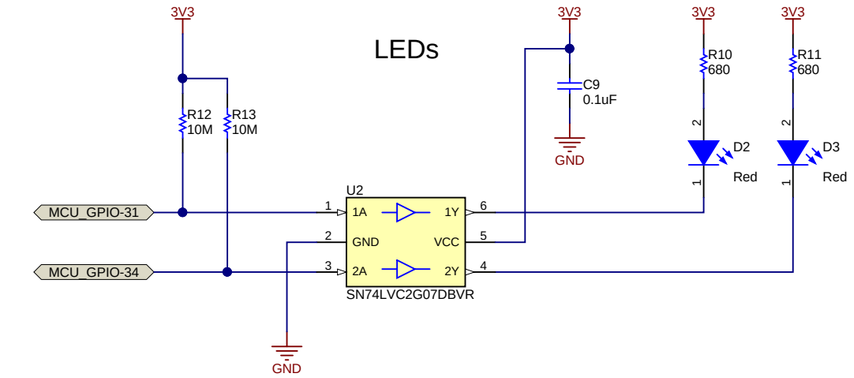

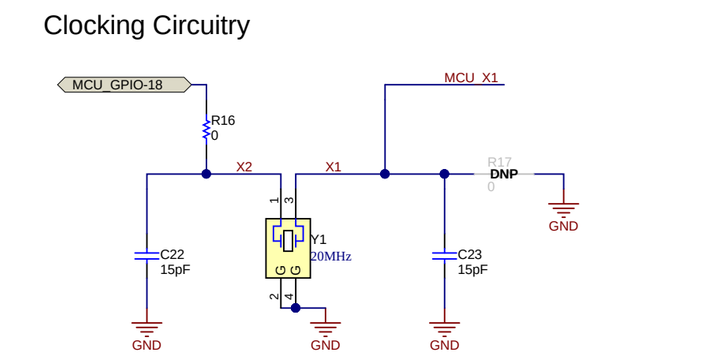

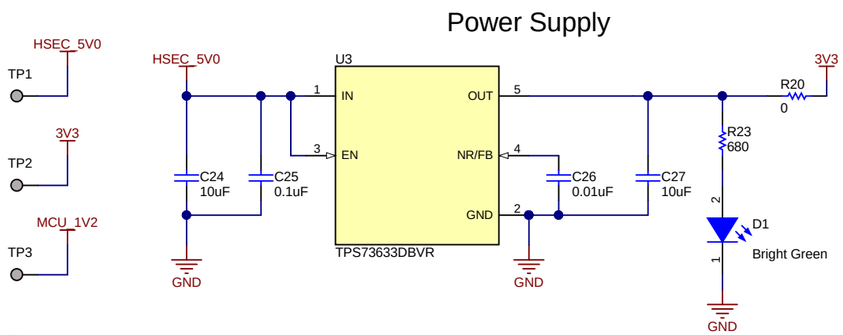

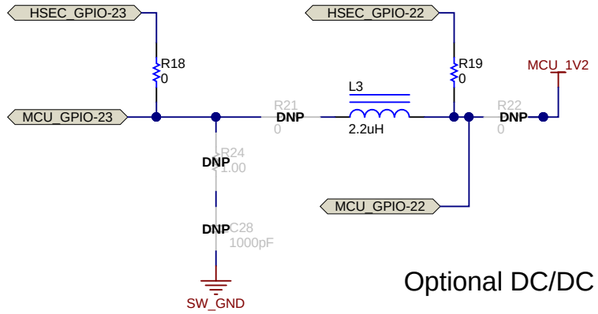

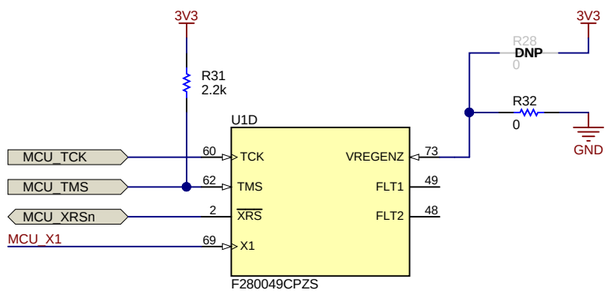

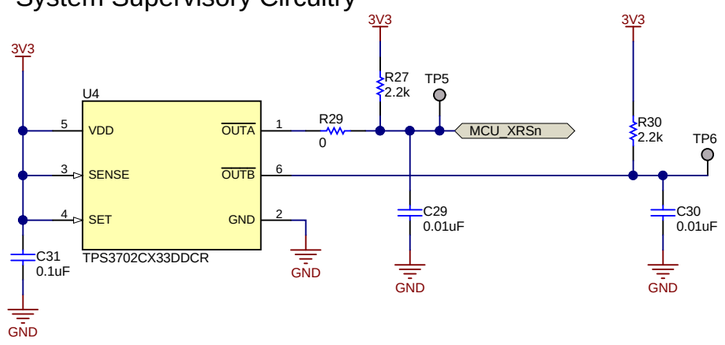

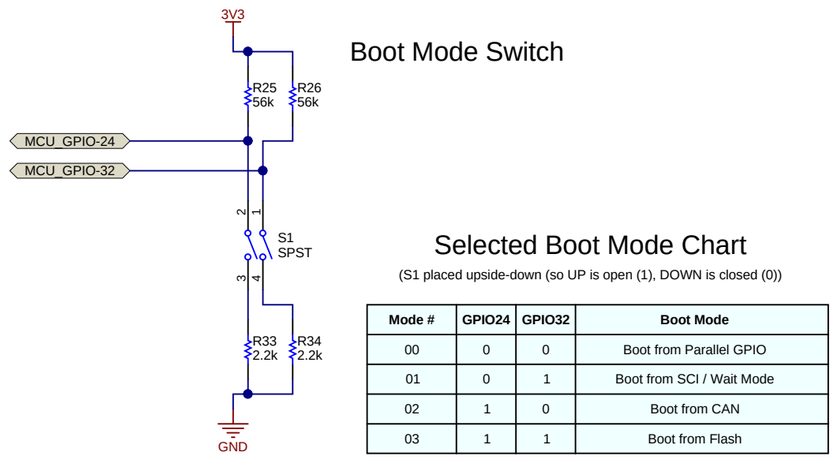

Selected Boot Mode Chart

(S1 placed upside-down (so UP is open (1), DOWN is closed (0))

Mode #	GPIO24	GPIO32	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN
03	1	1	Boot from Flash

Orderable: TMDSCNCD280049C		Designed for: Public Release	Mod. Date: 3/16/18
TID #: N/A		Project Title: F280049C controlCARD	
Number: MCU009	Rev: B	Sheet Title: Power+Misc	
SVN Rev: Version control disabled		Assembly Variant: 001	Sheet: 3 of 7
Drawn By:		File: MCU009B_Power+Misc.SchDoc	Size: B
Engineer: Brett Larimore		Contact: http://www.ti.com/support	

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S7 enables two methods of using the PGA

a) The PGA's respective switch in S7 is on
- the respective PGA can be used, but PGA output filtering may not be used
- the respective HSEC input ties to an ADC pin and can be measured with a gain of 1

b) The PGA's respective switch in S7 is off
- PGA and PGA filtering may be used for this PGA
- the respective HSEC input cannot be measured with a gain of 1

MCU_A_3V3 C32 0.1uF

U5 TPD4E001QDBVRQ1
- HSEC_ADC-A0,B15,C15,DACA
- HSEC_ADC-A1,DACB
- HSEC_ADC-A3
- HSEC_ADC-A5

U7 TPD4E001QDBVRQ1
- HSEC_ADC-A9
- HSEC_ADC-B0
- HSEC_ADC-B3,VDAC
- HSEC_ADC-C0

U9 TPD4E001QDBVRQ1
- HSEC_ADC-C1
- HSEC_ADC-C2
- HSEC_ADC-C4
- HSEC_ADC-C14

GND

C34 330pF, C35 330pF, C36 330pF, C37 330pF, C38 330pF, C39 330pF, C40 330pF

MCU_ADC-PGA1OF
MCU_ADC-PGA2OF
MCU_ADC-PGA3OF
MCU_ADC-PGA4OF
MCU_ADC-PGA5OF
MCU_ADC-PGA6OF
MCU_ADC-PGA7OF

S7 SPST

MCU_ADC-PGA1
MCU_ADC-PGA2
MCU_ADC-PGA3
MCU_ADC-PGA4
MCU_ADC-PGA5
MCU_ADC-PGA7

R35 0 HSEC_ADC-A8,PGA6_OF

C41 DNP, C42 DNP, C43 DNP, C44 DNP, C45 DNP, C46 DNP, C47 DNP

MCU_A_3V3 C33 0.1uF

U6 TPD4E001QDBVRQ1
- HSEC_ADC-A2,B6,PGA1_IN
- HSEC_ADC-A4,B8,PGA2_IN
- HSEC_ADC-B2,C6,PGA3_IN
- HSEC_ADC-B4,C8,C3,PGA4_IN

U8 TPD4E001QDBVRQ1
- HSEC_ADC-A6,PGA5_IN
- HSEC_ADC-A8,PGA6_OF
- HSEC_ADC-C5,PGA6_IN
- HSEC_ADC-B1,A10,C10,PGA7_IN

GND

U1C F280049CPZS

HSEC_ADC-A0,B15,C15,DACA	R36 0	23 A0/B15/C15/DACA_OUT	MCU_ADC-A0
HSEC_ADC-A1,DACB	R38 0	22 A1/DACB_OUT	MCU_ADC-A1
HSEC_ADC-A3	R41 0	9 A2/B6/PGA1_OF	MCU_ADC-A3
HSEC_ADC-A5	R44 0	10 A3	MCU_ADC-A5
HSEC_ADC-A9	R47 0	36 A4/B8/PGA2_OF	MCU_ADC-A9
HSEC_ADC-B0	R49 0	35 A5	MCU_ADC-B0
HSEC_ADC-B3,VDAC	R53 0	6 A6/PGA5_OF	MCU_ADC-B3
		37 A8/PGA6_OF	
		38 A9	
		41 B0	
		40 B1/A10/C10/PGA7_OF	
		7 B2/C6/PGA3_OF	
		8 B3/VDAC	
		39 B4/C8/PGA4_OF	
HSEC_ADC-C0	R60 0	19 C0	MCU_ADC-C0
HSEC_ADC-C1	R61 0	29 C1	MCU_ADC-C1
HSEC_ADC-C2	R62 0	21 C2	MCU_ADC-C2
HSEC_ADC-C4	R63 0	17 C4	MCU_ADC-C4
HSEC_ADC-C14	R64 0	44 C14	MCU_ADC-C14

		18 PGA1_IN	MCU_ADC-PGA1
		30 PGA2_IN	MCU_ADC-PGA2
		20 PGA3_IN	MCU_ADC-PGA3
		31 C3/PGA4_IN	MCU_ADC-PGA4
		16 PGA5_IN	MCU_ADC-PGA5
		28 C5/PGA6_IN	MCU_ADC-PGA6
		43 PGA7_IN	MCU_ADC-PGA7
HSEC_ADC-A2,B6,PGA1_IN	R37 0		
HSEC_ADC-A4,B8,PGA2_IN	R39 0		
HSEC_ADC-B2,C6,PGA3_IN	R40 0		
HSEC_ADC-B4,C8,C3,PGA4_IN	R42 0		
HSEC_ADC-A6,PGA5_IN	R43 0		
HSEC_ADC-C5,PGA6_IN	R45 0		
HSEC_ADC-B1,A10,C10,PGA7_IN	R46 0		
		14 PGA1_GND	
		15 PGA3_GND	
		13 PGA5_GND	
		32 PGA2_GND/PGA4_GND/PGA6_GND	
		42 PGA7_GND	
HSEC_PGA1_GND	R48 0		
HSEC_PGA3_GND	R50 0		
HSEC_PGA5_GND	R51 0		
HSEC_PGA246_GND	R52 0		
HSEC_PGA7_GND	R54 0		
		25 VREFHIA	
		24 VREFHIB/VREFHIC	
		27 VREFLOA	
		26 VREFLOB/VREFLOC	

R55 DNP, R56 DNP, R57 DNP, R58 DNP, R59 DNP

C48 DNP, C49 DNP, C50 DNP, C51 DNP, C52 DNP, C53 DNP, C54 DNP, C55 DNP, C56 DNP, C57 DNP, C58 DNP, C59 DNP

C60 2.2uF, C61 2.2uF

S8 SPST

HSEC_ADCVREFHI-Ext

Place near U1

S8 chooses whether the internal or external voltage reference will be used

a) The ADC's respective switch in S8 is on
- ADC should be configured to disable the internal reference and instead a reference voltage should be attached to HSEC pin 45

b) The respective ADC's switch in S8 is off
- ADC should use the internal voltage reference

Orderable: TMDSCNCD280049C		Designed for: Public Release	Mod. Date: 3/16/18
TID #: N/A		Project Title: F280049C controlCARD	
Number: MCU009	Rev: B	Sheet Title: ADC	
SVN Rev: Version control disabled		Assembly Variant: 001	Sheet: 4 of 7
Drawn By:		File: MCU009B_ADC.SchDoc	Size: B
Engineer: Brett Larimore		Contact: http://www.ti.com/support	

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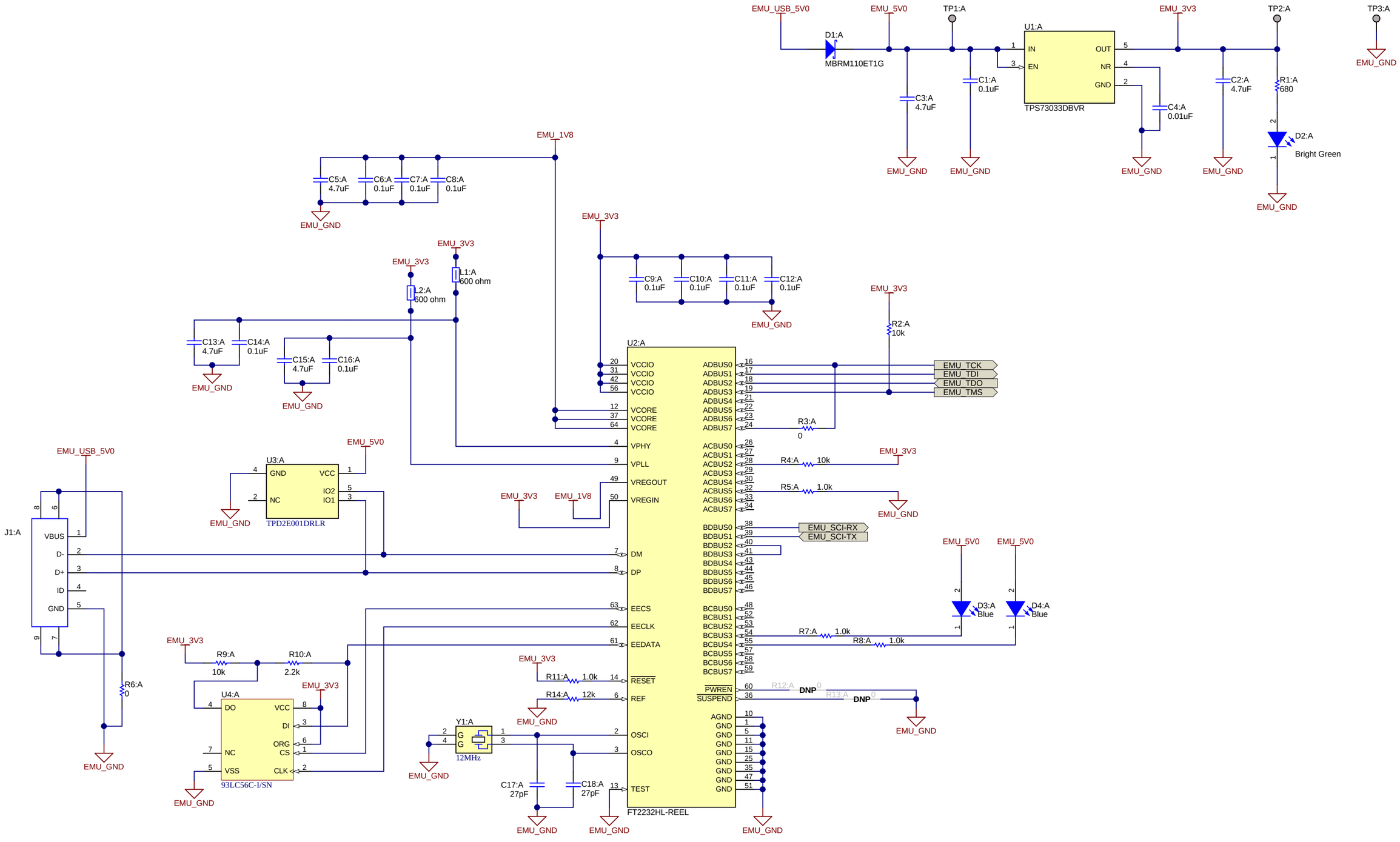

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Orderable: TMDSCNCD280049C	Designed for: Public Release	Mod. Date: 3/2/18
TID #: N/A	Project Title: F280049C controlCARD	
Number: MCU009 Rev: B	Sheet Title: Xds100v2Emu	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 5 of 7
Drawn By:	File: MCU009B_Xds100v2Emu.SchDoc	Size: B
Engineer: Brett Larimore	Contact: http://www.ti.com/support	

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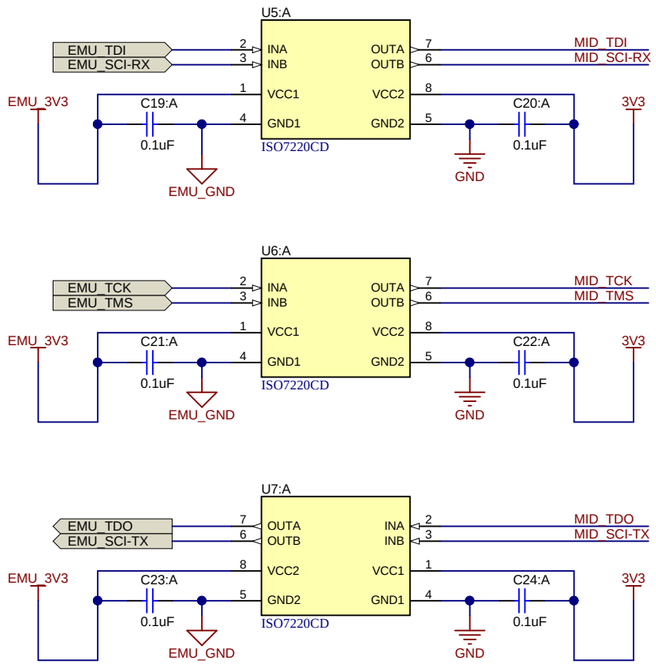
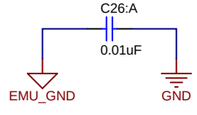




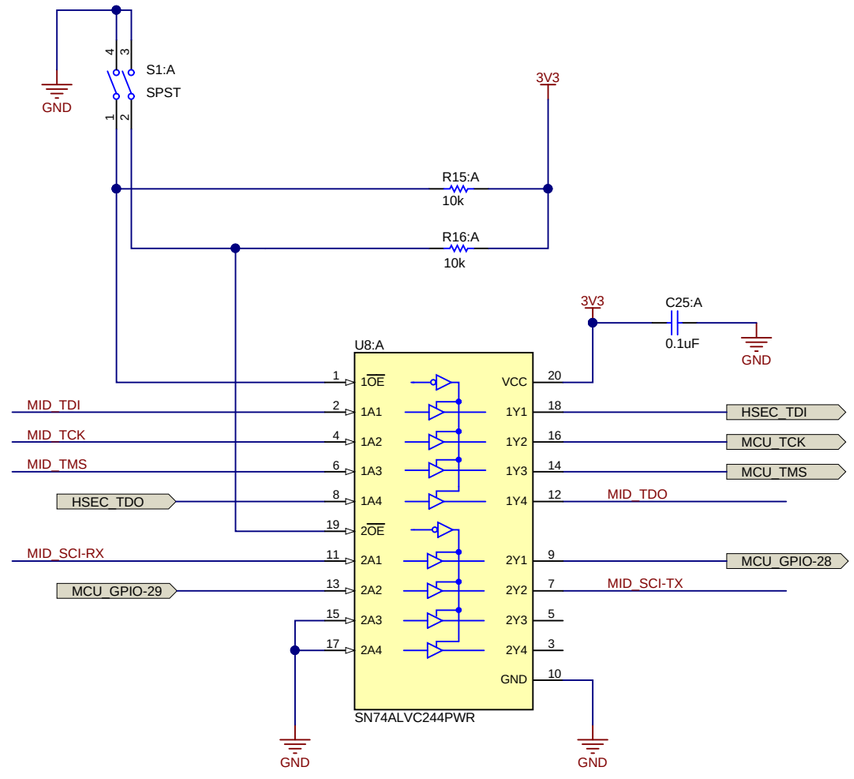
A:SW1 - Emulation & GPIO28 Switch

POS 1 ON: Use xds100v2 emulator that is on the cCARD

POS 1 OFF: Boot from FLASH/peripheral (see boot mode switch) OR use emulator on baseboard

POS 2 ON: GPIO-28 will be controlled by the USB-to-UART adapter on the FTDI chip

POS 2 OFF: GPIO-28 can be controlled by a pin in HSEC connector



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TID #: N/A		Project Title: F280049C controlCARD	
Number: MCU009	Rev: B	Sheet Title: EmuInterface	
SVN Rev: Version control disabled		Assembly Variant: 001	Sheet: 6 of 7
Drawn By:		File: MCU009B_EmuInterface.SchDoc	Size: B
Engineer: Brett Larimore		Contact: http://www.ti.com/support	

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DNP FID1 DNP FID2 DNP FID3 DNP FID4 DNP FID5 DNP FID6

PCB Number: MCU009
PCB Rev: B

PCB LOGO
Texas Instruments

PCB LOGO
WEEE logo

PCB LOGO
FCC disclaimer

CE Mark

ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: TMDSCNCD280049C	Designed for: Public Release	Mod. Date: 3/19/18
TID #: N/A	Project Title: F280049C controlCARD	
Number: MCU009 Rev: B	Sheet Title: EVM Hardware	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 7 of 7
Drawn By:	File: MCU009B_EVM_Hardware.SchDoc	Size: B
Engineer: Brett Larimore	Contact: http://www.ti.com/support	

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