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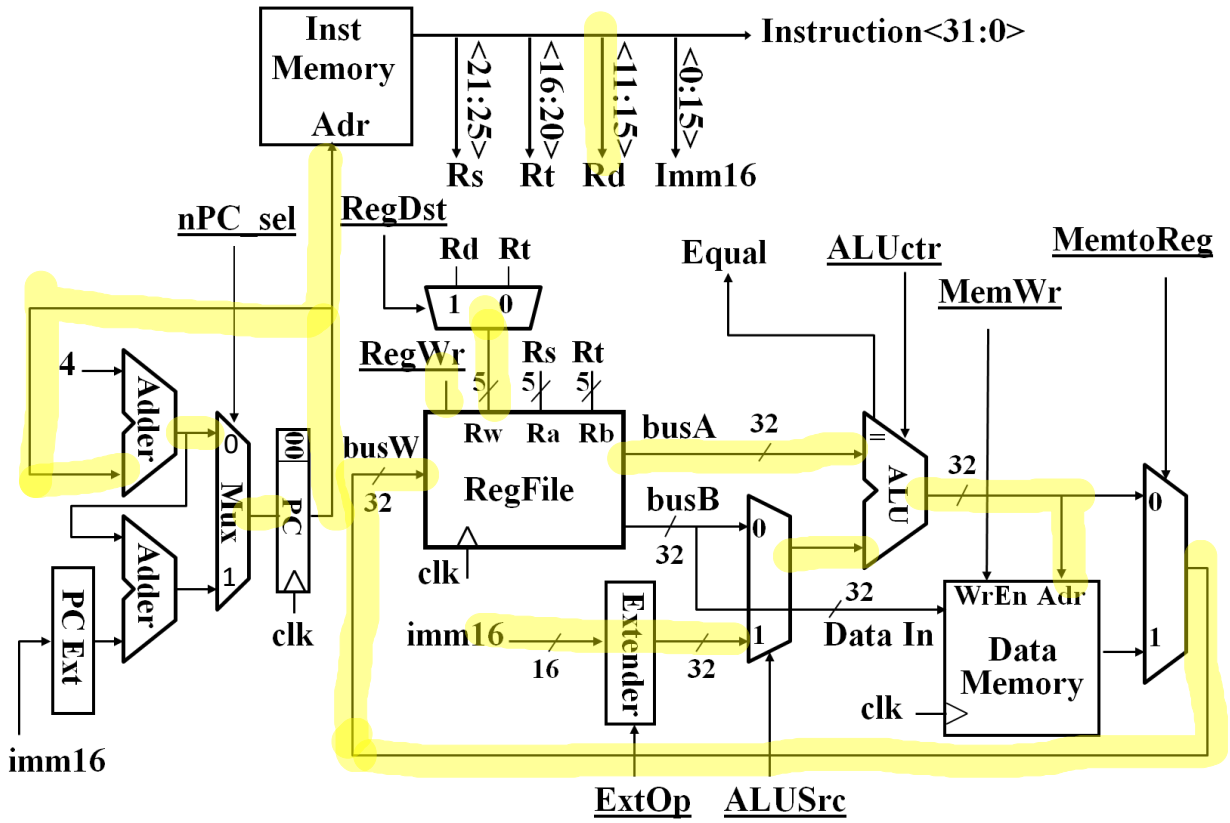
CSE 140

CSE 140 HW #1

Solve the following problems and place your answers in a text document for submission.

1. Trace through the paths the execution of **SLTIU** instruction in this single cycle datapath design. Fill in the appropriate control signal values in the table. If there are any modifications needs to make it work then draw them in the diagram and create appropriate control values.



nPc_sel	ExtOp	ALUsrc	ALUctr	MemWr	MemtoReg	RegDst	RegWr
+4	0	Sub	1	0	1	1	

2. For the problems in this exercise, assume that the breakdown of executed instructions is as follows:

add	addi	not	beq	lw	sw
20%	20%	0%	25%	25%	10%

   a. In what fraction of all cycles is the data memory used?
      Only lw and sw. 25% + 10% = 35% used.
   b. In what fraction of all cycles is the input of the sign-extend circuit needed? What is this circuit doing in cycles in which its input is not needed?
      Sign-extend circuit needed in all except add, so 80%.

3. Problem A.1 from textbook (page A-47)

4. Problem A.2 from textbook (page A-47)

5. Problem A.3 from textbook (page A-47)

A1)

Summation: Instruction category frequency * clock cycles
All ALU instructions: f or add, sub, compare, load immediate, cond move, shift, and xor, or = 48.5%

lw and sw = 37.6%, conditional branches = 10.7%, jumps = 3.0%

total = . 1.24

A2)

All ALU instructions: f or add, sub, mul, compare, load immediate, shift, cond move, and, xor, or = 51.1%

lw and sw frequencies = 35.0%, Conditional branches = 11%, Jumps = 2.8%

total = 1.23

A3)

All ALU instructions: f or add, sub, mul, compare, load immediate, shift, cond move, and, xor, or = 33.0%

lw and sw frequencies = 11.8%, Conditional Branches = 1.0%, Jumps = 0%,

FP add = 14.8%, Load-store FP = 28.1%, Misc FP = 3.0%

total = 2.12