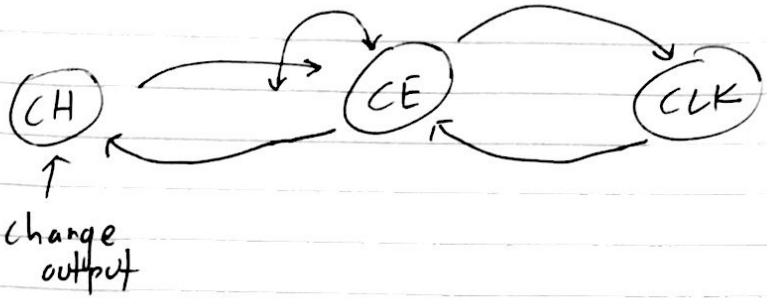
David Wang
Lab 10
CSE 31

collab w/ Diana Dang

Lab #10

① Create FSM

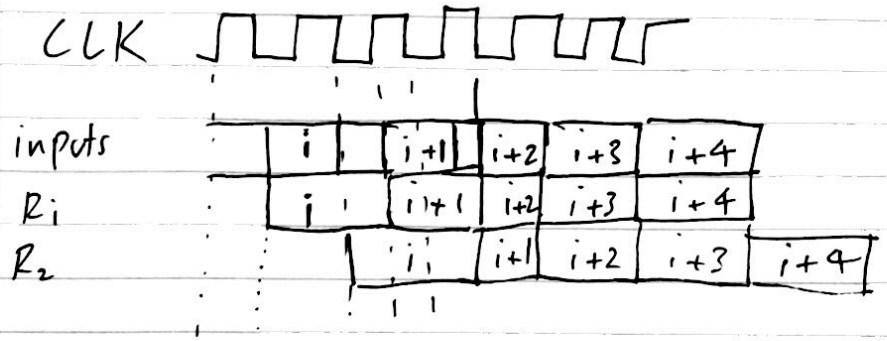


Q's

Q1. 8 bits hence minimum states would be 3

Q2. Relationship between state and outputs is dependent on whether or not CE=0. If CE=0, output change to 00, 01, 10, 11, 00.

② FSM2.C



Q3) Register 2 → 0-8
* initial value was 0

Q4) FSM continually adds the 2 value together, 10 times

Q5) FSM 2.C

```
int operation(int a=0; int b=1;){
    for(int i=0; i<10; i++){
        a+=1;
        b+=1;
    return a;}
```