

Department of Engineering and Computer Science, ECS
California State University, Sacramento CSUS



EEE 232 Key Mixed-Signal IC Blocks Project 2 Report

Fully Differential 4-bit Folding and Interpolating Flash ADC

Author: Vladislav Rykov

Table of Contents

<i>Section 1. Introduction</i>	4
<i>Block Specifications</i>	5
<i>Section 2. Preamplifiers</i>	6
<i>On Voltages (V_{on})</i>	6
<i>Gain</i>	7
<i>Common Mode Voltage</i>	8
<i>Connections</i>	8
<i>Section 3. Folding Blocks</i>	9
<i>On Voltages (V_{on})</i>	9
<i>Gain</i>	10
<i>Current Mismatches</i>	10
<i>Section 4. Folding Blocks Output Latches</i>	11
<i>Clock Frequency</i>	11
<i>Section 5. DNL</i>	11
<i>Folding Blocks</i>	12
<i>Output Latches</i>	13
<i>Conclusion</i>	13
<i>Figures</i>	14
<i>Project Schematic</i>	55

Section 1. Introduction

Present project report describes the work of design and simulation of a fully differential 4-bit folding and interpolating flash ADC.

Flash ADC is one of the common topologies used for ADC design. It provides the fastest comparison times on the cost of low-to-medium accuracy. It concurrently compares the input signal to all references, thus requiring larger number of area and power. The number of overall comparators for a straight flash ADC is $2^n - 1$ where n is the ADC resolution in bits. Another significant limitation is the input capacitance which grows exponentially with the resolution.

Tireless efforts were put into improvement of the straight flash ADC topology. Since the input comparators and latches were design points with the highest cost, the direction of improvement was clear. To reduce the number of input comparators the interpolation technique was proposed. Instead of having one comparator per reference voltage, a resistor averaging can be used to deduce intermediate voltages. The technique successfully reduced the number of input comparators. However, it introduced non-linearity when the interpolating factor is greater than 2. On the other hand, it also potentially reduces the overall ADC accuracy. Due to the ‘tagging’ effect, marginal inputs are shifted towards the center of the ADC range, thus increasing the DNL. That effect is attenuated adding extra preamplifiers on the top and bottom of the ADC range, thus ‘tagging back’ interpolation outputs.

Second improvement was focused on the number of latches used in the design. Folding technique was proposed, compressing portions of the ADC range into blocks capable of performing multiple simultaneous comparisons.

The present project covers the use of both improvements. It is split into various sections. First, preamplifier stages will be discussed in Section 1. Section 2 covers folding blocks key points and design nuances. Section 3 briefly discusses the output latches. Section 4 presents the DNL results for the folding blocks and latches. Finally, a brief meditation is provided in the conclusion section.

Block Specifications

Specification	Value
The voltage gain and differential pair Von for each preamplifier	Voltage gain = 2 Von = 205.5 mV
The number of extra preamplifiers needed to properly terminate each preamp stage	1 stage – 0 preamplifiers 2 stage – 1 preamplifier 3 stage – 2 preamplifiers
Values for the reference voltages needed for the first stage of preamplifiers	Vref1p = 1.457 V, Vref1n = 1.143 V Vref2p = 1.343 V, Vref2n = 1.257 V Vref3p = 1.229 V, Vref3n = 1.371 V Vref4p = 1.114 V, Vref1n = 1.486 V
The voltage gain and differential pair Von for the folding circuits	Voltage gain = 1.468 (folding block output peak at 304.858 mV) Von = 26.7 mV
Maximum mismatch allowed between the tail current sources in the folding circuits	Accounting 0.1 LSB for folding block errors, the mismatch can be up to 150 uA through load resistors (taking all errors on one folding

	block) or 50 uA per folding block.
The maximum input signal frequency for the entire preamp and folding block array	ADC input – 0.5 GHz Folding blocks frequency – 2.5 GHz

Section 2. Preamplifiers

On Voltages (V_{on})

Preamplifier stages is an important part of the interpolation. As previously described, the interpolation reduces the number of comparators used in the design. The improvement implies the voltage distance between two successive comparators to grow. Thus, it is necessary for a designer to account for it, and that is reflected in the on-voltages of the preamps.

The voltage distance grows with each stage according to the Equation 1.

$$V_{distance} = V_{LSB} * (\text{interpolation factor})^{stage} \quad (1)$$

where $V_{distance}$ is the voltage distance between two successive comparators/preamps and V_{LSB} is the LSB voltage.

$V_{distance}$ between two successive preamps on the highest interpolation stage will become V_{ON} for the higher limit for preamps' transistors. Actual V_{ON} should not exceed the $V_{distance}$ to achieve better results through the ‘tagging’ effect. On the other hand, the amount of V_{ON} affects the number of extra preamps required for proper termination of each preamp array. As V_{ON} grows, the number of extra preamps does grow too. For a straight flash ADC, there is no need for extra preamps, and V_{ON} can be equal to V_{LSB} . With each additional interpolation stage V_{ON} grows proportionally to the

$V_{distance}$. Since the gap between the preamps grows, there need to be extra preamps for proper termination of the array. Otherwise, DNL will increase significantly through heavy ‘tagging’ of preamps at the edges of the array.

For the present project, three stages of interpolation with factor of two were determined.

The other side of the coin is the ADC range that, in turn, determines the Least Significant Bit (LSB) size. The ADC range strongly depends on the ADC reference voltage. For the differential reference of 400 mV, the whole reference is 800 mV. Since the reference 28-resistor ladder that determines the actual LSB size was provided with the design skeleton, the LSB size can be easily

computed for a given ADC range. Therefore, for the present project, $V_{LSB} = \frac{800 \text{ mV}}{28} = 28.571 \text{ mV}$.

Given the V_{LSB} , *interpolation factor*, and *stage*, $V_{distance} = 28.571 \text{ mV} * 2^3 = 228.571 \text{ mV}$.

The on voltage for the preamp stages was decided to be 205.5 mV.

Gain

To keep output voltage consistent on each preamp stage, every preamp needs to amplify the input voltage according to interpolation factor on that stage. In other words, the interpolation factor dictates proportionally the magnitude of gain. To tune the preamp for a desired gain, several degrees of freedom can be exploited: differential pair load resistance, differential pair and bias current transistors dimensions, and the amount of bias current.

Finding a precise combination of all three factor is an iterative complex process with manifold dependencies and trade-offs. As transistors dimensioning, variation of transconductance, affects their on voltages, that in turn can narrow or widen the ADC range and modify the common mode voltage.

After a proper dimensioning of the MOSFETs, the gain of two has successfully been set for all preamp stages. Figure 1 shows DC sweep of the third preamp in the first stage of interpolation. Please, refer to Figures 2, 3, and 4 to see the output curves of each preamp stage.

Common Mode and Reference Voltages

Every preamplifier is constituted by a differential pair whether it compares input signal to reference or to zero. A fully operating condition of a preamp is achieved keeping all its MOSFETs in saturation. Hence, it is highly important to make sure that all preamp FETs are in saturation. It is also worth to mention that during this process a decision on the ADC range is taken.

The process was addressed iteratively running a bias test simulation in which a preamp was led to its operating point, setting equal input voltages on both sides of the preamp.

Bias transistors dimensions need to be high in order to provide enough current for the rest of the differential pair components. The rest of the transistors should have the lowest gate size to increase the preamp's operating frequency. Finally, the technology library VDD also ceils the input voltage on the preamp FETs. With these limitations in mind, the process of increasing reference voltage and re-dimensioning the FETs continues until a desired configuration has been reached.

Connections

One of the confusing parts of the project was the connection of preamp stages. In a case of straight flash ADC, the connection is straightforward as there is one preamp per LSB. Having multiple stages of preamps adds extra preamps on the borders of each stage.

The easiest way to address this problem is to start designing a straight ADC, and then go adding one interpolation stage at a time, from the last to the first stage. A need for additional preamps at each stage will become evident as the intermediate voltages will get tagged by its neighboring connections. Extra preamps at each stage loosen ‘tagging’ effect, and, that way, reduce output errors.

With interpolating factor of two, one extra preamp is a required minimum. Adding more preamps will result in less output errors. Continuing the design process, on the next stage of preamps (second), the distance between LSBs doubles, thus requiring extra preamps on both, the second and the third, stages. Finally, the first stage will be laid on the second one without need of extra preamps. However, it could not be the case for a different setting of interpolating factor and number of preamp stages.

Please, refer to the Connections page of the PSPICE project to see the preamps connections.

Section 3. Folding Blocks

On Voltages (V_{on})

Folding blocks and preamp stages use the same fundamental component – differential pair. However, the way they are used is based on different principles. In contrast to preamps, differential pairs must have a tail current steered to one side completely. The rule of thumb is to make the differential pair steer completely on one side when input voltage is greater than $2*V_{on}$. This rule works well will all cases. After a careful study, the amount the following formula from Equation 2 was derived.

$$V_{ON_{min}} = \frac{V_{input\ range}}{Number\ of\ Zero\ Crossings} \quad (2)$$

where $V_{input\ range}$ is the ADC one-sided input range, and *Number of Zero Crossings* is the total number of zero crossings throughout all folding blocks.

For the present project $V_{ON_{min}} = \frac{400\ mV}{15} = 26.67\ mV$. Actual V_{ON} can be increased when folding factor is greater than two. A derivation for real limits of V_{ON} is reflected in the Equation 3.

$$V_{ON} = [V_{ON_{min}}, V_{ON_{min}} * (1 + \frac{Folding\ Factor - 2}{2})] \quad (3)$$

Figure 2 shows the outputs of all three folding blocks during the DC sweep test.

Gain

Folding blocks gain is not of the highest importance, as there is no need to set it precisely. Folding block outputs need to be captured by output latches. Therefore, minimum accuracy of the output latch finally dictates how the folding blocks gain should accommodate.

For the present project, the gain equal to 27 was established.

Current Mismatches

Current mismatches are one of the error sources of folding flash ADC circuits. In practice, it shifts a corresponding zero crossing left or right from its predetermined position, therefore increasing the overall DNL of the ADC. Analog designer should always be aware of and account for these errors as the current source mismatches frequently appear as fabrication defects.

Section 4. Folding Blocks Output Latches

Clock Frequency

Designing latches for flash ADCs, it is necessary to estimate their clock frequency which is subject to input signal frequency. Since the folding blocks can ‘oscillate’ before becoming stable, this overhead sets the design bottleneck. Since the folding factor is five for the present project, it can be asserted that the folding blocks outputs work on a frequency that is five times greater than the input signal frequency.

After a number of iterative simulations, it was deduced that the ADC can handle input signals of 0.5 GHz with folding blocks operating at 2.5 GHz.

Section 5. DNL

Following MATLAB code was used to measure the DNL of the folding blocks and output latches.

```
clear all
close all

% size LSB in mV
LSB = 800/28;
% ideal codes positions
ideal = -200:LSB:200;
% real zero crossing locations for folding blocks and
% output latches
real_fold = [-181.4    -158      -136.6   -111.7   -83.691 -
55.1     -28       -1.3275   27.3    55.2    79.83   101.3   124.9
148.5    171.061];
real_ltch = [-181.096 -157.806 -136.128 -111.216 -83.671 -
54.706 -27.566 -0.829531 27.3    55.686  80.193  101.867
125.153 148.852 171.544];
```

```

% Making DNL
[DNL_fold, DNL_LSB_fold] = get_DNL_LSB(real_fold, ideal,
LSB);
[DNL_ltch, DNL_LSB_ltch] = get_DNL_LSB(real_ltch, ideal,
LSB);

% Making plots
figure(1)
plot(DNL_fold, 'b'), xlabel('Code'), ylabel('DNL'),
title('Figure 22. Folding Blocks DNL plot'), grid on, axis
equal, legend("Folding Blocks DNL")
figure(2)
plot(DNL_ltch, 'r'), xlabel('Code'), ylabel('DNL'),
title('Figure 40. Output Latches DNL plot'), grid on, axis
equal, legend("Output Latches DNL")
figure(3)
x = 1:14;
plot(x, DNL_fold, x, DNL_ltch), legend("Folding Blocks
DNL", "Output Latches DNL"), xlabel('Code'),
ylabel('DNL'), title('Figure 41. Folding Blocks DNL
plot'), grid on, axis equal

% Helper function to compute DNL in LSBs
function [DNL, DNL_LSB] = get_DNL_LSB(real, ideal,
lsb_size)
    INL = ideal - real;
    DNL = INL(2:end) - INL(1:end-1);
    DNL_LSB = max(abs(DNL))/lsb_size;
end

```

Folding Blocks

Please, refer to Figure 5 to see the “big picture” of all folding blocks outputs, Figure 6 for zero crossings, and Figures 7 through 21 to see zoomed-in individual zero crossings.

DNL of 0.251 LSB was achieved. It can be improved tuning separately each preamp stage. The majority of errors are due to the zero crossings at the end of last stage preamps array as the Figure

22 shows.

Output Latches

One important thing for the measurement of DNL was the alignment of latches' clock frequency with the input signal frequency. In a case of unaligned frequency, the output latches DNL will drastically grow as the distance between a corresponding folding block zero crossing and where the latch captured it increases. Since there were no constraints on the input signal frequency, it was decided that the input signal frequency will be reduced enough to achieve a fine alignment.

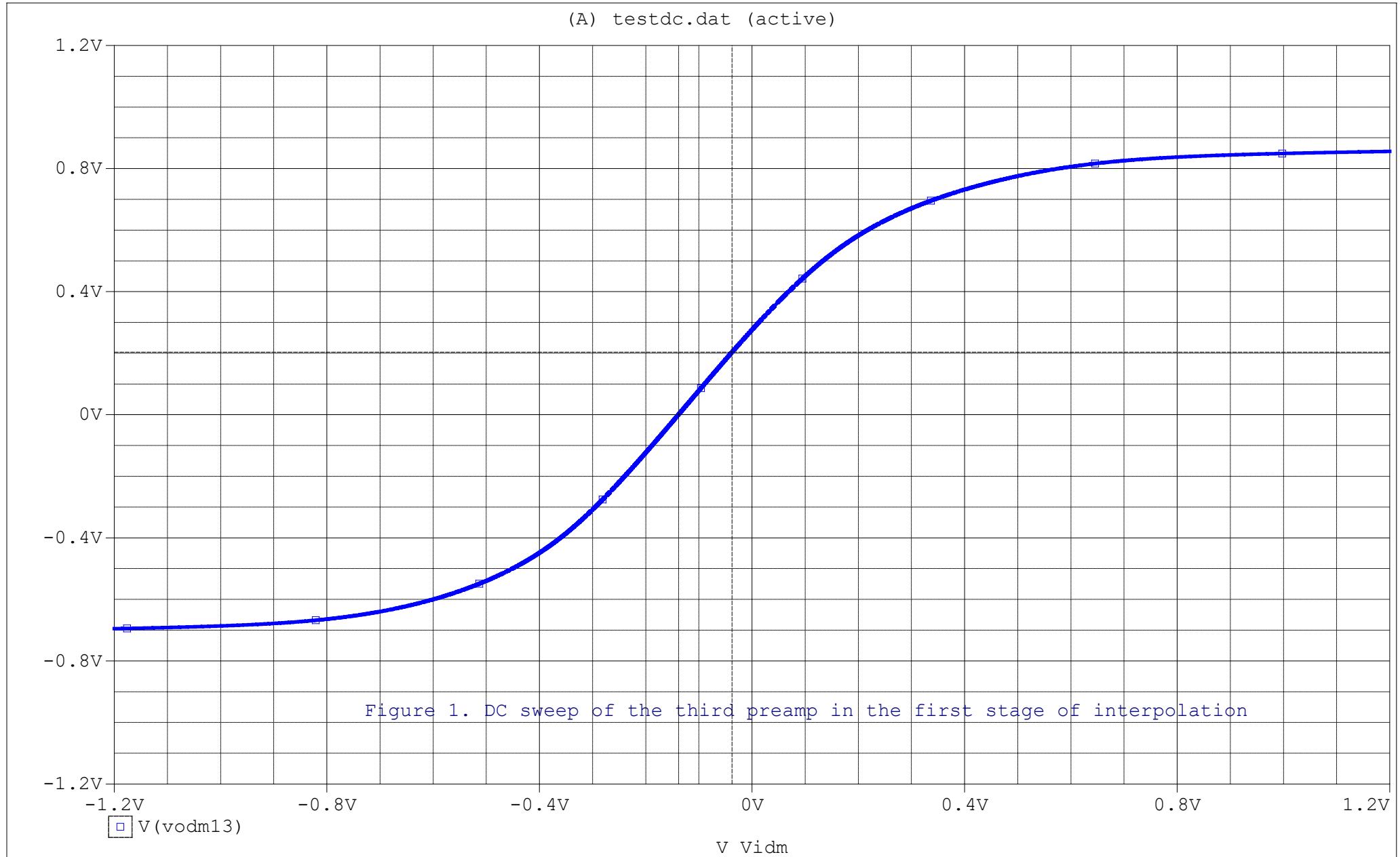
Figure 23 presents a “big picture” of the latches output, input signal, and folding blocks outputs. Figure 24 show a zoomed-in version of the latches zero crossings. Finally, Figures 25 through 39 show isolated zero crossings for the output latches.

DNL of 0.2414 was measured. Figure 40 shows the DNL plot and Figure 41 shows the both DNL for the folding blocks and the output latches.

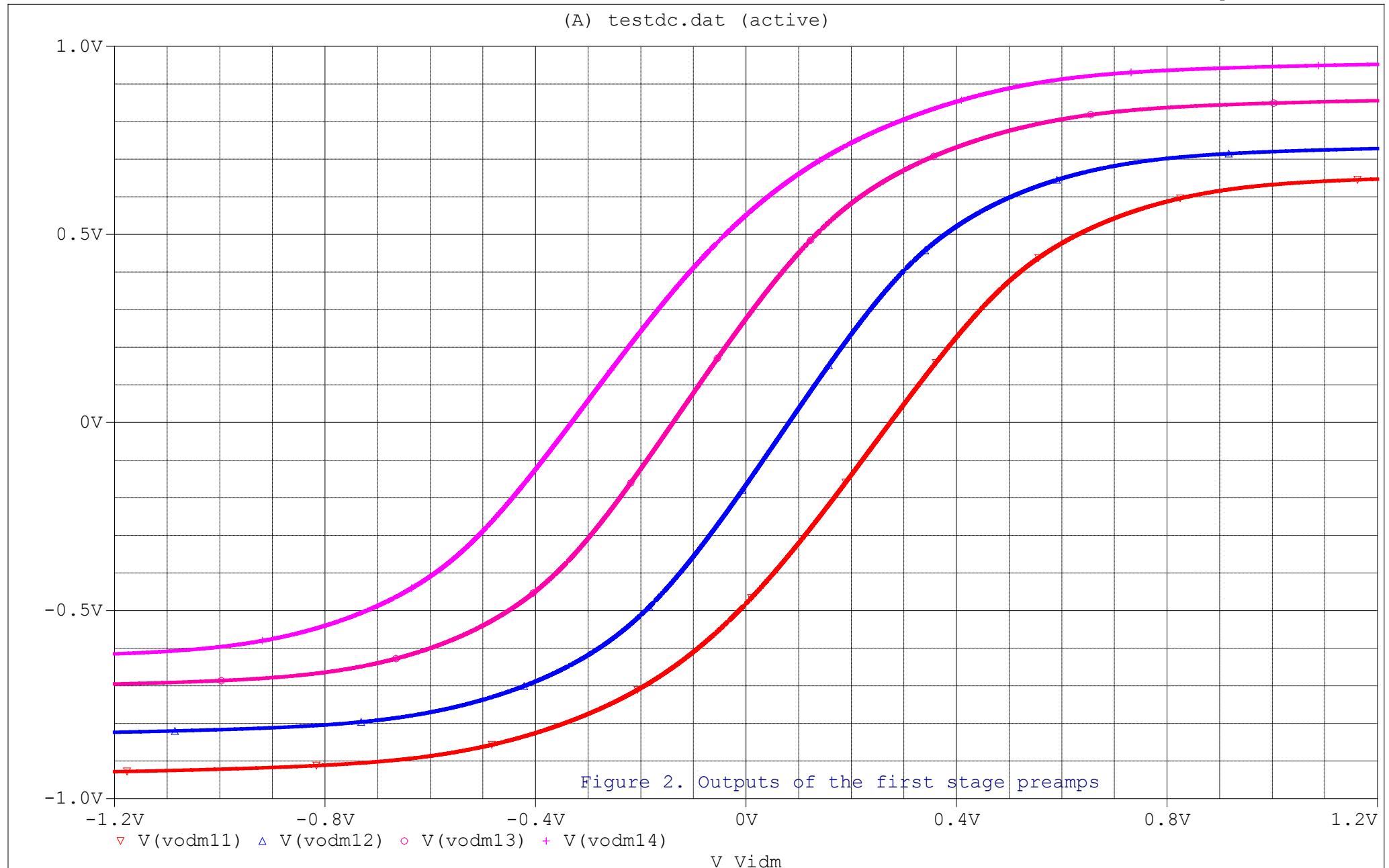
Section 6. Conclusion

This report described the results of design and simulation of an interpolating and folding flash ADC. It was a vary laborious project in which numerous degrees of freedom had to align to get a desired result. Construction of appropriate interpolation stages, tuning of preamplifiers, scrutinizing through folding blocks, adding analog latches were deeply explored, and the theory was put in practice. DNL of 0.251 was achieved on the folding blocks outputs.

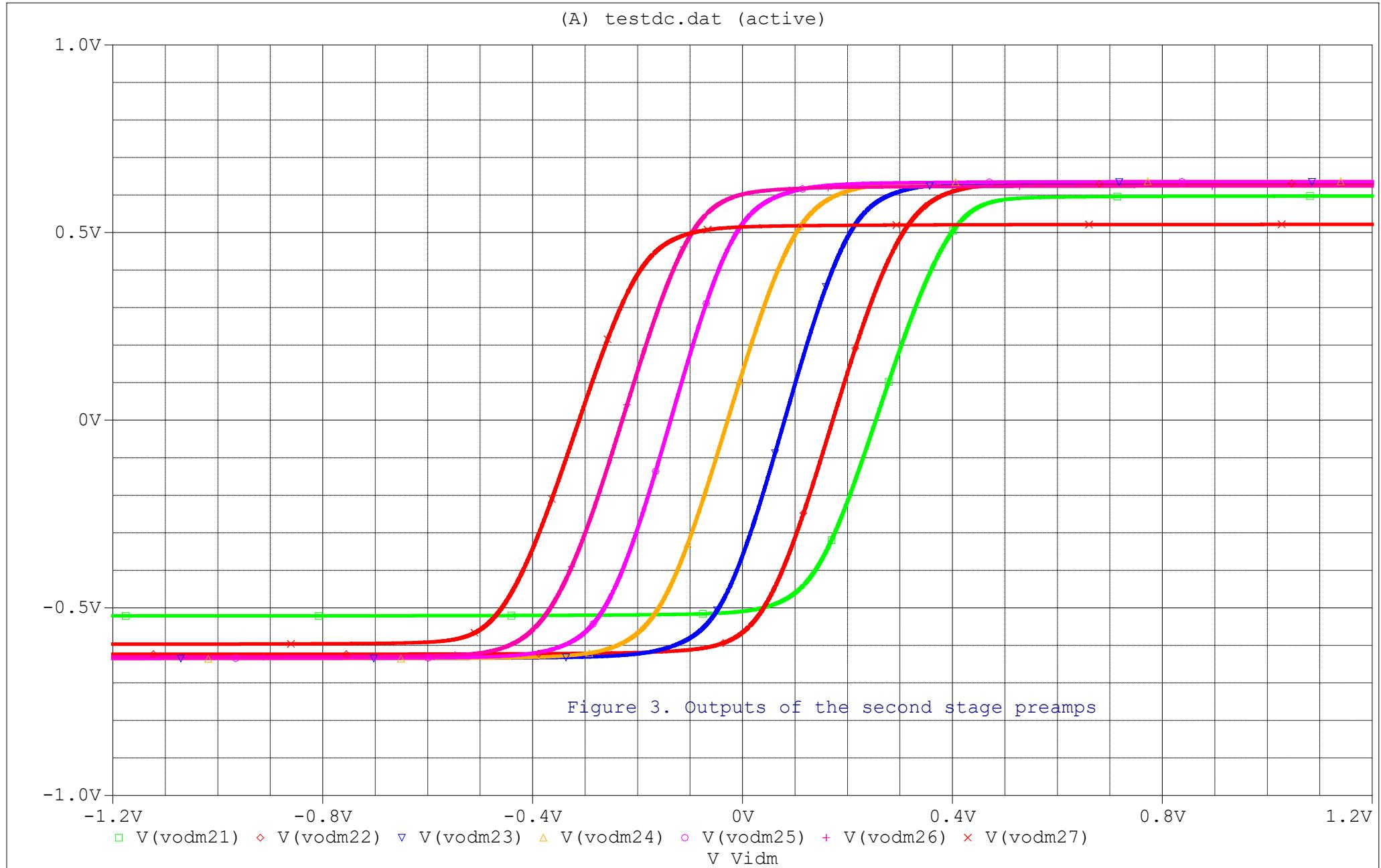
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



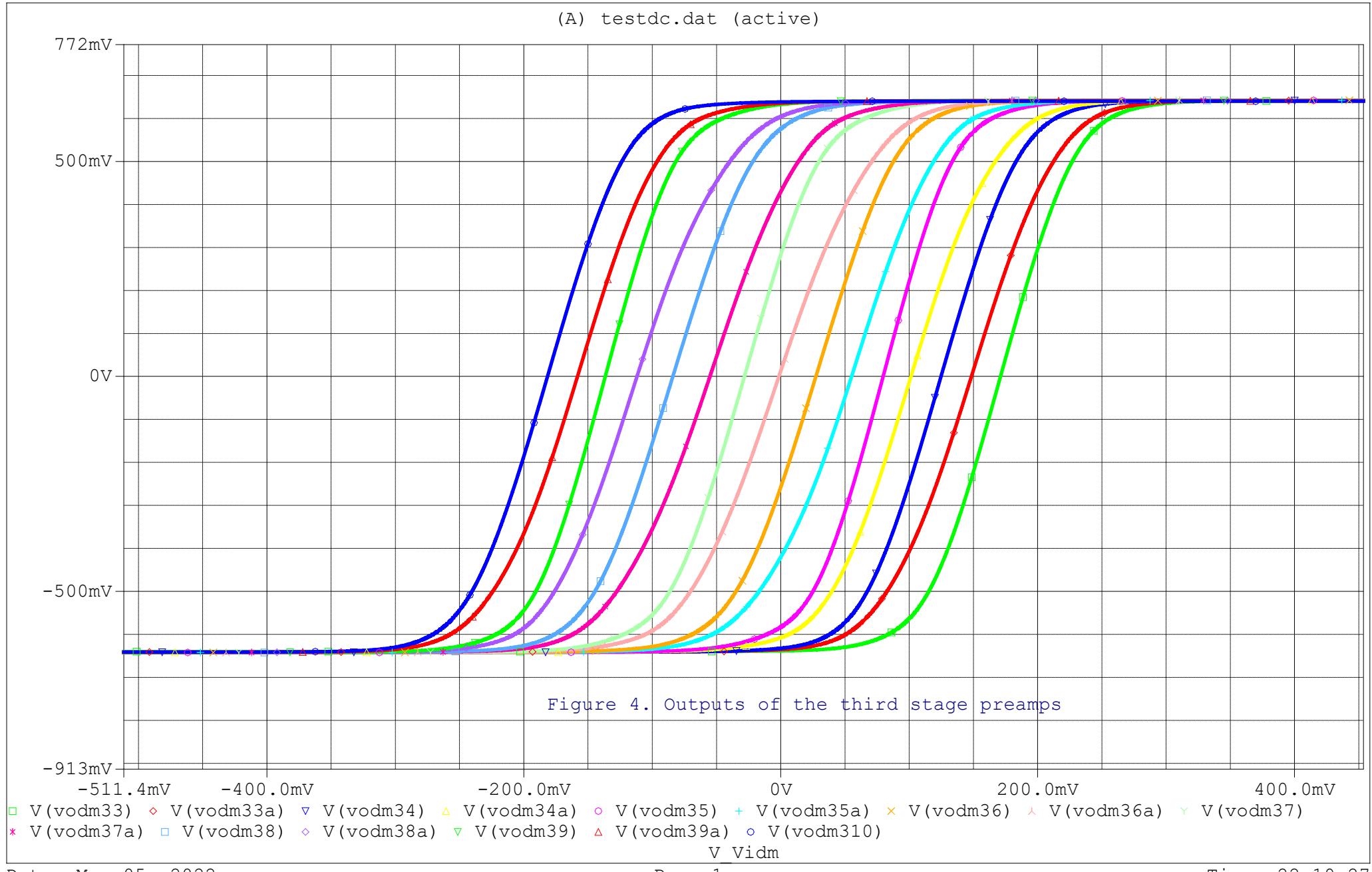
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



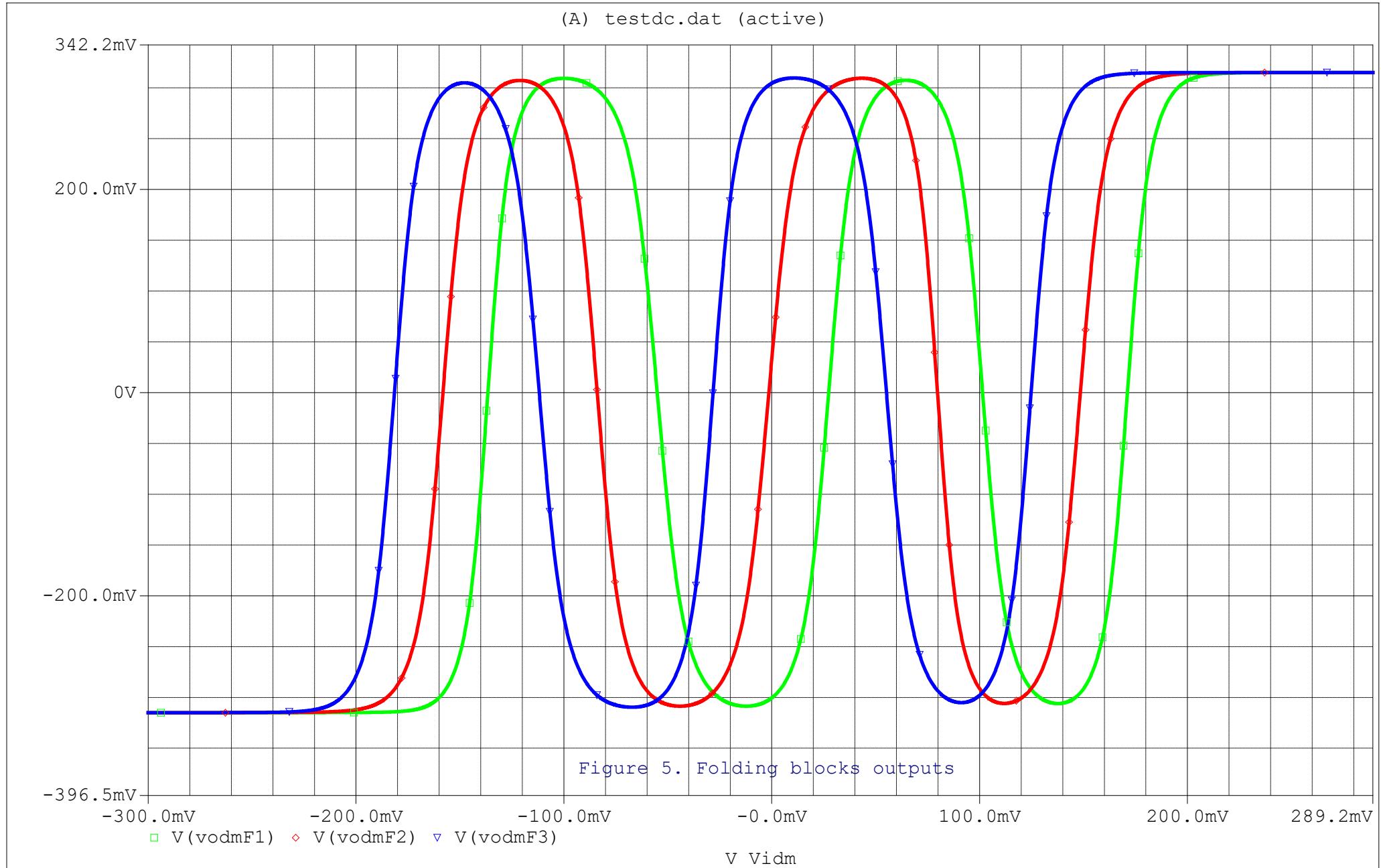
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



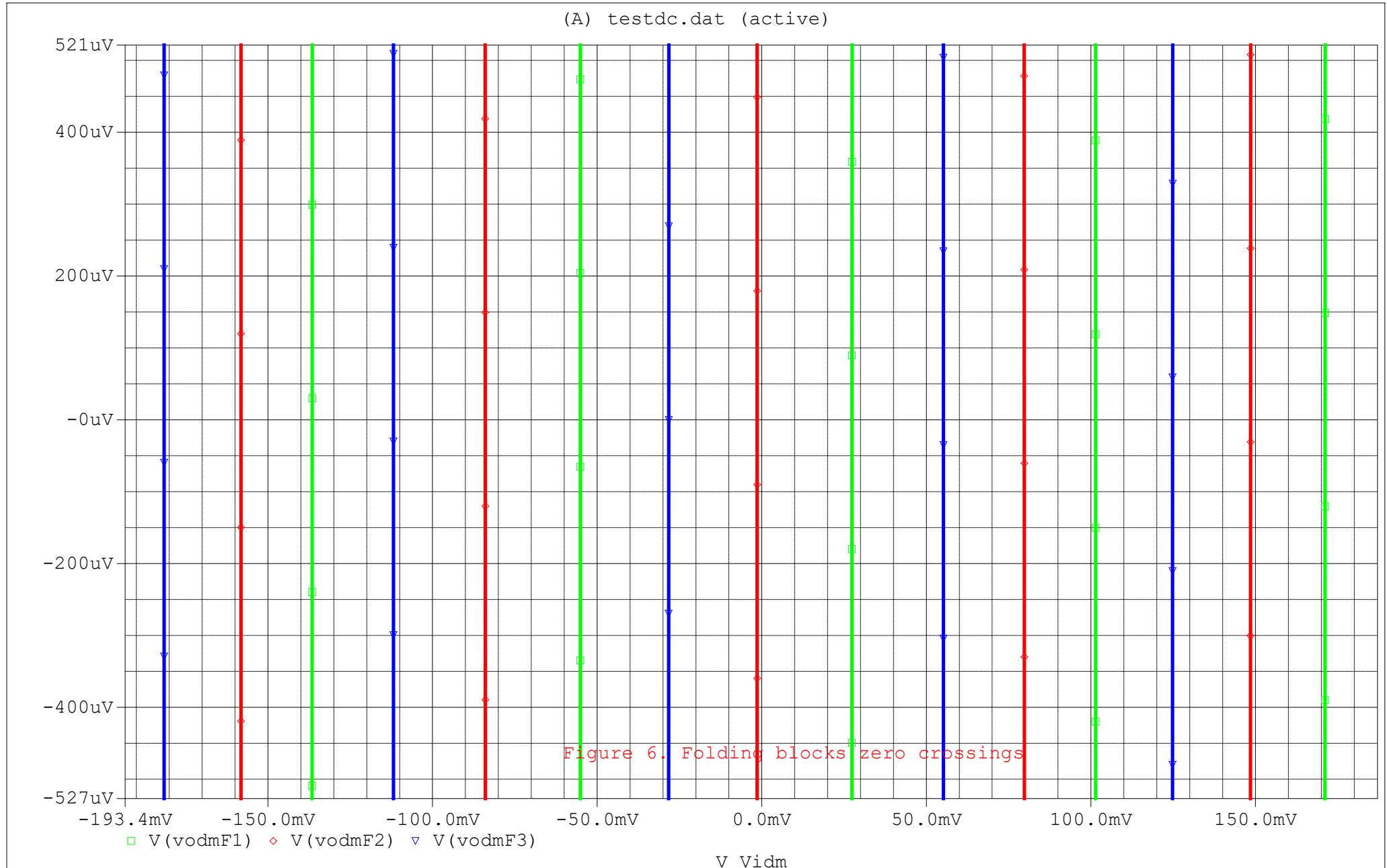
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



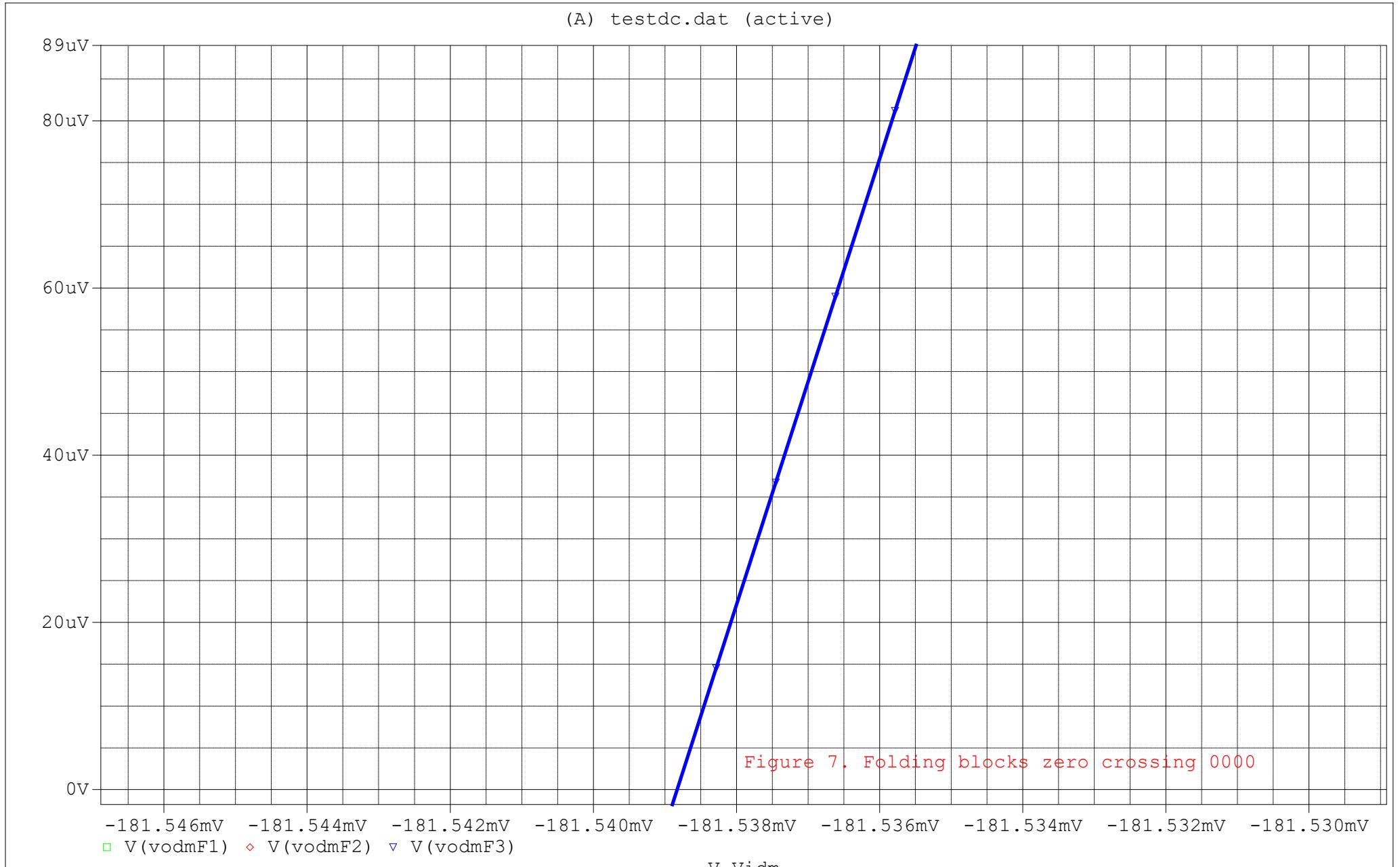
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



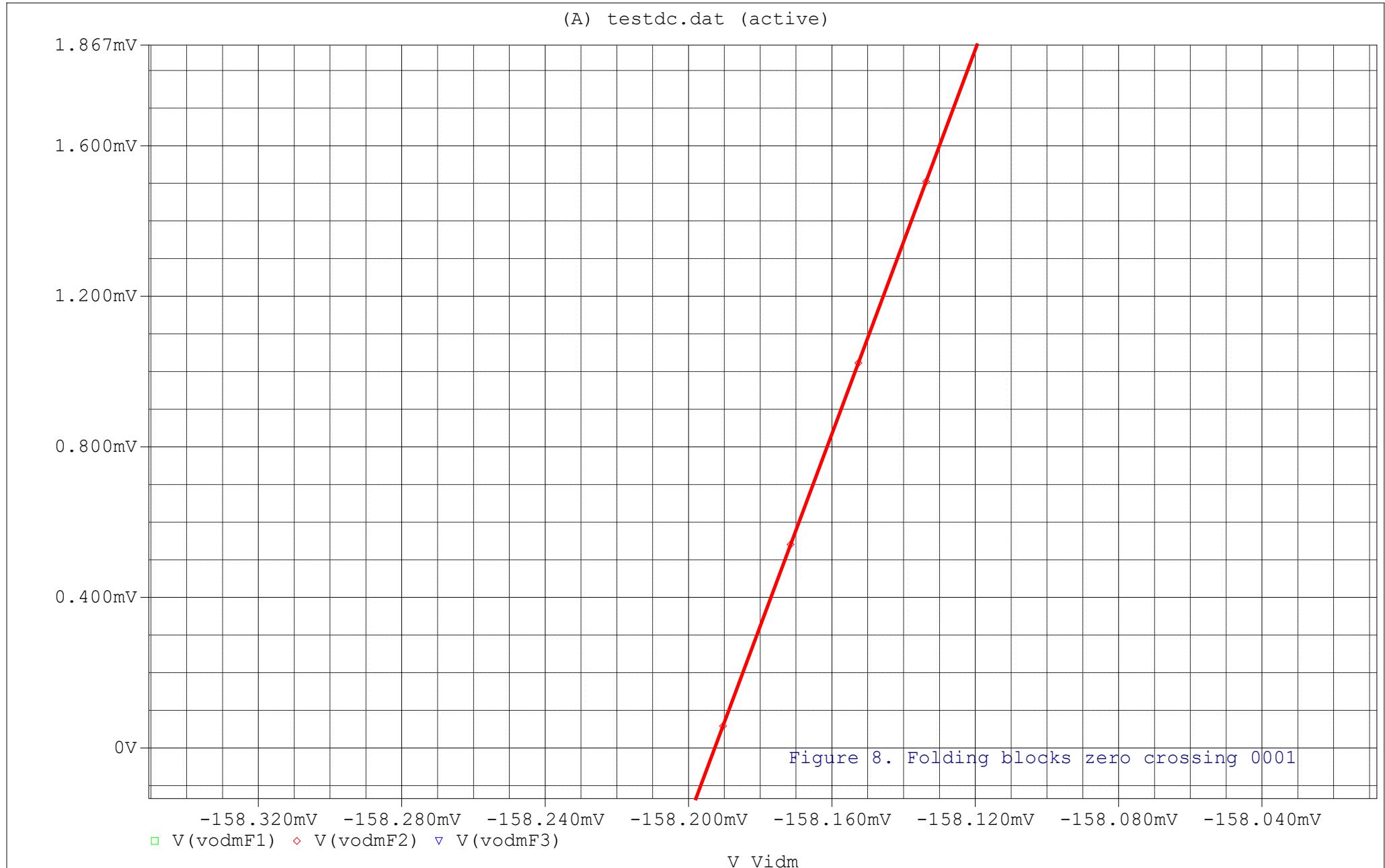
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



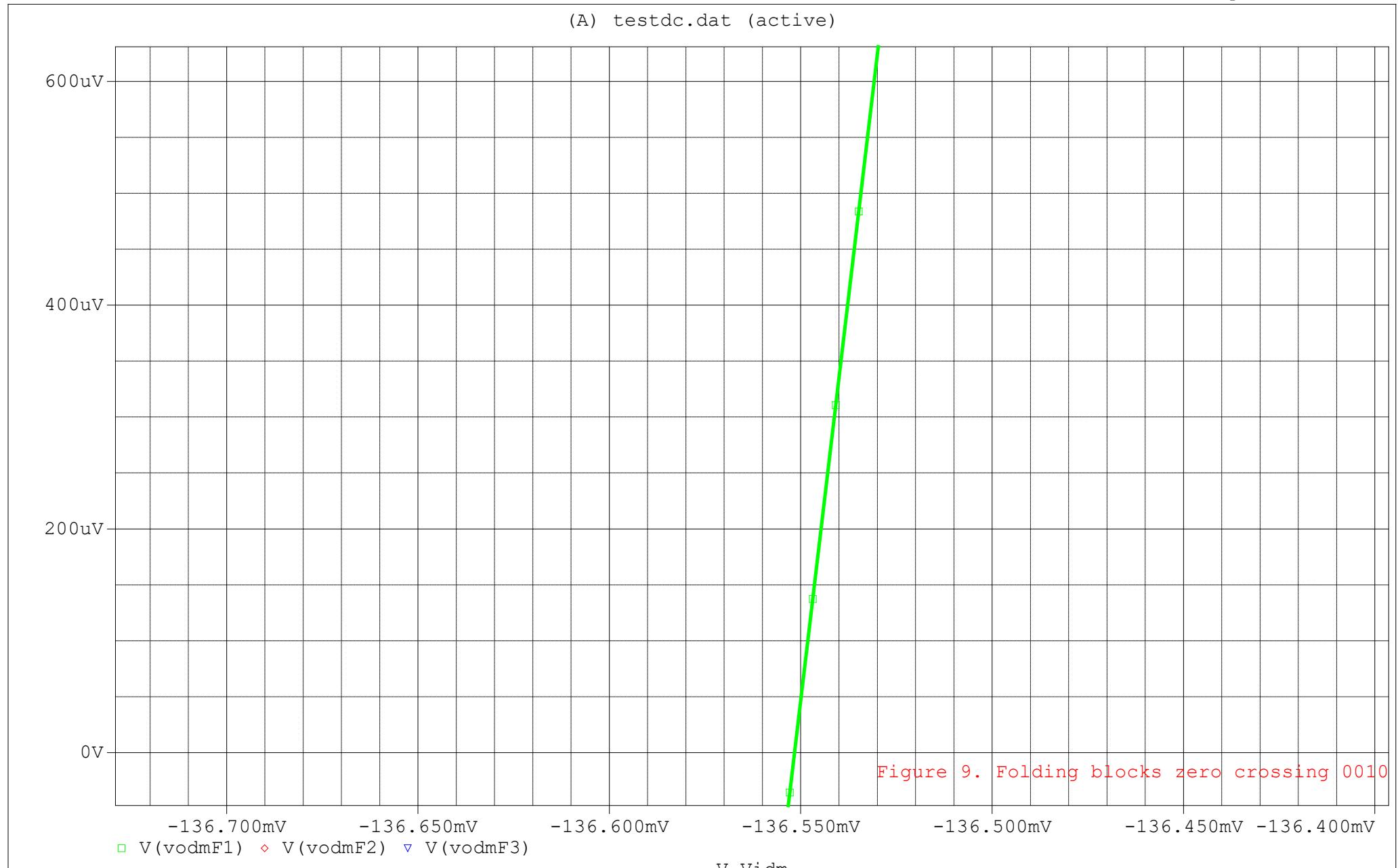
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



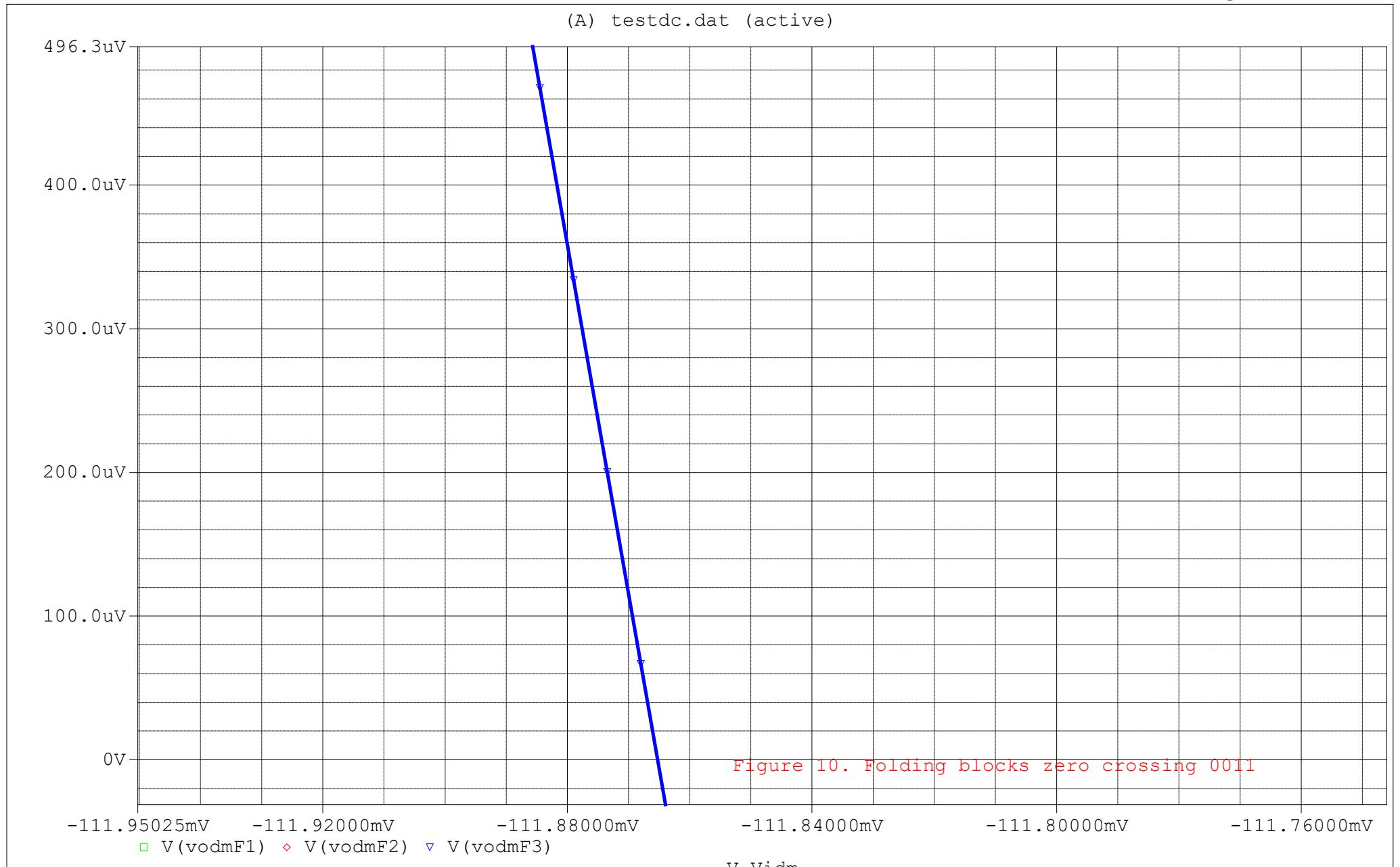
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



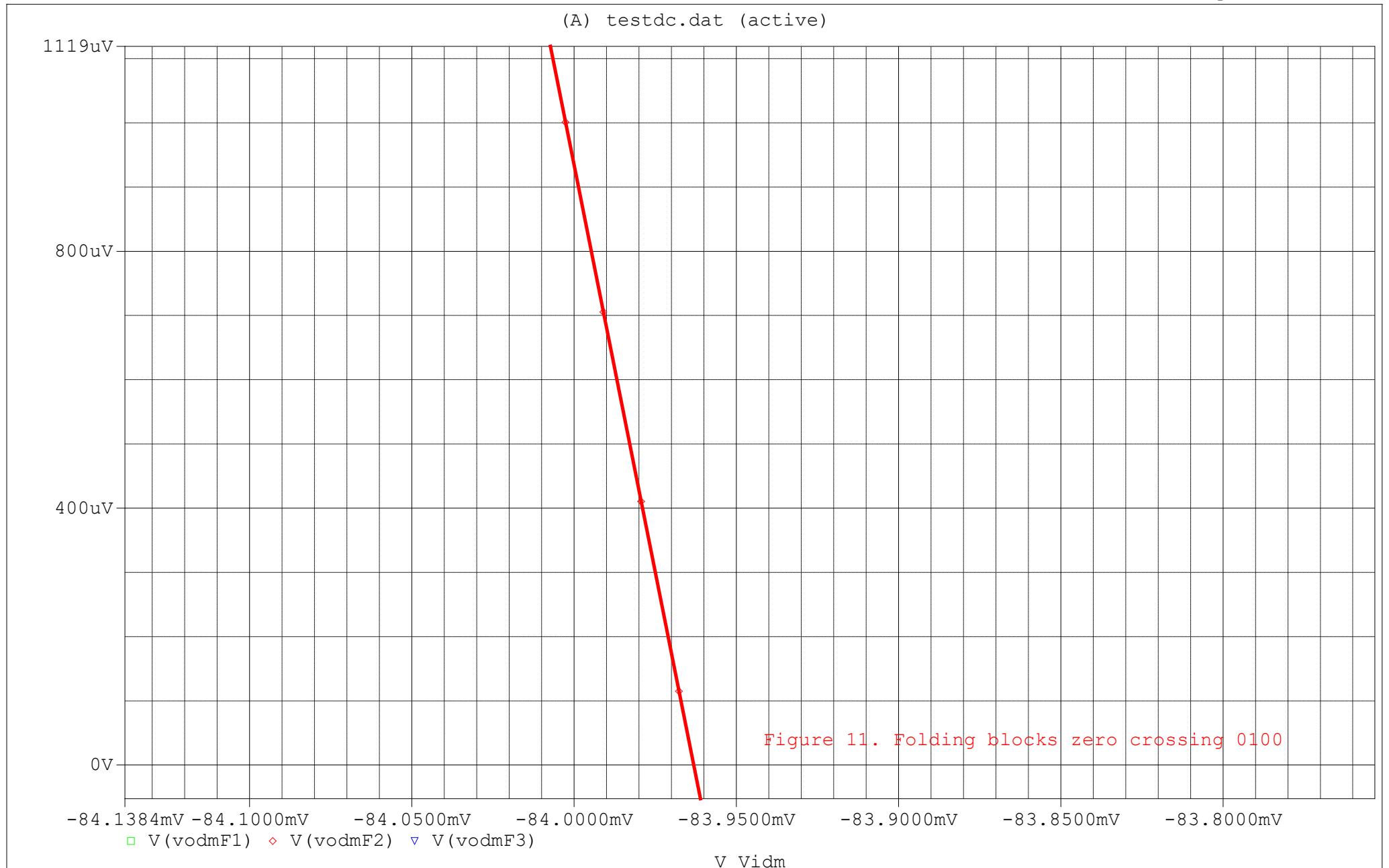
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



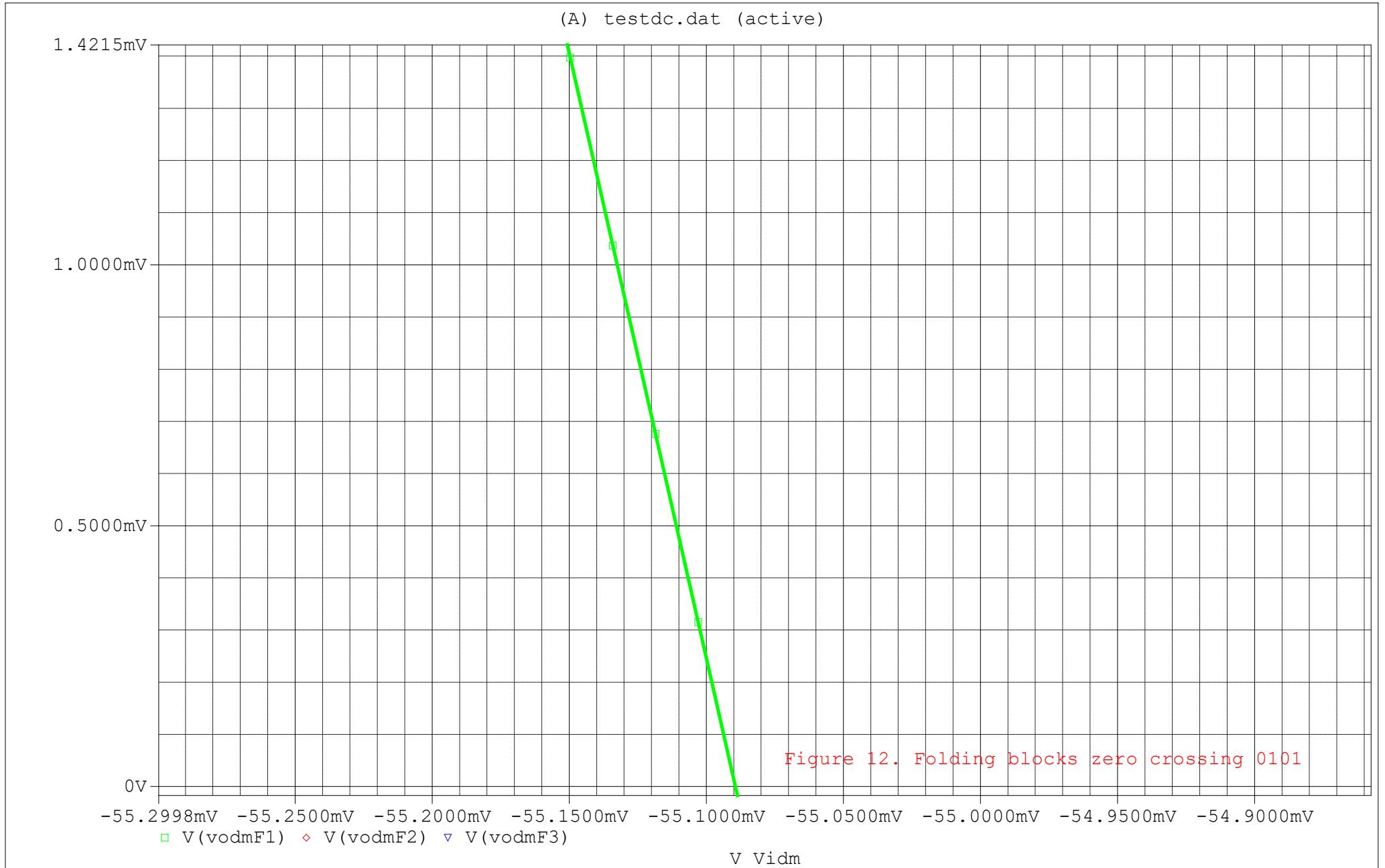
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



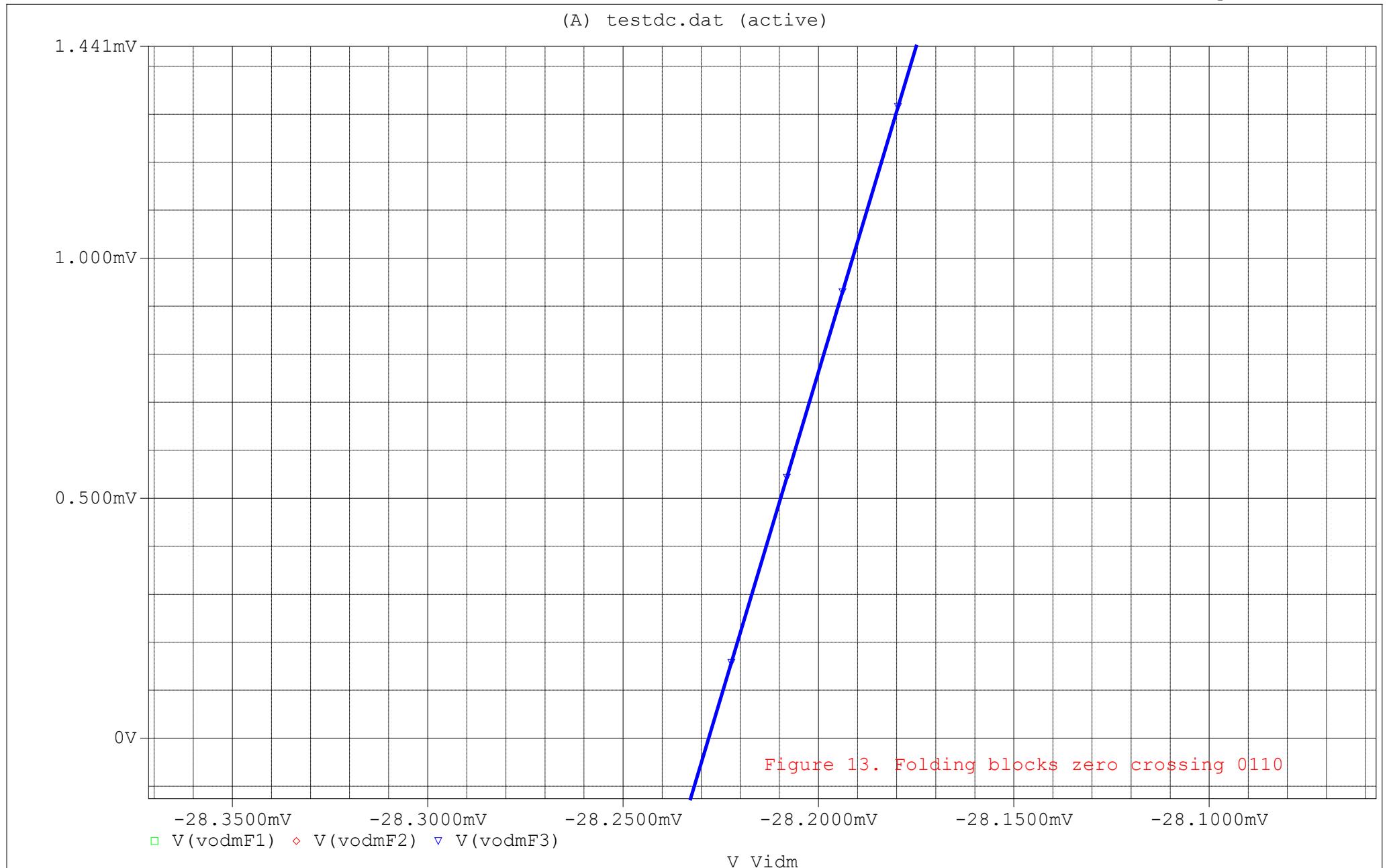
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



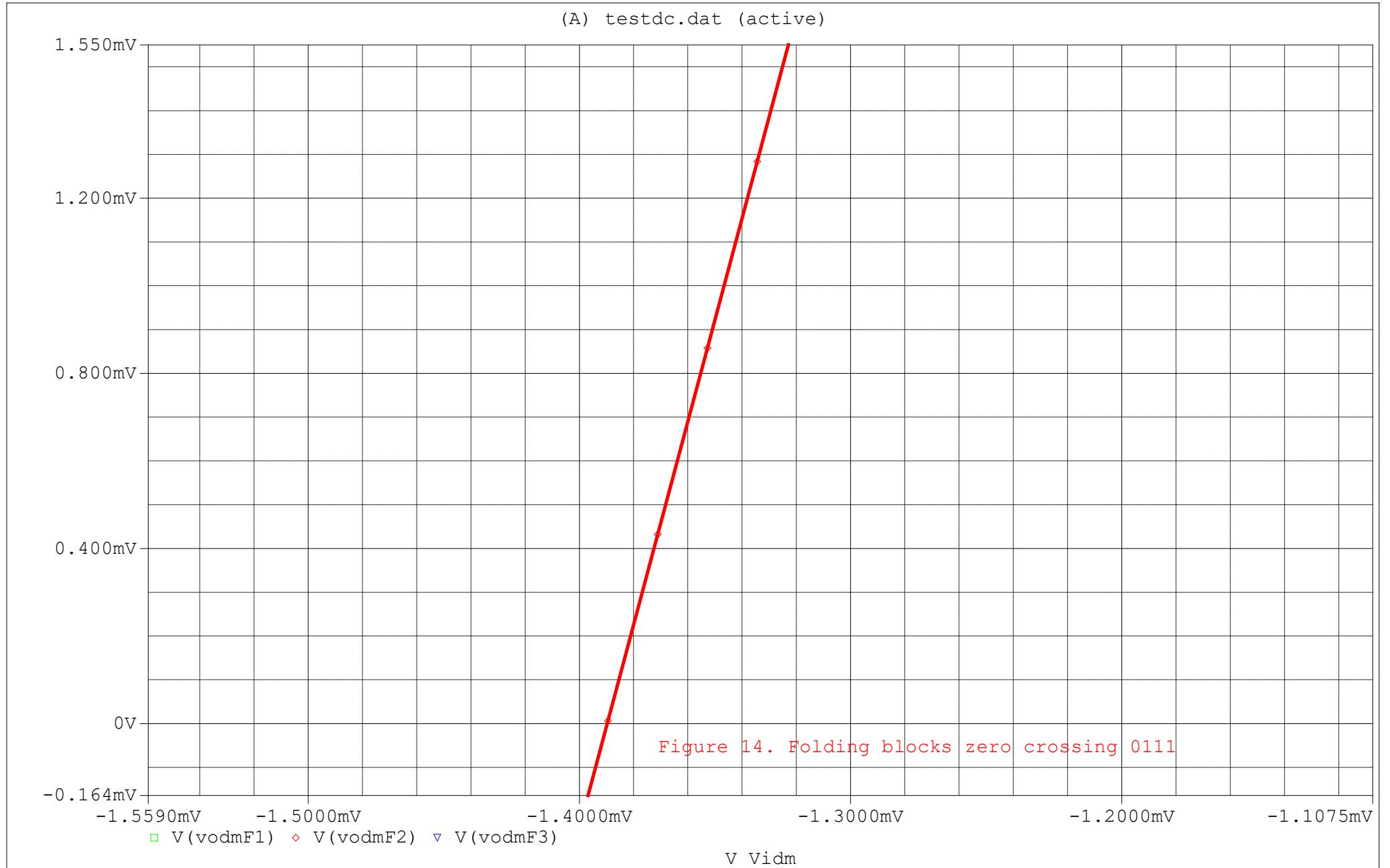
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



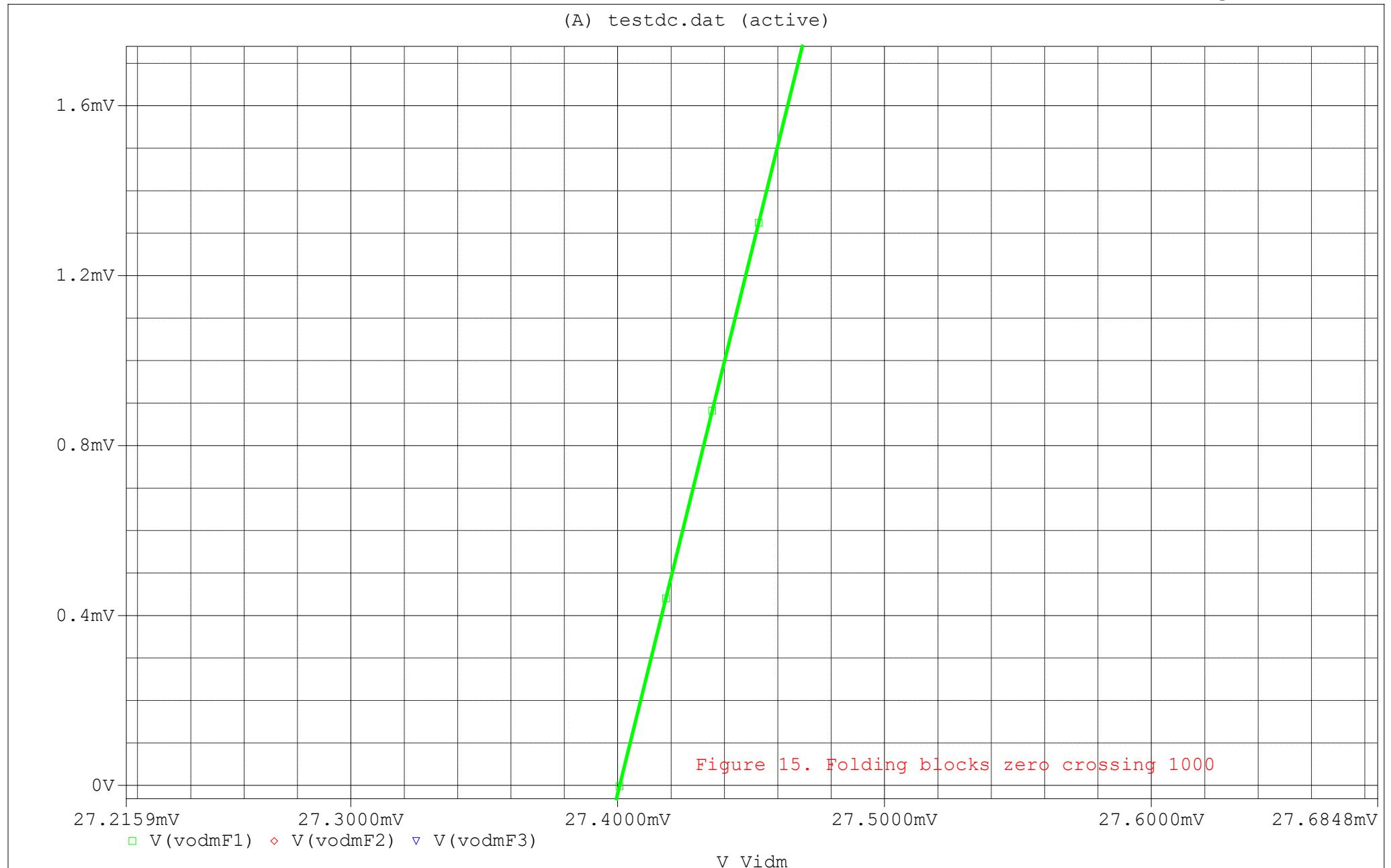
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



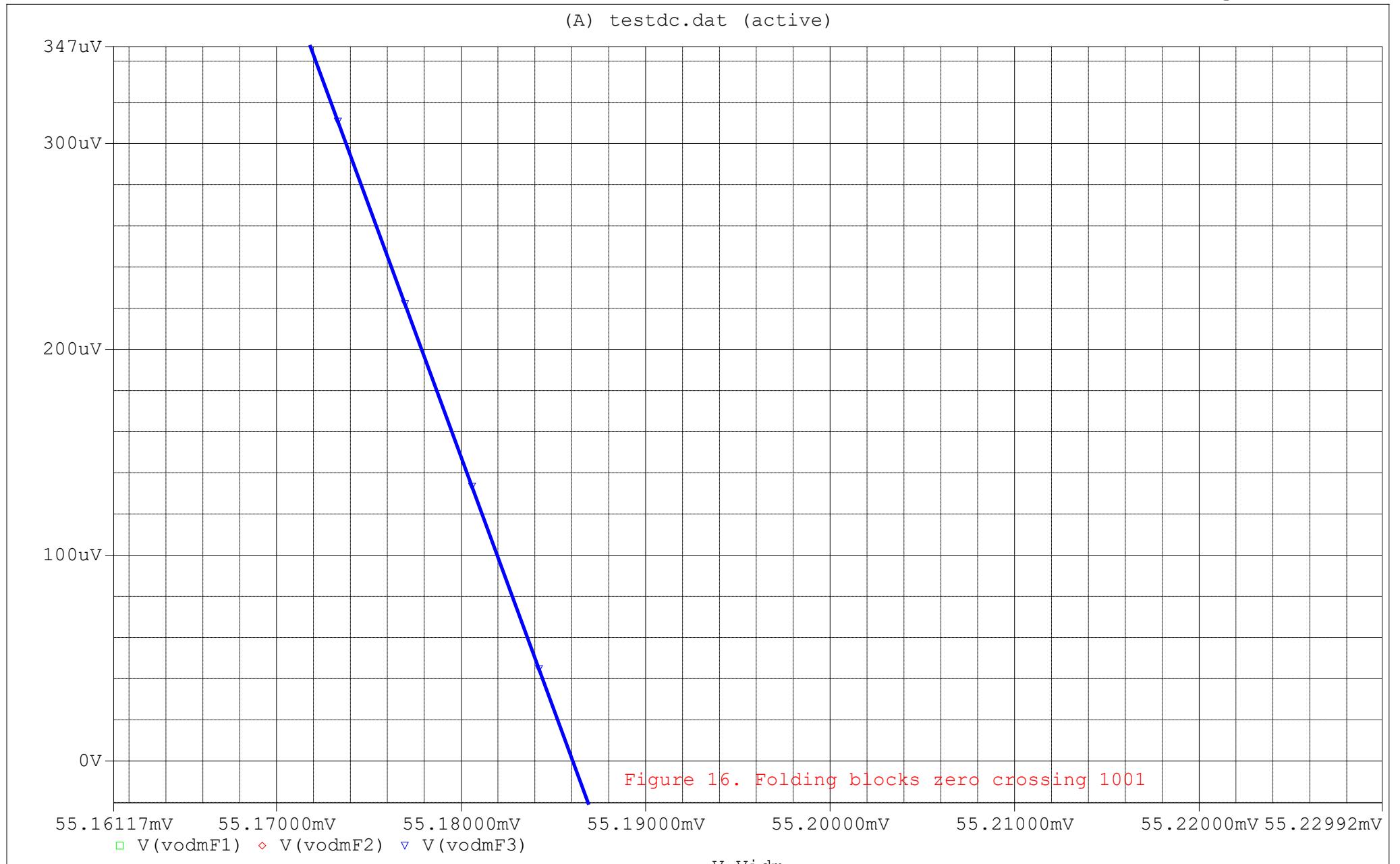
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



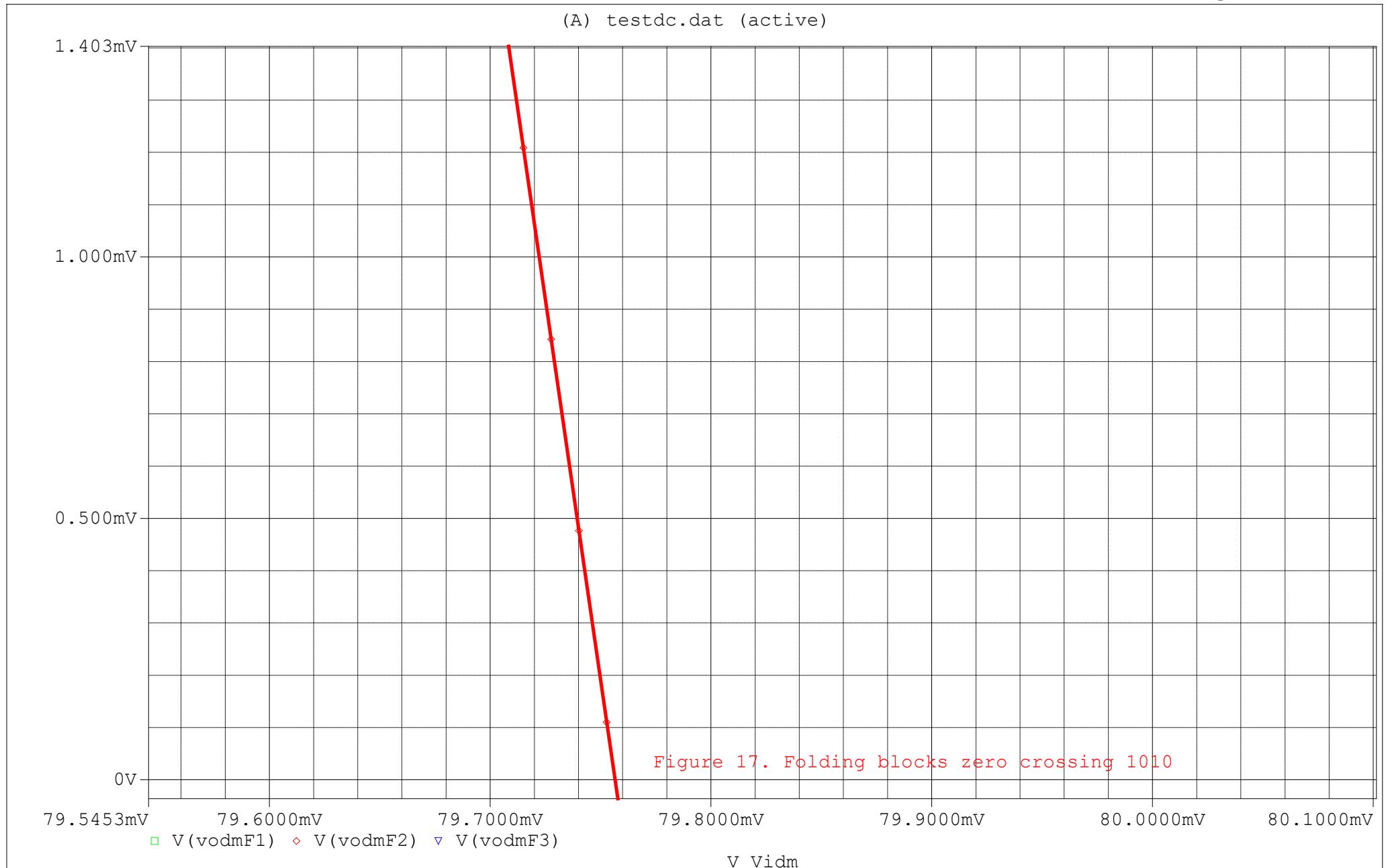
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



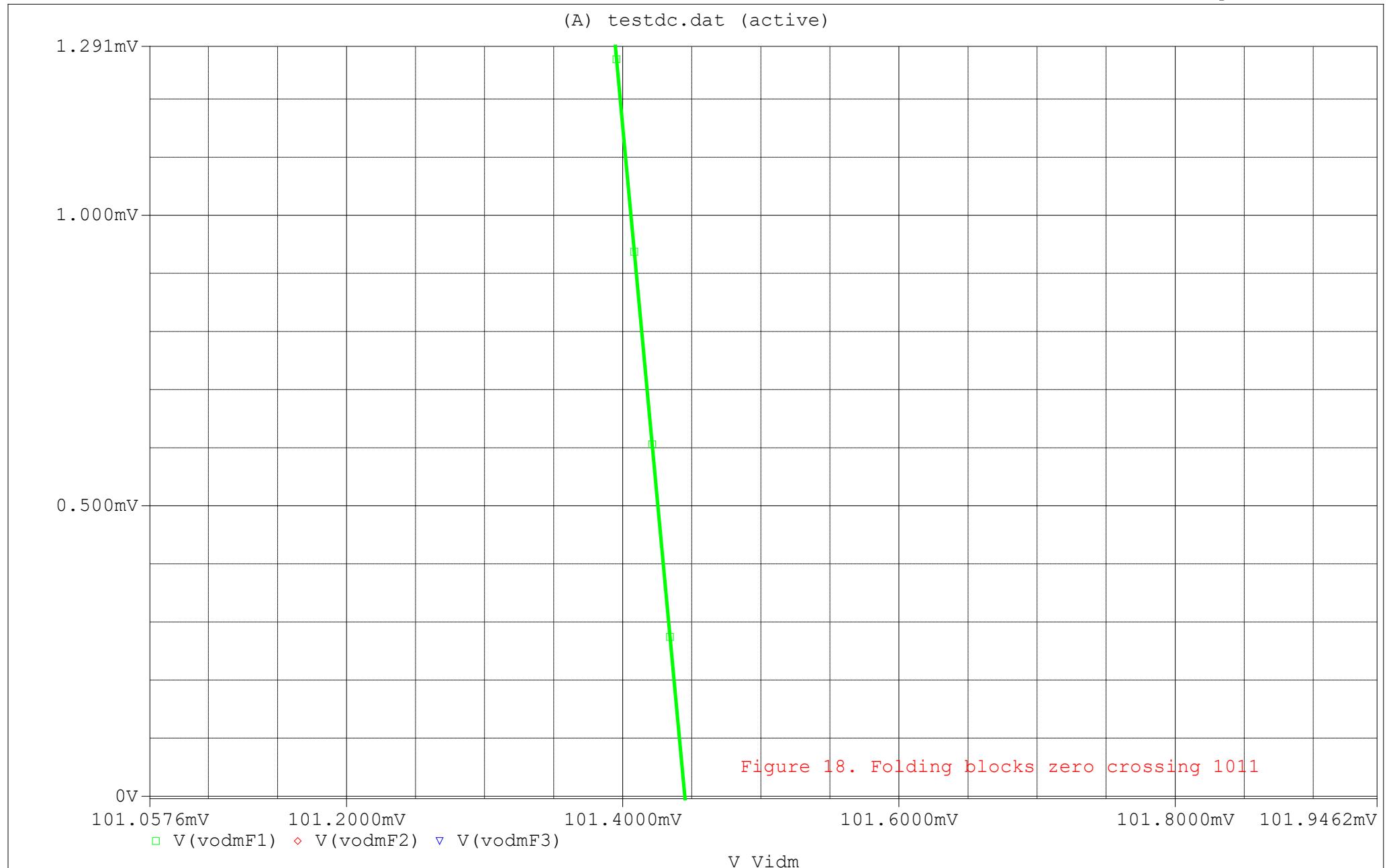
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



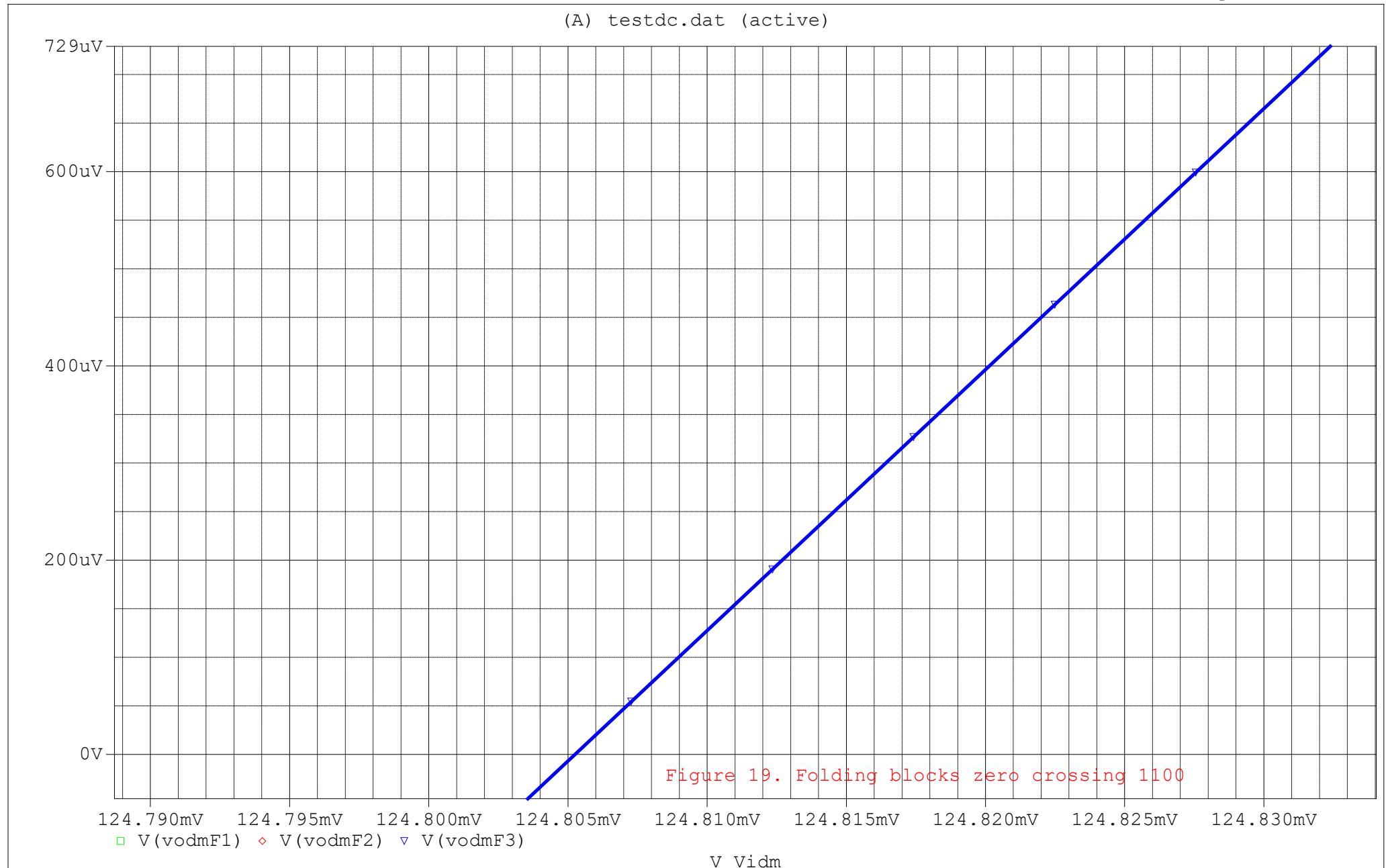
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



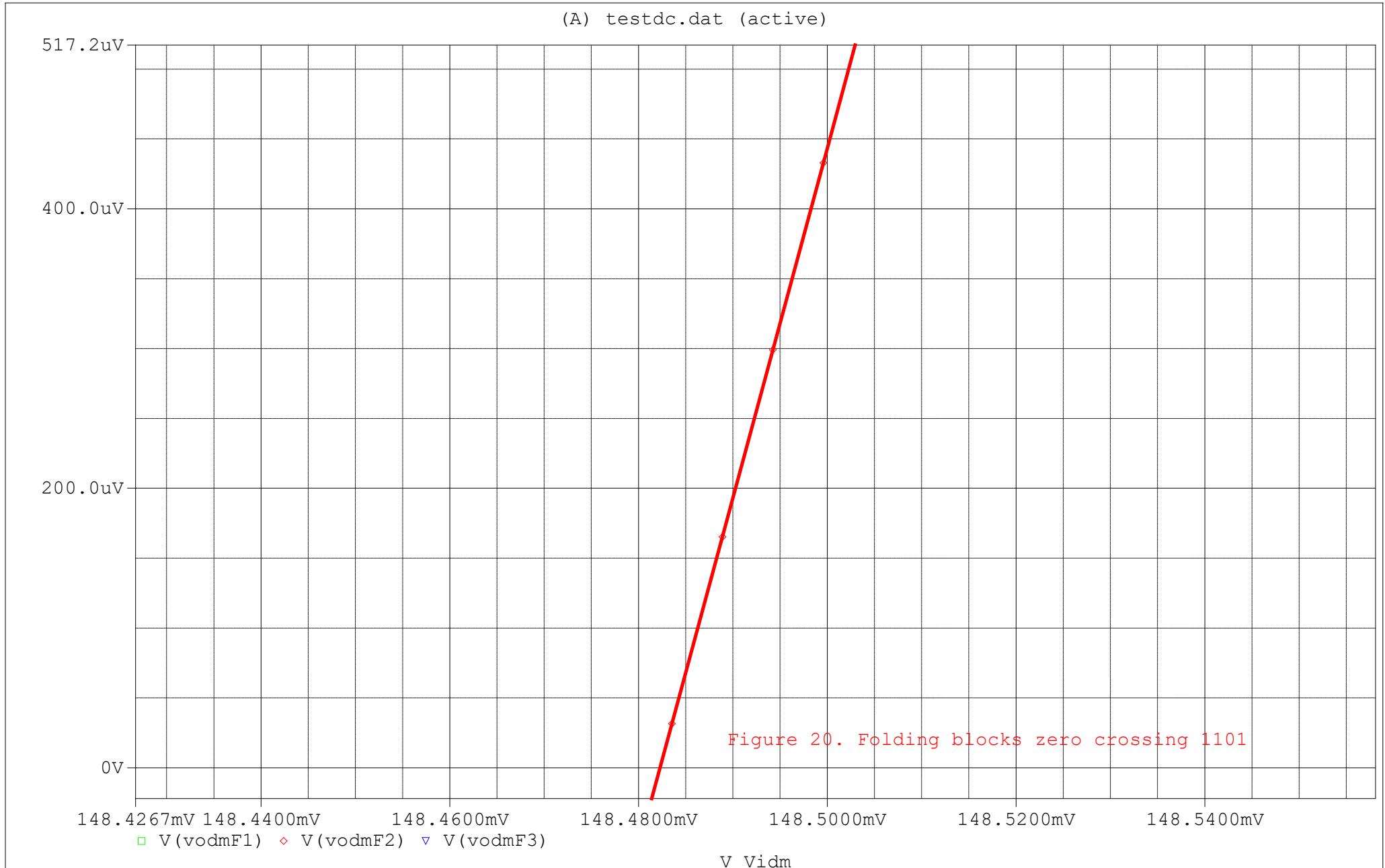
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



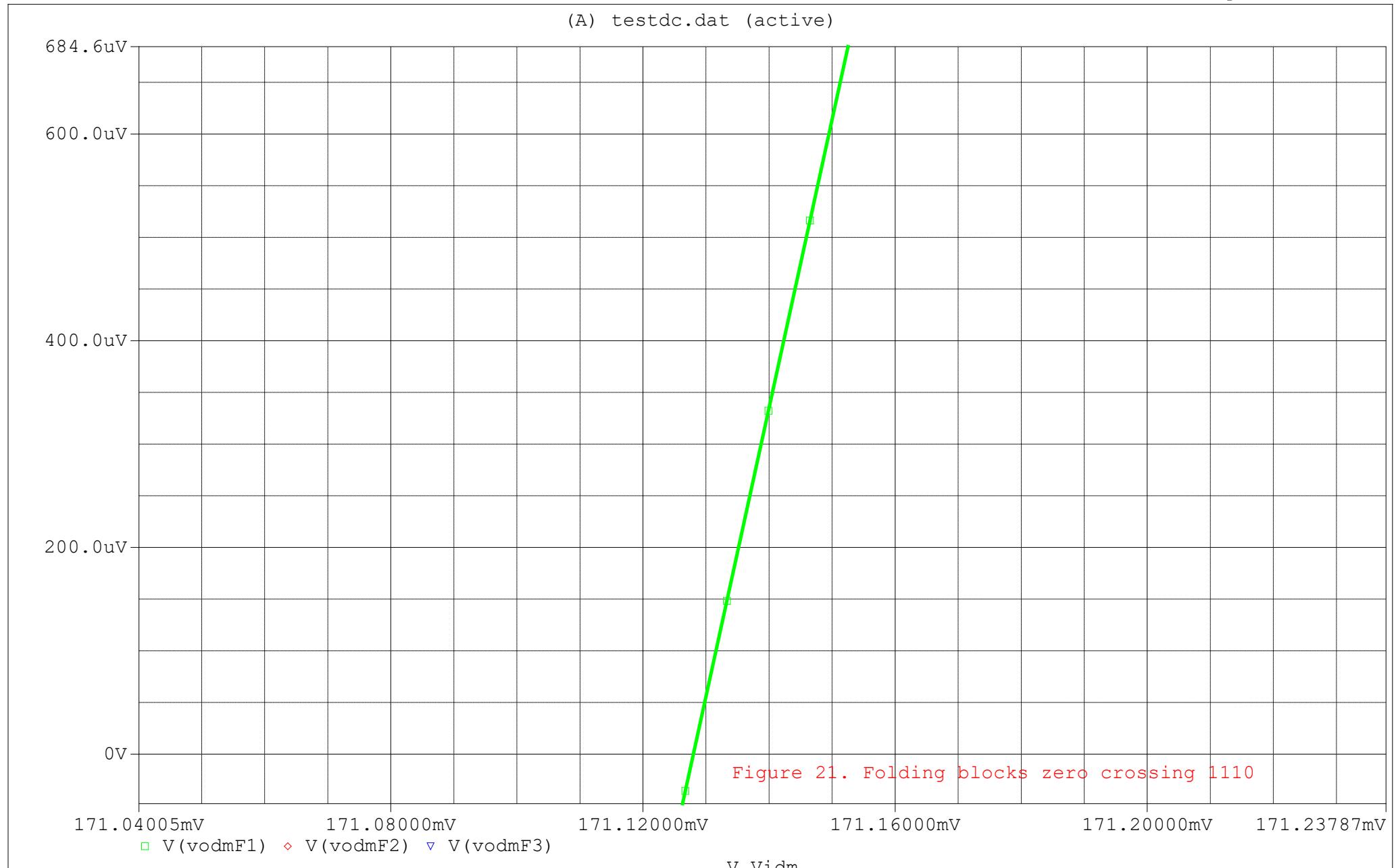
** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



** Profile: "SCHEMATIC1-testdc" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Project ...
Date/Time run: 05/05/22 16:48:01 Temperature: 27.0



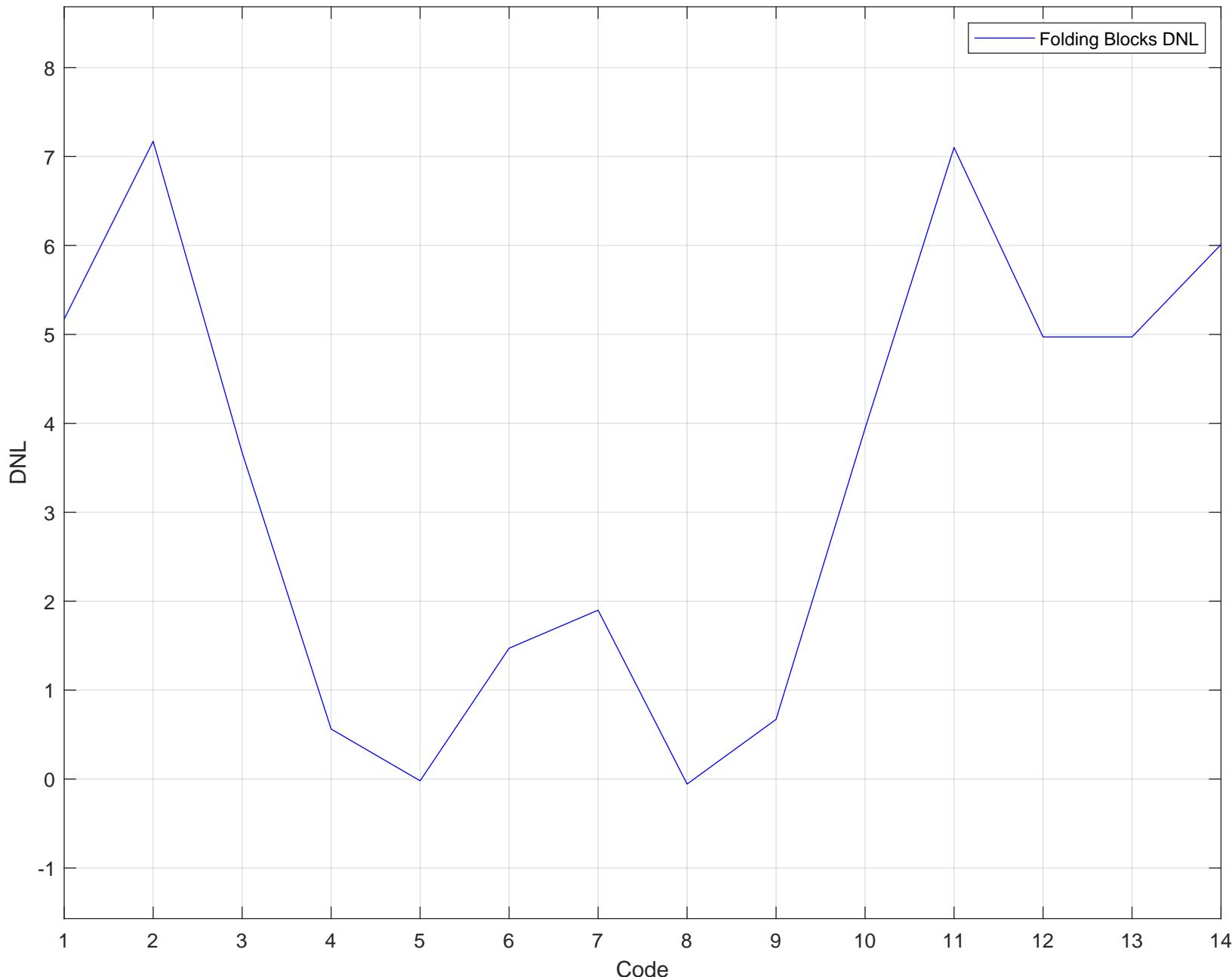
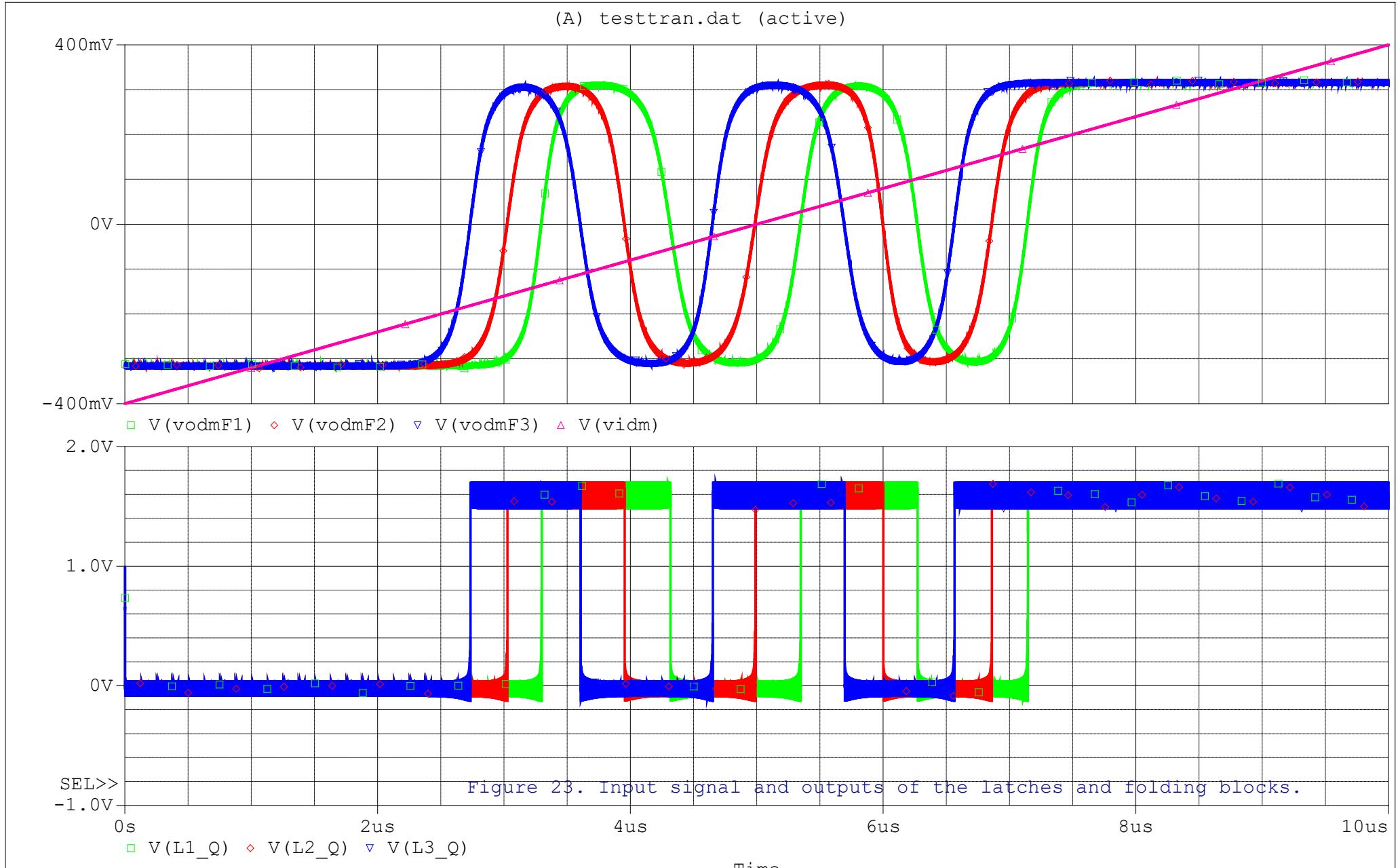
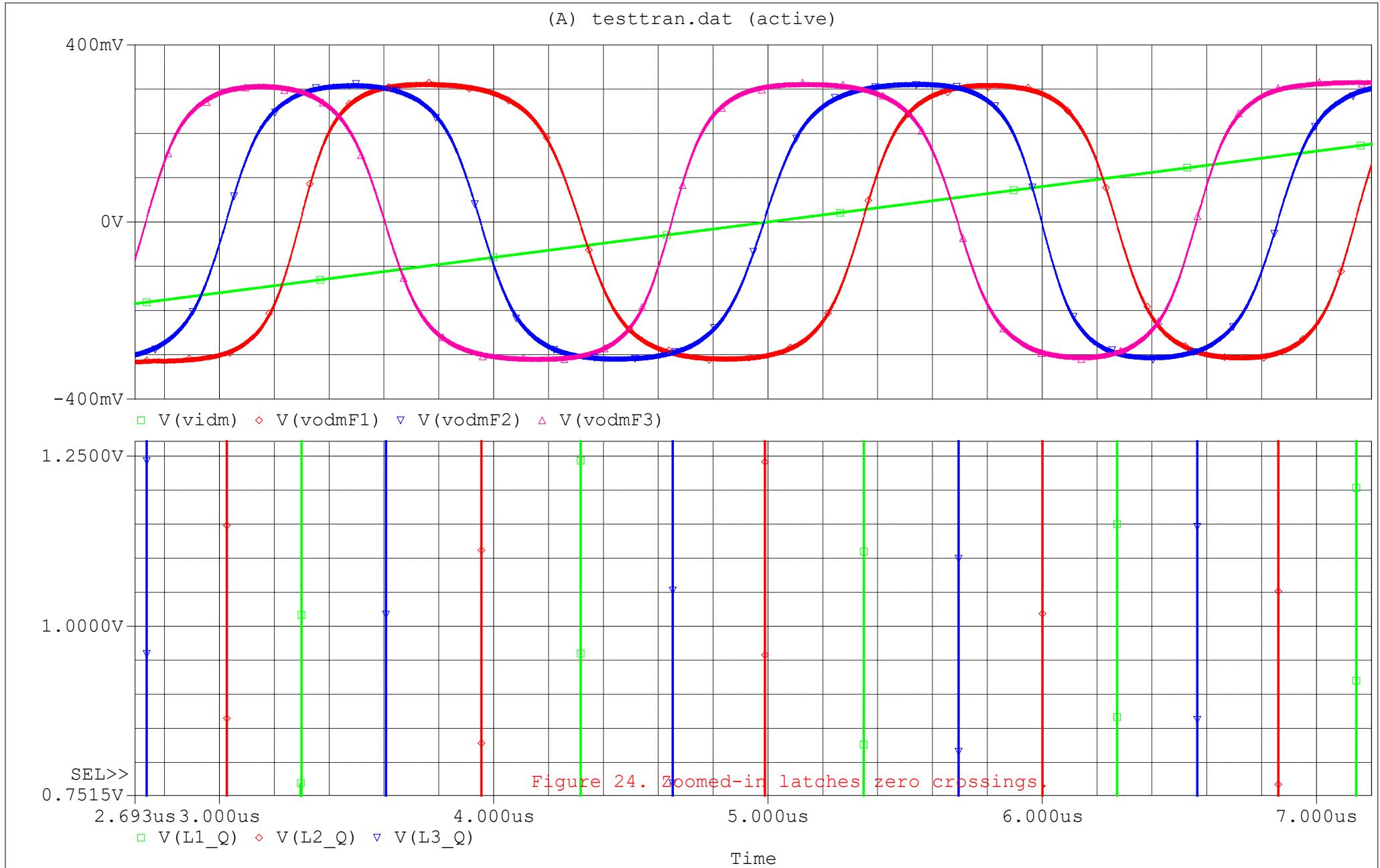


Figure 22. Folding Blocks DNL plot

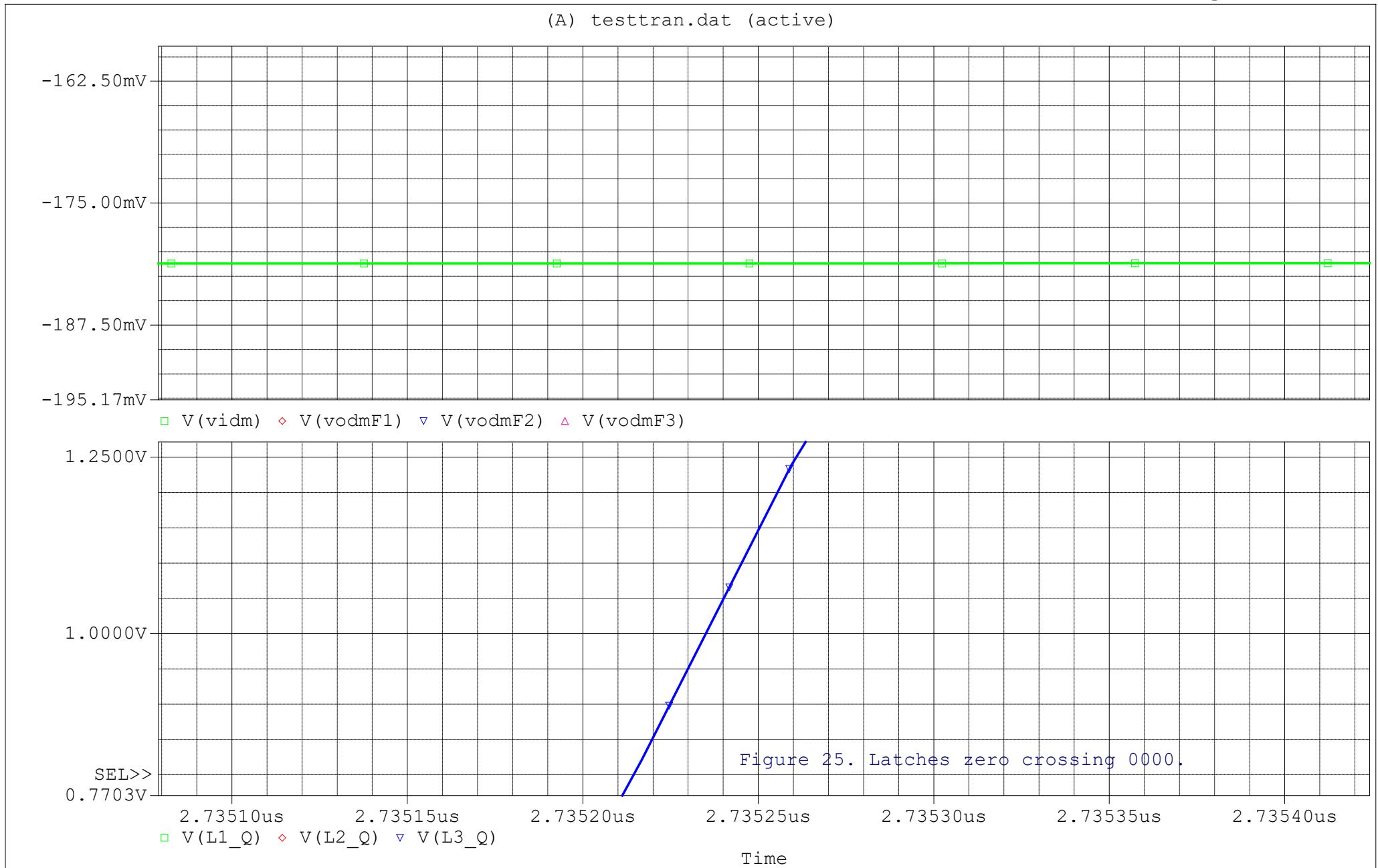
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



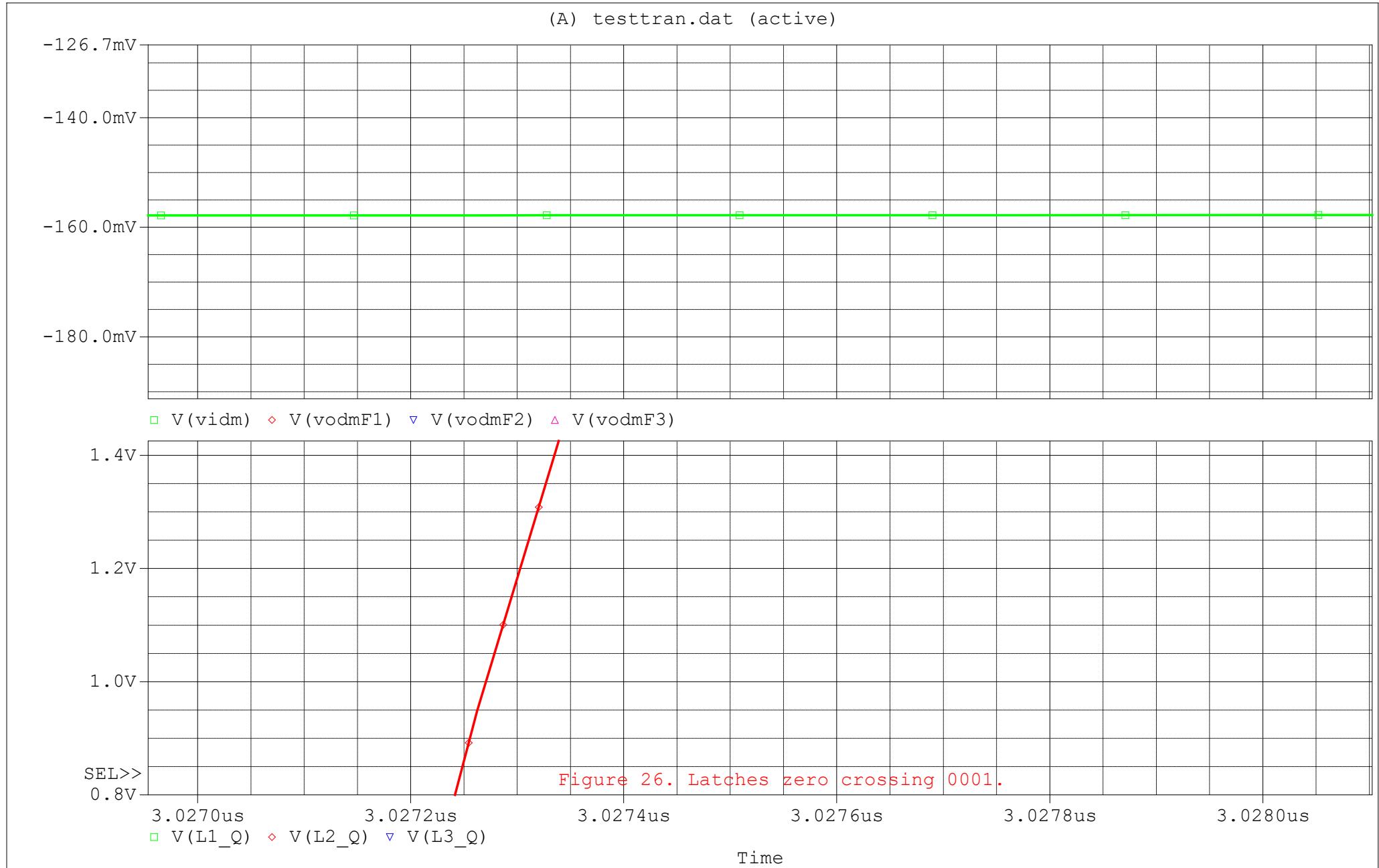
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



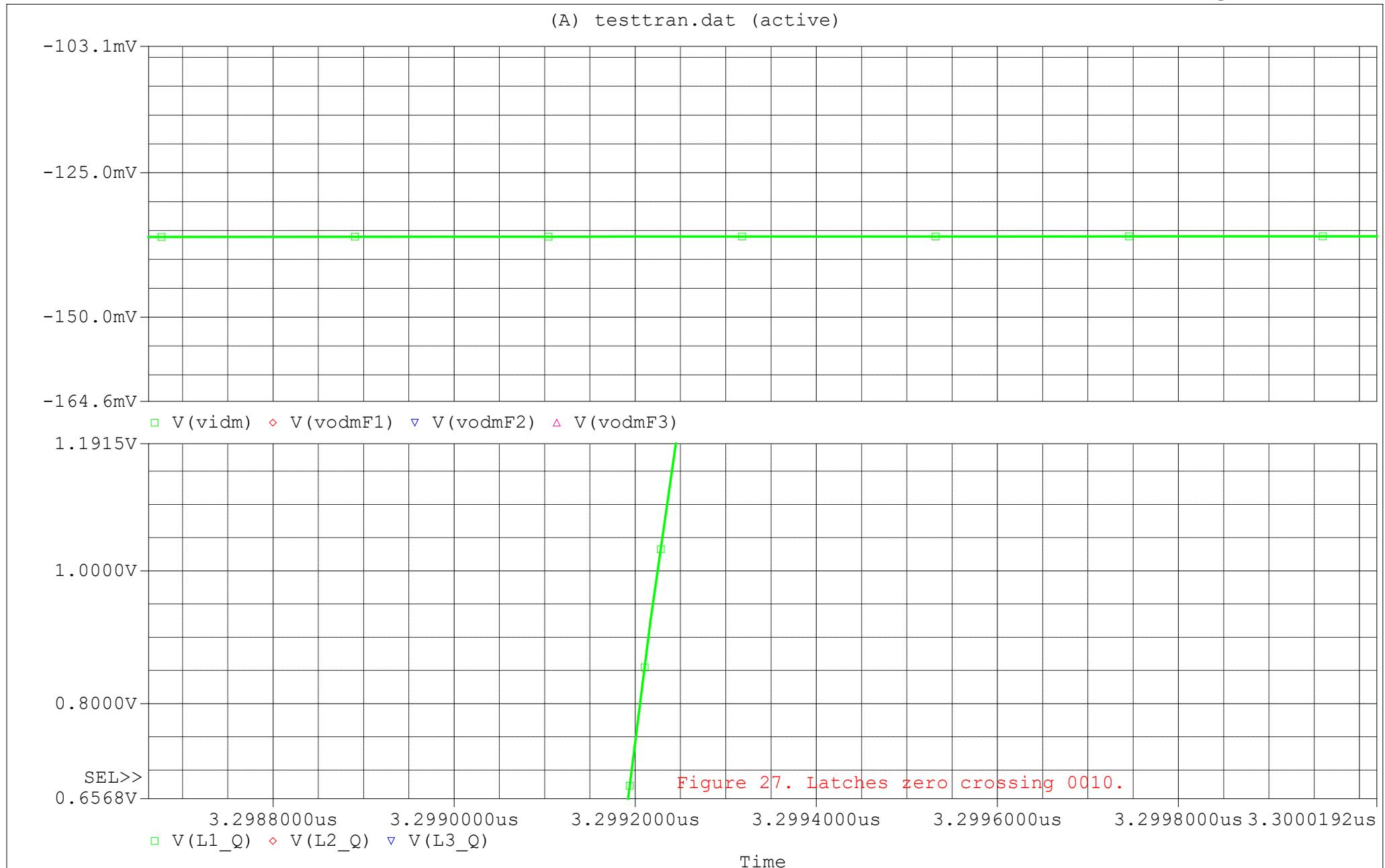
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



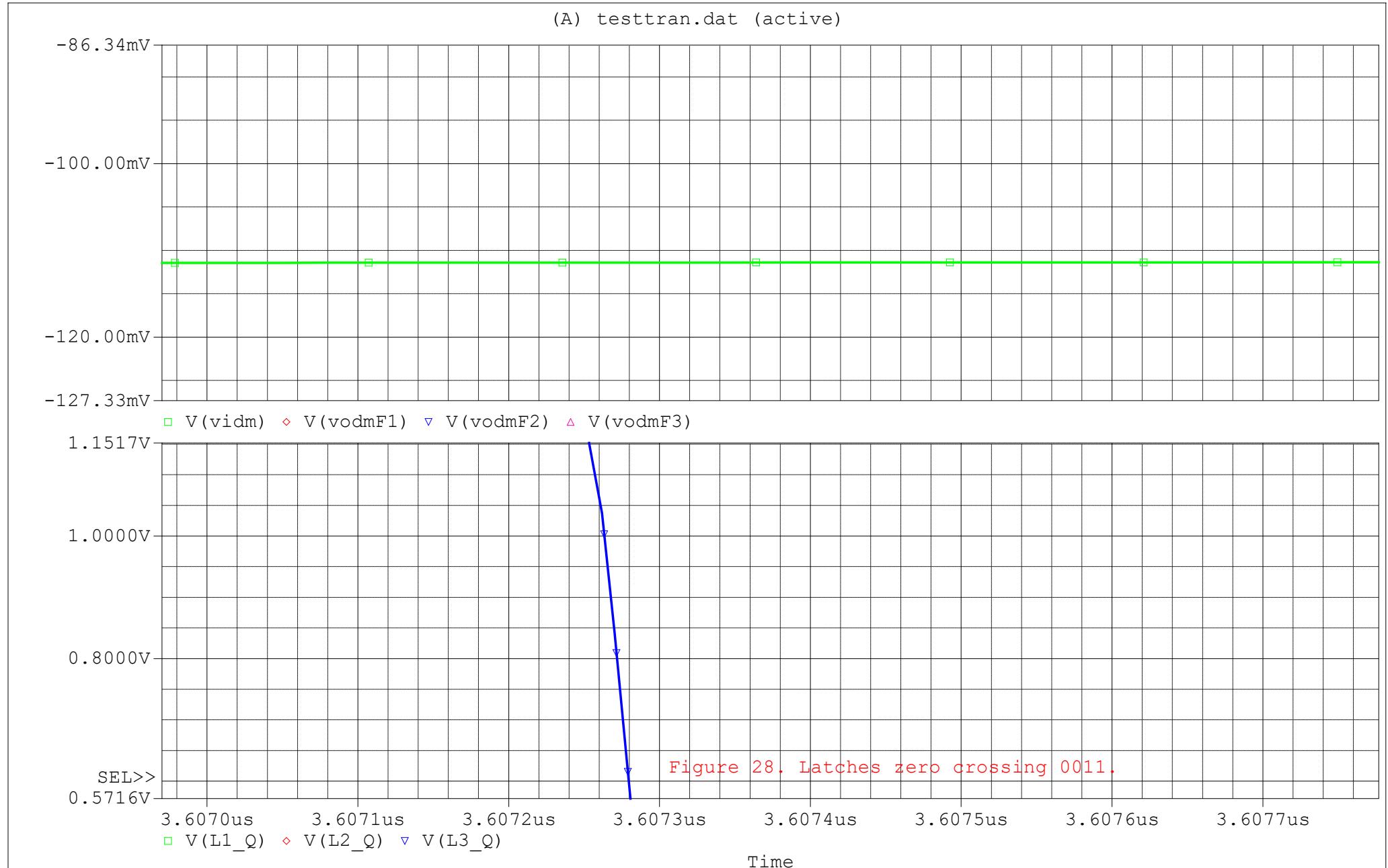
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



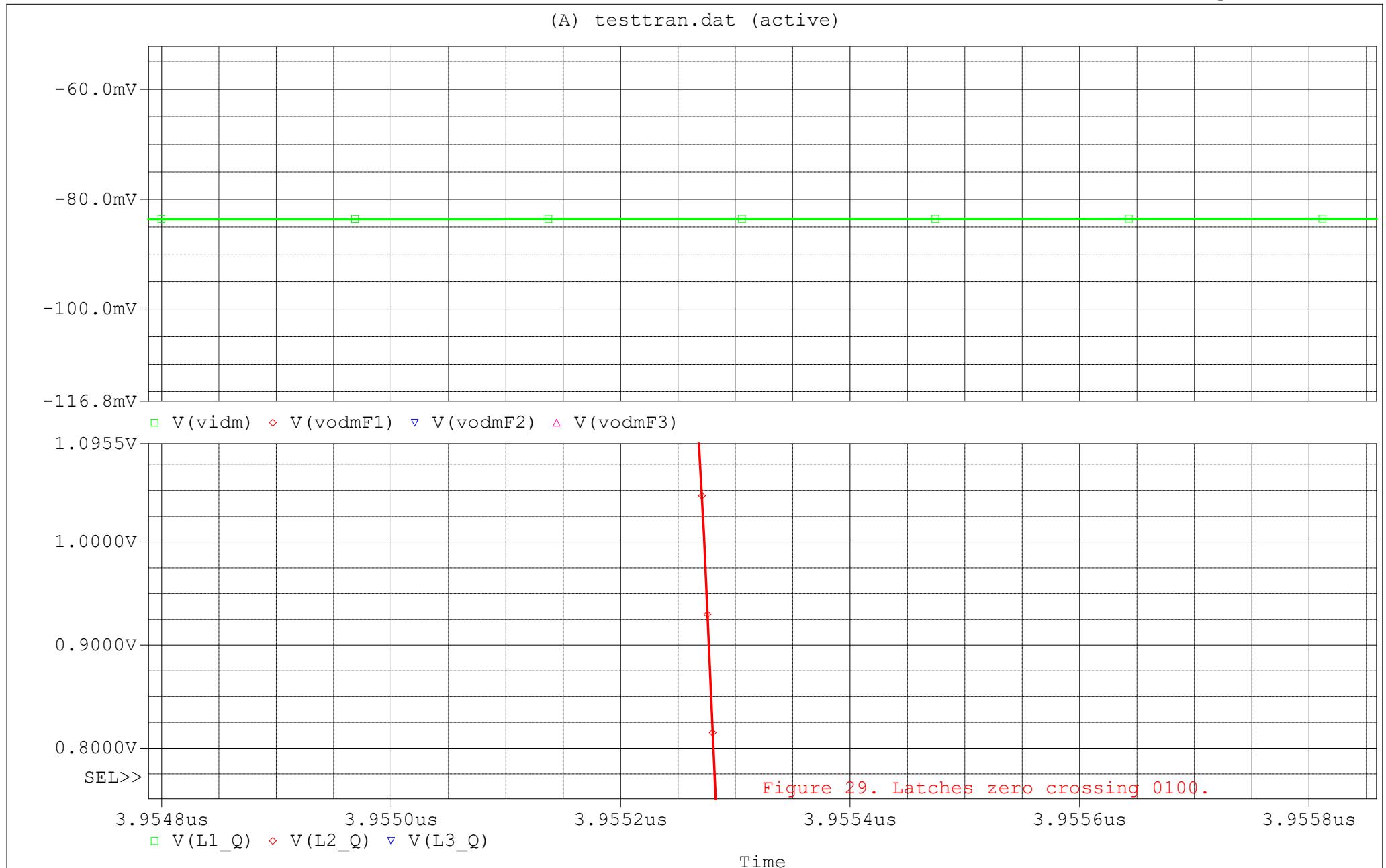
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



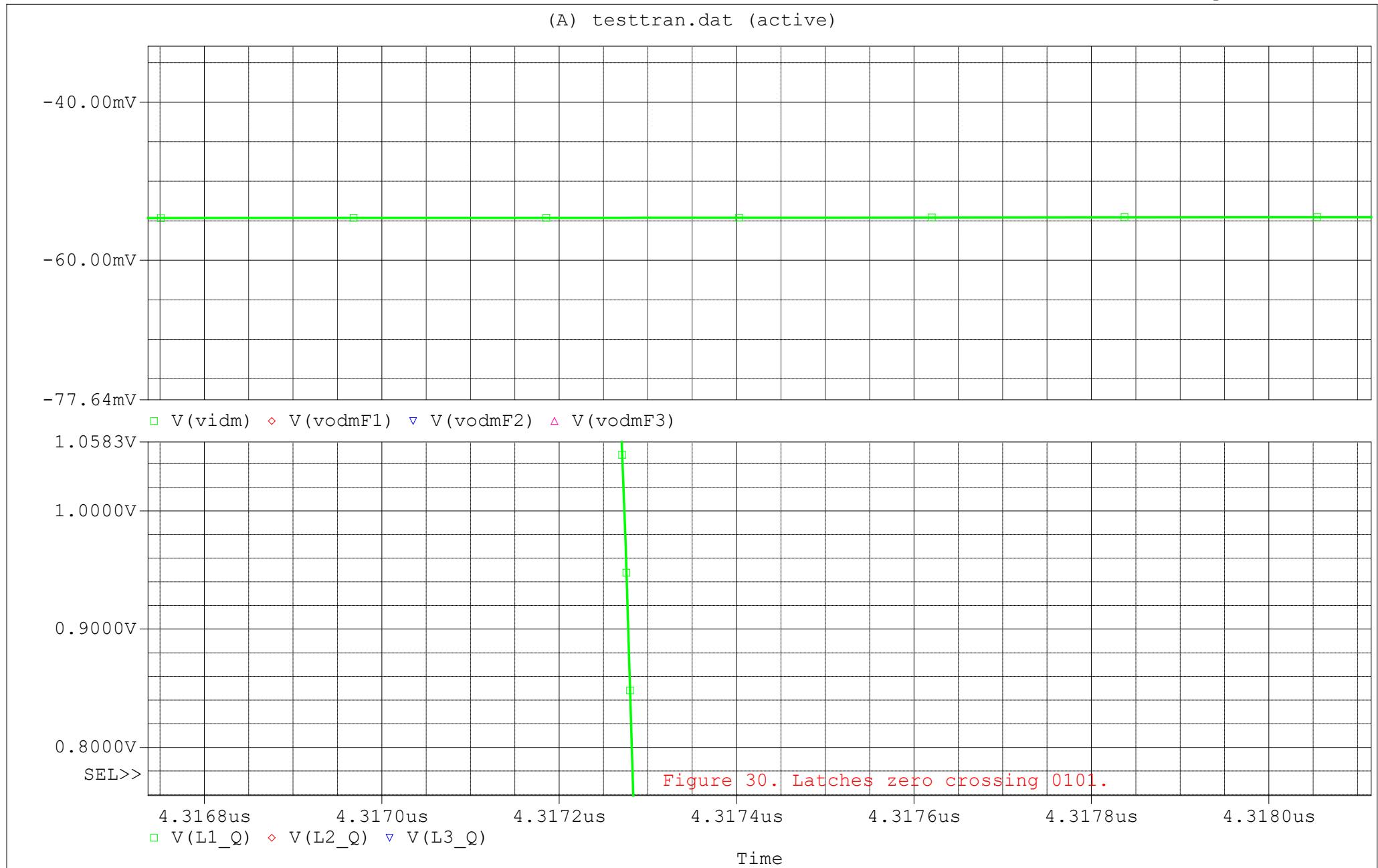
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



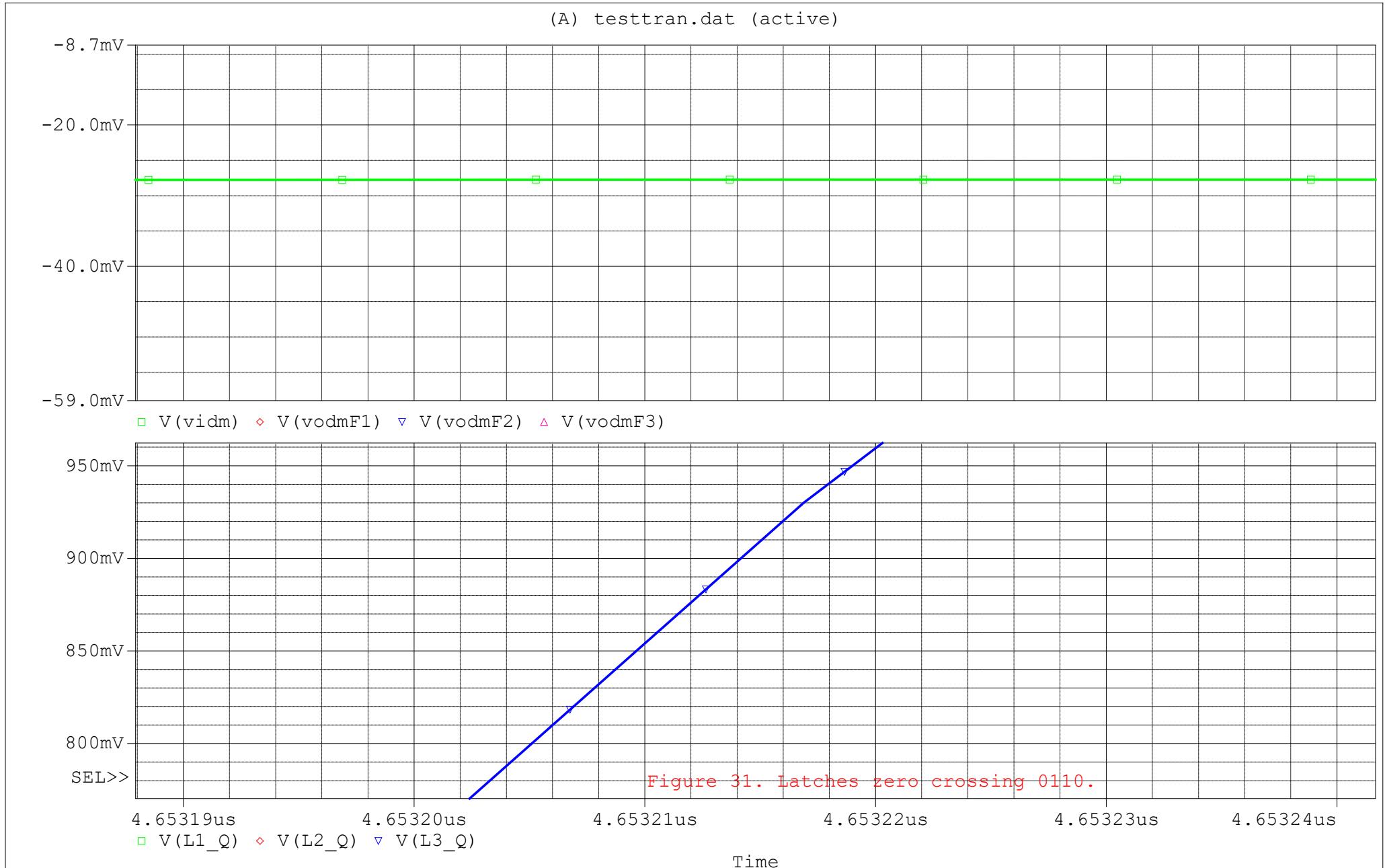
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



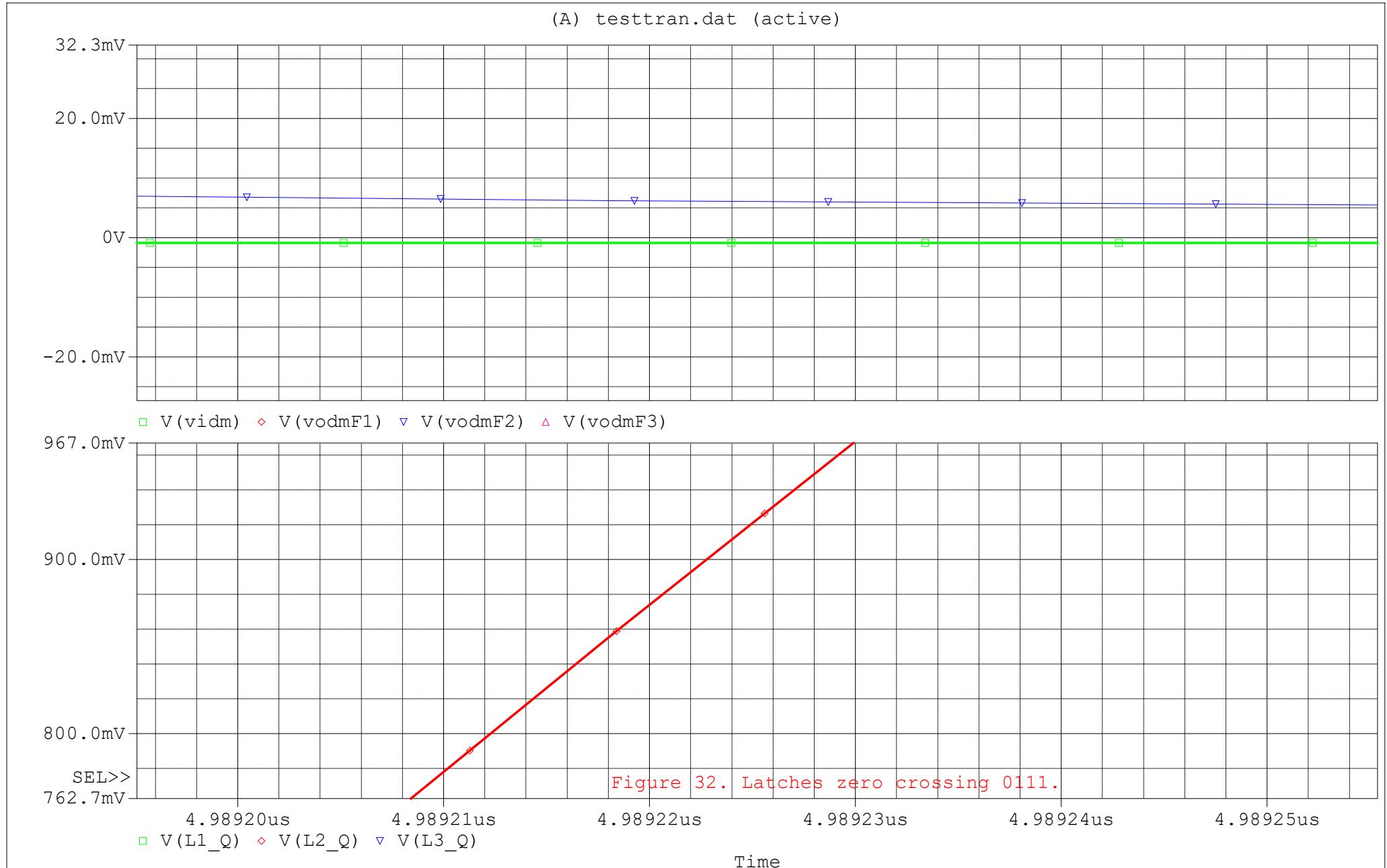
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



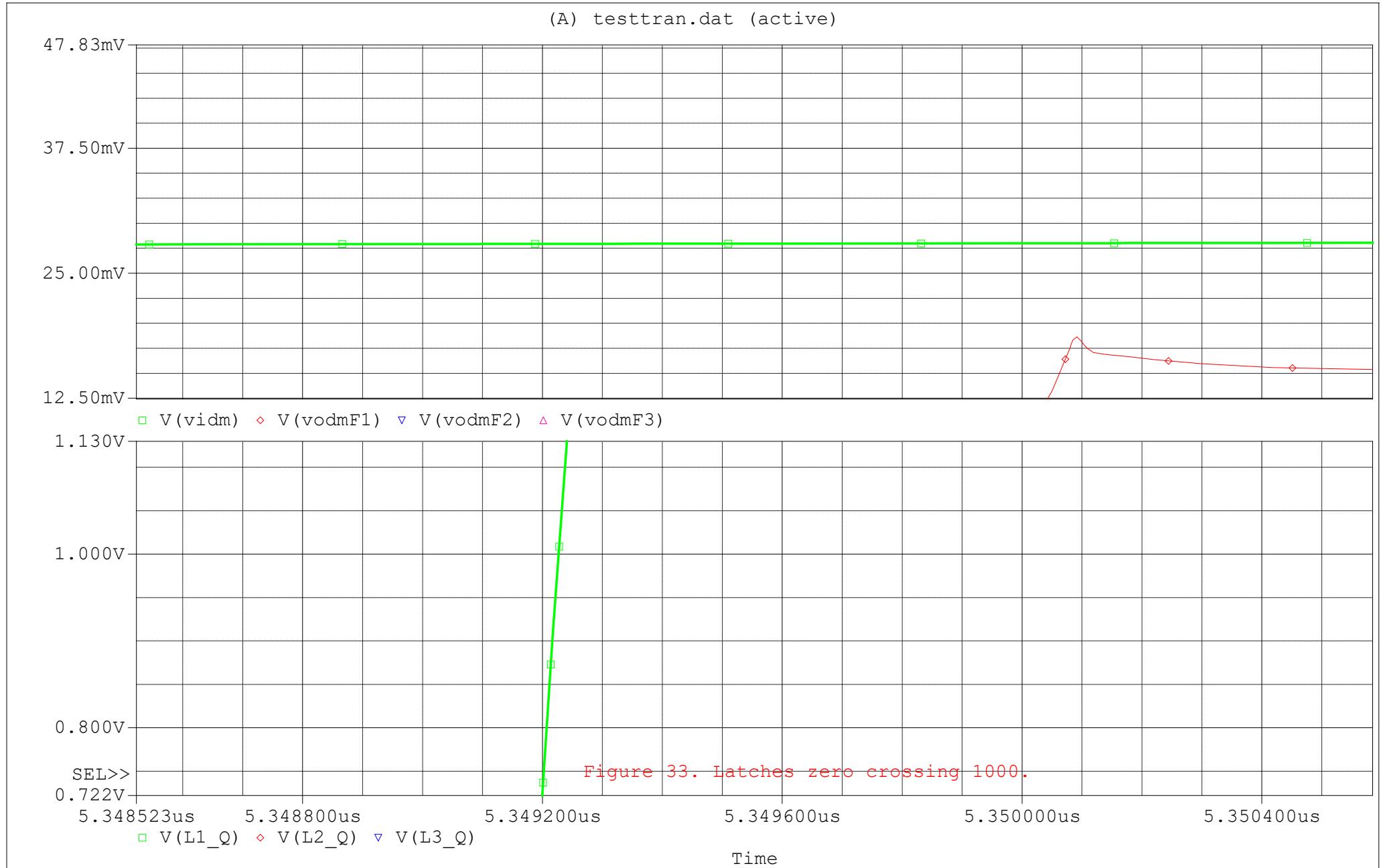
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



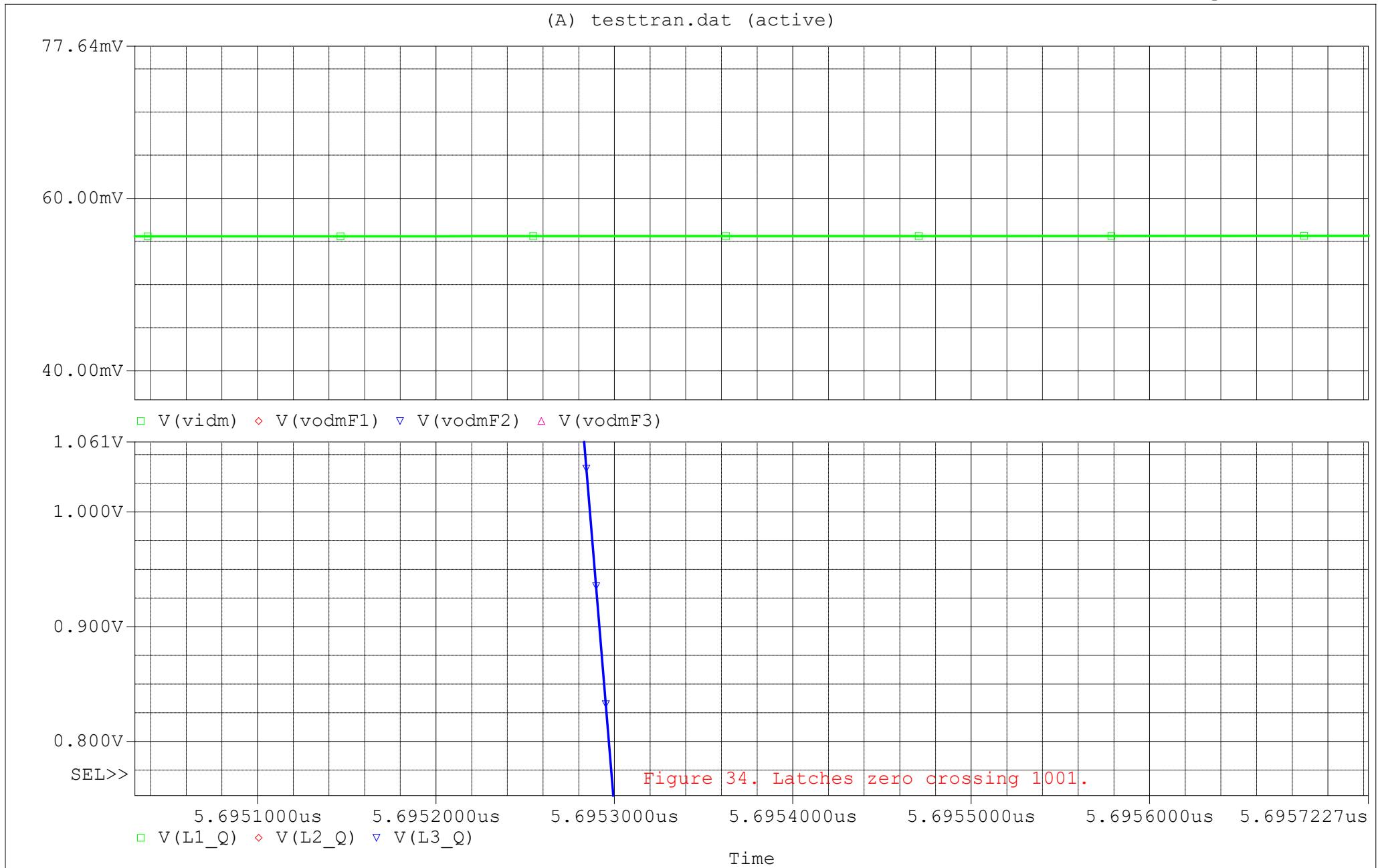
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



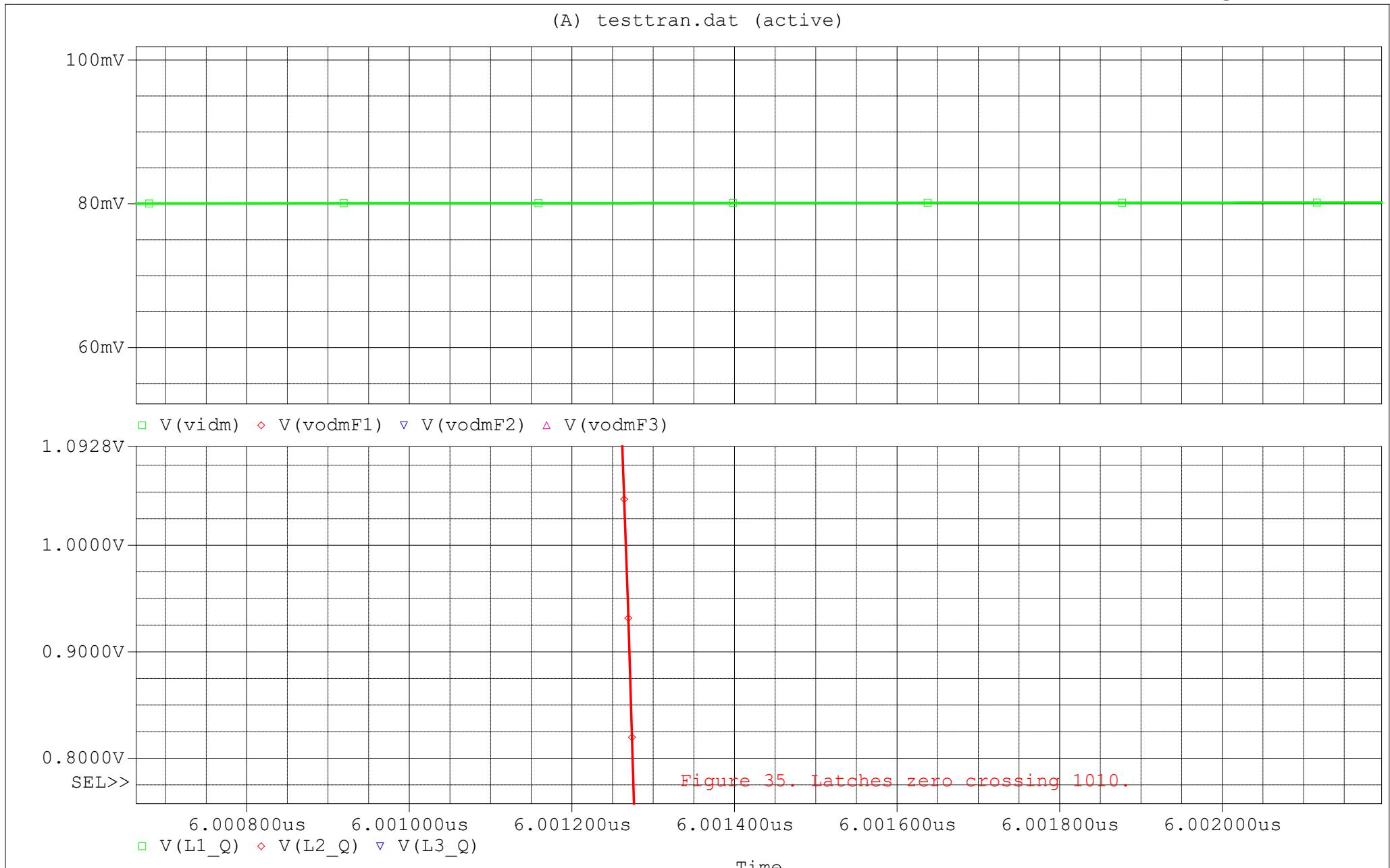
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



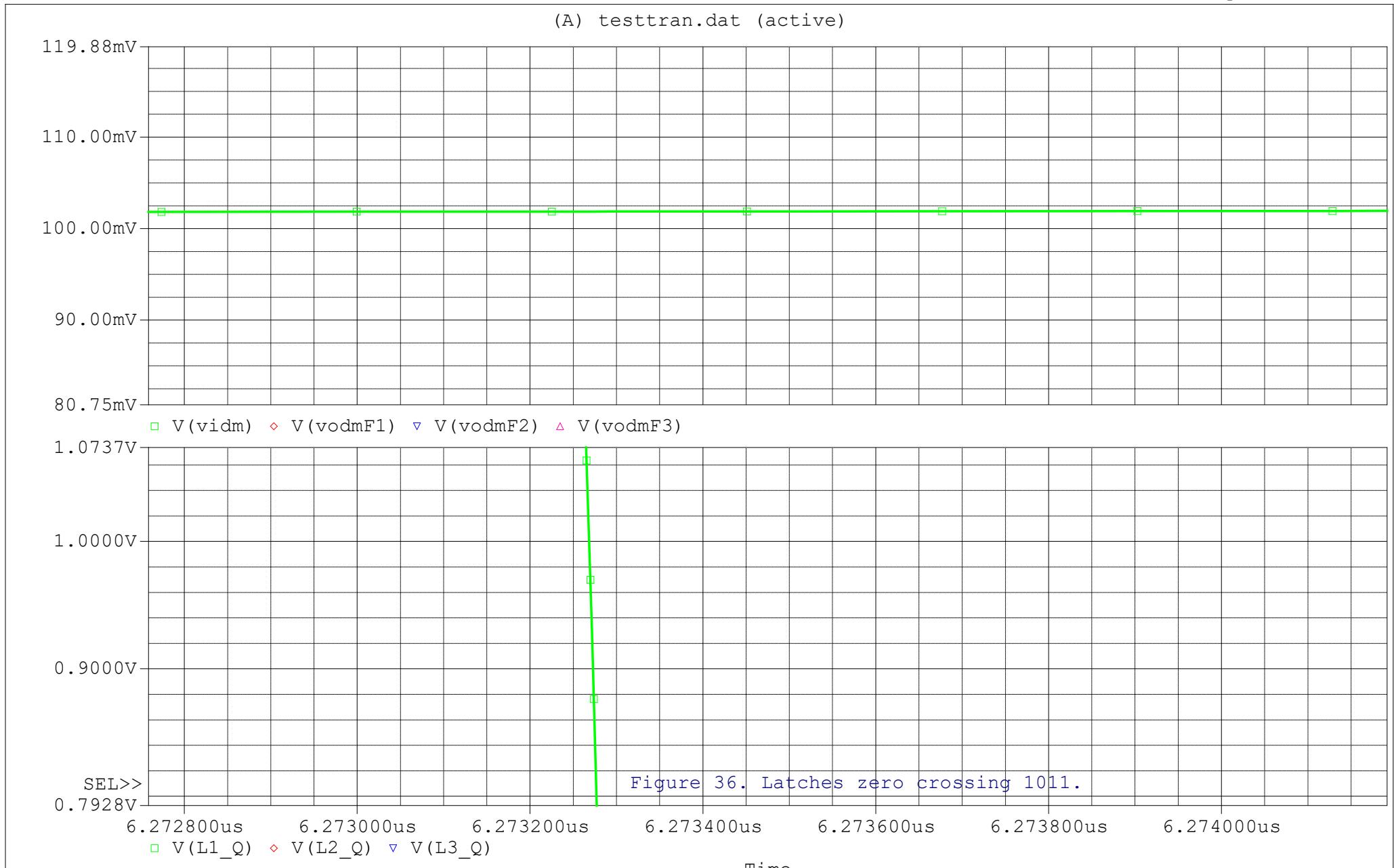
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



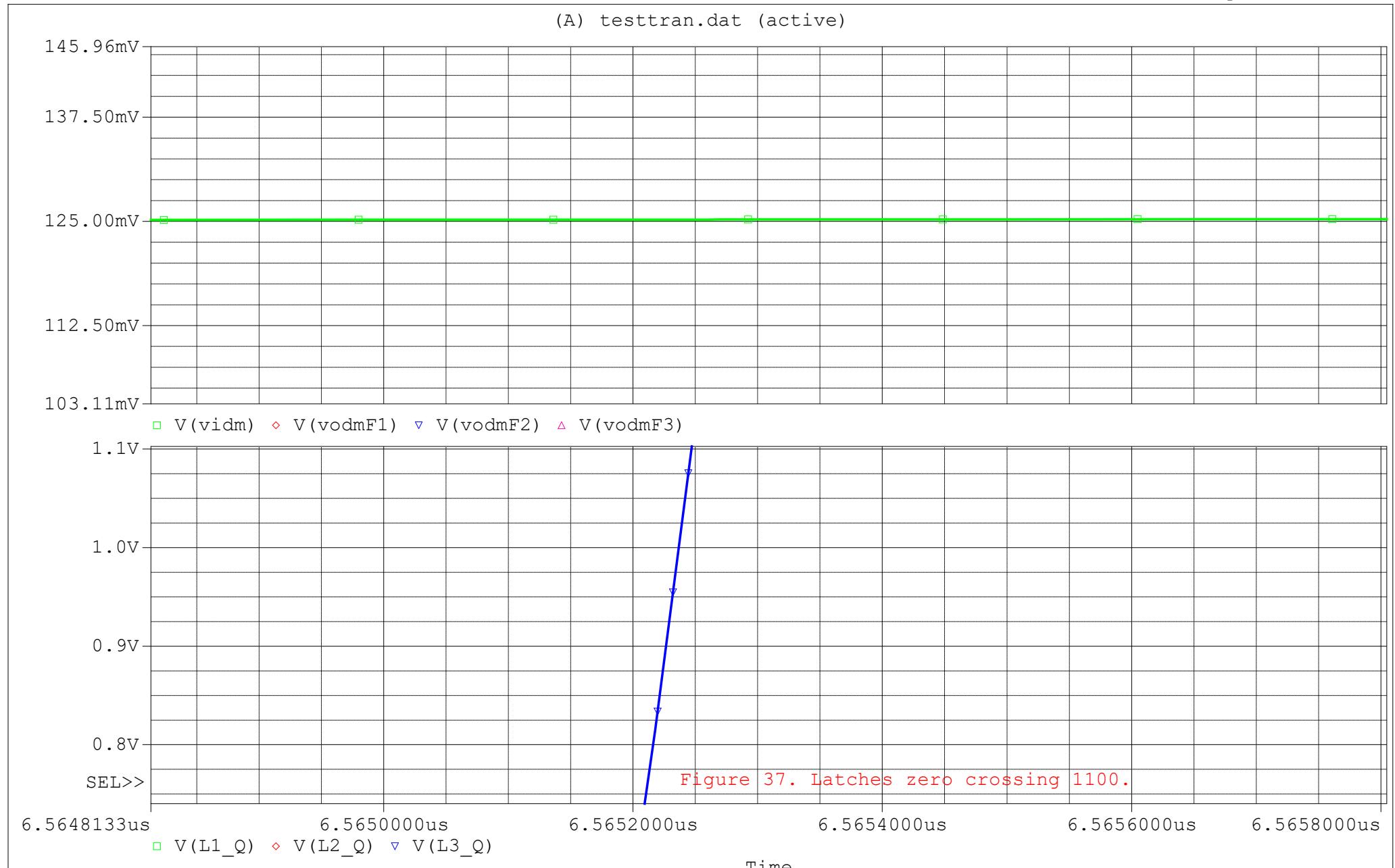
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



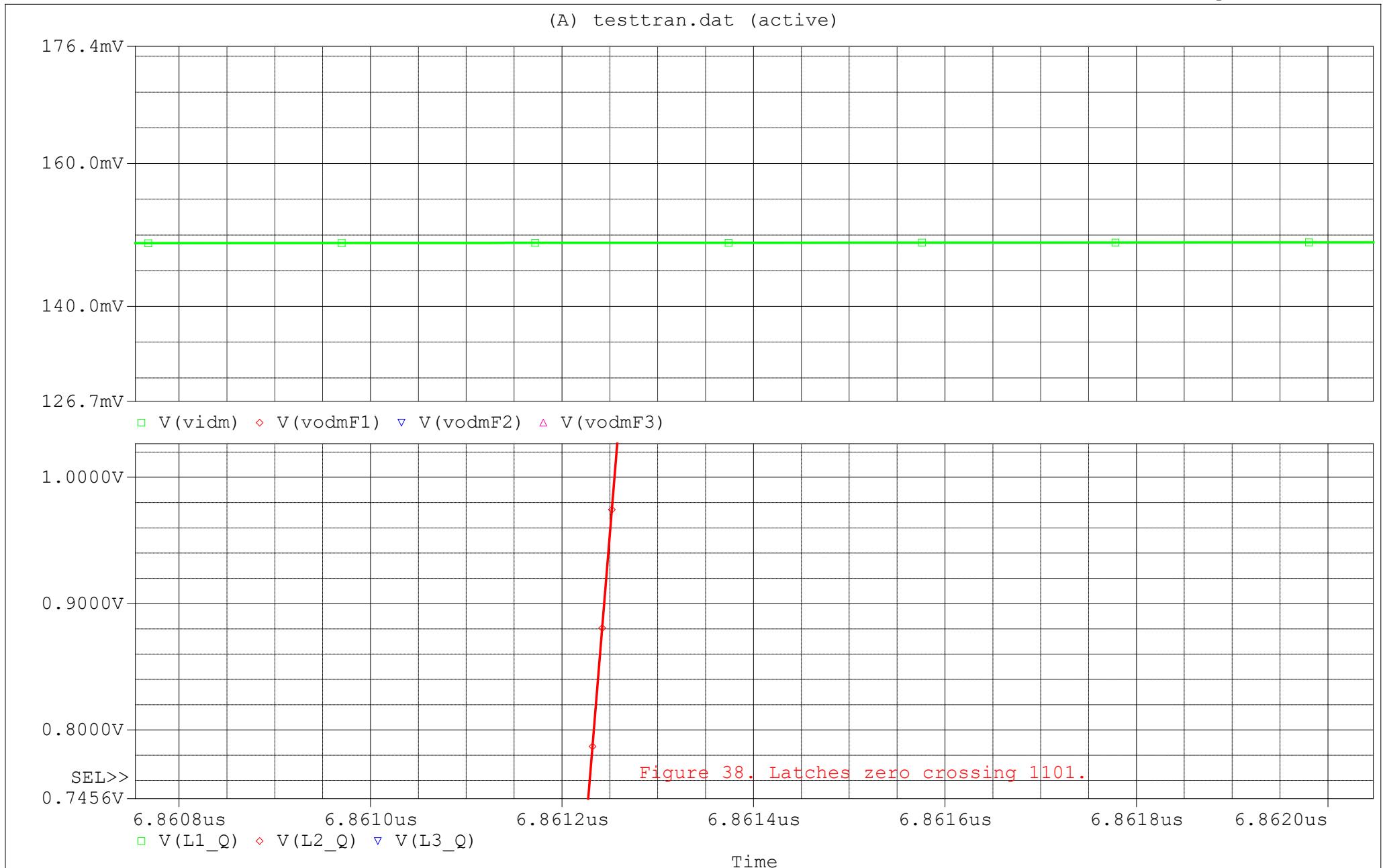
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



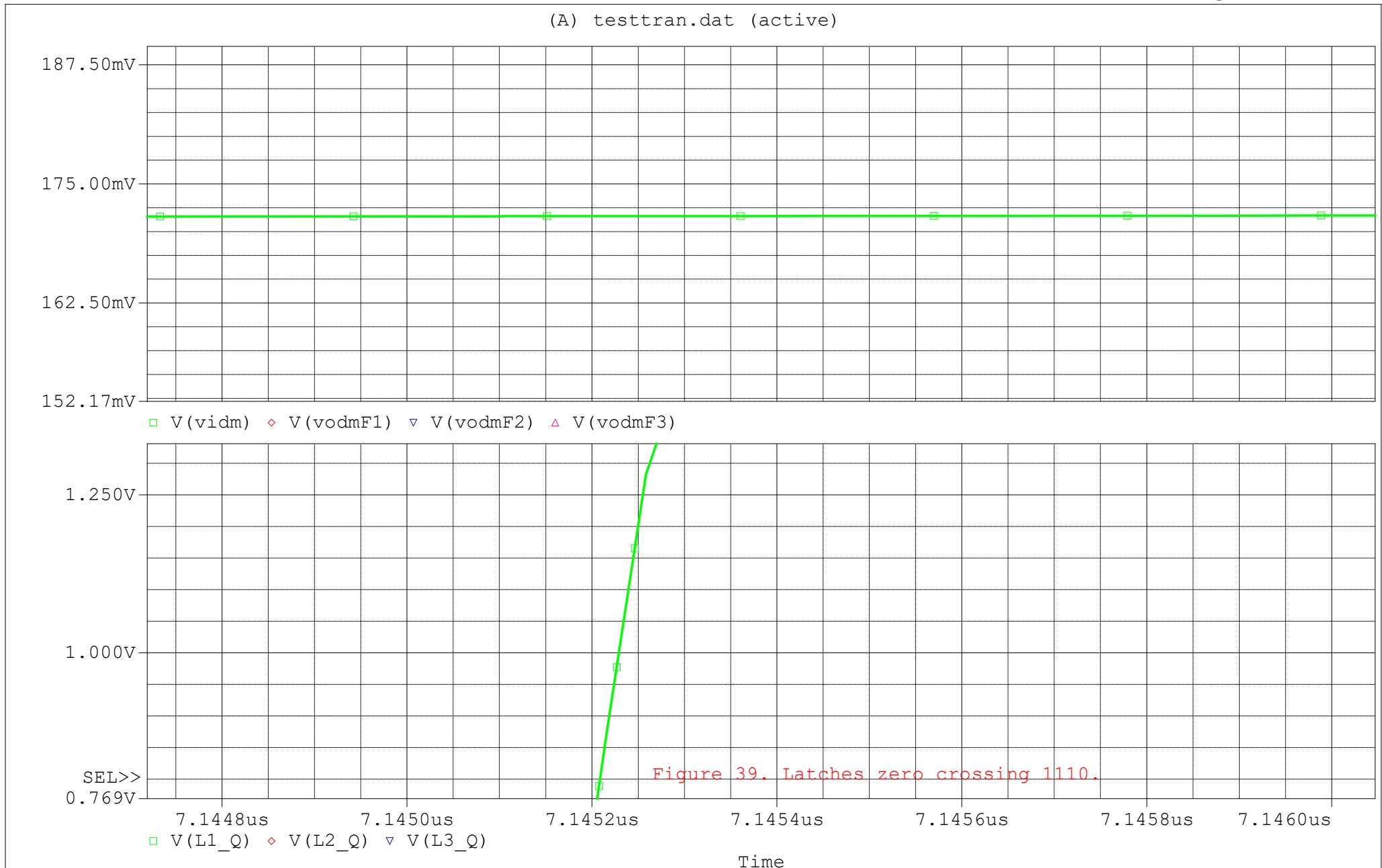
** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 05/07/22 22:38:36 Temperature: 27.0



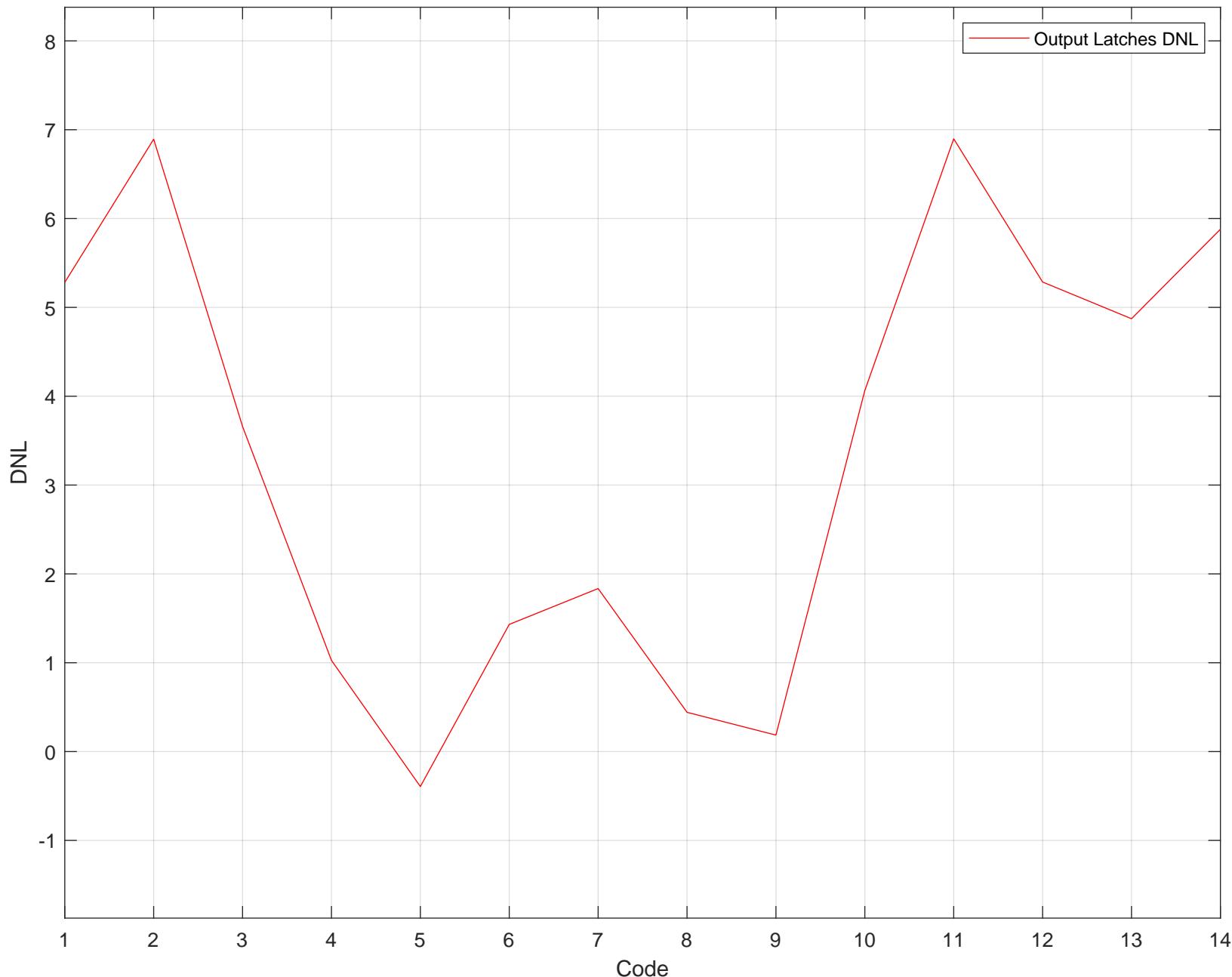


Figure 40. Output Latches DNL plot

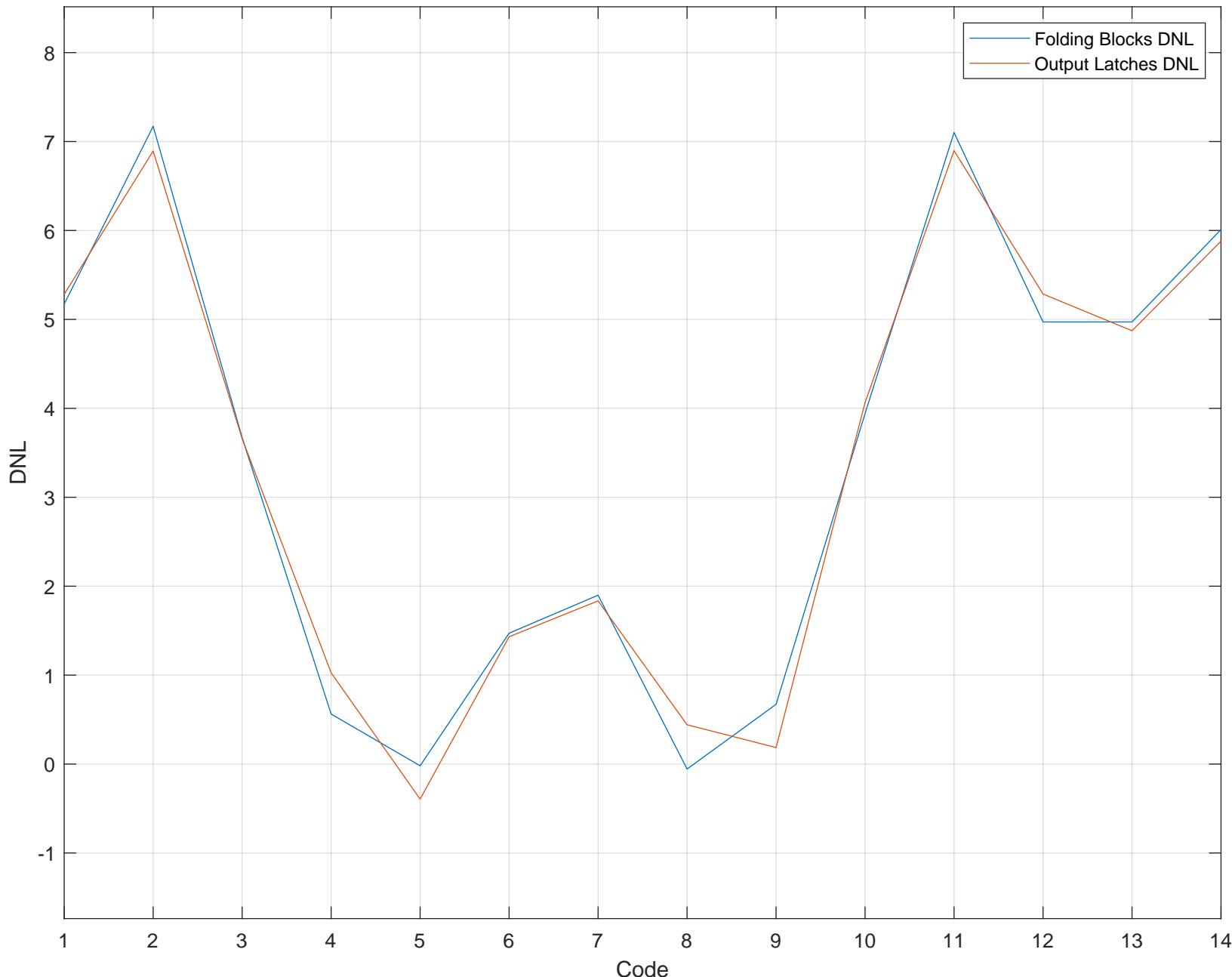


Figure 41. Folding Blocks DNL plot

