California State University, Sacramento
College of Engineering & Computer Science
Electrical & Electronic Engineering Department

EEE 232, Spring 2022 – Project 2
due by Sunday, 5/8/2022

Project Description

The objective of Project 2 is to design and simulate a fully-differential version of the preamplifier and folding block array for a 4-bit folding and interpolating flash ADC, as shown in the attached block diagram. The process to be used is 0.18μm CMOS, with VDD = 1.6V. Models for the MOSFETs should be obtained from the Moodle class page.

Specifications

- Process = 0.18μm CMOS, V_{DD} = 1.6V
- Full scale differential input voltage range = As large as possible
- DNL < 0.25 LSB (the total error from all sources in the zero crossings at the outputs of the folding blocks must be < ¼ LSB)

Key block specifications to consider

- The voltage gain and differential pair Von (V_{GS} -V_T) for each preamplifier
- The number of extra preamplifiers needed to properly terminate each preamp stage
- Values for the reference voltages needed for the first stage of preamplifiers
- The voltage gain and differential pair Von (V_{GS} -V_T) for the folding circuits
- Maximum mismatch allowed between the tail current sources in the folding circuits
- The maximum input signal frequency for the entire preamp and folding block array

Bonus

A bonus of 20 points will be awarded to any design which also includes the latches at the outputs of the folding blocks, and determines the DNL values for each ADC code based on both the folding block zero crossings and also the output bits of the latches.

Suggested steps

First study the PSpice models provided for the folding and interpolation circuits and run some simulations to become familiar with them. (Note that these models only work with the full version of PSpice available on the ECS lab computers, not student versions!)

Simulation profiles are provided for bias analysis, DC, AC and transient sweeps. These models are parameterized with variables to allow easy changes (e.g., W, L and M values) for quick "what if" analysis of tradeoffs.

Pay particular attention to :

- The relationship between the size of the differential pair Von (V_{GS} -V_T) used and the number of adjacent differential pairs which are fully switched (e.g. < 1μA in 1 side). Note the importance of keeping adjacent diff pairs fully switched in folding circuits, but the need to have some number of adjacent preamps not fully switched (i.e., in the linear portion of their transfer curves) for interpolation and resistor averaging. Carefully consider how this impacts your choices for the Von's of these circuits!
- The errors in the locations of the zero crossings for the preamplifiers if too small a value is used for the Von (V_{GS} -V_T) of these differential pairs.
- The errors in the locations of the zero crossings near the edges of the preamp arrays if too few extra preamps are used at the ends of each array.
- The errors in the locations of the zero crossings for folding circuits if too large a value is used for the Von (V_{GS} -V_T) of these differential pairs.
- The errors in the locations of the zero crossings for the folding circuits due to mismatches in the differential pair tail currents.

Report contents

At the beginning of your report include a table showing all your block specifications, in the same order as on page 1. Discuss the Von (V_{GS} -V_T) values you selected for the differential pairs used in both your preamps and folding circuits. Explain how your choices for these Von values impacted your choices for the number of extra preamps required to properly terminate each preamp array. Also discuss and explain all other important issues encountered during your design and how you addressed them.

Include Spice simulation plots which clearly show the input signal voltages where each of the zero crossings at the output of the folding blocks occur. Be sure to include a zoomed-out plot showing all zero crossings (the "big picture") as the input voltage is swept across the entire ADC input signal range. And also include zoomed-in plots for each individual zero crossing, to allow it to be viewed and measured accurately. If you included the latches in your design, then also include both a zoomed-out plot and individual zoomed-in plots showing the input voltages where the output bits for each latch changes as the input voltage is swept across the the entire ADC input signal range.

Calculate and plot the DNL values for each ADC code, based on the measured input voltages where each zero crossing occurs at the outputs of the folding blocks. If you

included the latches in your design, then also include a plot of the DNL values calculated based on the measured input voltages where the latch bits switch.

Report Submission

- All simulation plots should be printed to full-page PDFs in landscape mode, and these included in the single PDF file you submit. Be sure to add titles and text notes to plots to draw attention to key items. **Screen captures will be given zero credit**.
- Be sure to use either dark colors or black and white for all signals plotted, so that these signals are easy to see on your plots.
- Your project report must be submitted as a single PDF file. Word files and zip files and will not be accepted.
- Name your report "eee232_s22_proj2_Your_Name.pdf", with your name at the end.
- All project reports must be submitted through Moodle. Email will not be accepted.
- Late submissions will not be accepted. No exceptions.
- Please note that this is not a group project. While discussion between students at a general level regarding circuit choices, tradeoffs and issues is allowed (and even encouraged!), the designs and reports turned in MUST represent the individual work of each student.

  Copying all or part of another student's work will be dealt with severely, as will any form of cheating.

4-bit Flash ADC with Interpolation and Folding