California State University, Sacramento
College of Engineering & Computer Science
Electrical & Electronic Engineering Department

EEE 232, Spring 2022
Project 1
due by Sunday, 3/13/2022

Project Description

The objective of Project 1 is to design and simulate a latching comparator similar to the one by Op't Eynde and Sansen (JSSC Feb 1992) discussed in class. The process to be used is 0.18μm CMOS, with VDD = 1.6V Models for the MOSFETs should be obtained from the Moodle class page. You are free to use the circuit of your choice to meet these specifications, however only MOSFETs should be used in your design. BJTs and resistors should not be used. Ideal voltage and current sources may be used in your testbench, but not in your comparator. Full-swing CMOS clocks can be used as needed.

Specifications

- Comparisons must be accurate to better than 2mV, not including mismatches.
- Time required to make a comparison < 400ps, not including input tracking time. This comparison time must be measured using the overdrive recovery test.
- Overdrive recovery test must be successful for differential inputs up to at least ± 400mV.
- Comparison is to a differential reference voltage of ± 200mV.
- Outputs = Q and QB, with a full digital CMOS output swing.
- Minimum Von = Vgs - Vt for all saturated FETs = 100 mV.
- Process = 0.18μm CMOS, with VDD = 1.6 V and temperature = 27° C.
- Full swing digital CMOS input clocks with 10%-90% rise/fall times of 100ps

Bonus

A bonus of 20 points will be awarded to the design with the smallest comparison time on the overdrive recovery test, while meeting all other specifications. In the case of a tie, the highest accuracy wins.

Report format and submission

- Your report must contain an *introduction, a body and a conclusion.*
- Be sure to discuss and explain all results obtained.
- Include in your report a summary table comparing the target specifications with both your hand calculations and your final simulation results. Explain any differences.
- Be sure to include in your project report all requested information, including your circuit schematic and all simulation plots, etc., needed to prove that you met all specifications. **Any specification not supported by simulation results will be assumed to have been missed, and points will be deducted!**
- Be sure to clearly label the W and L values for every MOSFET in your schematic, as well as all other component values (e.g., source values).
- All nodes in your schematic must be clearly labeled.
- Be sure to include a title on your plots to indicate what information each contains.
- All plots must be clear and easy to read, even when zoomed in. **Do not use screen captures!** Instead, print each plot to a full page PDF, and include these in your final report.
- Your project report must be submitted as a single PDF file. Other formats such as Word files and zip files will not be accepted. Include PDFs of schematics and simulation plots in a single PDF file. Combine multiple PDFs into a single PDF using Acrobat, which is available on the ECS lab computers.
- The file name for your report should contain "eee232_s22_proj1" followed by your name. For example, if your name is John Smith then the file name for your report would be "eee232_s22_proj1_John_Smith.pdf".
- In addition to your project report, use zip to compress your PSpice files into a single zip file. Use the same name for your zip file as you used for your report, but with an extension of .zip instead of .pdf
- Submit both the PDF of your project report and the zip file containing your PSpice files through Moodle. All files must be submitted through Moodle. Email and hardcopy will not be accepted.
- **This is an individual project. Copying all or part of another student's work will be dealt with severely, as will any form of cheating.**
- **Late submissions will not be accepted.**