Department of Engineering and Computer Science, ECS
California State University, Sacramento CSUS

EEE 232 Key Mixed-Signal IC Blocks Project 1 Report

Author: Vladislav Rykov

Table of Contents

Introduction

Living in the age of greatest technology advancement allows us to witness a new industrial revolution. Automation and remote process control are the heart of optimization and sustainability. But how have got here? Certainly, we heired knowledge and experience of those who were before us. Sir Isaac Newton coined a famous metaphor: “Standing on the shoulders of giants”. That means, we are where we are not by chance, but rather by progressive steps of those who were before us.

This report describes a latching comparator design, a tiny circuit that allows a vast variety of technologies to push forward the progress. A comparator is a circuit that compares to voltage or current inputs and produces an output. Integrating comparators to digital circuits requires their outputs to swing between ground and supply voltage.

The latching comparator consists of three parts: input amplifier, analog latch, and SR flip-flop. The report is structured in a way that each section discusses one part of the comparator. The hand calculations, simulations results, and design criteria will be presented and discussed. The final section of the body provides a summary, contrasting project’s specifications, hand calculations, and simulation results. The report ends with a conclusion.

The latching comparator was designed to operate under 0.18µm CMOS, with VDD = 1.6V.

Input Amplifier

Current Mirror

The input preamplifer consists of two parts: current mirror and two differential amplifiers. The current mirror is designed to replicate the input current proportional to transistor dimensions. The ‘left’ side of the mirror establishes a unit current. The dimensions of the ‘right’ side are established in multiples of the unit transistor. An array current mirror was used in the design to supply current for two differential pairs.

Since the current mirror is not a switching part of the comparator, its dimensions can be assigned larger values. Furthermore, higher dimensions will make the supply current more stable. Transistors M0, M1, and M2 consistute the current mirror. The following table provides their dimensions.

Table 1. Characteristics of transistors M0, M1, and M2

Transostor label	Width, µm	Length, µm	Ratio	Von, V
M0	7.2	1.8	1:4	-1.513
M1	14.4	1.8	1:8	-1.511
M2	14.4	1.8	1:8	-1.511

A crucial element is the bias current source. It must be set to a particular current value which will be enough to saturate the current mirror and further suffice the circuit to have optimal transconductance of its active components. The bias current of 200µA was asserted enough to saturate the MOSFETs with the on-voltages listed in the table above. The saturation voltage for all 3 transistors is -1.18V.

Additionally, the amount bias current affects the transconductance of all active components of the circuit. It must be carefully picked up so the influence on the time constant and the input amplifier gain are foreseen and fitted with the specificiations.

Differential Pair Amplifier

The second part of the input amplifier is the differential pair. For the present design two diffirencial pair amplifier scheme was chosen not compare the input differential signal to a known reference voltage, specifically +/- 200mV, instead of the ground.

Transistors M3, M4, M5, and M6 consistute the differential pair. This part of the circuit is actively switching, hence their dimensions should be minimized to increase speed of the circuit. Since MOSFET switching frequency is proportional to $\frac{V_{on}}{L^2}$, minimum channel length of 0.18μm was taken for them. Widths were picked up to satisfy the reset action for the latching transistors M7 and M8. The following table presents their characteristics.

Table 2. Characteristics of transistors M3, M4, M5, and M6

Transostor label	Width, μm	Length, μm	Ratio, L/W	Von, V
M3	1.8	0.18	1:10	-0.573
M4	1.8	0.18	1:10	-0.272
M5	1.8	0.18	1:10	-0.525
M6	1.8	0.18	1:10	-0.229

The most important part property of the differential pair is its gain. For calculating the gain, latching transistors M7 and M8 from the analalog latch will be used.

$$A_v = G_m * R_L \quad (1)$$

For the current circuit,

$$R_L = \frac{1}{4 * g_{m15} - g_{m7,8}} \qquad (2)$$

It was not clearly deduced how two differential pairs affect the overall transconductance. The next formula was used for the calculations.

$$G_m = g_{m3,4,5,6} \qquad (3)$$

In order to get the transconductance value, K'n and K'p should be estimated first. It was noted that every transistor has its own K' value. Thus, it was preferred to calculate K' for each transistor individually and pick the average value. Since all transistors that determine the gain value are in saturation, the following formula was used to determine the transconductance.

$$I_d = \frac{1}{2} * K' * \frac{W}{L} * (V_{GS} - V_t)^2 \qquad (4)$$

$$K' = \frac{2 * I_d}{(V_{GS} - V_t)^2} * \frac{W}{L} \qquad (5)$$

To reduce the dimension effects, a unit transistors was used with $\frac{W}{L} = 1$. Following table presents the calculated transconductance.

Table 3. Calculated transconductance for transistors M3, M4, M5, M6, M7, M8, and M15

Transistor label	Transconductance, A/V^2
M3	743.157µ
M4	956.964µ
M5	783.673µ
M6	999.218µ
M7	7.276m
M8	7.61m
M15	444.957µ

The mean value for $g_{m3,4,5,6} = 870.753\,\frac{\mu A}{V^2}$ and $g_{m7,8} = 7.668\,\frac{mA}{V^2}$. The value for g_{m15} was left as is. Therefore, the value for the input amplifer gain while in the tracking phase is

$$Av = \frac{870.754\mu}{4 * 444.957\mu - 7.668m} = 4.892e - 7 \qquad (6)$$

During the tracking phase

$$Av = \frac{870.754\mu}{-7.668m} = -0.1136 \qquad (7)$$

The low value for the amplifier gain was enough to achieve 206psec comparison speed. However, there is an uncertainty factor as, on one hand, the effect of 2 differential pairs was correctly estimated. On the other hand, the estimation of K' may be wrong as well.

Analog Latch

The analog latch regenerates the initially impressed differential voltage on the nodes a and b to a full CMOS logic level. It has multiple phases, the reset phase, where the value of a previous comparison on the latching transistors M7, M8 is removed using the advanced clock clk1a. This clock must be advanced. The first non-overlapped portion of the clock is dedicated to the reset. Further, the clk1a clock overlaps with the clock clk1b when the signal regeneration happens. The upper part of the latch is disconnected during the reset as the transistors M9 and M10 are off.

In order to calculate the regeneration time it is necessary to estimate the time constant.

Regeneration Time and Time Constant

The time consant is calculated using the following formula

$$\tau = \frac{C_{a,b}}{4 * g_{m15} - g_{m7,8}} \qquad (8)$$

Since the nodes a and b are identical, it will be enough if only one of them will be analized for the capacitance.

After the approximate analysis, the following equivalent circuit was deduced. Note, the analysis

assumed full logic levels reached in the latch.

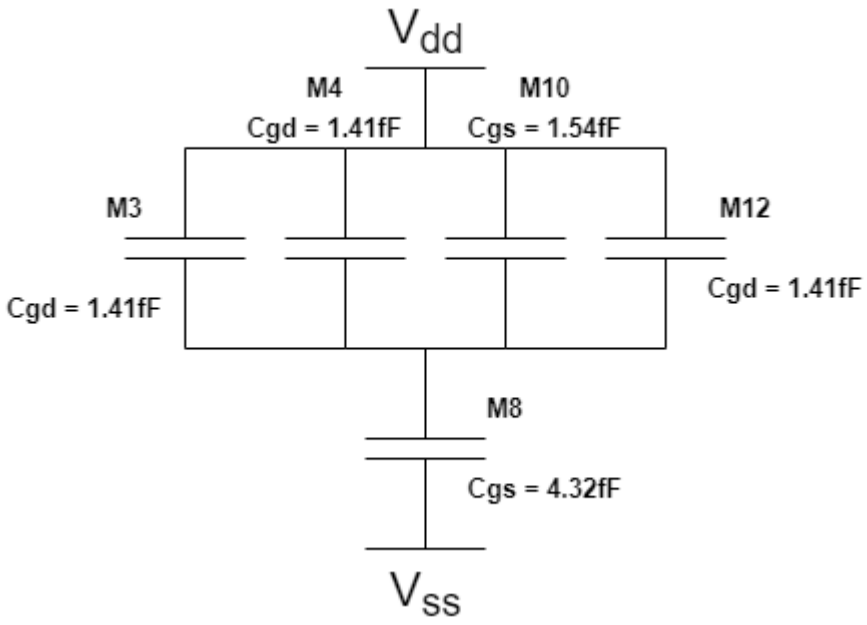


Figure 1. Equivalente capacitance circuit for the node b.

The equivalent capacitance of the M3, M4, M10, and M12 is 5.77fF. Therefore, the overall capacitance is

$$C_{a,b} = \frac{1}{\frac{1}{4.32f} + \frac{1}{5.77f}} = 2.47fF \qquad (9)$$

It can be noticed that the node a and b capacitances determine how big the time constant will be. Therefore, the MOSFET dimensions of the input amplifier along with the reset and switch transistros need to be picked up for the overall nodes capacitance to be 1, for the optimal speed. Finally, the time constant

$$\tau = \frac{C_{a,b}}{4 * g_{m15} - g_{m7,8}} = \frac{2.47f}{4 * 444.957\mu - 7.668\text{m}} = -41.949\, psec \qquad (10)$$

The regeneration time can be deduced from the next formula

$$\Delta V = \Delta V_0 * e^{-\frac{t_{regen}}{\tau}} \qquad (11)$$

$$t_{regen} = -\tau * \ln\left(\frac{\Delta V}{\Delta V_0}\right) = 372.876\, psec \qquad (12)$$

The presented hand calculations do not conincede with the simulation results. The comparison time achived by the simulation was 206psec. The reason is a rough estimation of the nodes a and b capacitance, that has direct relation with the time constant calculation. On the other hand, the estimated values of K' in the denominator is another possible source of deviation.

SR Latch

The SR latch has a purely digital logic. The dimensions of the transistors were set to have increased operating frequency.

Summary

The following table contrasts the project specifications, hand calculations, and simulation results.

Specification	Met	Simulation result
Comparisons must be accurate to better than 2mV	Yes	See overdive test/schematic/project
Time required to make a comparison < 400ps	206ps	372.876ps
Overdrive recovery test must be successful for differential inputs up to at least ± 400mV	Yes	See overdrive test/project/schematic

Comparison is to a differential reference voltage of ± 200mV	Yes	See project/overdrive test
Outputs = Q and QB, with a full digital CMOS output swing	Yes	See project/overdrive test
Minimum Von = Vgs - Vt for all saturated FETs = 100 mV	Yes	See Tables 1 through 3
Process = 0.18µm CMOS, with VDD = 1.6 V and temperature = 27° C	Yes	See project/overdrive test/schematic
Full swing digital CMOS input clocks with 10%-90% rise/fall times of 100ps	Yes	See schematic/project/overdrive test

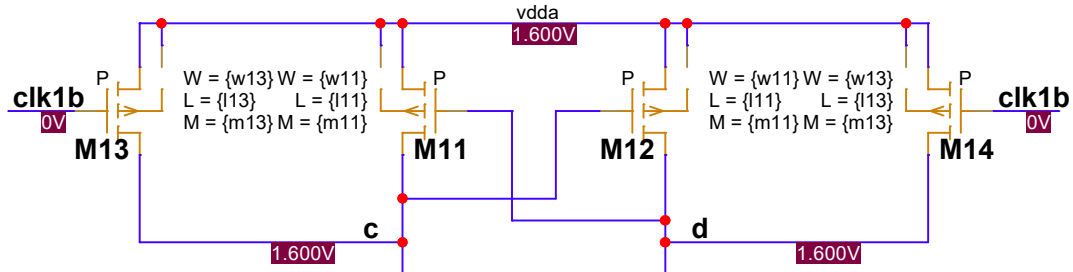
Conclusion

This report described the results of design and simulation of a latching comparator. The design process is different to analysis, though they cannot live without each other. I got acquainted with the analog design process unknown to that scale for me so far. It is hard to find appropriate words to express usefulness of this kind of exercise. I have applied in practice the concepts learned in the class and achieved a deeper understanding of how the latching comparator works, and what considerations needs to take into account a designer to meet particular project specifications.

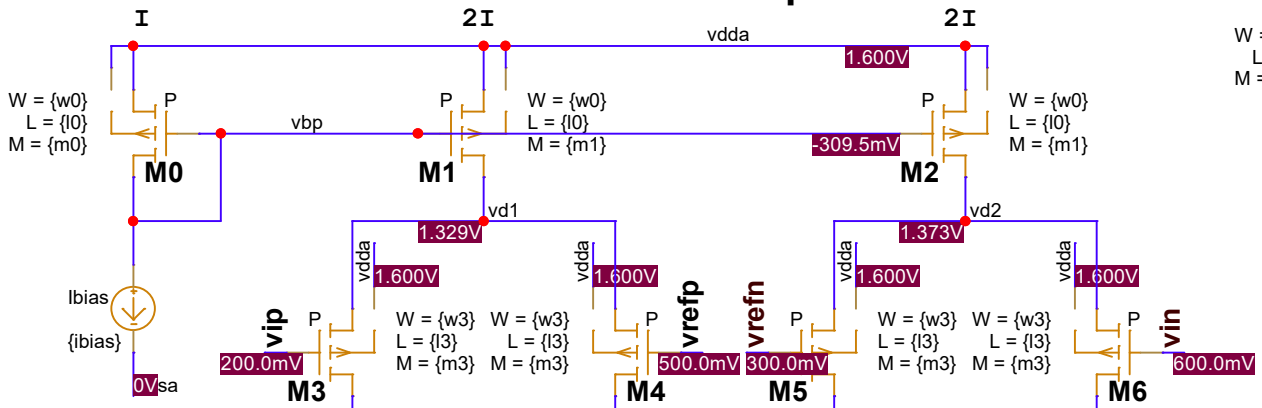
PARAMETERS:

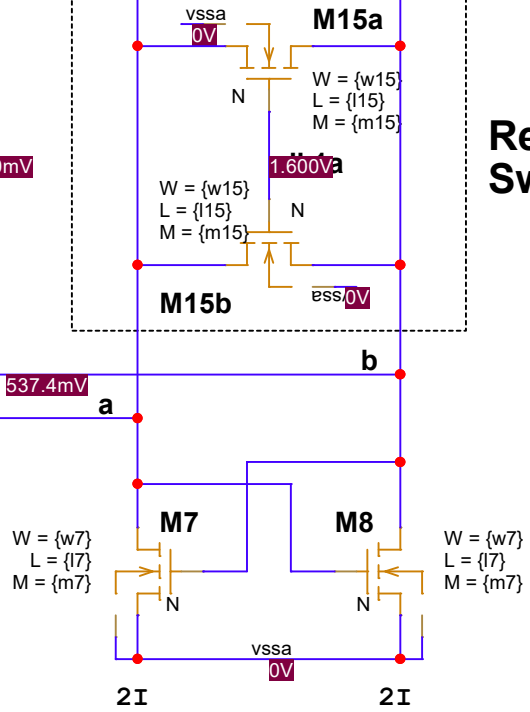
			m1 = 4	
vdda = 1.6	w0 = 3.6u	l0 = 1.8u	m0 = 2	per = 10ns
vssa = 0.0	w3 = 0.9u	l3 = 0.18u	m3 = 2	pw = {per/2 - tr}
	w7 = 0.18u	l7 = 0.18u	m7 = 28	tr = 100ps
ibias = 200u	w9 = 0.9u	l9 = 0.18u	m9 = 2	
	w11 = 0.9u	l11 = 0.18u	m11 = 2	td1 = {(0.5*per) - 5p}
vref = 200mV	w13 = 0.9u	l13 = 0.18u	m13 = 2	td2 = {0.5*per}
vi1 = -0.4V	w15 = 0.9u	l15 = 0.18u	m15 = 1	tdi = {0.75*per}
vi2 = 201.8mV	w16 = 0.36u	l16 = 0.18u	m16 = 1	
vicm = 400mV	w18 = 0.36u	l18 = 0.18u	m18 = 1	

Analog Latch

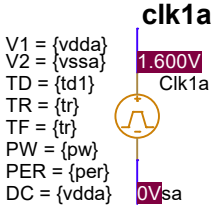


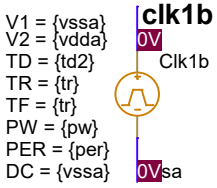
Preamp

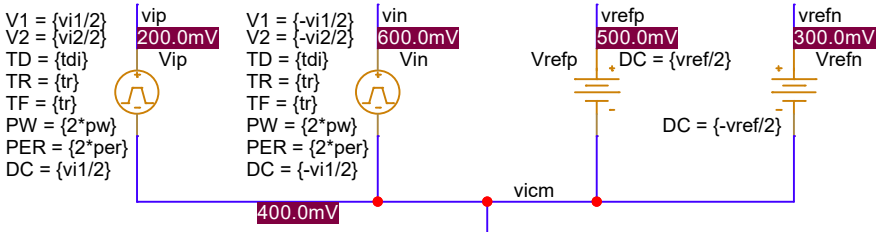


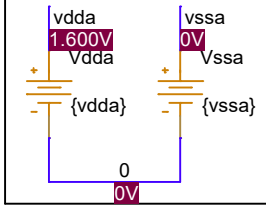


Reset Switch

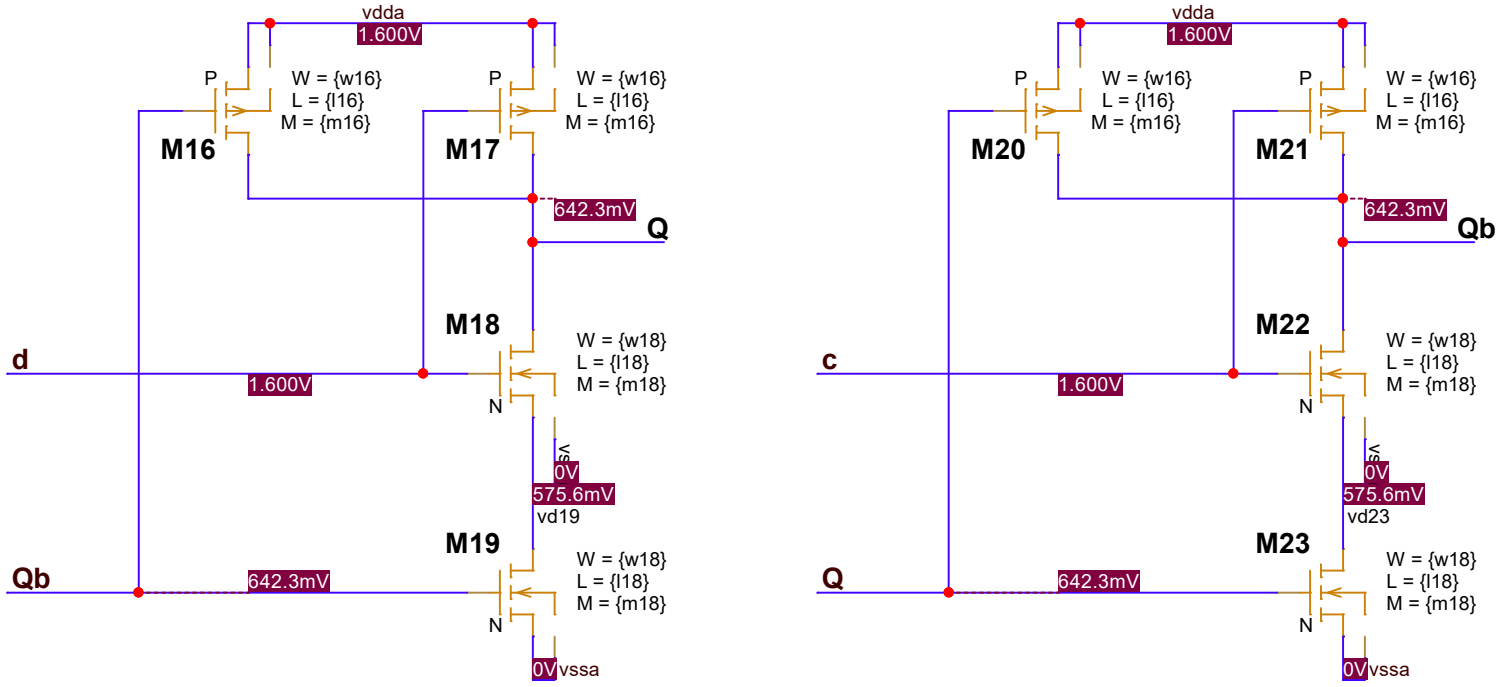






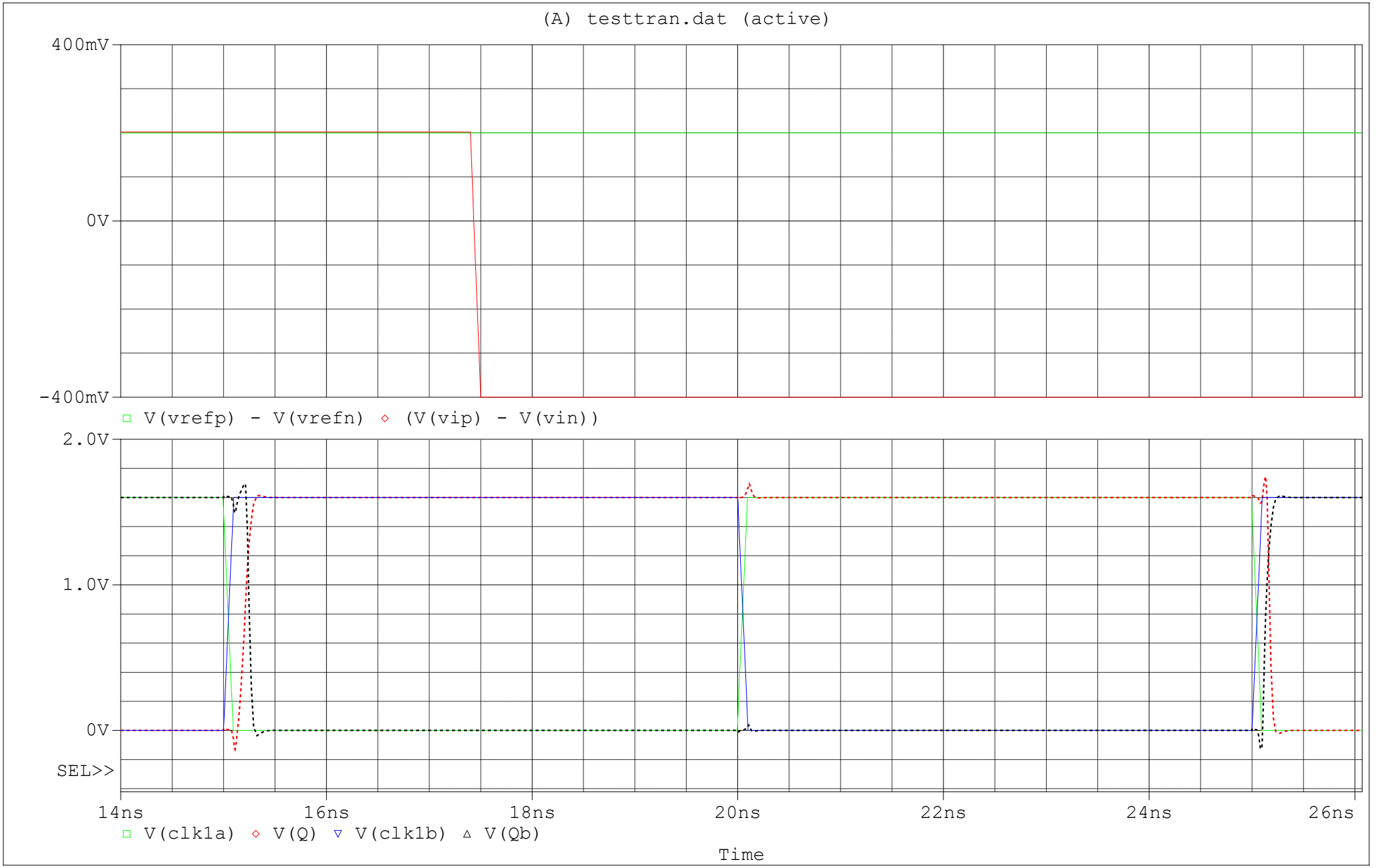


Designer = Vladislav Rykov		
Title: Differential Latching Comparator. Preamp and Analog Latch		
Size: A	Document Number: comparator_latching	Rev: A0
Date: Sunday, March 13, 2022	Sheet 1 of 1	

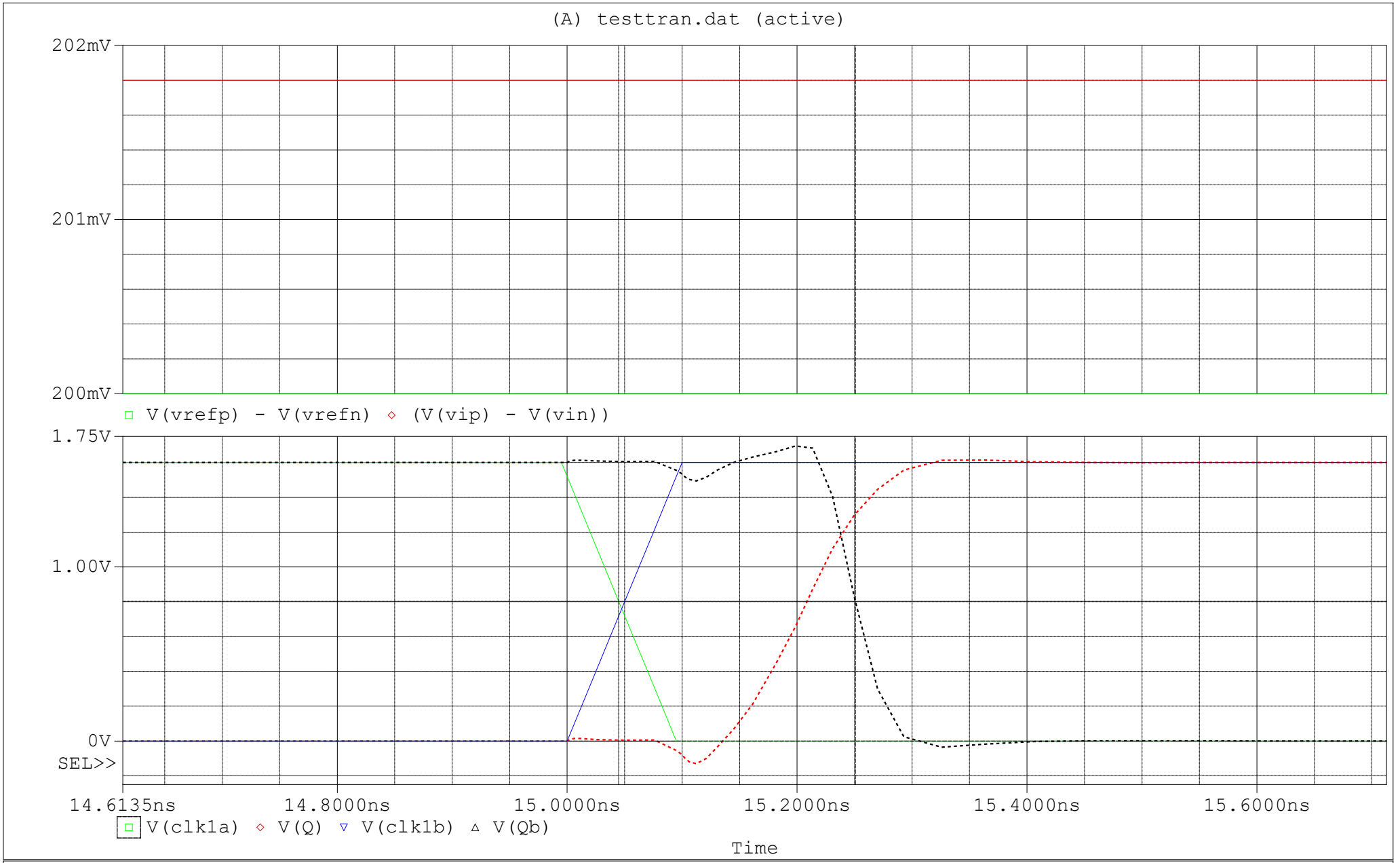


Digital S/R Latch

Designer = Vladislav Rykov		
Title: **Differential Latching Comparator. SR Flip-Flop**		
Size: A	Document Number: **comparator_latching**	Rev: A0
Date: Sunday, March 13, 2022	Sheet 1 of 1	

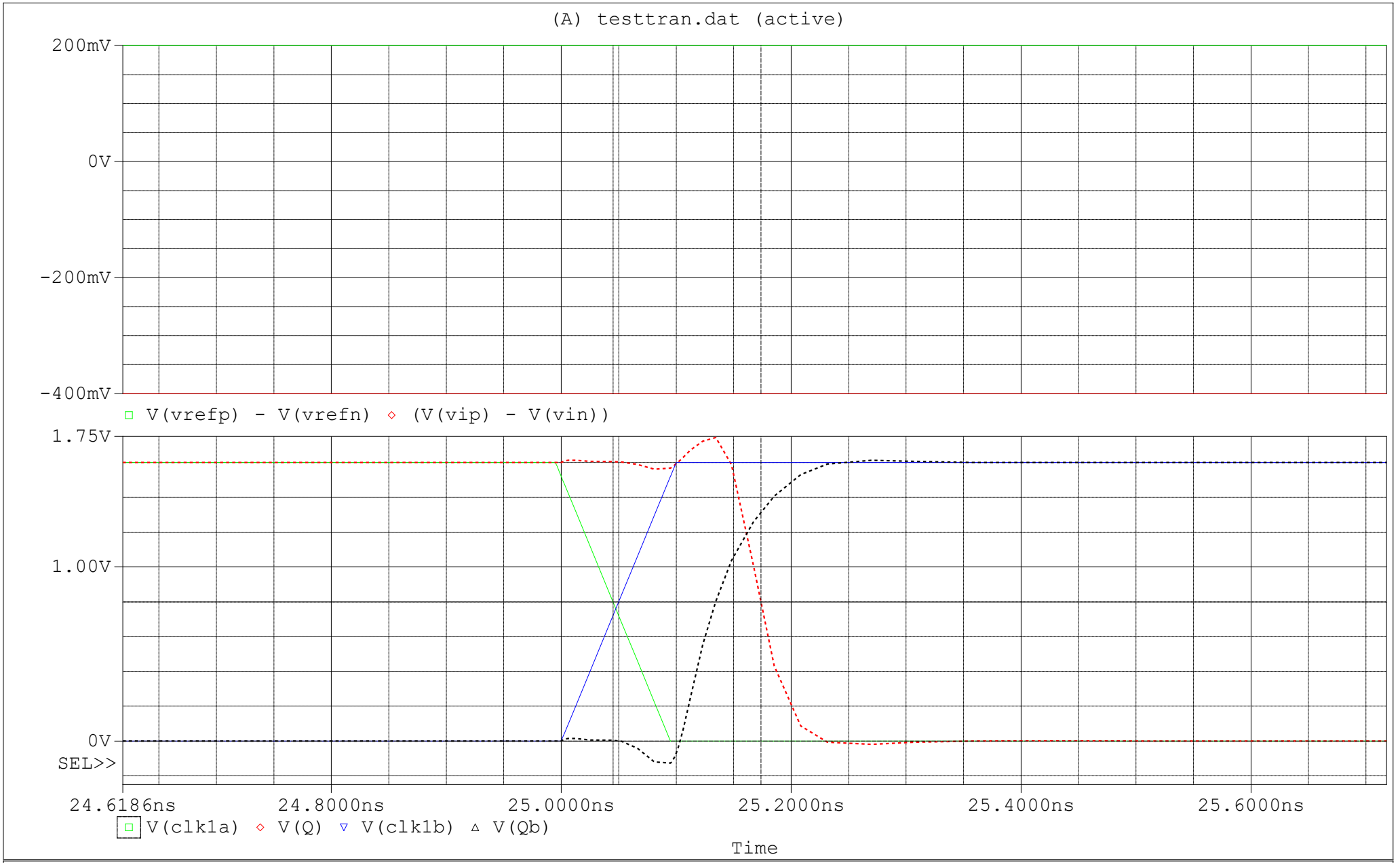

(A) testtran.dat (active)
400mV
0V
-400mV
V(vrefp) - V(vrefn)
(V(vip) - V(vin))
2.0V
1.0V
0V
SEL>>
14ns
16ns
18ns
20ns
22ns
24ns
26ns
V(clk1a)
V(Q)
V(clk1b)
V(Qb)
Time

** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 03/14/22 00:58:51 Temperature: 27.0



A1:(15.045n,803.571m) A2:(15.251n,0.000) DIFF(A):(-206.003p,803.571m)

** Profile: "SCHEMATIC1-testtran" [D:\OneDrive\OneDrive - Asian Answers\Documentos\CSUS\EEE232\Projects\Projec...
Date/Time run: 03/14/22 00:58:51 Temperature: 27.0



A1:(25.045n,796.729m) A2:(25.174n,0.000) DIFF(A):(-128.597p,796.729m)