

Introduction to Operating system

Q What is OS?

Web, browser

OS is a program/
software that creates
interface/module for
users to use raw
hardware

Hardware: keyboard,
monitor, sound, graphics.

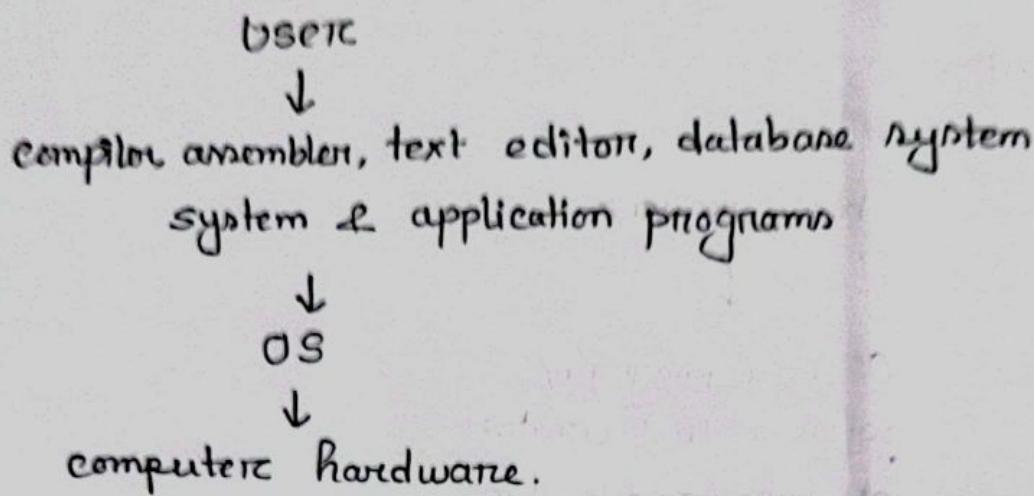
Q System software vs application software

↓
Directly communicates
with hardware.

↓
designed for end users.
people who are using the
applications.

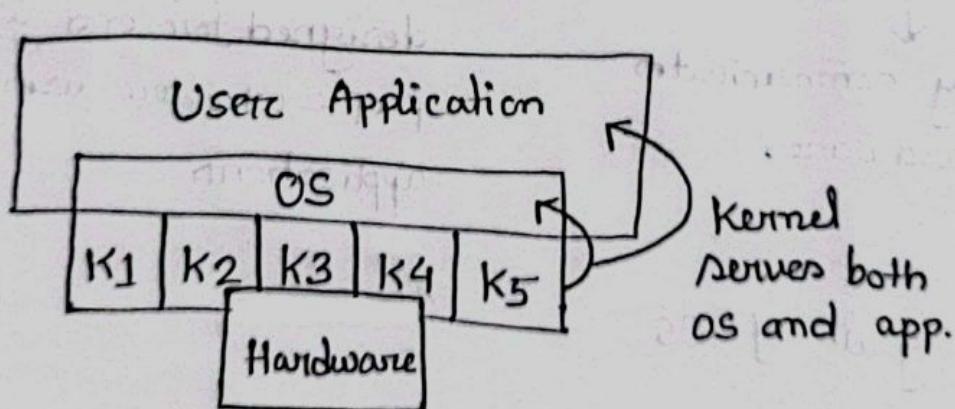
Q Major goals of OS.

Q1 Computer system organization



Q2 Kernel.

- One program running at all times
- smaller the better
- loads first
- remains in main memory.



- loaded into a protected area so that they can't be overwritten.

☒ Bootstrap program

→ stored in ROM or EEPROM.

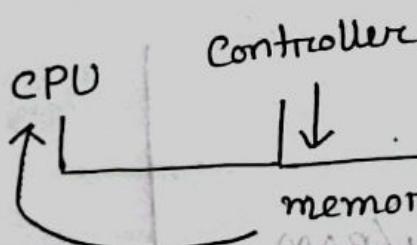
☒ Computer system organization

→ there can be 1 or more CPU

→ data communication is through bus.

☒ Operation of a controller

Keyboard



☒ Device driver vs device controller

kernel / software

Device controller manages the communication

between device driver and OS.

device

Driver
controller

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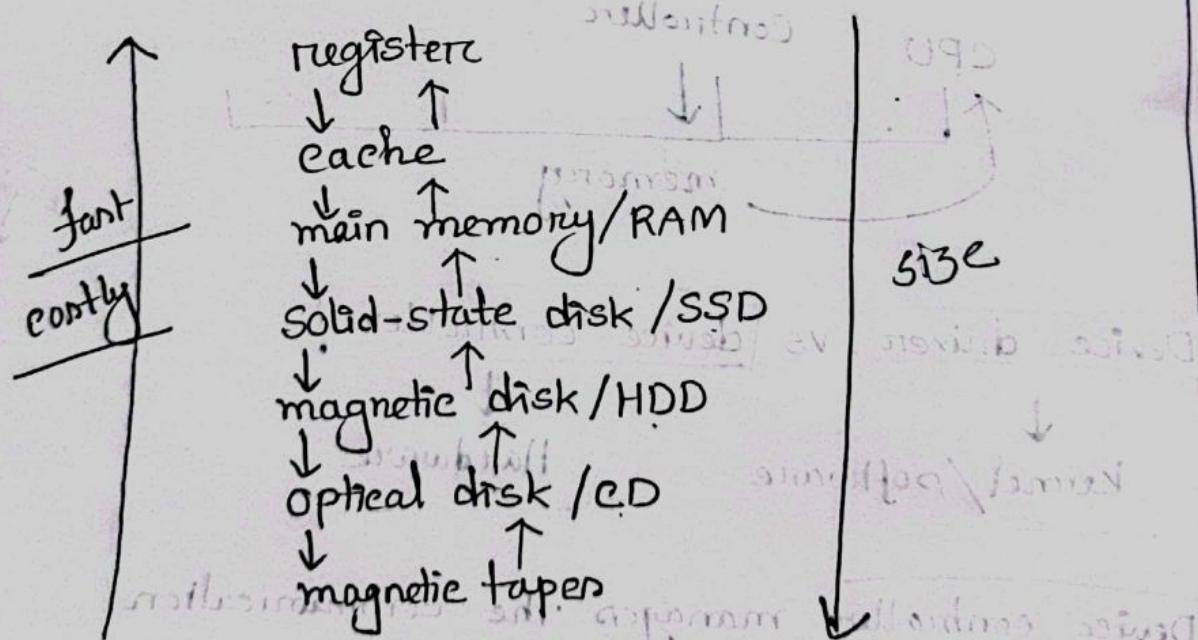
Storage Structure

I) Main memory : RAM, deleted after PC is shutdown, volatile.

II) Secondary memory : non volatile

Suppose a movie file is in HDD but our media and CPU can't access it as HDD is secondary memory. So movie is first transferred to main memory and media shows it.

→ kernel is in EEPROM / firmware



Q1 OS architecture

- 1] Single processor \rightarrow 1 CPU + special purpose processor
- 2] Multipurpose processor \rightarrow multiple CPU
- 3] Clustered system \rightarrow individual systems/nodes closely linked via local area network (LAN). Fast communication. Example: InfiniBand

Q2 Multiprogramming

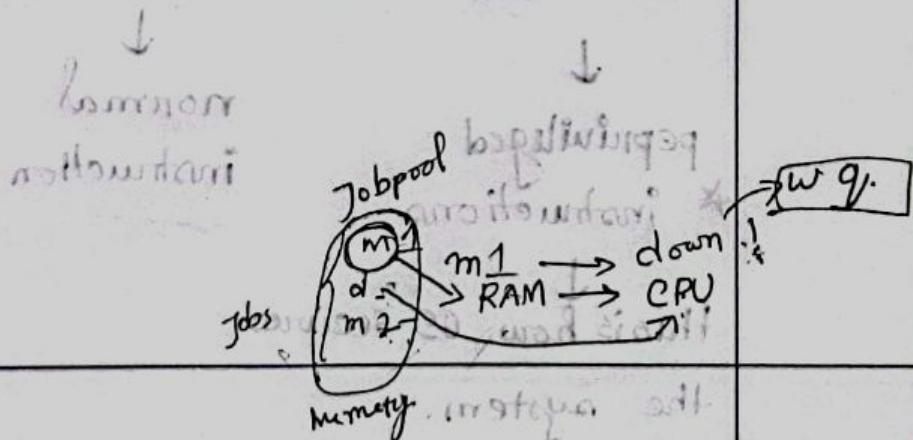
* CPU is never idle

Job $\xrightarrow[\text{pool}]{\text{OS}}$ memory \rightarrow processor

* ensures jobs are listed in memory from pool.

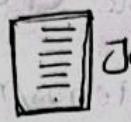
Q3 Time Sharing

- interactive system
- response time is very less.



Requirement of multiprogramming

1] Job scheduling



Job pool

↓ OS (job scheduler) → decides which job will be loaded into memory.

2] CPU scheduling



memory

↓ CPU scheduler

CPU

* Virtual memory

OS operations

interrupt driven

Dual mode operation → mode change

as code
↓
kernel(0)
↓
privileged
instructions

this is how OS secures

the system.

user code
↓
(1)
↓
normal
instruction

System call.

OS ଯାଏ - ଯେହି functionalities / module ପ୍ରଦାନ କରିଛା

Hardware ଯାଏ - ଯେହି functionalities user application

କେବଳ provide କରାଯାଇ - କଥା - ଯେହି scope ଯାଏ - କେବଳ

System call Interface

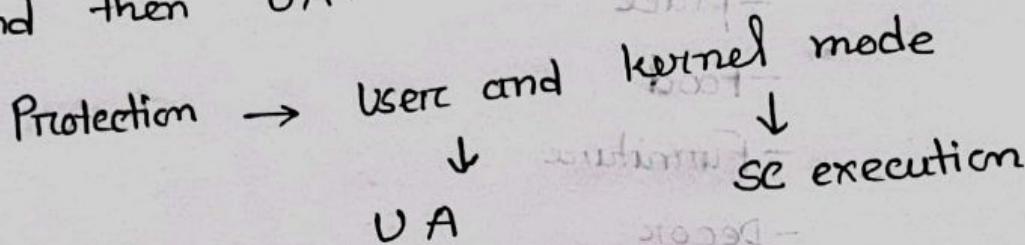
ଯୁଧନ - user application ଏବଂ କୋନାଟକ

complete ରହିଥାଏ, ତଥାନ୍ତି ତା - ଜୋନାଟି System

call interface ହୁଏ, SCI ଏବଂ କାହିଁ table ଥାଏ ଯାଏ

ଏବଂ system call list ରୁବୁ ଥାଏବା After the lines
of codes are executed, value will return to

SCI and then UA.



SCI knows everyone and works for everyone

fork() → create process()

OS System Program

OS System boot

execute bootstrap program

OS Process

Batch system → jobs

Time sharing system → tasks / user programs

Modern OS → process → a program that is in execution

Example: Farewell program

- place

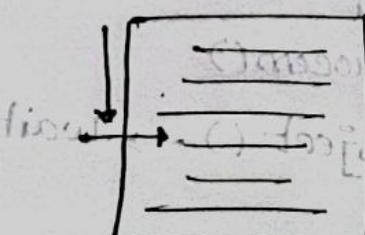
- Food

- Furniture

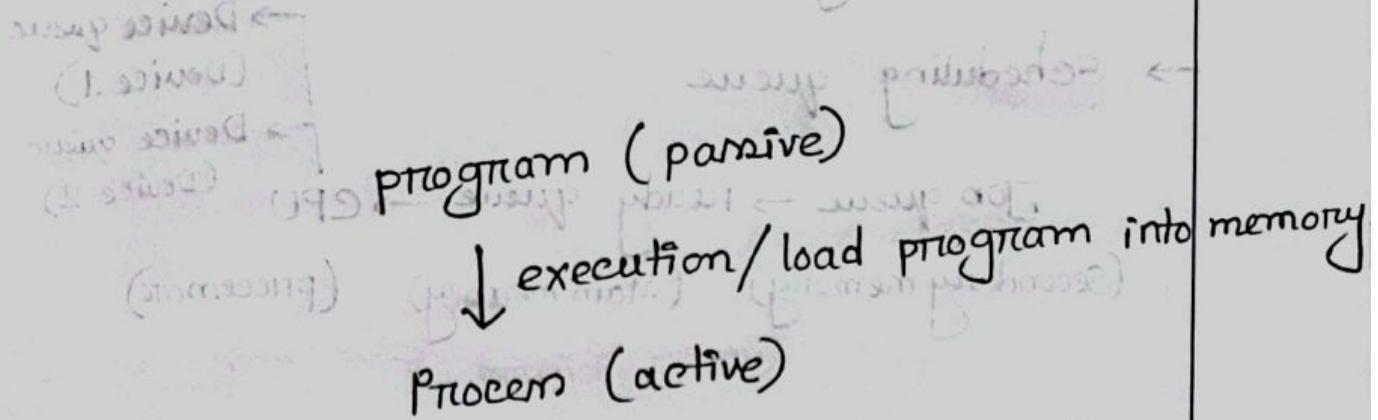
- Decor

process has:

- program counter



- Stack : temporary data (function param, local var, return address)
- Data section : global var
- Heap : dynamically allocated memory during runtime.
- text : programming code



{ 1 program can have multiple process.
google chrome having multiple windows.

States of a process : 5 states

- New → [HDD] → [RAM memory]
- Running → [RAM memory] → CPU
- Waiting → [RAM memory] if CPU is busy, wait in RAM memory, or other waiting
- Ready → process is ready to go from RAM memory to CPU
- Terminated

Q Process State Diagram

Representation of process in OS

process control block (PCB)

Waiting queue

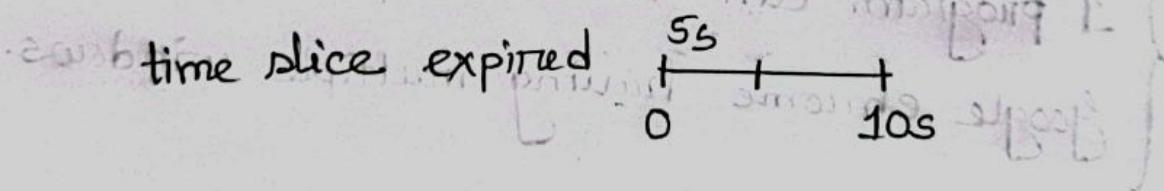
Q Process Scheduling

→ Scheduling queue

Job queue → ready queue → CPU
(Secondary memory) (Main memory) (Processor)

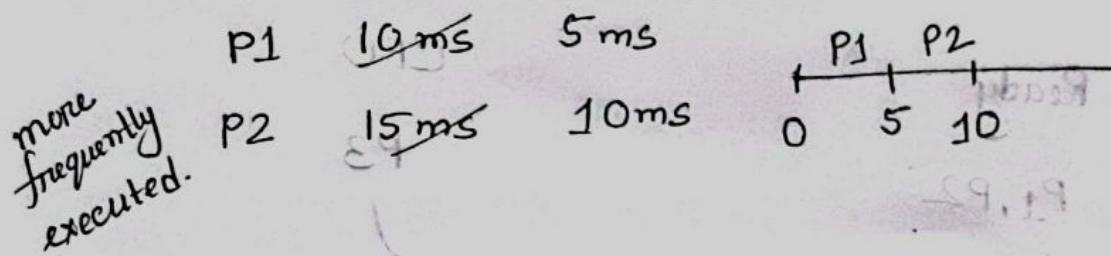
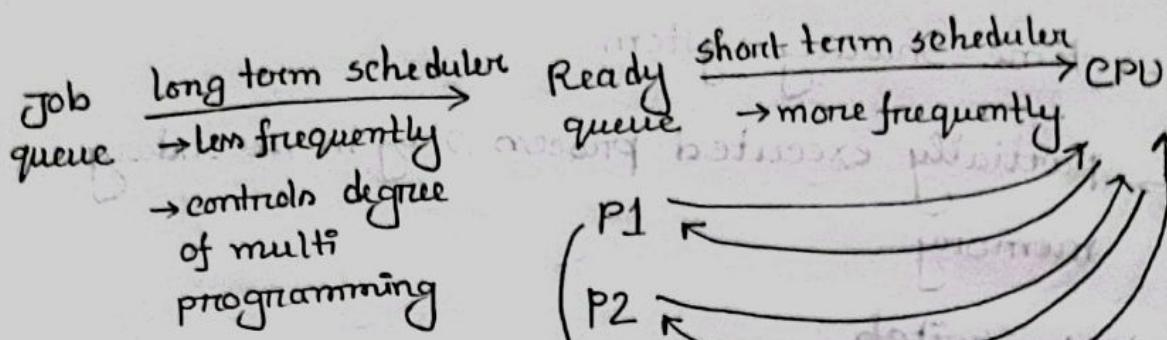
Device queue
(Device 1)
Device queue
(Device 2)

→ Queuing Diagram



Except for ready queue, if a process is in any other queue, it is in waiting state.

Scheduler

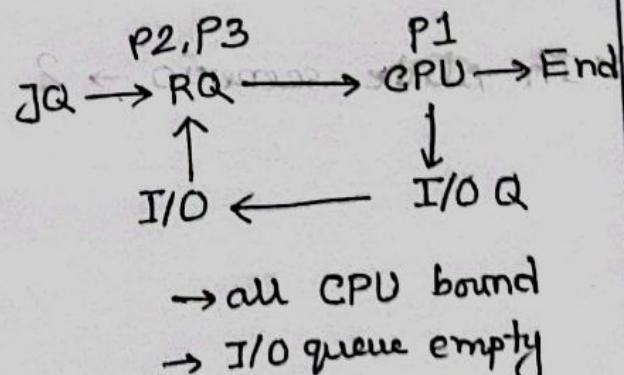
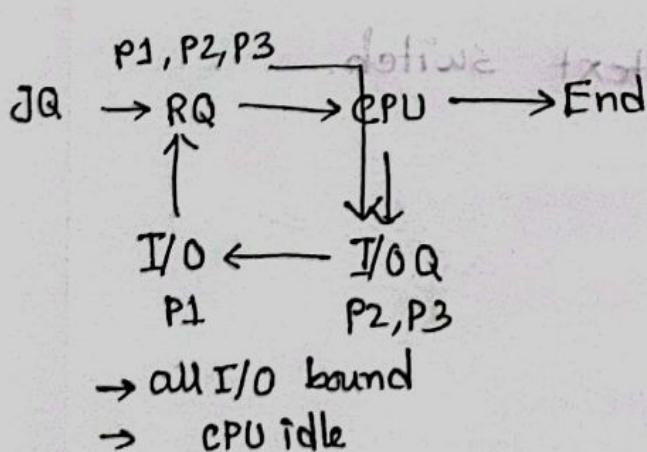


CPU bound vs I/O bound process

CPU bound → find prime #

I/O bound → calculate input

Long term scheduler must select wisely. They can't all be CPU bound or I/O bound only.

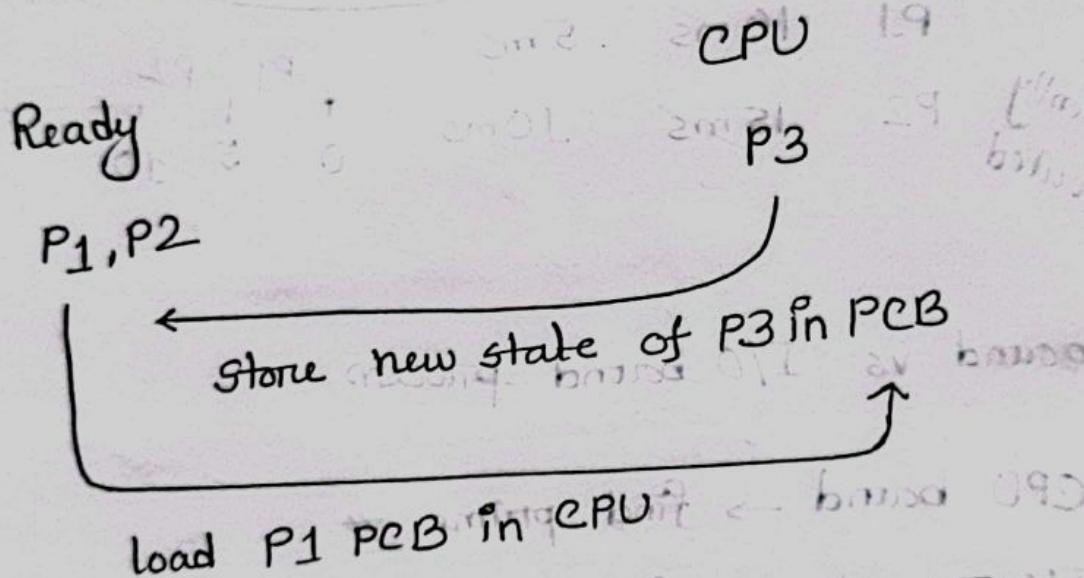


→ RQ empty because we can't bring new process.

Q5 Medium term scheduler

- time sharing system
- partially executed process stay in secondary memory

Q6 Context switch.



during this switch, CPU stays idle. This is called context switch time. This time is overhead, no CPU utilization.

* In slide scenario \rightarrow 2 context switch.

Operations on process

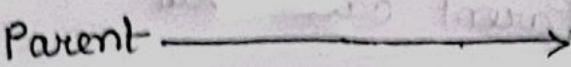
unique PID

→ Process Creation

①

Parent

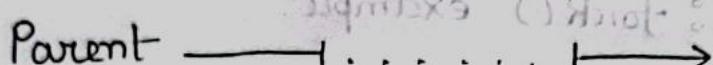
child



②

Parent

child



→ process creation in Unix

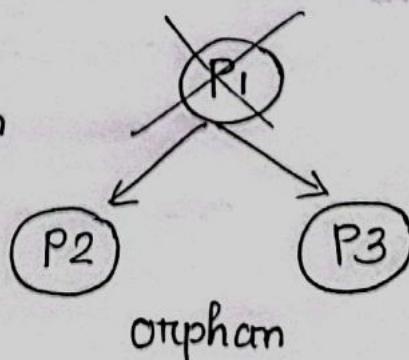
fork() → creates new child process

parent PID > 0

child PID = 0

→ process termination

cascading termination

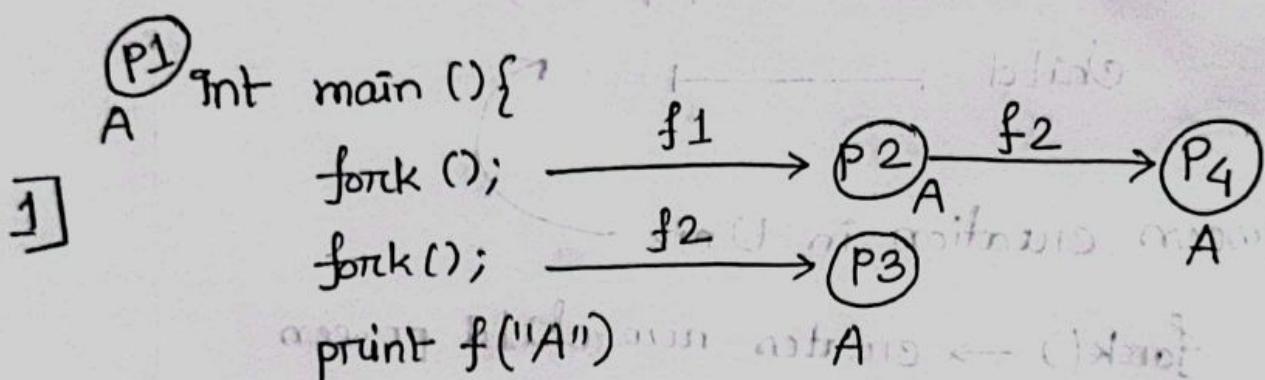


orphan

Zombie process in Unix

child process ends but parent doesn't call wait. System thinks child resources are running but in reality the resources are not running, hence zombie process. Parent calls wait function late.

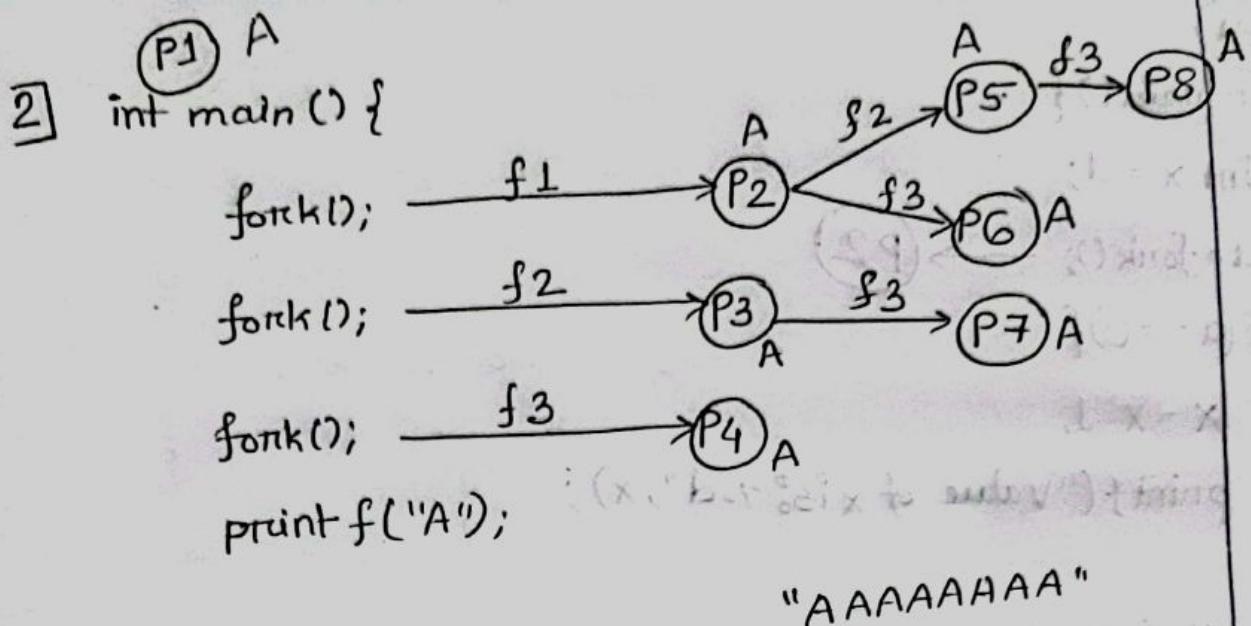
Process Creation : fork() example.



4 process

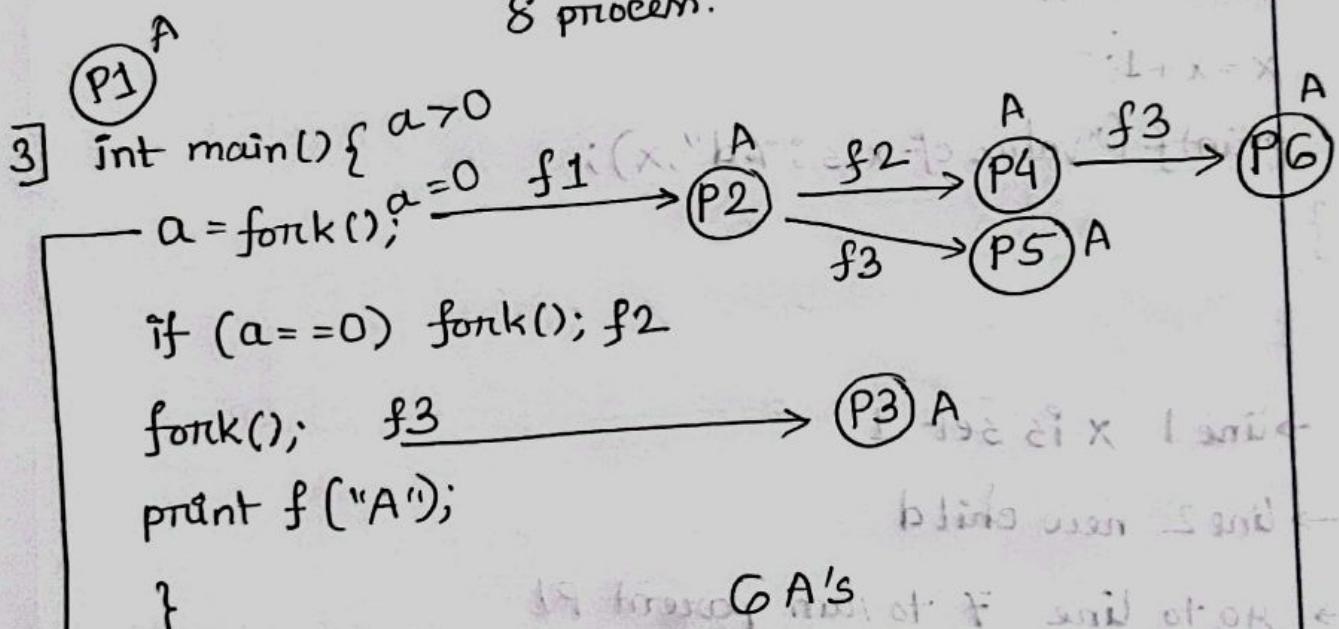
3 child process

4 A's



8 A's

8 process.



}

6 A's

6 process

a has fork return value

if $a > 0 \rightarrow$ parent

if $a = 0 \rightarrow$ child.

"AAAAAA"

P1
4] int main() {

1. int x = 1;

2. a=fork(); → P2

3. if(a==0){

4. x=x-1;

5. printf("Value of x is %d",x);

6. }

7. else if(a>0){

8. wait(NULL);

9. x=x+1;-

10. printf("Value of x is : %d",x);

11. }

12. }

→ line 1 x is set 1

→ line 2 new child

→ go to line 7 to run parent P1

→ line 8 wait for child to finish

→ line 3 a == 0 of child.

→ x = 1 - 1 = 0 , print "value of x is 0"

→ return to line 9 , x is now 1 → global var

→ x = 1 + 1 , print "value of x is 2"

5] $\text{int main}()\{\text{P1}$

$a = \text{fork}();$ $\xrightarrow[\text{if } a < 0]{f1} \text{P2}$

$\text{if } (a == 0) \{$

$\text{print}('B');$

}

$\text{else if } (a > 0) \{$

$\text{wait}(NULL);$

$\text{fork}();$ $\xrightarrow{f2} \text{P3}$

}

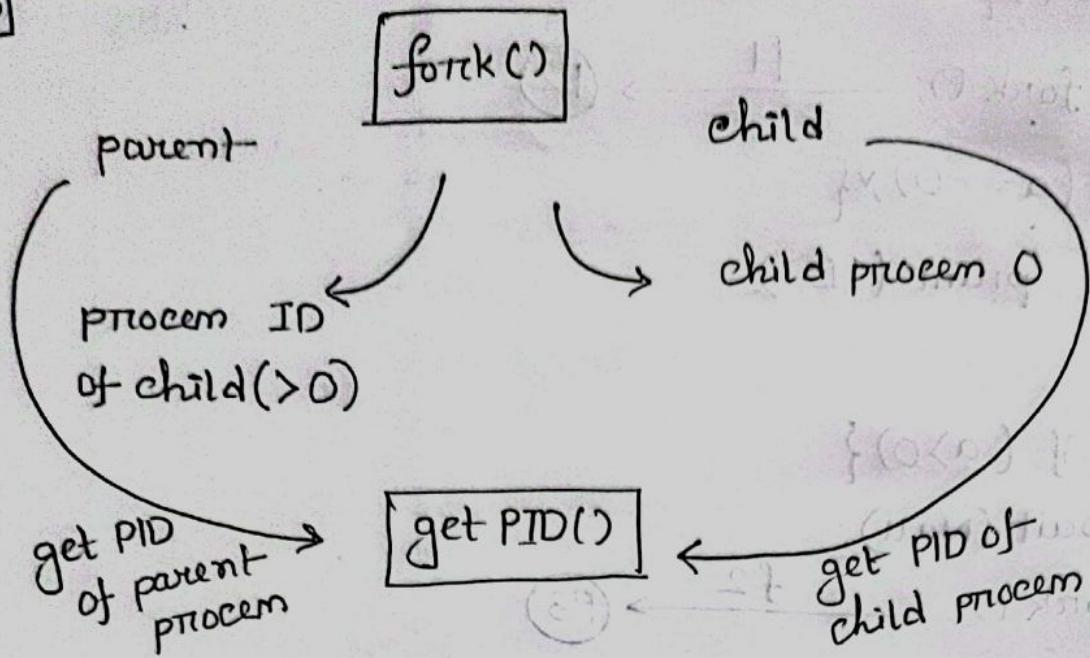
$\text{print}('A');$

B A A A
↓ ↓ ↓ ↓
P2 P2 P1 P3

If no wait :

A B A A
↓ ↓ ↓
P1 P2 P3

6



p1
7 int main () {

 fork(); → f1

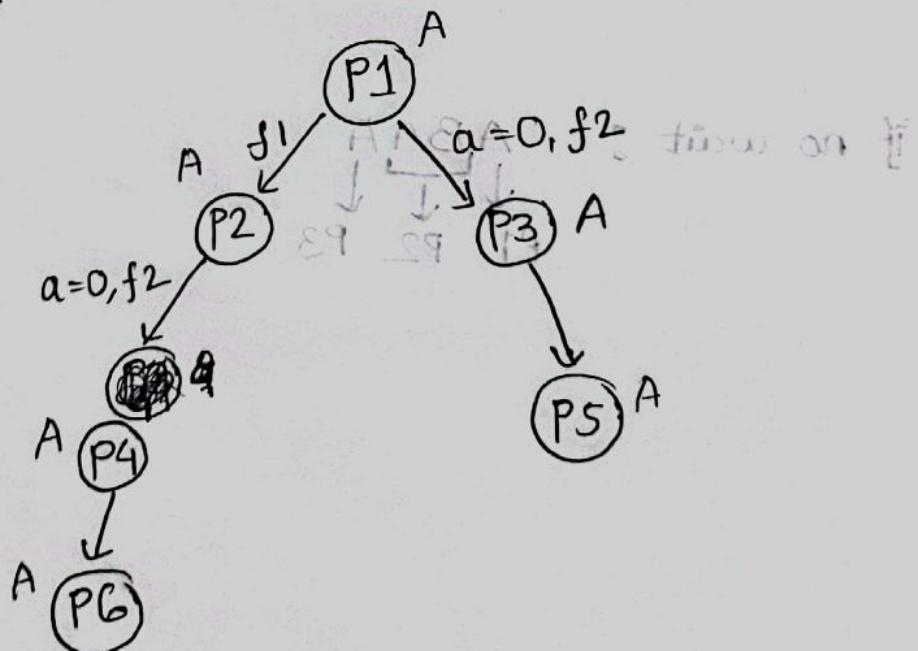
 a=fork(); → f2

 if (a == 0) fork(); → f3

 printf("A");

}

A A A B
↓ ↓ ↓ ↓
89 19 19 89



Interprocess Communication (IPC)

- 1) Independent
- 2) Cooperating → why we need it?

- info sharing
- computational speedup
- modularity
- convenience

two types of IPC's

1. Shared memory → fast

distributed system
small amount of data

2. Message passing → slower because it needs kernel to pass messages. So it is costly as well

→ Shared memory system

producer

buffer / shared space

consumer

producer-consumer problem (Producer)

buffer : 2 types → Bounded (limited space)

→ Unbounded (unlimited space)

Code is not efficient : n size buffer, (n-1) full.

(Consumer)

Message passing system

→ no shared space but distributed system.

→ systems reside in different locations

→ small amount of data.

→ implementation of producer consumer

using semaphores

message premium buffer ←

recursion

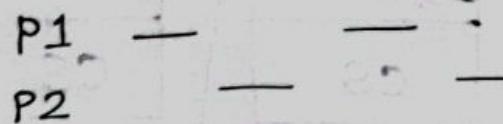
single buffer / offset

counter

Process Synchronization.

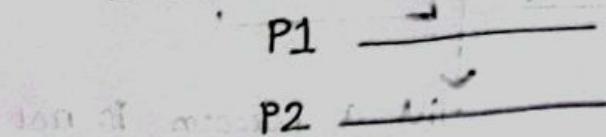
Q Background.

Concurrent:



Issue:-
} Shared
variable }
} data
integrity
problem.

Parallel:



Q Producer Consumer problem

counter → shared variable
during parallel execution, if both producer and consumer tries to update counter, data integrity problem arises.

Q Data integrity problem.

Q Race condition.

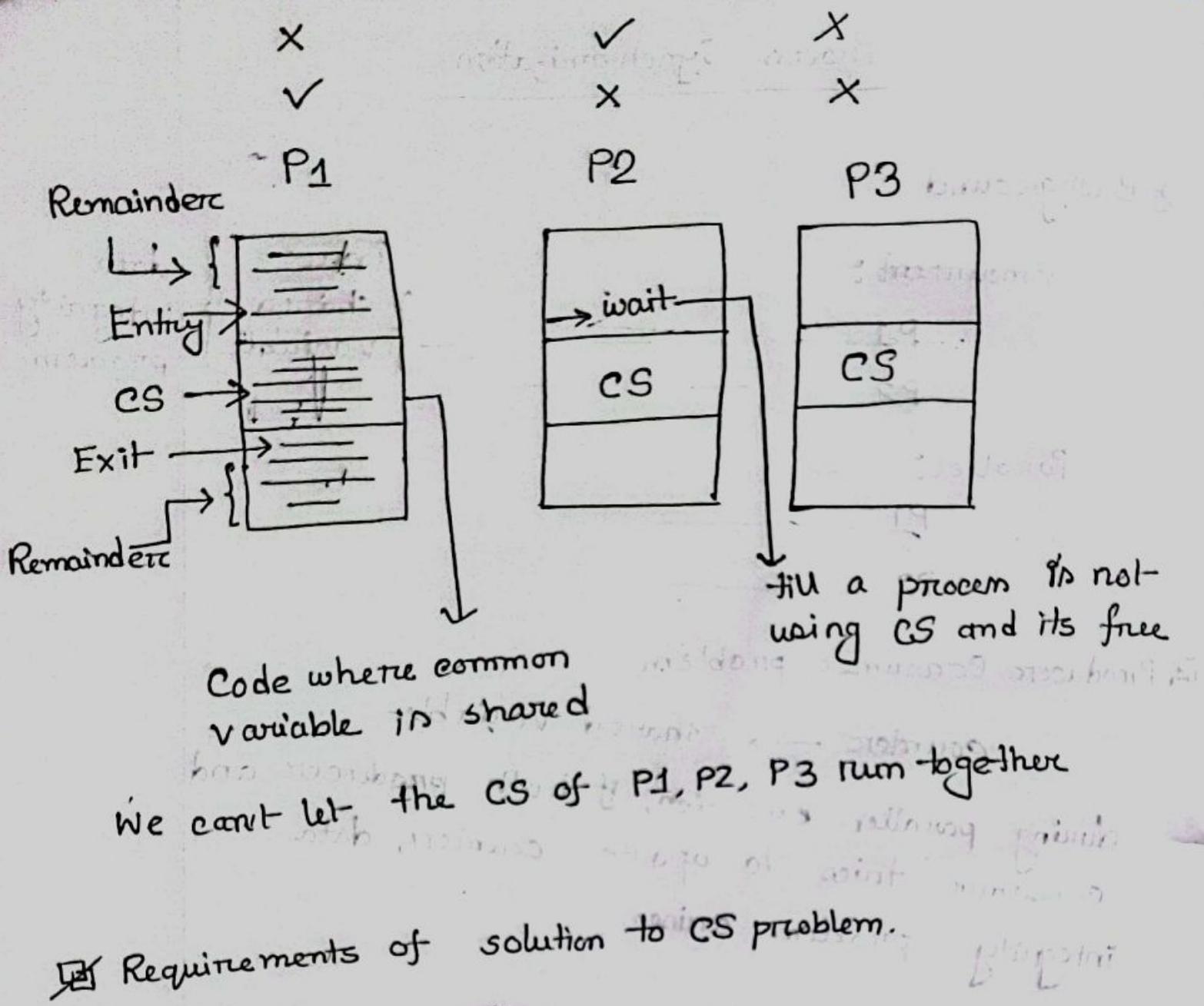
Solution

Q Critical Section.

Entry Section

Exit Section

Remainder Section.



Requirements of solution to CS problem.

- ① Mutual exclusion
- ② Programs
- ③ Bounded waiting

Critical Sections in OS.

① Preemptive kernel \rightarrow race condition

② Non - " " \rightarrow no " "

Peterson Solution for CS problem:

Software based solution

2 process only.

int turn \rightarrow variable

boolean flag [2] \rightarrow array

Suppose 2 process P_i and P_j

turn = \square next in line

flag = $\begin{array}{|c|c|} \hline T & F \\ \hline \end{array}$ ready to go to CS

Flag = $\begin{array}{|c|c|} \hline F & T \\ \hline \end{array}$

P_j ready for CS

limitation: can't be solved for multiple processes.

flag true \rightarrow ready to go to CS, false \rightarrow not ready.

Q) Hardware based solution

locking → flag.

test and set(), compare and swap()

word → memory unit/location

atomically → 3 instructions in a single part,
no other instruction will go
in between.

Q) Test and set()

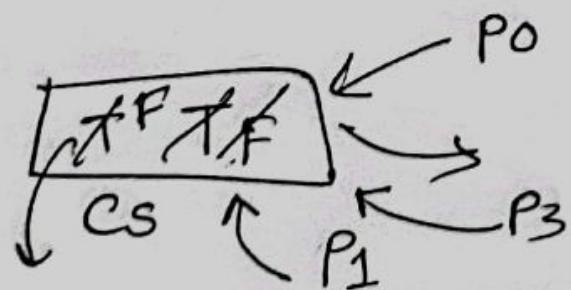
executed atomically.

* target → location of variable

* target = true → check and modify

& lock → flag location

True → already CS or CLR
wait till false.



☛ Compare and swap()

1 → already CS @ working

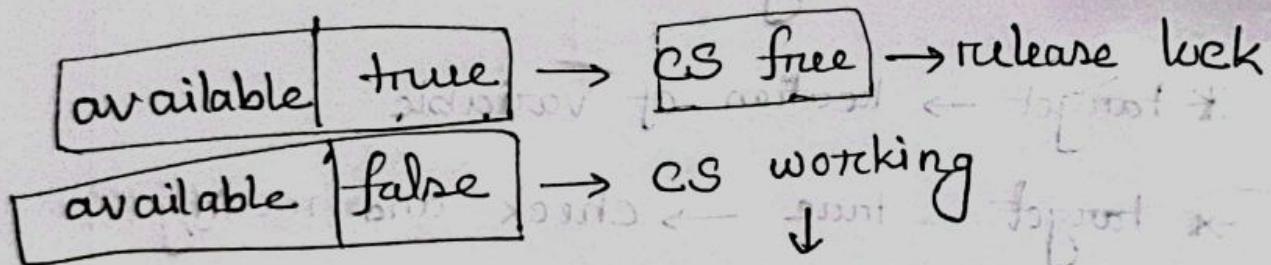
0 → CS free

& lock → flag

0/1 → int * value → int variable

☛ Mutex lock

Simplest solution of Hardware solution.



acquire lock

method

09

Semaphore

Synch technique

int variable

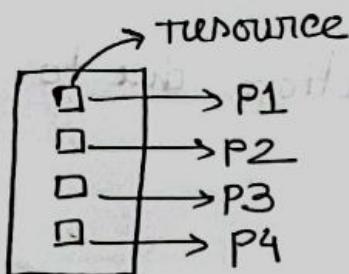
wait(), signal() \rightarrow atomic operation

CS এর দ্রোণার
যোজা - call করে

CS এর কাজ
শেষ হলে call করে

2 types of semaphore

① Counting semaphore



$s = 4 \rightarrow 4$ resource instance

$$S = n = 5$$

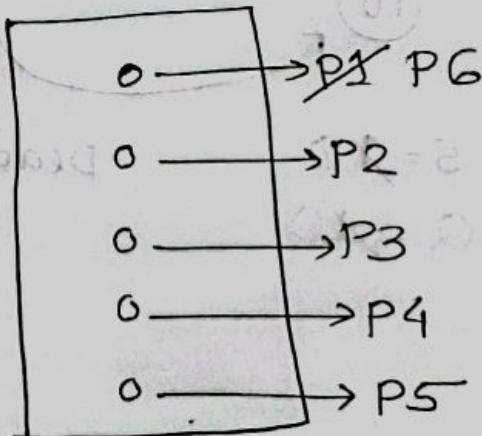
$$P_1.\text{wait}(s) \rightarrow S = 4$$

$$P_2.\text{wait}(s) \rightarrow S = 3$$

$$P_3.\text{wait}(s) \rightarrow S = 2$$

$$P_4.\text{wait}(s) \rightarrow S = 1$$

$$P_5.\text{wait}(s) \rightarrow S = 0$$



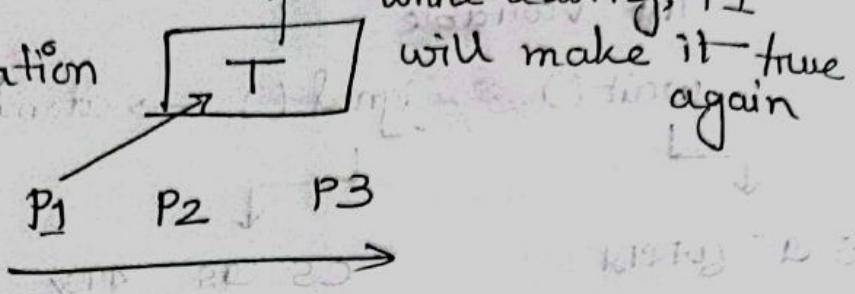
P6.wait(s) \rightarrow has to wait for signal() because $S = 0$

$$P_1.\text{signal}(s) \rightarrow S = 1$$

$$P_6.\text{wait}(s) \rightarrow S = 0$$

⑪ Binary Semaphore

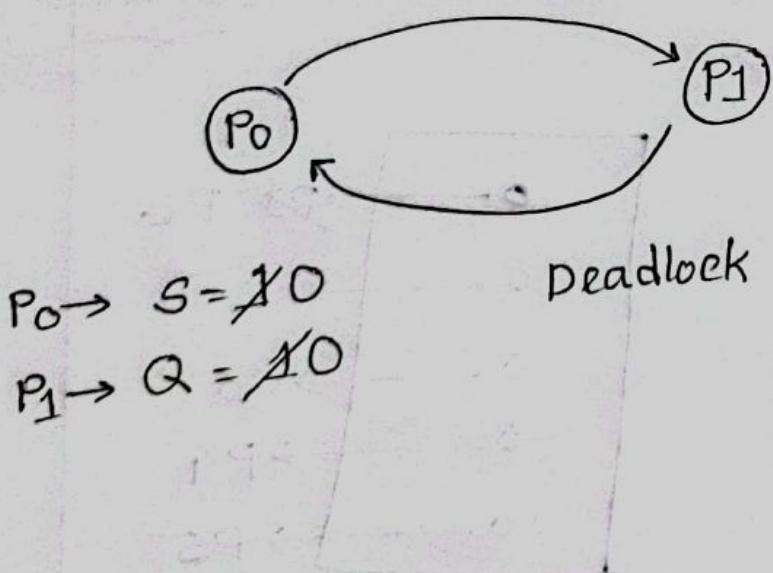
Resource / location



☒ Mutual exclusion with Semaphore

Binary semaphore \rightarrow mutex

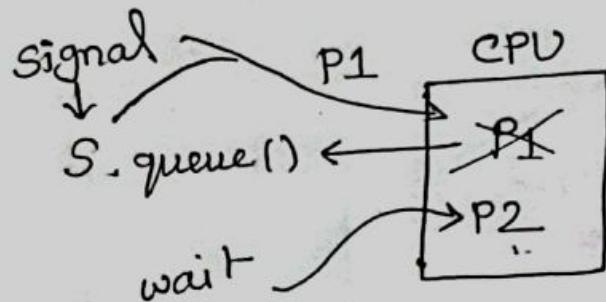
☒ Deadlock and Starvation due to semaphore



Semaphore Implementation.

resource call \rightarrow wait

exit \rightarrow signal



$s \rightarrow value = \emptyset$ $-1 < 0$

$s \rightarrow list = \{ P_1 \}$ \rightarrow block P_1 so that another process can use CPU

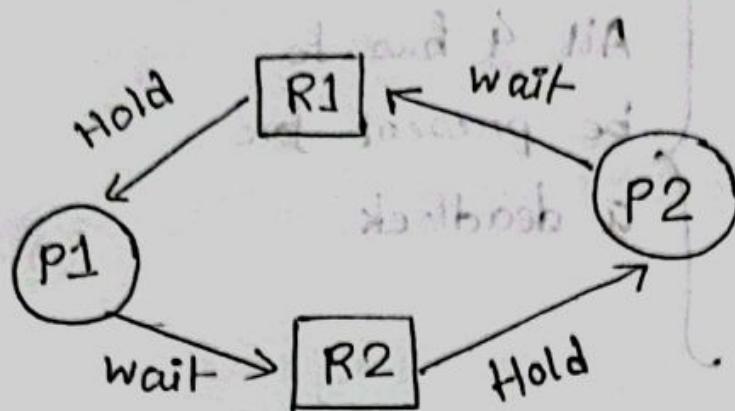
$P_1.wait()$

$P_1.signal()$

$s \rightarrow value = \cancel{\emptyset} \cancel{1} 0 \rightarrow$ wake up P_1
because $s.value \geq 0$

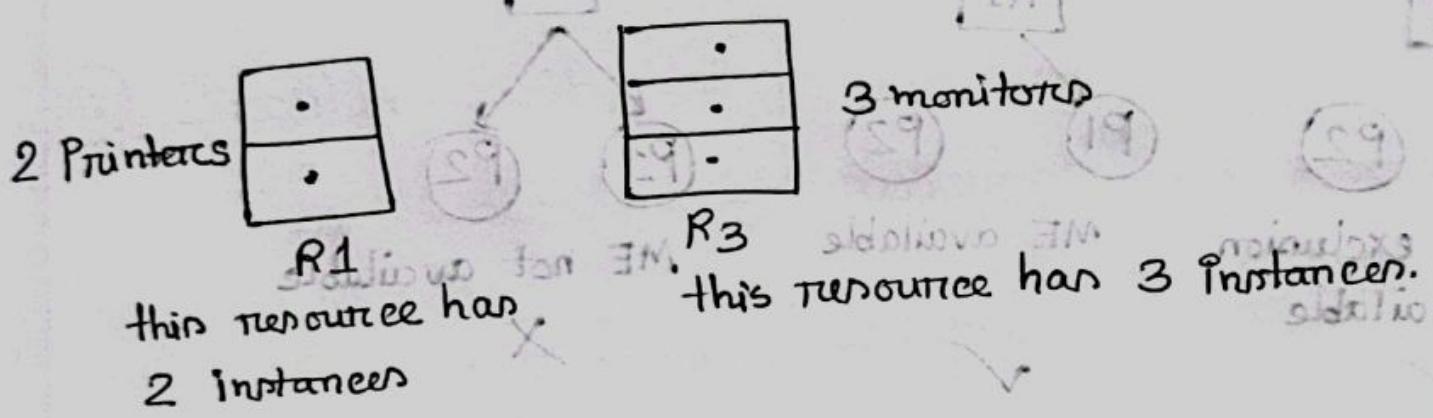
Deadlock

⇒ Deadlock



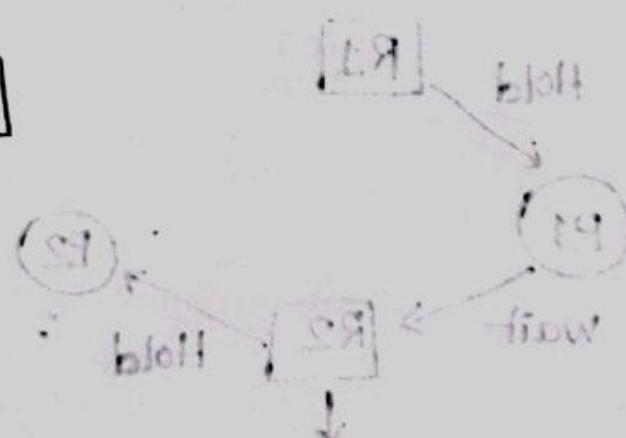
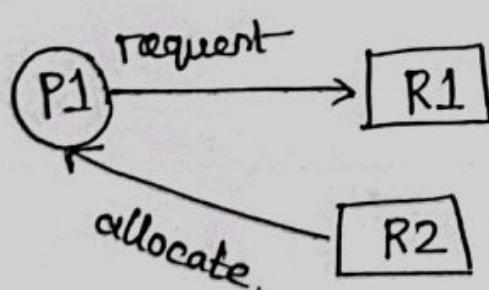
⇒ System model.

Finite resource → CPU cycles, file, I/O devices.



Sequence of process using a resource :

Request → Use → Release

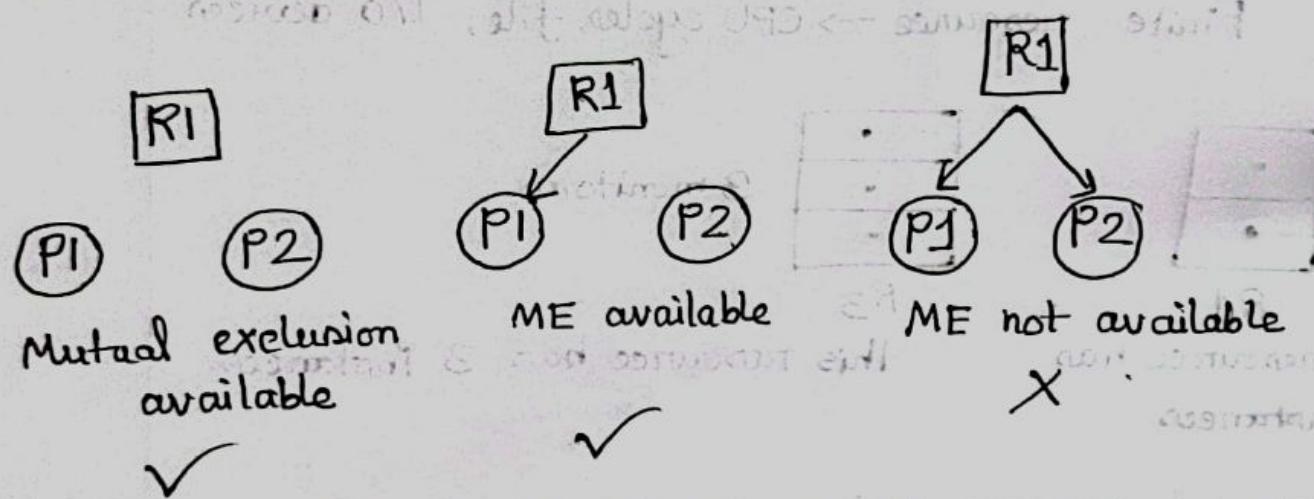


Conditions for Deadlock :

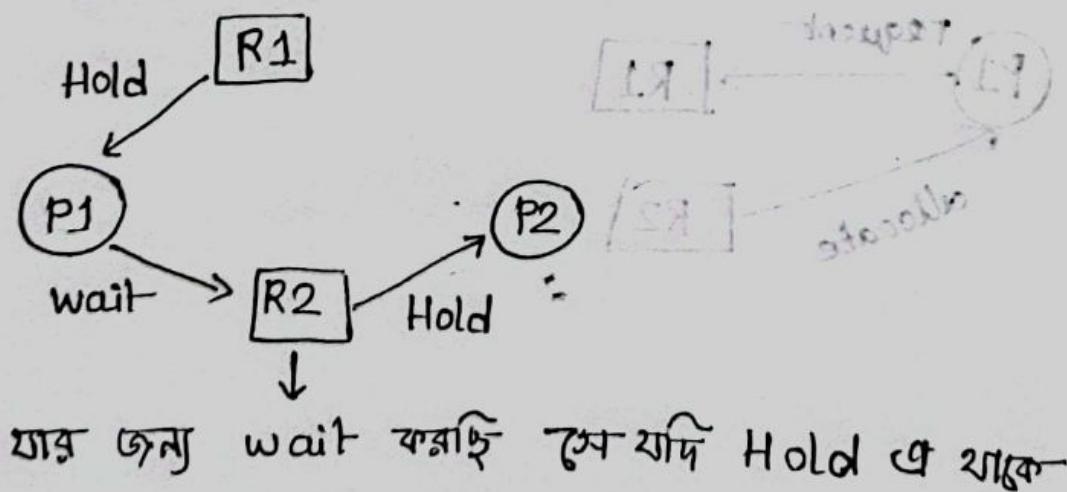
- ① Mutual exclusion.
- ② Hold and wait
- ③ No preemption.
- ④ Circular wait

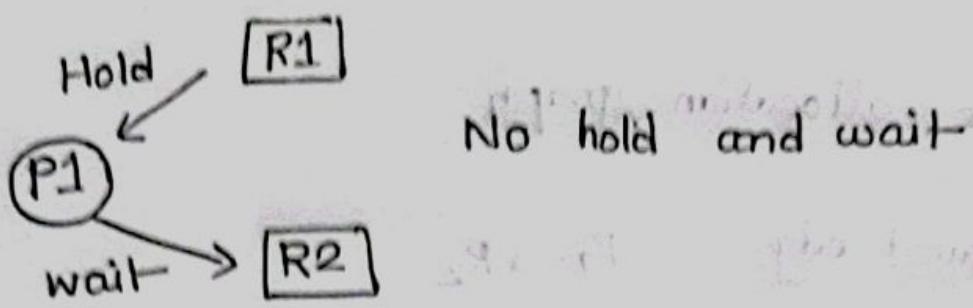
All 4 has to
be present for
a deadlock.

① Mutual exclusion

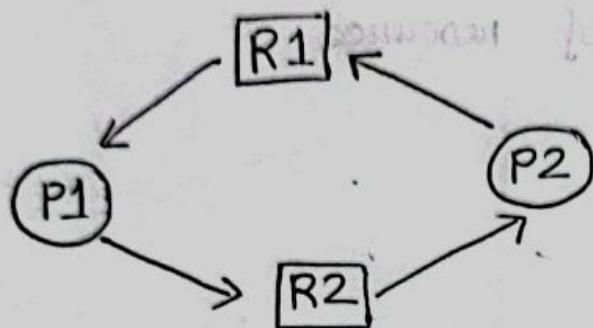


② Hold and wait



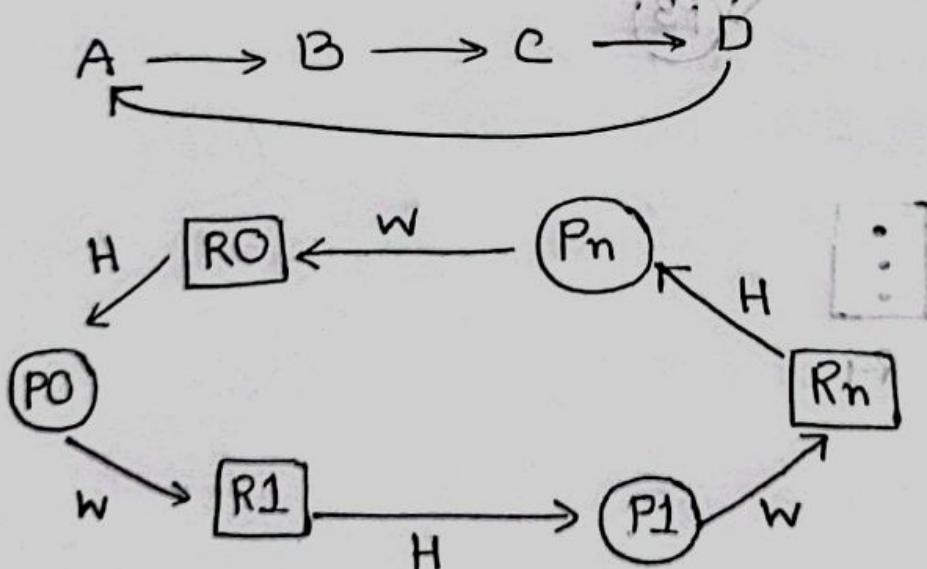


(III) No preemption



(IV) Circular wait

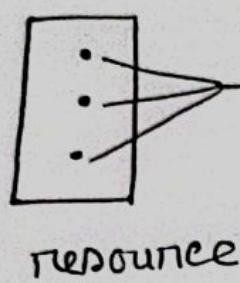
n = number of resources and processes



Resource allocation graph.

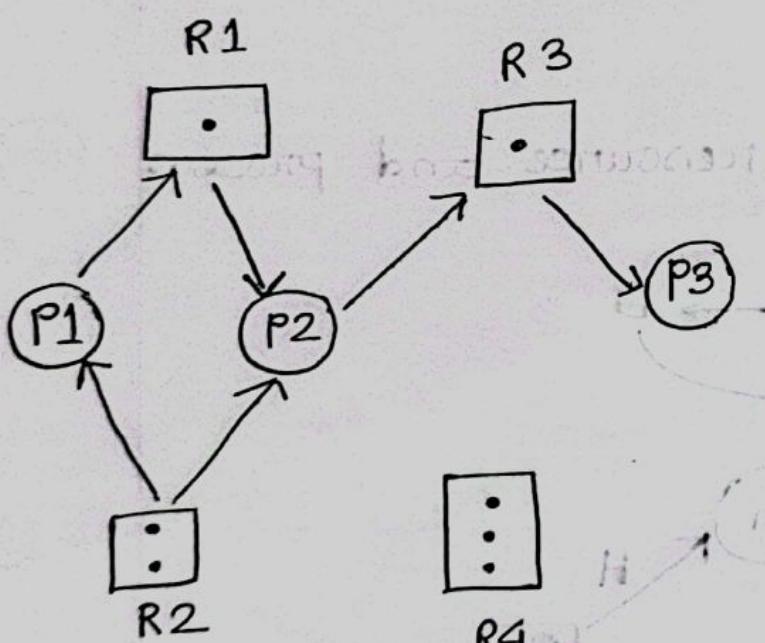
Request edge : $P_1 \rightarrow R_2$

Assignment edge : $R_1 \rightarrow P_2$



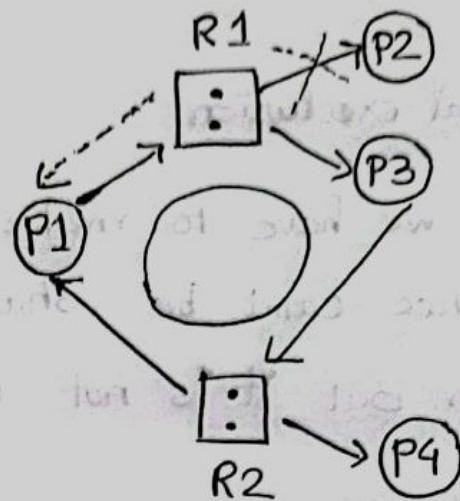
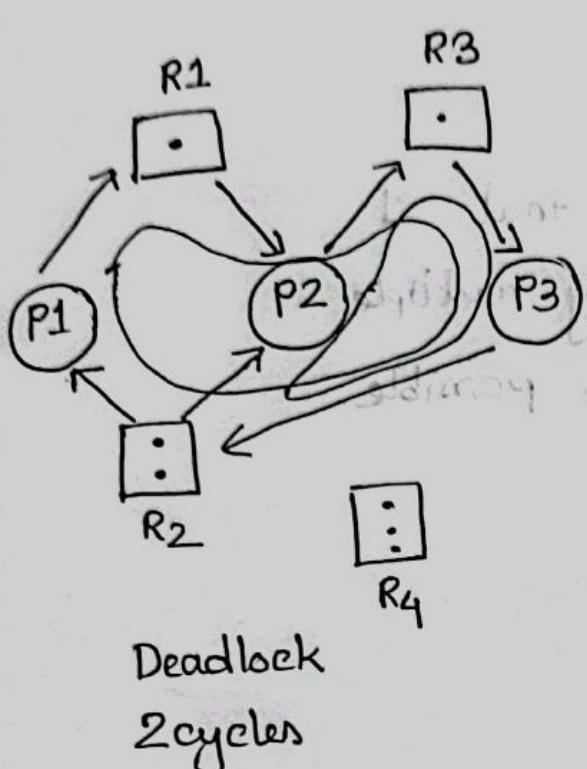
instances of resource

resource

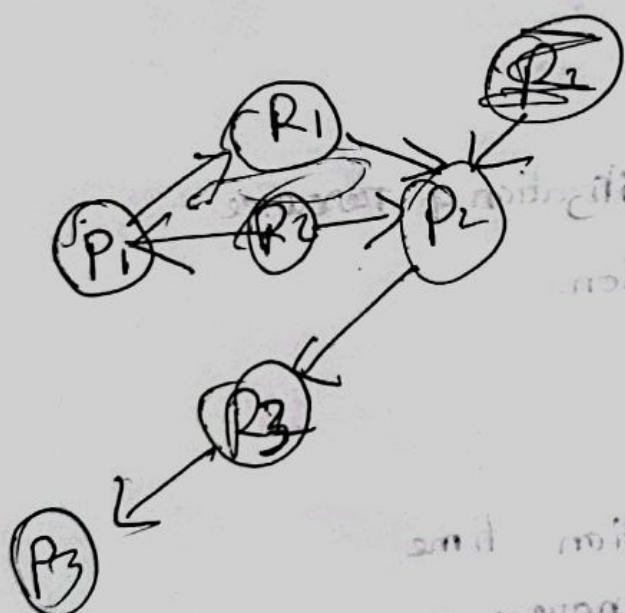


Cycle: Possibility of deadlock

No cycle: No deadlock



Cycle, but no deadlock because P2 process do not request for any resource. So after some time, it will stop using R1 and release it. After that, P1 process will be able to use R1 and break the cycle.



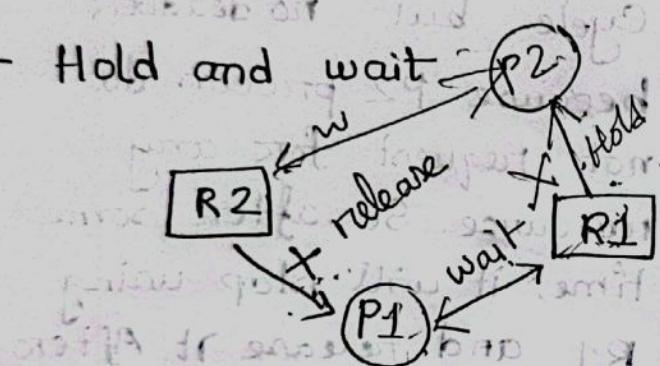
Methods for handling deadlock.

① Prevention

- Mutual exclusion

We have to make sure that 1 resource can't be shared by multiple process. But it is not always possible to do so.

- Hold and wait



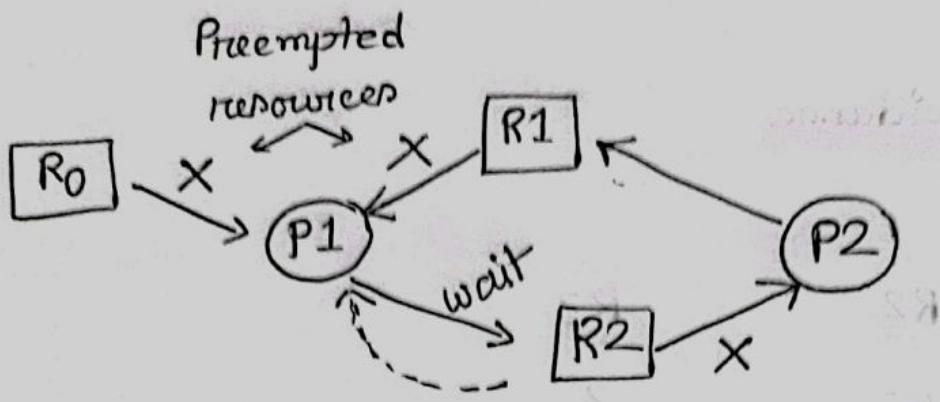
Disadvantage:

- low utilization of resource
- starvation.

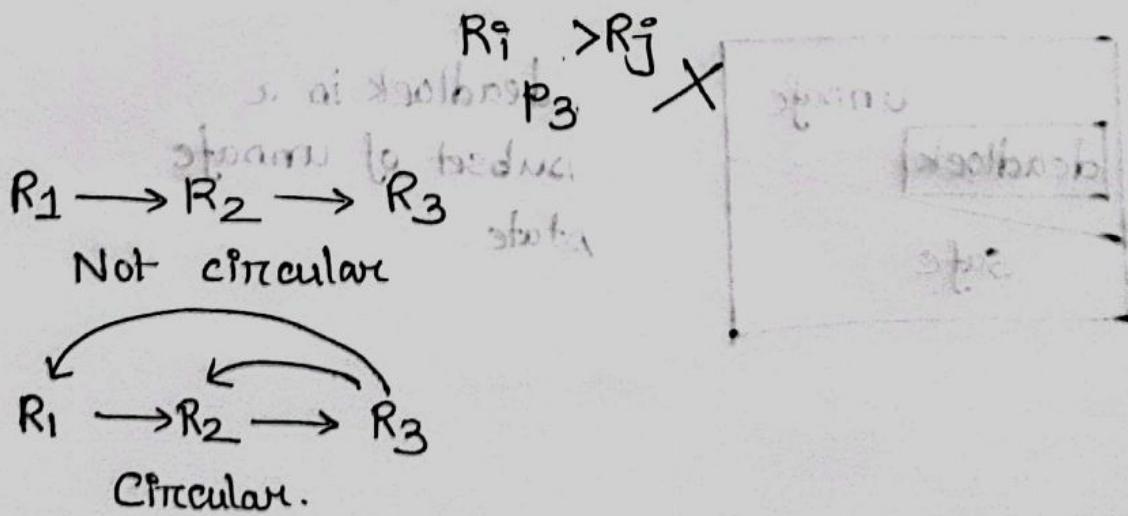
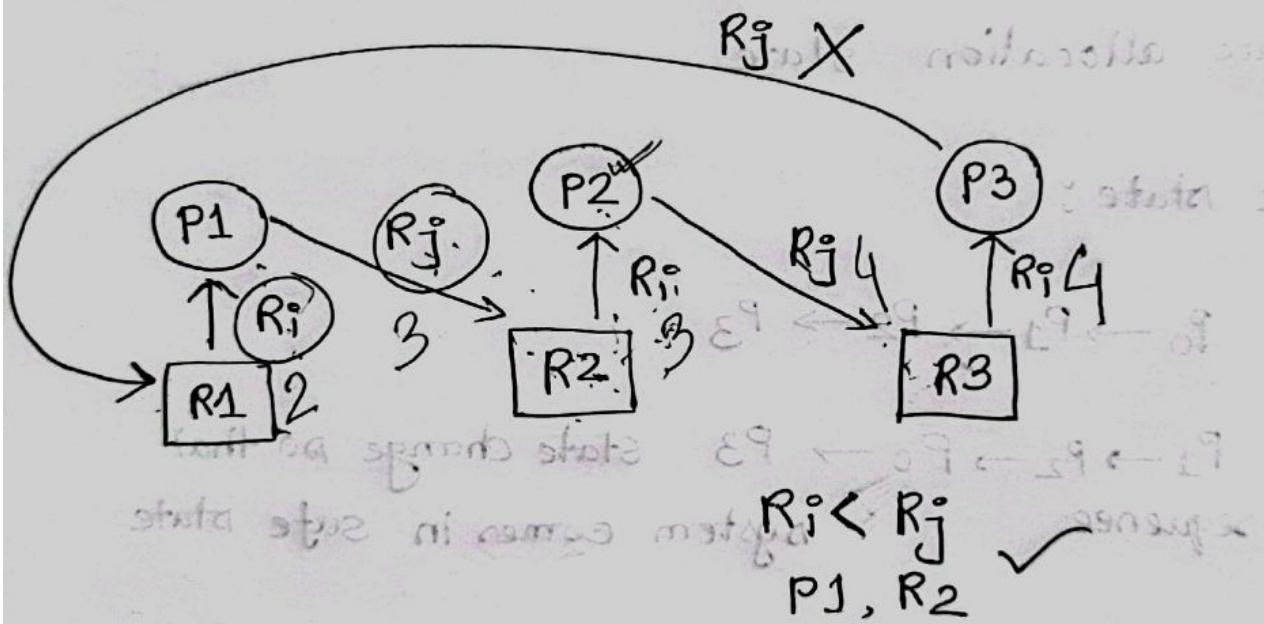
- No preemption

Disadvantage:

- execution time may increase.



- Circular wait
 - Break circle
 - Most efficient



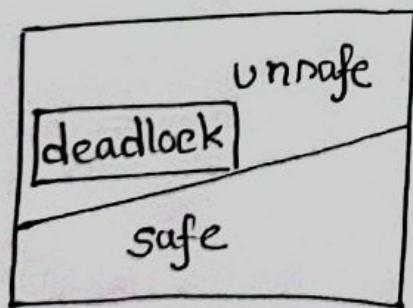
Deadlock avoidance

R1	R2	R3
2	5	3
$P_1 = 1$	2	1
$P_2 = 1$	1	2

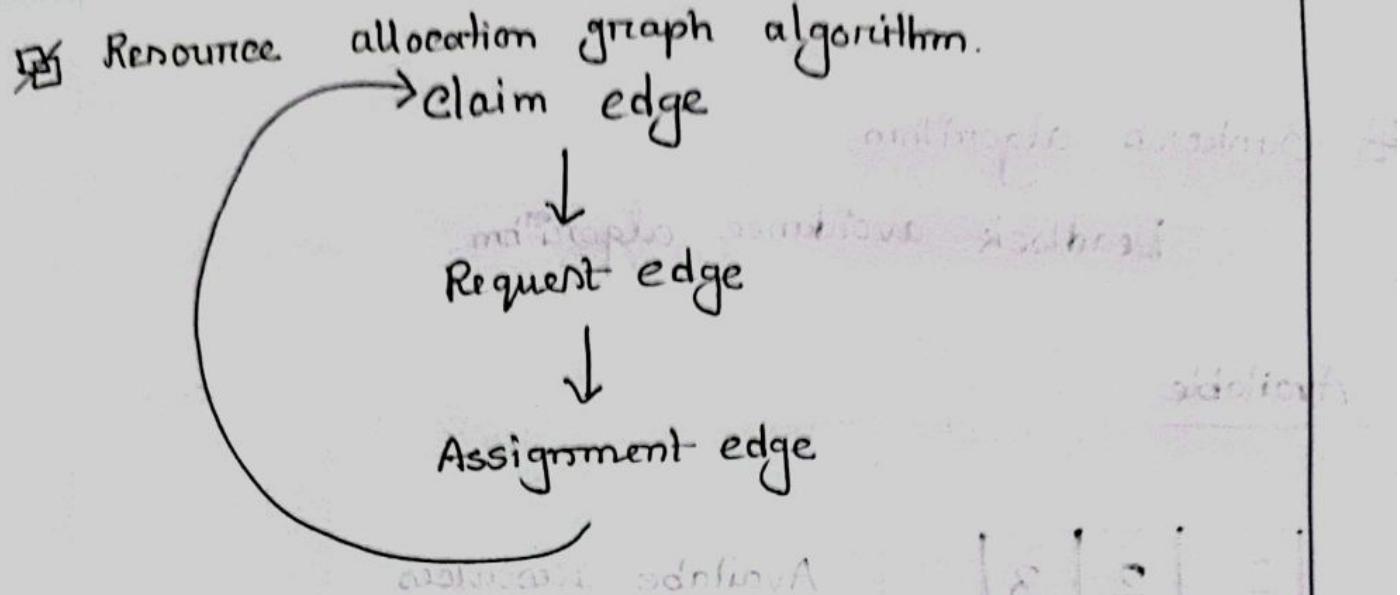
- Resource allocation state

- safe state:

$P_0 \rightarrow P_1 \rightarrow P_2 \rightarrow P_3$ state change so that
safe sequence $P_1 \rightarrow P_2 \rightarrow P_0 \rightarrow P_3$ system comes in safe state



deadlock is a
subset of unsafe
state



claim edge info দিয়ে যায়া ক্ষয়তি পাই
 এখন কোন resource কে কোন process এ
 allocate ক্ষয়তি রঙে হাত cycle create
 না হয়। Thus is deadlock avoidance algo.

0	8	5	12
2	6	3	9
6	2	12	18

deadlock detection algorithm

0	0	1	12
2	8	5	9
6	4	11	18

deadlock detection algorithm

0	3	1	12
0	2	4	9
6	5	11	18

Banker's algorithm

Deadlock avoidance algorithm.

Available

2	2	3
R1	R2	R3

Available Resources

Max

P1	2	3	0
P2	6	5	2
	R1	R2	R3

P1 ক্ষেত্রে ২টি R1,
3টি R2 এবং ০টি R3 আছে।

Allocation

P1	1	0	0
P2	2	3	2
	R1	R2	R3

currently ক্ষেত্রে resource
use হচ্ছে

P1	1	3	0
P2	4	2	0
	R1	R2	R3

বাকি ক্ষেত্রে resource প্রয়োজন

If not enough resource available : deadlock

Ex Example 1

Available

3	3	2
R1	R2	R3

$P_1 \rightarrow P_3 \rightarrow P_4 \rightarrow P_2 \rightarrow P_0$
safe sequence

Max

P_0	7	5	3
P_1	3	2	2
P_2	9	0	2
P_3	2	2	2
P_4	4	3	3
	R1	R2	R3

Allocation

P_0	0	1	0
P_1	2	0	0
P_2	3	0	2
P_3	2	1	1
P_4	0	0	2
	R1	R2	R3

Need

P_0	7	4	3
P_1	1	2	2
P_2	6	0	0
P_3	0	1	1
P_4	4	3	1
	R1	R2	R3

x wait ✓

✓

x wait ✓

✓

✓

Work : (Copy of available)

3	3	2

Finish :

F	F	F	F	F
P_0	P_1	P_2	P_3	P_4

F	T	F	F	F
P ₀	P ₁	P ₂	P ₃	P ₄

3+2=5	3+0=3	2+0=2
-------	-------	-------

F	T	F	T	F
---	---	---	---	---

5+2=7	3+1=4	2+1=3
-------	-------	-------

F	T	F	T	T
---	---	---	---	---

7+0=7	4+0=4	3+2=5
-------	-------	-------

T	T	F	T	T
---	---	---	---	---

7+0=7	4+1=5	5+0=5
-------	-------	-------

T	T	T	T	T
---	---	---	---	---

7+3=10	5+0=5	5+2=7
--------	-------	-------

Amount of total number of instances
of resources

No deadlock

Example 2

	Allocation			Max			Available			Need			
	A	B	C	A	B	C	A	B	C	A	B	C	
P0	1	0	1	2	1	1	2	1	1	1	1	0	✓
P1	2	1	2	5	4	4				3	3	2	X → deadlock
P2	3	0	0	3	1	1				0	1	1	✓
P3	1	0	1	1	1	1				0	1	0	✓

Work:

2	1	1
---	---	---

2+1	1+0	1+1
-----	-----	-----

3+3	1+0	2+0
-----	-----	-----

6+1	1+0	2+1
-----	-----	-----

7	1	3
---	---	---

Finish:

F	F	F	F
P0	P1	P2	P3

T	F	F	F
P0	P1	P2	P3

T	F	T	F
P0	P1	P2	P3

T	F	T	T
P0	P1	P2	P3

P0 → P2 → P3

Avoid P1 because it is deadlock.

Resource-request algorithm.

Process sends new resource request

→ Request \leq Need

→ Request \leq Available

→ Available = Available - Request

→ Allocation = Allocation + Request

→ Need = Need - Request

→ Run Banker's algo

→ if we find safe sequence \rightarrow accept request

89 89 19 09

1	1	7	7
---	---	---	---

89 89 19 09

7	T	7	T
---	---	---	---

89 89 19 09

T	1	1	T
---	---	---	---

89 89 19 09

0+P	0+I	0+E
-----	-----	-----

0+S	0+H	1+E
-----	-----	-----

S	L	F
---	---	---

89 \leftarrow 89 \leftarrow 89

deadlock if it happened no more

Q) Example 3

Suppose in example 1, P1 requests more $(1, 0, 2)$

- request \leq Need $\rightarrow (1, 0, 2) \leq (1, 2, 2)$ True
- request \leq Available $\rightarrow (1, 0, 2) \leq (3, 3, 2)$ True
- If both true : Available : $(3, 3, 2) - (1, 0, 2) = (2, 3, 0)$

$$\text{Allocation} : (2, 0, 0) + (1, 0, 2)$$

$$= (3, 0, 2)$$

$$\text{Need} : (1, 2, 2) - (1, 0, 2)$$

$$= (0, 2, 0)$$

Available	Allocation			Max	Need		
2 3 0	P0	0	1	0	7 5 3	7 4 3	x
	P1	3	0	2	3 2 2	0 2 0	✓
	P2	3	0	2	9 0 2	6 0 0	x
	P3	2	1	1	2 2 2	0 1 1	✓
	P4	0	0	2	4 3 3	4 3 1	✓

work :

2	3	0
---	---	---

2+3	0+3	0+2
-----	-----	-----

5+2	3+1	2+1
-----	-----	-----

7+0	4+0	3+2
-----	-----	-----

7+0	4+1	5+0
-----	-----	-----

7+3	5+0	5+2
-----	-----	-----

Finish:

F	F	F	F	F
P0	P1	P2	P3	P4

F	T	F	F	F
---	---	---	---	---

F	T	F	T	F
---	---	---	---	---

F	T	F	T	T
---	---	---	---	---

T	T	F	T	T
---	---	---	---	---

T	T	T	T	T
---	---	---	---	---

10	5	7
----	---	---

P1
 ↓
 P3
 ↓
 P4
 ↓
 P0
 ↓
 P2
 Safe
 Sequence

→ If P4 requests for $(3, 3, 0)$ in example 1

Request \leq need $\rightarrow (3, 3, 0) \leq (4, 3, 1) \rightarrow$ True

Request \leq available $\rightarrow (3, 3, 0) \leq (3, 3, 2) \rightarrow$ True

$$\therefore \text{Available: } (3, 3, 2) - (3, 3, 0) = (0, 0, 2)$$

$$\text{Allocation: } (0, 0, 2) + (3, 3, 0) = (3, 3, 2)$$

$$\text{Need: } (4, 3, 1) - (3, 3, 0) = (1, 0, 1)$$

- Available:

0	0	2
---	---	---

Max

P0	7	5	3
P1	3	2	2
P2	9	0	2
P3	2	2	2
P4	4	3	3

Allocation

0	1	0
2	0	0
3	0	2
2	1	1
3	3	2

Need

7	4	3
1	2	2
6	0	0
0	1	1
1	0	1

WORK

0	0	2
---	---	---

Finish

F	F	F	F	F
---	---	---	---	---

Can't run. Banker's algo.

→ If PO requests for $(0, 2, 0)$
 request \leq need $\rightarrow (0, 2, 0) \leq (7, 4, 3) \rightarrow \text{true}$
 request \leq available $\rightarrow (0, 2, 0) \leq (3, 3, 2) \rightarrow \text{true}$
 $\therefore \text{Available: } (3, 3, 2) - (0, 2, 0) = (3, 1, 2)$
 $\text{Allocation: } (0, 1, 0) + (0, 2, 0) = (0, 3, 0)$
 $\text{Need: } (7, 4, 3) - (0, 2, 0) = (7, 2, 3)$

	Max			Allocation			Need				
	P0	P1	P2	P3	P4	P0	P1	P2	P3	P4	
P0	7	5	3	0	3	0	7	2	3	X	✓
P1	3	2	2	2	0	0	1	2	2	X	-
P2	9	0	2	3	0	2	6	0	0	X	-
P3	2	2	2	2	1	1	0	1	1	✓	-
P4	4	3	3	0	0	2	4	3	1	X	✓

$$\text{Available: } (3, 1, 2)$$

work:

3	1	2
---	---	---

3+2	1+1	2+1
-----	-----	-----

5+2	2+0	3+0
-----	-----	-----

7+3	2+0	3+2
-----	-----	-----

10+0	2+3	5+0
------	-----	-----

10+0	5+0	5+2
------	-----	-----

10	5	7
----	---	---

Finish:

F	F	F	F	F
P0	P1	P2	P3	P4

F	F	F	T	F
---	---	---	---	---

F	T	F	T	F
---	---	---	---	---

F	T	T	T	F
---	---	---	---	---

T	T	T	T	F
---	---	---	---	---

T	T	T	T	T
---	---	---	---	---

P3
↓
P1
↓
P2
↓
PO
↓
P4

Thread

DEF Basic unit of CPU utilization

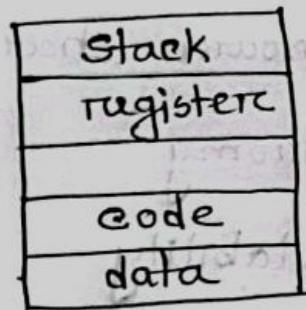
- Thread id
- program counter
- register set
- Stack

DEF A process can have single/multiple threads

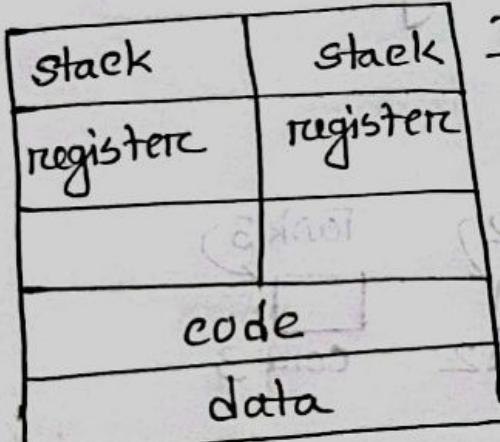
- code section
- data section
- OS resources.



copy creation
(child)



if 1 process
goes to wait
state, other
process follows it.



Independent processes

Shared resources

create own thread

Shared items: code, data, files

Individual items: registers, stack.

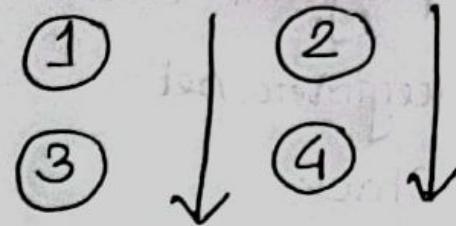
Q Suppose a process has to do 4 tasks:

Single thread:

- (1)
- (2)
- (3)
- (4)



Multi-threaded:

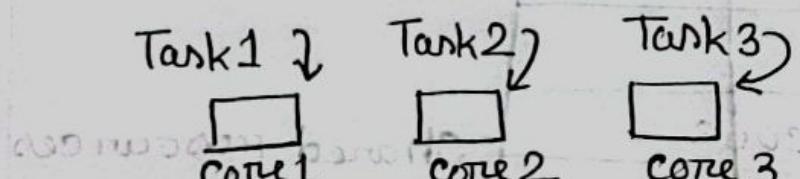


Q Benefits

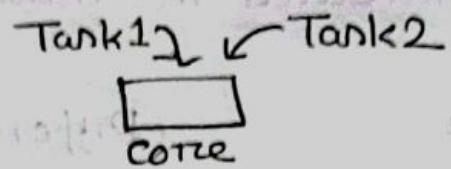
- responsiveness
- resource sharing
- economy
- scalability

Q Multicore programming

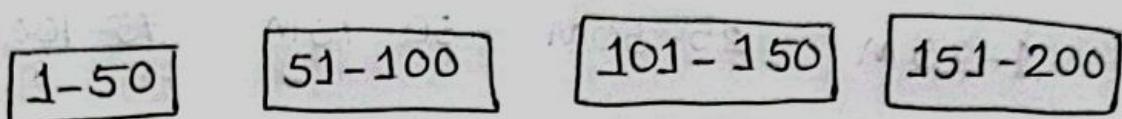
- parallelism



- concurrency (scheduler provides concurrency)

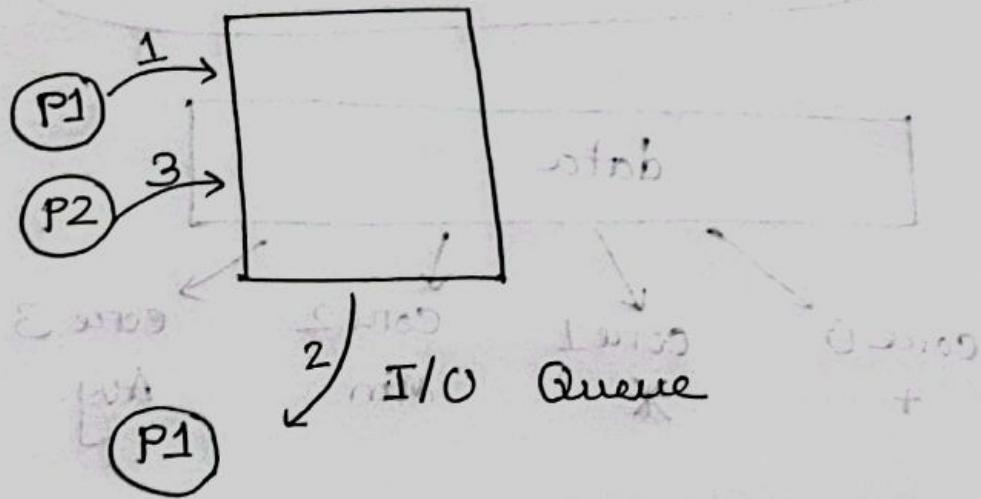


→ parallel tank : Add 1-200



Thread context switch is not expensive

child process creation doesn't cost load.

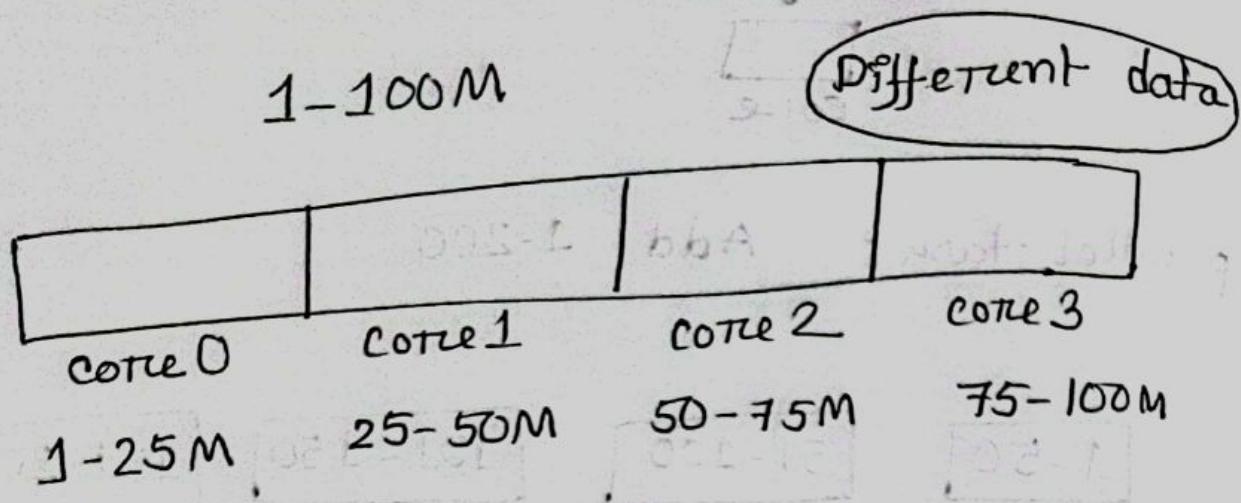


Single core or threading possible -

→ In slide, core1 has 2 threads T1 and T3
core2 " 2 " T2 " T4

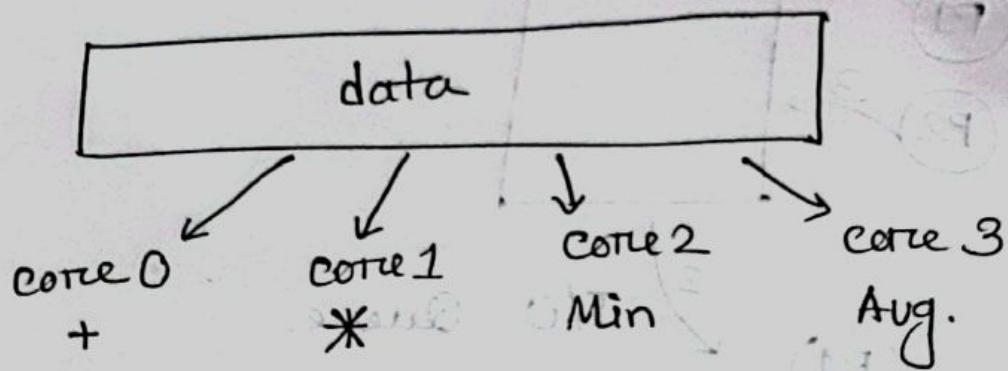
>Data Parallelism

1 operation distributed in multiple cores.



Task parallelism

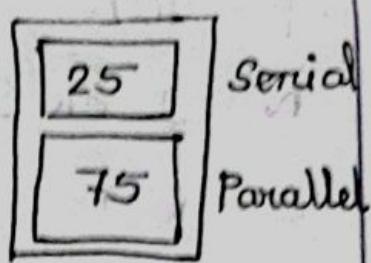
Same data, different operations



Amdahl's Law.

s → serial portion

N → Number of processing cores.



if $N = 1$, $s = 0.25$

$$\text{speedup} \leq \frac{1}{s + \frac{(1-s)}{N}}$$

$$= \frac{1}{0.25 + \frac{1-0.25}{1}} = 1$$

if $N = 2$,

$$\text{speedup} \leq \frac{1}{0.25 + \frac{(1-0.25)}{2}}$$

$$= 1.6$$

speedup of 1.6 times

if N is α , $\frac{1-s}{N}$ becomes 0. So speed depends only on s . Speed is inversely proportional to s .

$$\rightarrow P = 40\%$$

$$N = ? \text{ or } 8$$

$$S = 60\%$$

$$\text{If } N = 2; \quad \frac{1}{0.6 + \frac{1-0.6}{2}} = 1.25$$

$$\text{If } N = 8; \quad \frac{1}{0.6 + \frac{1-0.6}{8}} = 1.5465$$

$$\frac{1.5465}{1.25} = 1.23 \text{ times increase}$$

Serial + parallel $\rightarrow N$

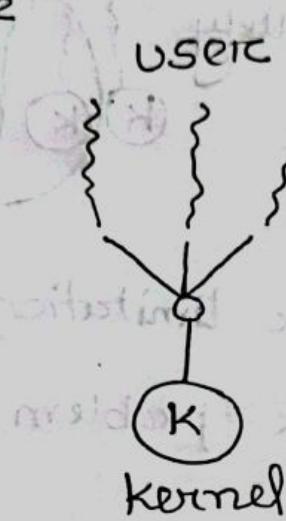
④ Multithreading model

- user thread → function
 - kernel thread → system call
- } thread library;

4 models :

① Many to one

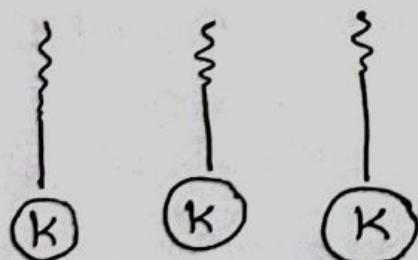
- If one user invokes block, whole system stops working



- kernel executes one task at a time. So no parallelism possible

② One to One

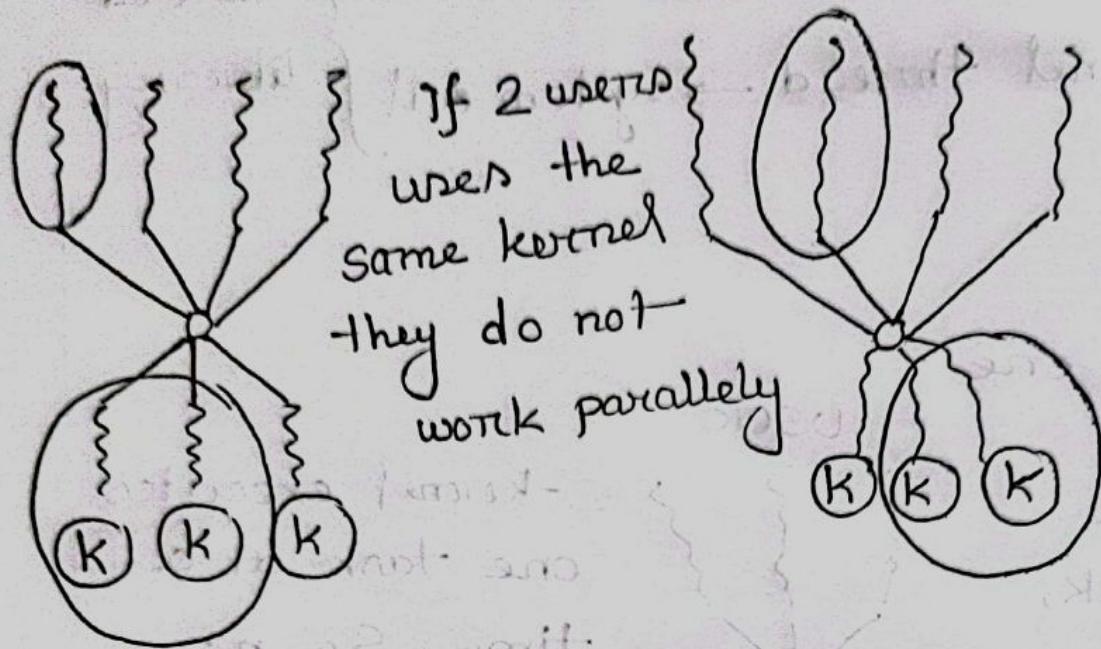
windows, Linux



+ parallelism

- we can't create infinite user because we have limited kernel.
- overhead.

III Many to Many.



+ Solves user limitation

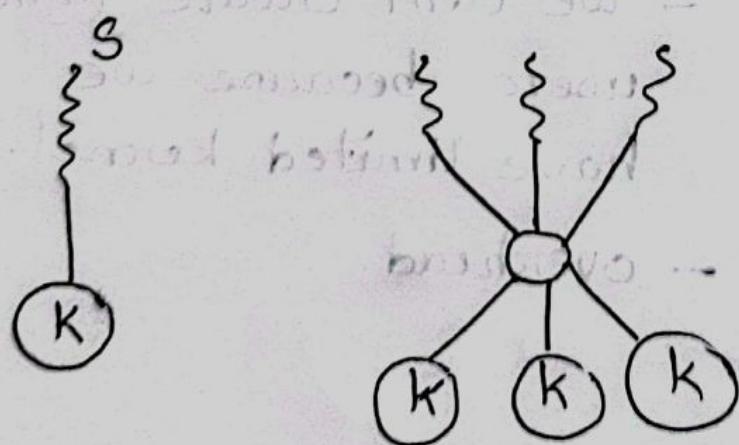
+ Solves block problem

+ parallel

- slower

IV Two-level model

mix of II and III



Thread Library
API → creates bridge between services,
provides API for creating / managing

Java threads
managed by JVM
- extending thread class
- implementing the runnable interface
(standard)

Threading Issues

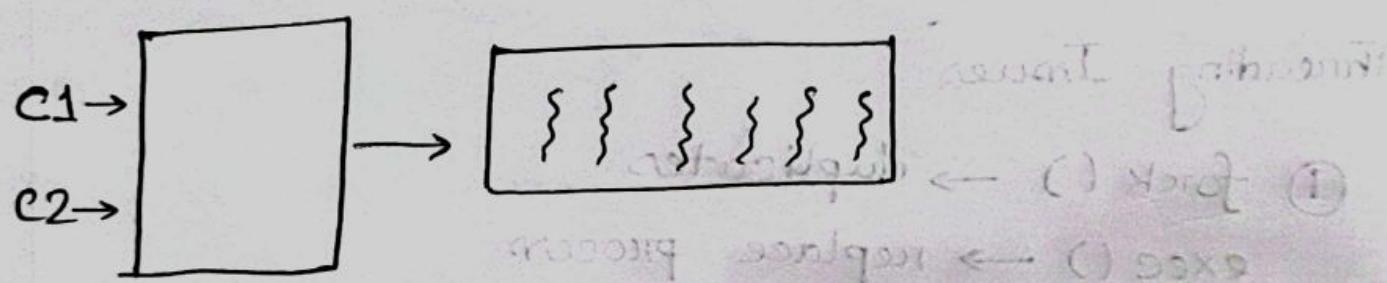
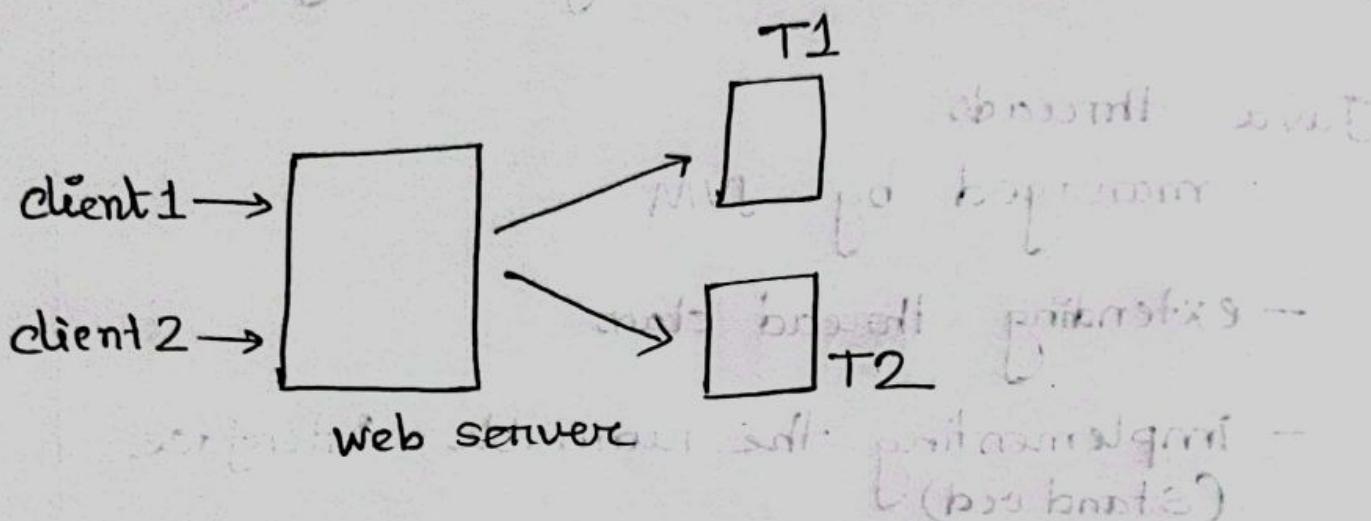
I) fork () → duplicates
exec () → replace process

II) Thread cancel → terminate thread
Asynchronous : call ~~प्राप्ति करने का लिए~~ cancel
Deferred : wait till task is finished

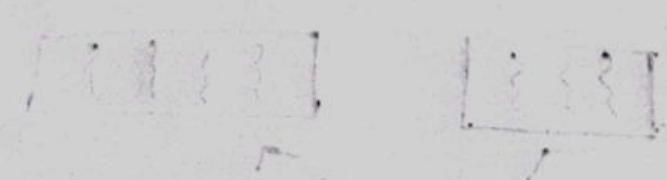
III) Single Handling :
Signal



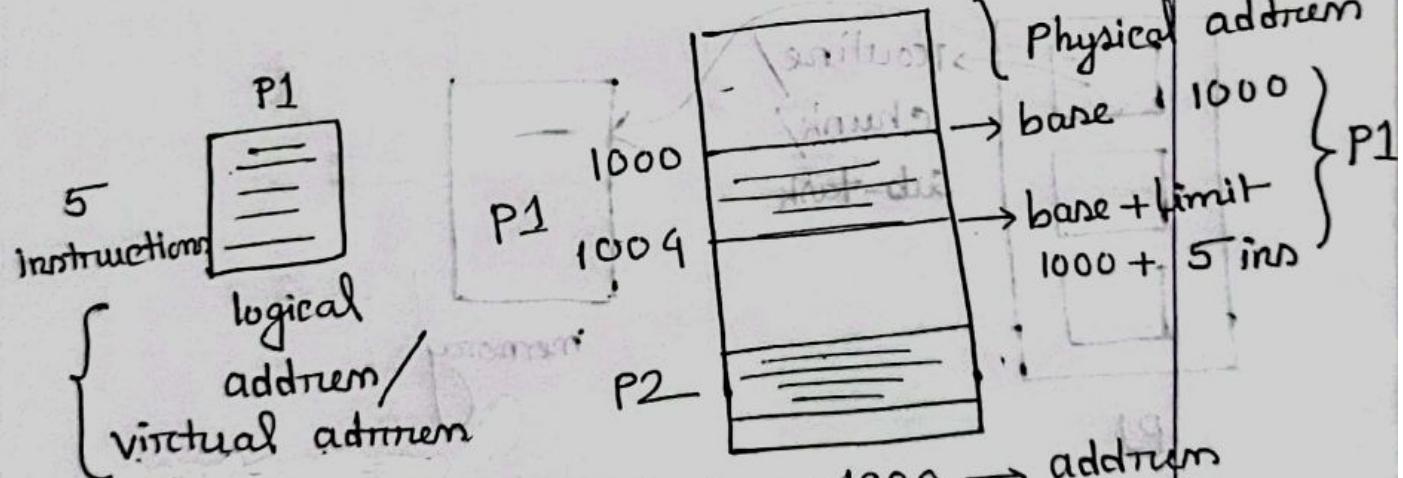
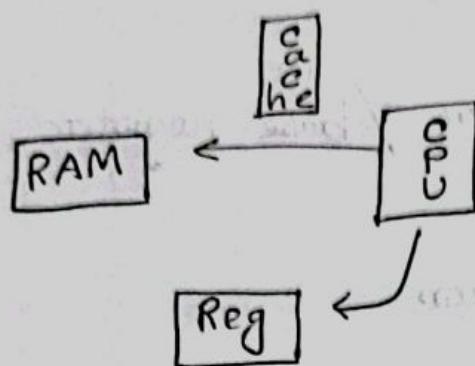
IV Thread pool → create a number of threads at the process start-up



V Thread specific data → might need it's own copy of certain data.

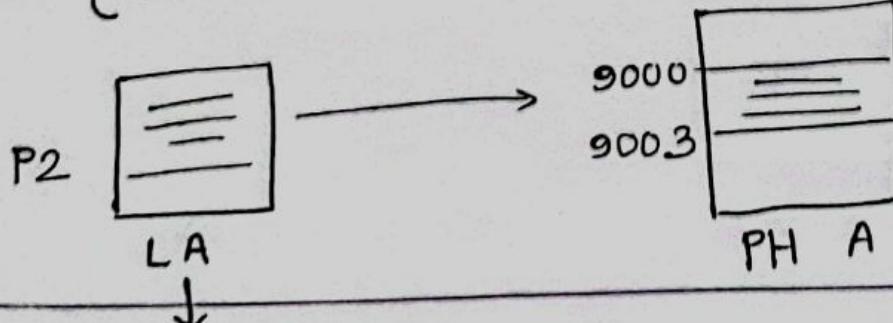


Main Memory



only OS can access this.

Base → address start → 1000 → address
limit → 5 → integer



human readable
error detection.

Memory management Unit

Relocation registers / base registers

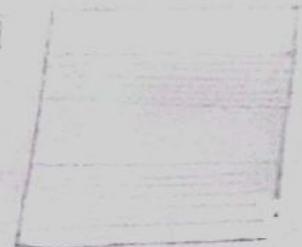
+

logical address

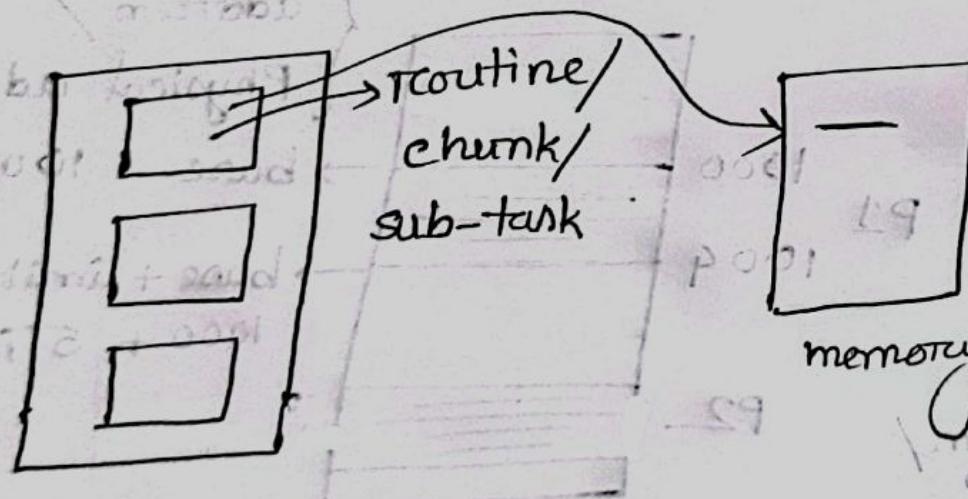


physical address

1000

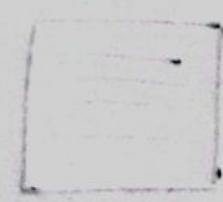
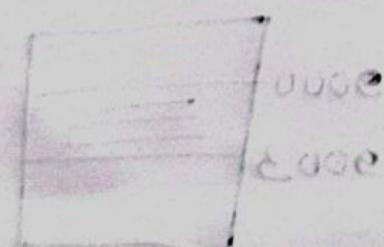


Dynamic loading

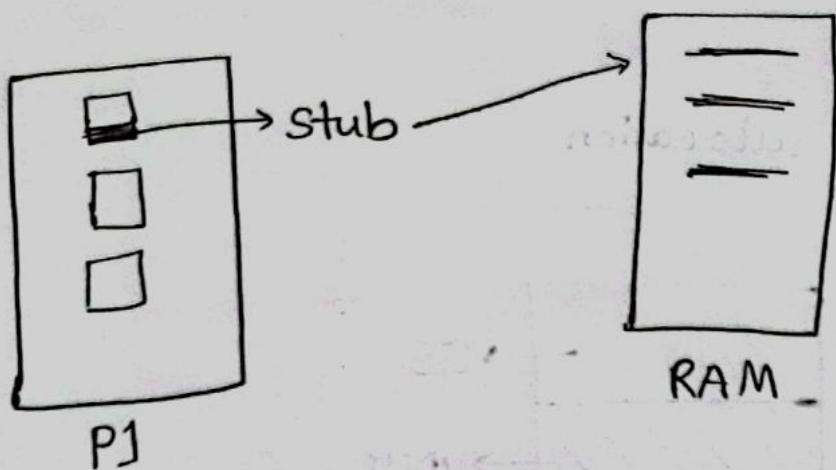


P1

signature - 8 - limit



Dynamic Linking.

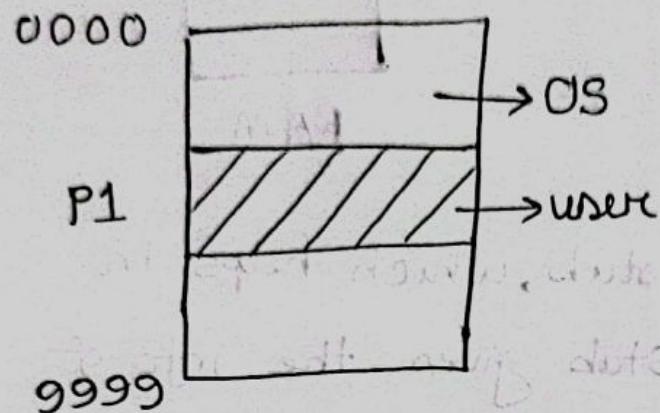


each routine has stub, which helps in dynamic linking. Stub gives the info of which function will be used now.

```
if (True){  
    f1();  
}  
else {  
    f2();  
}
```

```
void function1();
```

Contiguous allocation



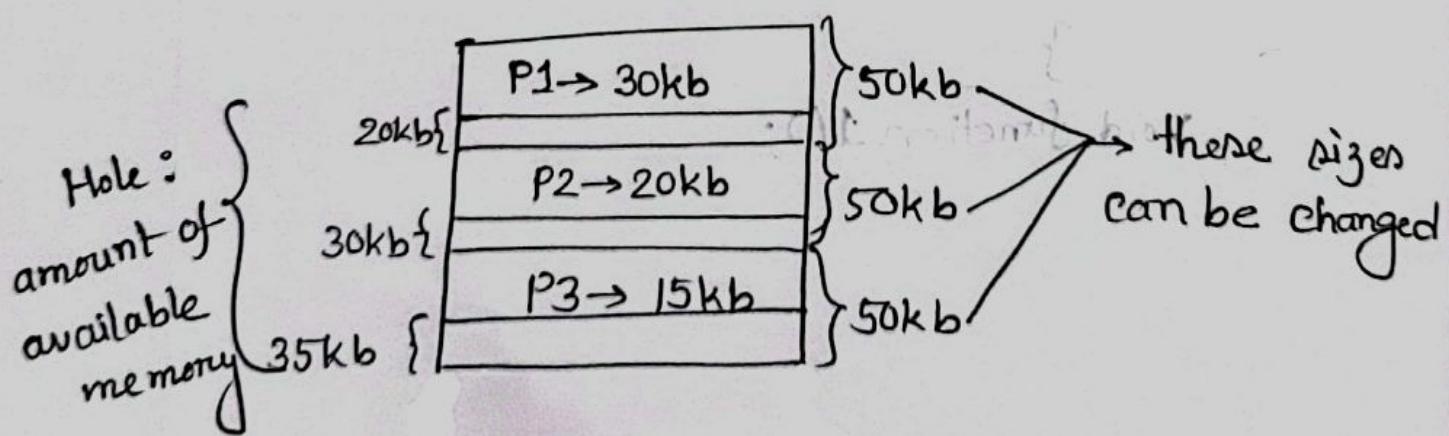
P1 has to be continuous, no break

Logical / Local address

easier to find address because of C.A.

Multiple

Mutual partition allocation



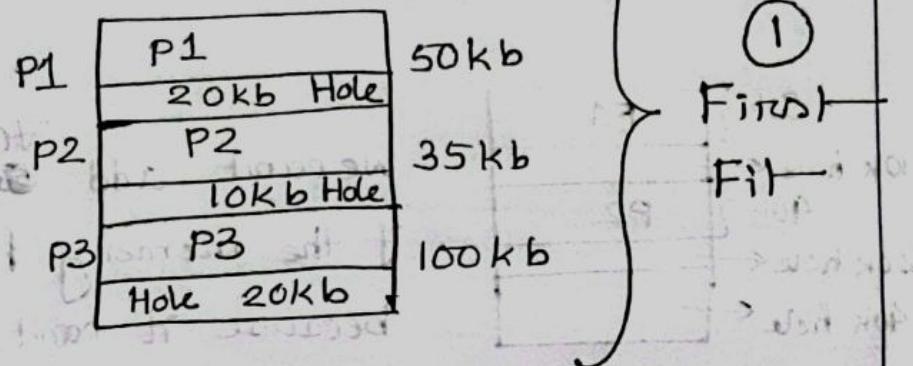
P4 → 50kb but CA is not possible.
Solution → variable partition

Dynamic storage allocation

P1 → 30kb

P2 → 25kb

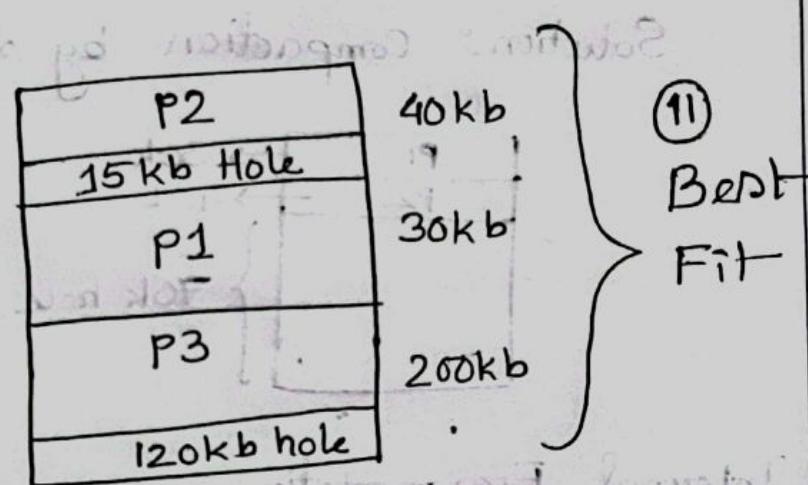
P3 → 80kb



P1 → 30kb

P2 → 25kb

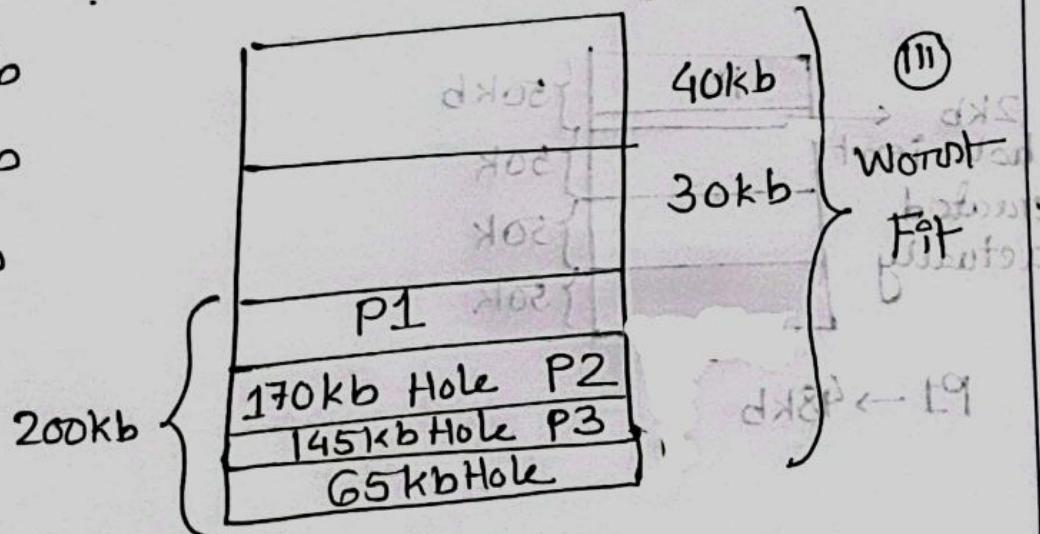
P3 → 80kb



P1 → 30kb

P2 → 25kb

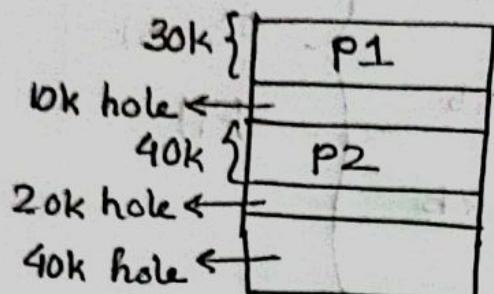
P3 → 80kb



Problem : Fragmentation

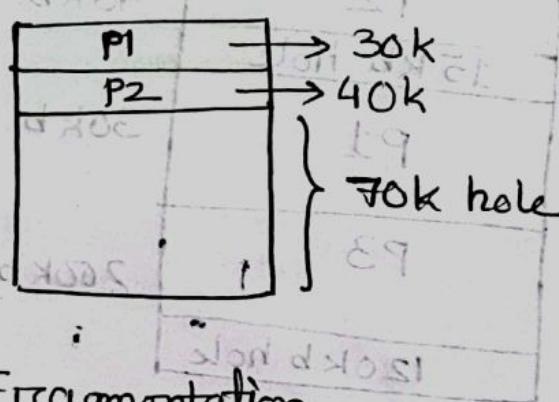
Q1 Fragmentation : 2 types

① External fragmentation

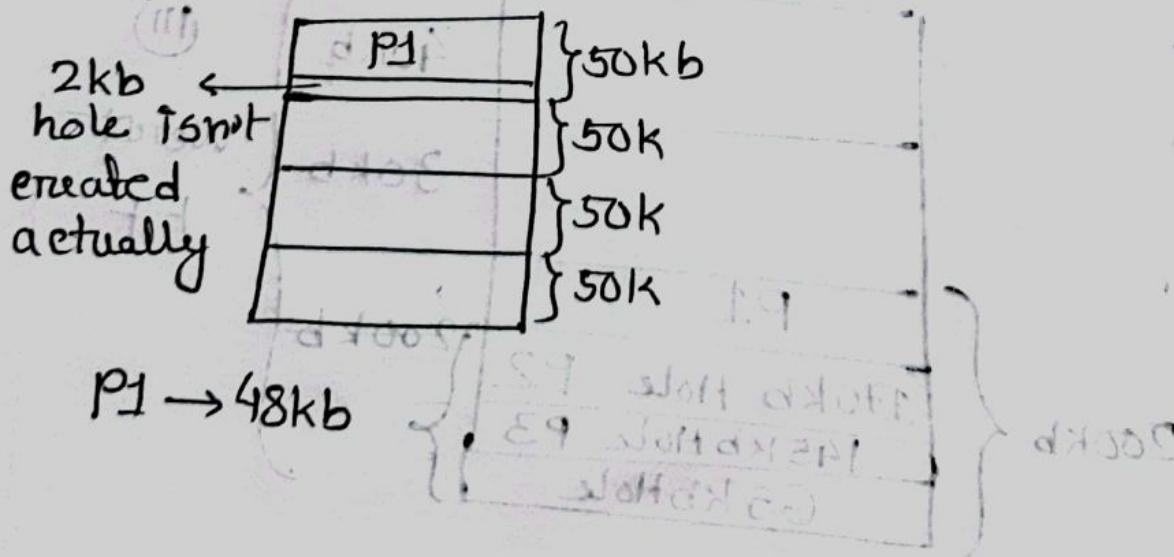


We can't add kb even if the memory have space because it can't be C.A.

Solution: Compaction by shuffle



② Internal Fragmentation

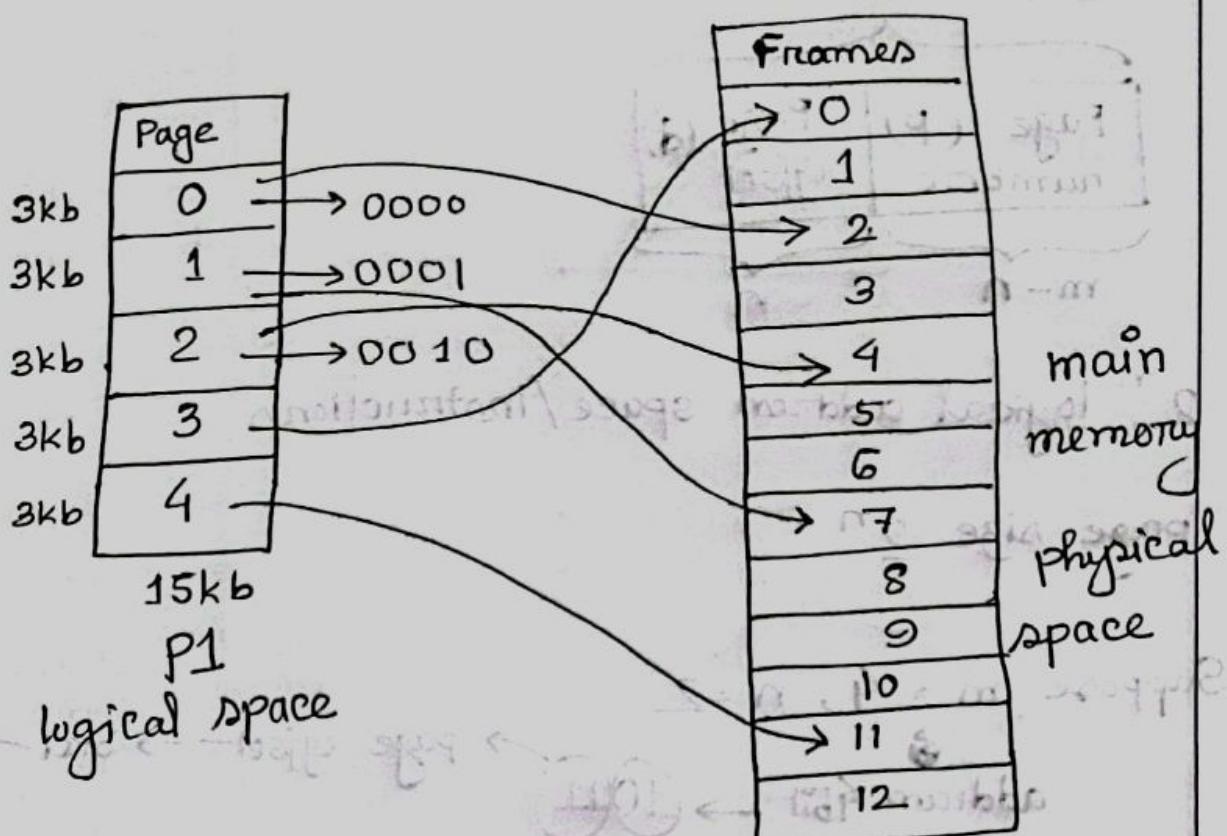


$$P1 \rightarrow 48\text{kb}$$

internal fragmentation ? malloc?

Paging → non-contiguous technique → tough to locate

available frames
not used



page table

P	F
0	2
1	7
2	4
3	0
4	11

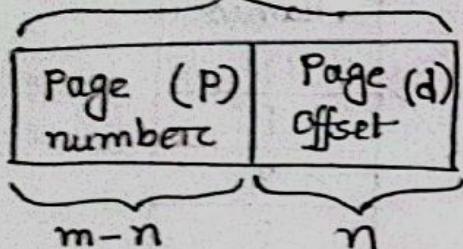
Free frames

1
3
5
6
8
9
10
12

Solves external fr
but there might be internal fr

Address translation scheme

Logical address:



2^m logical address space/instructions

page size 2^n

Suppose $m = 4$, $n = 2$

address 4bit → 1011 → page offset → 3
page number → 2 no এর ঘোষণা
 $2^4 = 16$ address

page size $2^2 = 4$ pages [যেহেতু ডায়া 2টিক্স]

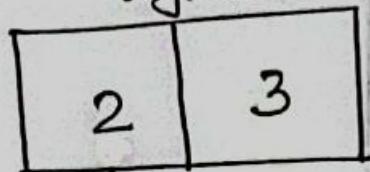
4 ঘৰ মত পন্থ লভন address

0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
1																

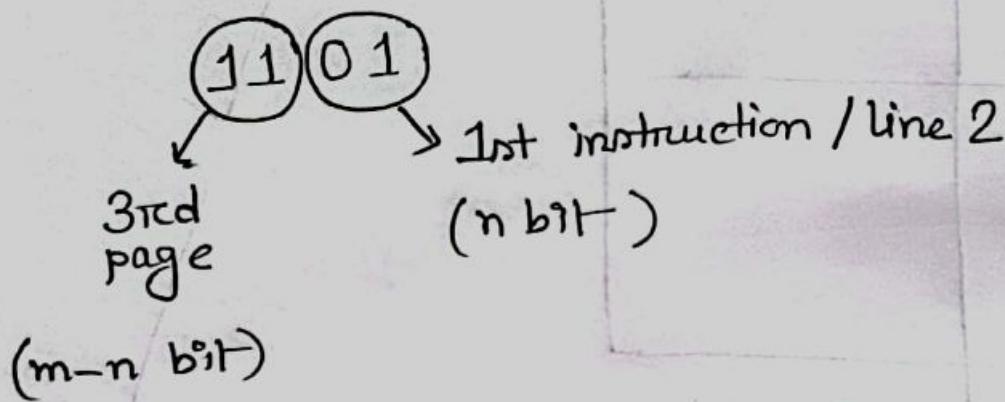
physical address.

Suppose we want to find 3rd instruction of page 2

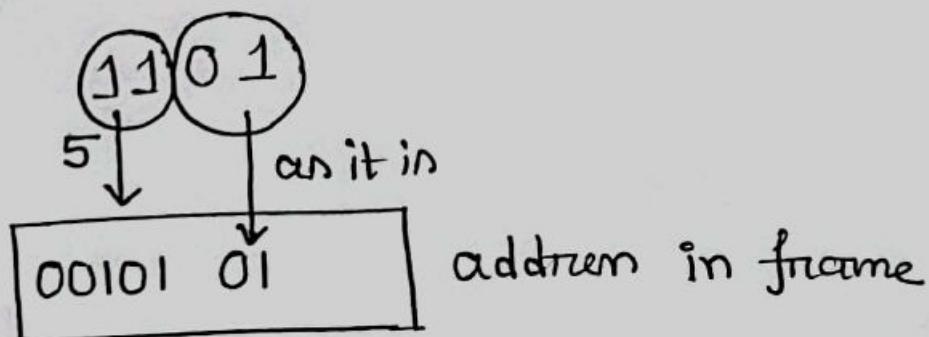
logical:



where is 1101?



Suppose 1101 is in frame 5 [using page table]



Paging Hardware

physical address

frame number	offset (d)
--------------	------------

find from page table

32 byte memory $\rightarrow 2^5$
 $\therefore m = 5$

4 byte page size $\rightarrow n = 2 ; 2^2$

— — — — —
page # / offset

frame #

$2^3 = 8$ pages possible

Pages

0	a
1	b
2	c
3	d
4	e
5	f
6	g
7	h
8	i
9	j
10	k
11	l
12	m
13	n
14	o
15	p

logical

Page table

0	5
1	6
2	1
3	2

frames

0		
4	i j k l	0
8	m n o p	1
12		2
16		3
20	a b c d	4
24	e f g h	5
28		6
		7

Physical

size of page

page size \rightarrow 2048 bytes

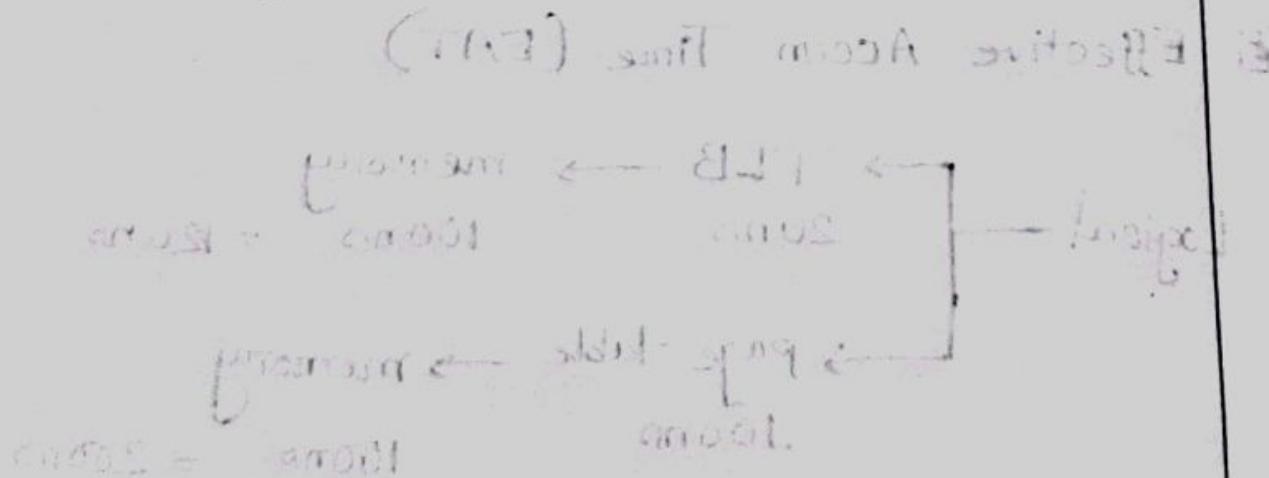
process size \rightarrow 72766 bytes

$$\frac{72766}{2048} = 35 + 1 \text{ new frame}$$

35 pages + 1086 bytes

Internal fragmentation : $2048 - 1086 = 962$ bytes empty

If we reduce page size, we can reduce this waste but then page table size would increase, which also has to be stored in main memory. So we can't reduce page size as we want.



$$\{(4096 \times 5.0) + (1024 \times 0.0)\} \times 35$$

↪ Free frame

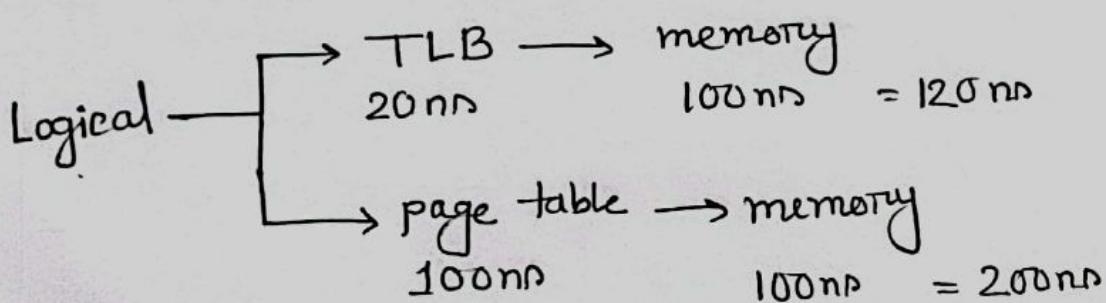
↪ Implementation of page table

solve repetitive search by cache memory
(associative memory / translation look-aside
buffers (TLBs))

↪ Associative memory → do not need to go to
page table.

↪ TLB → buffer.
Data থাকলে → TLB hit
না থাকলে → TLB miss

↪ Effective Access Time (EAT)



$$\text{EAT} : \{(0.80 \times 120) + (0.2 \times 200)\}$$
$$= 136 \text{ ns}$$

$\alpha \rightarrow$ Hit ratio, $\epsilon \rightarrow$ cache access.

shared pages

a
b
c
d

a
b
c
e

a
b
c
f

Shared page slide example:

9 common page → 3 frame
memory optimized

Virtual Memory

Q If virtual memory: process exceeds main memory, computer runs out of physical memory and writes its requirements to the hard disc in a swap file or 'VM'.

Q Demand paging

paging system with swapping

page table with valid-invalid bit
secondary memory.

Q Page fault

trap means the OS failed to bring the desired page into memory.

Access to a page marked invalid causes page fault. Trap → set → 0

{ valid → loaded in memory frame
invalid → not in logical address space of process / valid but currently on disk and hasn't been loaded.

* How to solve page fault

Page replacement Algorithm

① FIFO

time	1	2	3	4	5	6	7	8	9	10	11	12
page	P2	P3	P2	P1	P5	P2	P4	P5	P3	P2	P5	P2
P2	P2	P2	P2	P5	P5	P5	P5	P3	P3	P3	P3	P3
P3	P3	P3	P3	P3	P2	P2	P2	P2	P2	P5	P5	P5
*	*	hit	*	*	*	*	*	hit	*	hit	*	*

main memory size \rightarrow 3 \rightarrow frame

pages \rightarrow 12

$$\text{hit ratio} : \frac{3}{12} \times 100\% = 25\%$$

fault \rightarrow 9

LRU

time	1	2	3	4	5	6	7	8	9	10	11	12
page	P2	P3	P2	P1	P5	P2	P4	P5	P3	P2	P5	P2
*	*	*	hit	*	*	hit	*	hit	*	*	hit	hit
*	*	*	hit	*	*	hit	*	hit	*	*	hit	hit
*	*	*	hit	*	*	hit	*	hit	*	*	hit	hit

hit ratio : $\frac{5}{12} \times 100\%$

fault $\rightarrow 7$

Optimal

time	1	2	3	4	5	6	7	8	9	10	11	12
page	P2	P3	P2	P1	P5	P2	P4	P5	P3	P2	P5	P2
*	*	*	hit	*	*	hit	*	hit	*	*	hit	hit
*	*	*	hit	*	*	hit	*	hit	*	*	hit	hit
*	*	*	hit	*	*	hit	*	hit	*	*	hit	hit

hit ratio : $\frac{6}{12} \times 100\%$

fault $\rightarrow 6$

* hit ratio একই রক্ষা করে।

P5	P5	P1	P5	P2	P1	P3	P3	P0	P7	P0	P1	FIFO
P5	P5	P5	P5	P5	P5	P5	P5	P0	P0	P0	P0	5 hits
		P1	P1	P1	P1	P1	P1	P1	P7	P7	P7	
			P2	P2	P2	P2	P2	P2	P2	P2	P1	
				P3	P3	P3	P3	P3	P3	P3	P3	
hit	hit	hit		hit				hit				

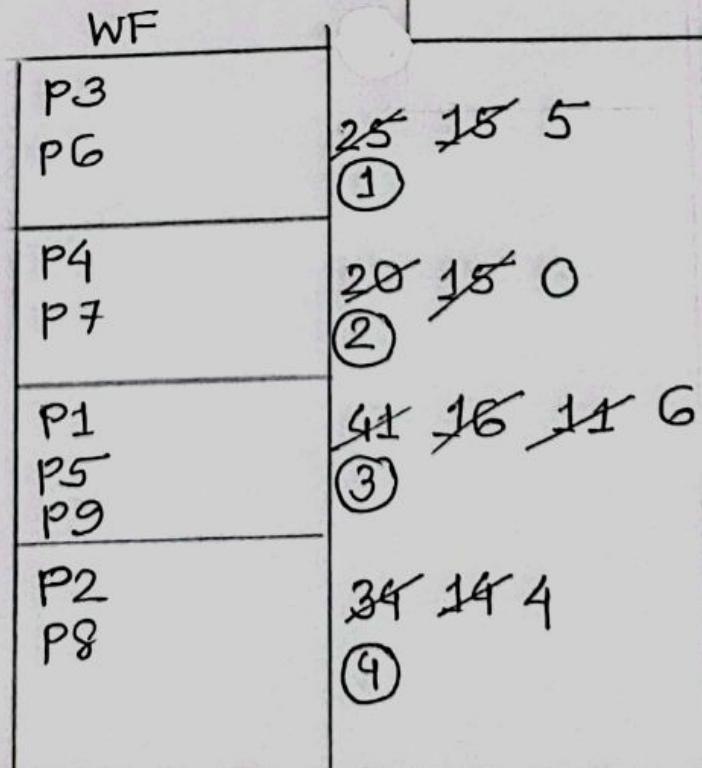
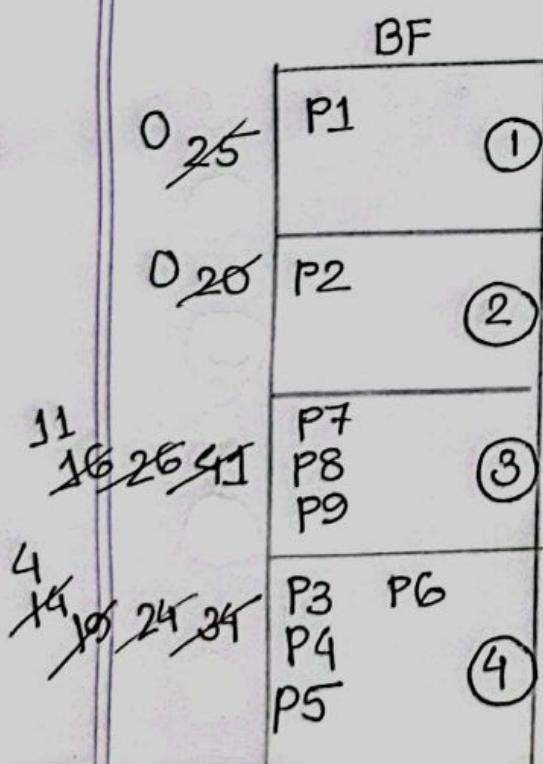
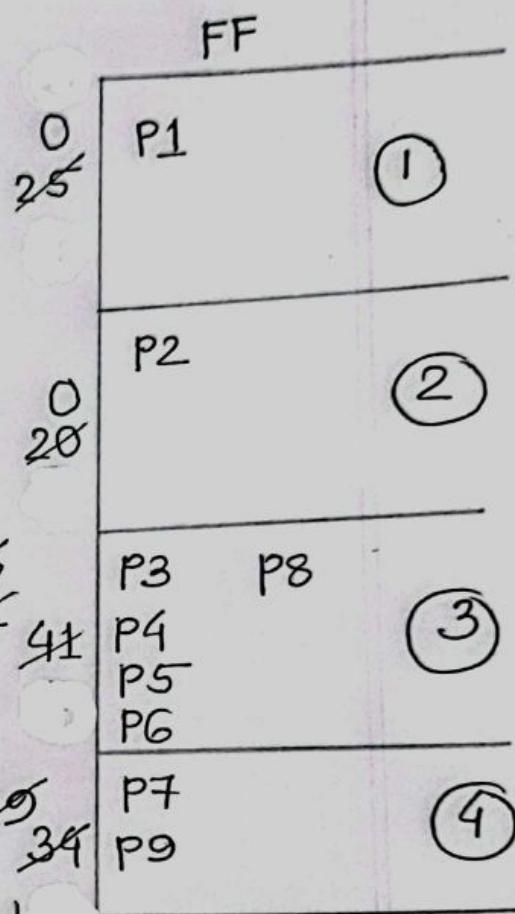
P5	P5	P1	P5	P2	P1	P3	P3	P0	P7	P0	P1	LIFO
P5	P0	P0	P0	P0								
		P1	6 hits									
			P2	P2	P2	P2	P2	P7	P7	P7	P7	
				P3								
h	h	h		h				h	h			

P5	P5	P1	P5	P2	P1	P3	P3	P0	P7	P0	P1	Optimal
P5	P0	P0	P0	P0								
		P1	6 hits									
			P2	P2	P2	P2	P2	P7	P7	P7	P7	
				P3								
h	h	h		h				h	h			

Dynamic Storage Allocation : First Fit, Best Fit, Worst Fit

P	Size	FF	BF	WF
P1	25	1	1	3
P2	20	2	2	4
P3	10	3	4	1
P4	5	3	4	2
P5	5	3	4	3
P6	10	3	4	1
P7	15	4	3	2
P8	10	3	3	4
P9	5	4	3	3
P10	15	N/a	N/a	N/a

25
20
41
34

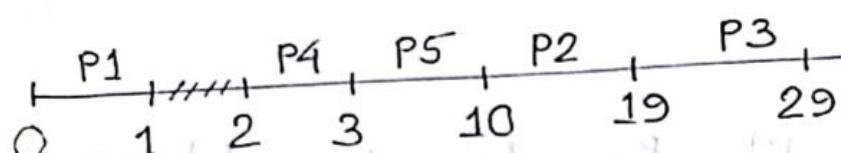


CSE 321

Scheduling Algorithms

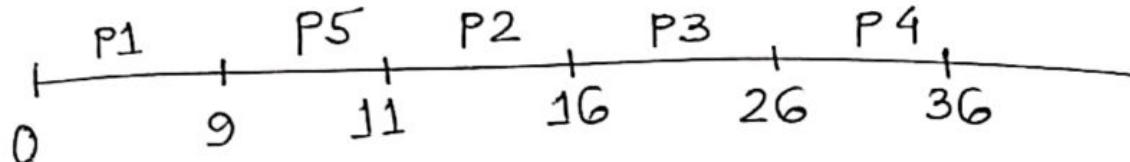
FCFS

PID	AT	BT	WT	T _t
P1	0	1	0	1
P2	3	9	7	16
P3	9	10	10	20
P4	2	1	0	1
P5	2	7	1	8



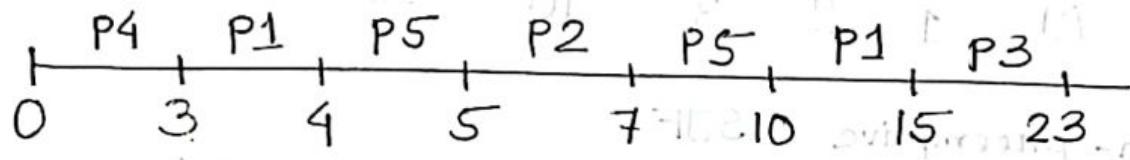
Non-preemptive SJF

PID	AT	BT	WT	T _t
P1	0	9	0	9
P2	2	5	9	14
P3	2	10	14	24
P4	1	10	25	35
P5	3	2	6	8



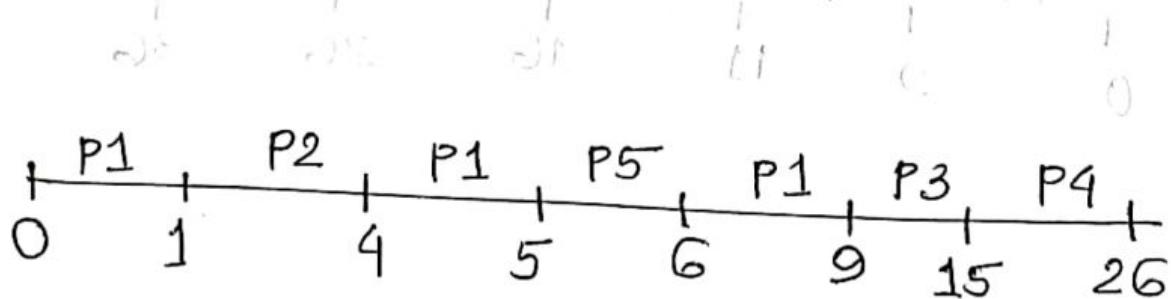
~~P~~ Preemptive SJF

PID	AT	BT	WT	TT
P1	2	6.80	1+6	13
P2	5	20	0	5
P3	1	80	14	22
P4	0	30	0	3
P5	4	430	2	6



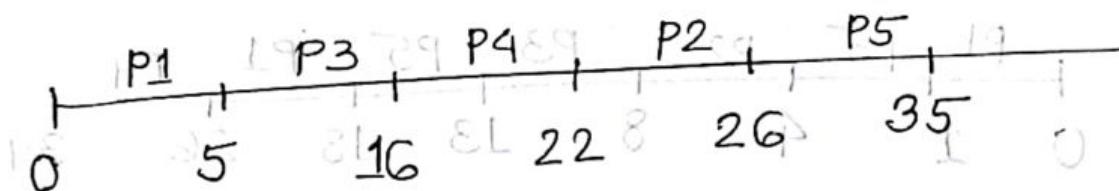
~~P~~ Preemptive SRTF

PID	AT	BT	WT	TT
P1	0	5.430	0+3+4=9	9
P2	1	30	0	3
P3	1	80	8	14
P4	5	110	10	21
P5	5	10	0	1



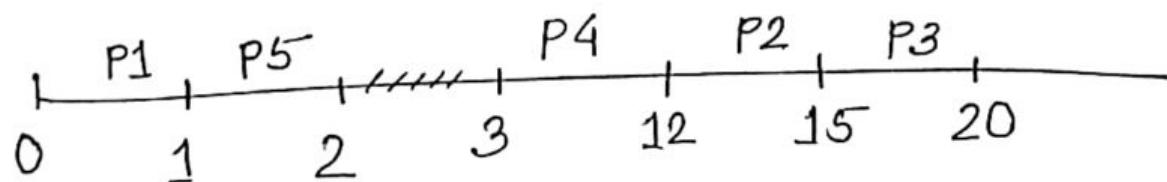
Non Preemptive Priority Queue

PID	AT	BT	PQ	WT	TT
P1	0	5	2	0	5
P2	2	9	4	20	24
P3	2	11	1	3	14
P4	1	6	3	15	21
P5	5	9	5	21	30



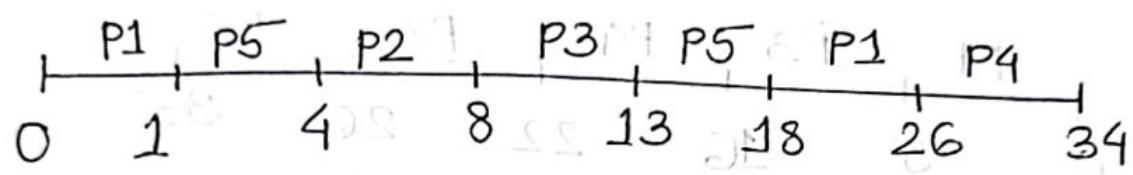
Preemptive Priority Queue

PID	AT	BT	PQ	WT	TT
P1	0	1	3	0	1
P2	4	3	4	8	11
P3	5	5	5	10	15
P4	3	9	1	0	9
P5	1	1	2	0	1



Preemptive Priority Queue

PID	AT	BT	PQ	WT	TB
P1	0	98	4	17	26
P2	4	90	2	0	4
P3	8	50	1	0	5
P4	5	8	5	21	29
P5	1	85	3	9	17



Round Robin Scheduling

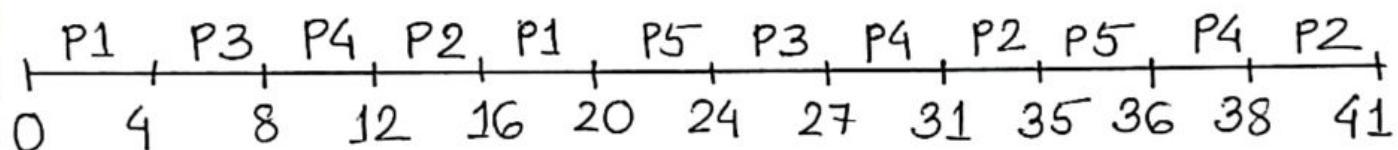
FT	WT	RR	ID	IP
1	0	3	1	0
11	8	3	2	1
21	9	3	3	2
31	7	3	4	3
41	4	3	5	4

1 2 3 4 5
0 11 21 31 41

Round Robin

$$q = 4$$

PID	AT	BT	WT	TT
P1	0	8 4 0	12	20
P2	3	11 7 3 0	27	38
P3	2	7 3 0	18	25
P4	2	10 6 2 0	26	36
P5	6	5 1 0	25	30



~~P1~~ ~~P3~~ ~~P4~~ ~~P2~~ ~~P1~~ ~~P5~~ ~~P3~~ ~~P4~~ ~~P2~~
~~P5~~ ~~P4~~ ~~P2~~