Final -A #11+=2 Afault = 10 - Facily reaction # Facily = 83.33%

final-B Offimal e) # Frame = Right 7,3,2,1,2,3,7,8,3,5,8,2 2 2 7 Hit y + Hit X Hit 3 8 1+1+ 414 Hit 6 5 #-hit= 6 : hit tradio= #hit * 00 12

$$=\frac{6 \times 100}{12} = 50\%$$

Problem 6 : Griven, LAS=8 bits Page Size= 16 Bytes Each Page = 4 " Main memory Size=512Bytes Frage = Page Size = 16 = 4 = 2 = 2 out page impage offset re ii) Given, Logical Add = 179 out off = inner page 10/3/0011 page > 2 off > 3 off > 3 inner page > 3 off > 3 off > 3 PA = (frame # * page size) + Offset = [(14 * 16) + 3] = 227

Problem 7; Given, Civer,

16 27m=16

LAS=16 bits = 2

Page Size=16 Bytes = 2 => n=9

Fach Page Entry Each Page = 2 Bytes:2 Main memory = IKB = 1024 Bytes (11) = size of inner PMT = 2 x each page = 211 * 21 $= 2^{13}$ 213 > 27; so 2 level paging needed. 7. # of pages in PMT = $\frac{2^{13}}{2^{4}} = 2^{9} \rightarrow n$ Size of PMT

Offset : size of outer PMT = 2 * 2 = 210

2¹⁰
$$> 2^{9}$$
; so 2-level paging needed.
: # of pages in PMT = $\frac{2^{10}}{2^{1}} = 2^{6}$ in PMT = $\frac{2^{10}}{2^{10}} = 2^{6}$ in PMT = $\frac{2^{10}}{2^{10}} = 2^{6}$ in PMT = $\frac{2^{10}}{2^{10}} = 2^{10}$ in PMT = $\frac{2^{10}}{2^$

Question 2 (CO1 - 6 points): A process runs in a system with multi level paging and it has a logical address space of 8 bits. In the system page size is 16 Bytes, size of each entry of the page table is 4 Bytes and size of the main memory is 512 Bytes. In order to fit the pages of the process in the main memory the OS applies a two-level paging technique in outer page number bits of the logical address

space until the outer most page table can be allocated in a frame of the main memory. Illustrate the logical address space of the process including the necessary outer page

bits, inner page bits and offset bits of every step with proper mathematical calculations during the paging mechanism of the system described above.

In this system, if the CPU generates logical addresses 130 and 104 then map the corresponding physical addresses of these logical addresses.

Necessary page table information is given below:

	Outer page ta	ble
	Frame #	valid/invalid bit
age#	Litanio	i
		v
	6	v
	11 -	

		Inner p	age tables		
			PMT at frame 11		
PMT at frame 6		TOTAL CONTRACT	Frame #	valid/invalid	
Page #	Frame #	valid/invalid bit	Page #	Figure "	bit
			0	25	V
0	3	V			i
1	20	V	1		
		i	2	12	V
2		v	3	14	V

Geiven, LAS=8 bits = 28 m=8

Page Size = 16 Bytes = 29 n=9

Each Page Entry = 9 Bytes = 22 Main memory = 512 Bytes

NOW, P (m-n) 2P & Each Page # of inner Paga= = z4 * z2

26 > 24 -> Need two Level

of Size in PMT =
$$\frac{26}{29}$$
 = 2^2

in = 2

2 | 2 | 4 |

P d

tof outer Page in PMT = 2^p * Fach Page

= 2^2 * 2^2

= 2^4

= 2^4

So, Completed

1) Need = 86 it 6 in any.

11) | 130 = 1000 0010

104 = 0110 1000

Fore, 1000 0010

$$F=25$$
 offset
 $F=25$ offset
 $F=25$ offset
 $F=25$ offset
 $F=25$ offset
 $F=25$
 $F=25$ offset
 $F=25$
 $F=$

Forty 010 0010

F=6 F=invalid

Logical Address Invalid