CSE350: Digital Electronics & Pulse Techniques

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Contents

Chapter 1

ADC (Analog to Digital Conversion)

Analog: Information or data that can be any real value at any instant of time. Physical world signals are of analog nature. For instance, a sinusoidal voltage or current. The voltage $V(t) = 5sin(\omega t)$ is an analog voltage, that can take any value between $[-5, 5]$.

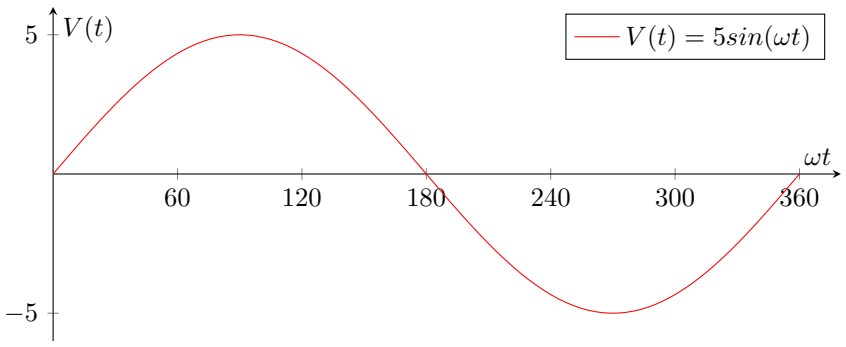


Figure 1.1: An analog signal

Digital: Information in the form of binary bit streams (0 & 1). Only *two* real values are used to represent the two binary bits. Computers and all digital devices need digital signals to operate. In most of the cases, a higher voltage is used to represent '1', while a lower voltage represents '0'.

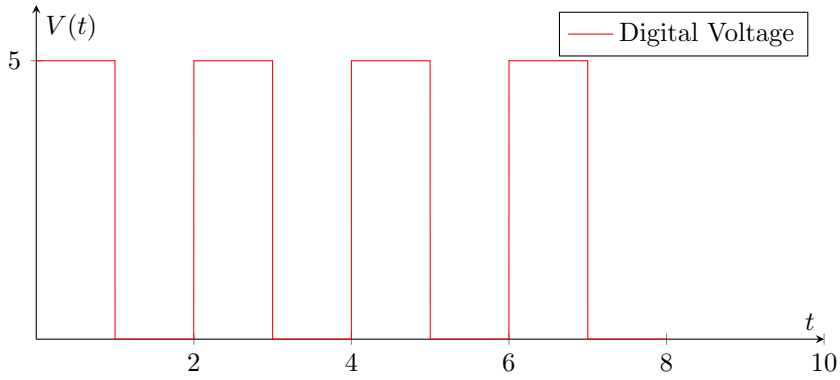


Figure 1.2: A digital signal

ADC is the process of converting an analog signal to a digital signal. The full process can be split into a few steps, and it can be modeled as the following flow chart:

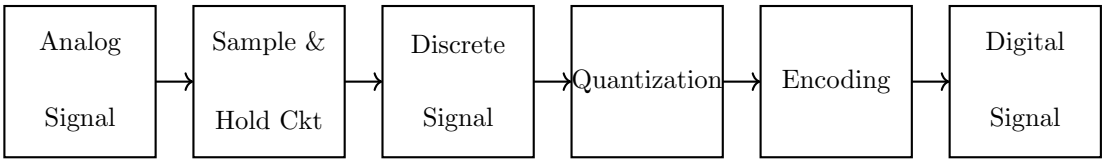


Figure 1.3: A flow chart of ADC process

Sample & Hold Circuit: The analog signal is sampled at regular intervals of a clock pulse. A *capacitor* is used to hold the peak value of the preceding interval until the next one arrives. Thus, instead of all the real values of the original signal, we get a signal with **reduced number of values** (still possibly greater than two), i.e., a *discrete signal*.

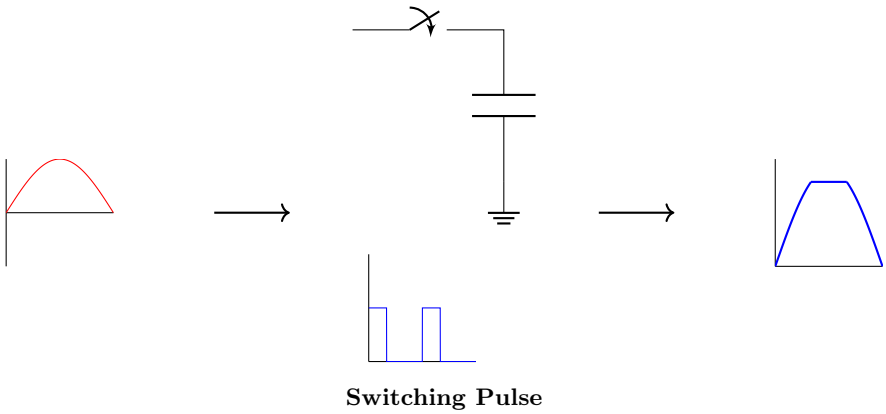


Figure 1.4: Sample & Hold circuit

Here, when the switch is closed, the capacitor charges according to the input analog signal. When the switch is open, it holds the last charged value until the next closing of the switch. This results in the output to miss out on the values of the input signal, that were between two successive closing of the switch. The faster the switching, the shorter is the duration of the pulse, and at very high frequencies, we effectively get about a single value of the input across the capacitor in each switching interval. These are called the *sampled values* of the input. These are then quantized using a certain quantization scheme.

Quantization: The sampled values from the previous stage still have a lot of values. The maximum allowable number of different values is determined by the *resolution* of the ADC process, which is the number of bits used in the output digital signal. We know that there be 2^n numbers for n bits. Thus, the maximum number of allowable values at the output is 2^n. We call these values the *quantization levels*. Now, the question is, which values do we select as the quantization levels? This depends on the *quantization scheme* we use. We will discuss two popular such methods next.

Mid-rise Quantization: In this method, the range of the input signal is divided into a set of *equal-sized intervals*, and the output levels are assigned to the *midpoints* of these intervals. The quantization levels are *symmetric* about the *signal zero*, but **do not include** the signal zero as a quantization level. Here, by signal zero we mean the midpoint between the signal maximum & minimum.
For example, consider a signal with maximum value of 5 and minimum value of -3. If we use 3 bits as the output digital signal, we will get $2^3 = 8$ quantization levels. Since the levels are equally spaced, the difference between any two successive quantization levels can be calculated as follows,

$$\text{Step size}, \Delta = \frac{V_{max} - V_{min}}{2^n} \tag{1.1}$$

Where, V_{max} & V_{min} are the maximum and minimum values of the input analog signal respectively. For our example, equation 1.1 gives,

$$\Delta = \frac{5 - (-3)}{2^3} = 1$$

Thus, the quantization intervals will be as the following, starting at signal minimum:

Quantization Interval	**Quantization Level**
$[-3,\ -2)$	-2.5
$[-2,\ -1)$	-1.5
$[-1,\ 0)$	-0.5
$[0,\ 1)$	0.5
$[1,\ 2)$	1.5
$[2,\ 3)$	2.5
$[3,\ 4)$	3.5
$[4,\ 5]$	4.5

Table 1.1: Mid-rise Quantization

As you can see, there is no 1 among the quantization levels, which is the signal zero for our example.

You might wonder, the sampled signal from the sample & hold circuit still has more values than the number of the quantization levels. What do we do with the values other than the quantization levels? Do we discard them? No. We map all the sampled values according to table 1.1. A sampled value will be changed to the quantization level value of the quantization interval it lies within. For instance, suppose a sampled value is -1.2. It falls within the quantization interval [-2,-1], for which the quantization level is -1.5. Thus, -1.2 will be treated as -1.5 after the quantization process.

Mid-tread Quantization: The main difference of this scheme with mid-rise quantization is that, it *uses* the signal zero as a quantization level. Consequently, we cannot make all the intervals of equal length, even if we wanted to. Why? Well if you closely observe table 1.1, you will realize that it is not possible to include the signal zero as the quantization level if we begin and end at signal minimum and maximum respectively, and also keep all the intervals of equal length. Thus, we have to adjust at the two ends. A mid-tread quantization scheme for our previous example signal with unequal intervals at the first & last one is shown below:

Quantization Interval	Quantization Level
$[-3,\ -2.5)$	-2.75
$[-2.5,\ -1.5)$	-2
$[-1.5,\ -0.5)$	-1
$[-0.5,\ 0.5)$	0
$[0.5,\ 1.5)$	1
$[1.5,\ 2.5)$	2
$[2.5,\ 3.5)$	3
$[3.5,\ 5]$	4.25

Table 1.2: Mid-tread Quantization

Encoding: Now that we have the quantized signal with only 2^n different values, we need to convert them to binary bit streams of n bits to get our final digital output. This process is called *encoding*. In this step, the quantized signal is assigned a bit stream each. Simply, the 2^n quantization levels are represented with the 2^n binary numbers possible with n bits. For our previous example, the encoding would be as follows:

Quantization Level	Encoded Output
-2.5	000
-1.5	001
-0.5	010
0.5	011
1.5	100
2.5	101
3.5	110
4.5	111

Table 1.3: Encoding of Mid-rise Quantized Signal

Now we shall go the main part. Our main focus in this course is how this encoding is done. For this we will discuss two ADC circuits that do the job — Flash & Dual Slope ADC.

Flash ADC

The Flash ADC circuit for a 3-bit ADC is given below:

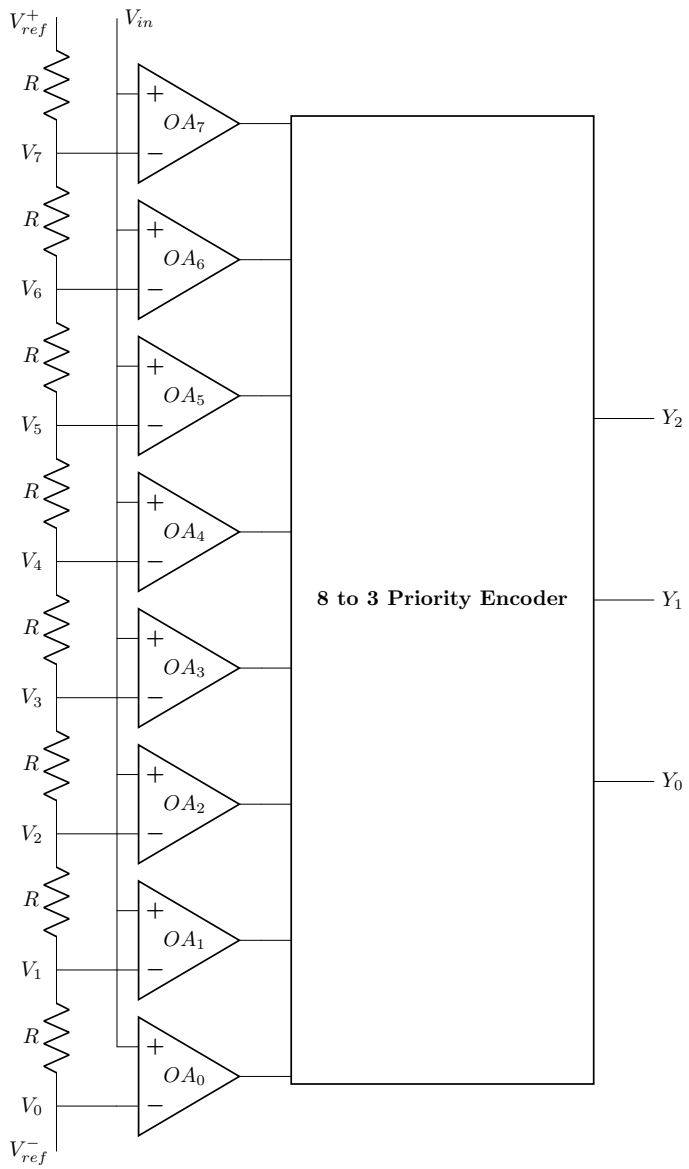


Figure 1.5: 3-bit Flash ADC (Mid-rise Quantization)

Let's discuss its several parts one by one.

Op Amps: Try to recall your learning on Op Amps from CSE251. When they are used in *open-loop* configuration, they act as comparators. The output from them is the high bias voltage V_H if $V_+ > V_-$. Ohterwise, the output is the low bias voltage, V_L.

As we can see from figure 1.5, the non-inverting or positive terminal takes in the analog input voltage, while the inverting or negative terminal is connected to a resistance ladder in between two resistances. We should recall also that, in any configuration, ideal Op Amps do not draw any current in either of their terminals. Hence, these connections from the inverting terminals to the resistance ladder, are just taking the voltage, and are effectively open circuits. Consequently, the resistances are actually in series.

Priority Encoder: A Priority Encoder is a special type of encoder, that outputs the binary of the serial number of the *highest* input terminal that receives high voltage. It ignores the input terminals with a lower serial number than the one mentioned. The truth table of an 8 to 3 Priority Encoder is the following:

I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	×	0	0	1
0	0	0	0	0	1	×	×	0	1	0
0	0	0	0	1	×	×	×	0	1	1
0	0	0	1	×	×	×	×	1	0	0
0	0	1	×	×	×	×	×	1	0	1
0	1	×	×	×	×	×	×	1	1	0
1	×	×	×	×	×	×	×	1	1	1

Table 1.4: Truth table of an 8-to-3 Priority Encoder

Here, '×' represents 'don't care' logic.

Analysis of Operation: As we stated earlier, the resistances in the ladder are in series. Thus, the total resistance of the ladder is 8R. Using Ohm's law, we can write the current in this resistance ladder as,

$$I = \frac{V_{ref}^{+} - V_{ref}^{-}}{8R} \qquad \Rightarrow IR = \frac{V_{ref}^{+} - V_{ref}^{-}}{8}$$

Here, 8 resistances are used, because the ADC is a 3-bit one. Thus, the *resistance count* of a Flash ADC is 2^n. Let's bring back our previous example of the analog signal with maximum value 5 and minimum value -3. If we use these values as the reference voltages of the resistance ladder, then we get,

$$IR = \frac{5 - (-3)}{8} = 1$$

Which is the step size, Δ. Now, using KVL along the ladder we can write,

$$V_1 = V_0 + IR = -3 + 1 = -2$$

This was the lower boundary of the 2^{nd} quantization interval of mid-rise quantization, [-2,-1). In general, we can observe that,

$$V_i = V_0 + i \times IR = V_0 + i \times \Delta$$

The whole circuits operates this way — the input voltage is compared with the inverting terminal voltages of all the Op Amps (V_i). The Op Amps for which $V_{in} > V_i$, the output is high. Thus

the corresponding input of the encoder, I_i is high. The other Op Amps will output low voltage and the corresponding encoder inputs will be low. Now, the encoder output is decided based on what is the highest serial of the Op Amps giving high output, as explained in table 1.4.
For our example, suppose the input voltage is -1.2 V. This is higher than the V_- of OA_0 & OA_1 (-3 V & -2 V respectively). Thus, I_0 & I_1 will be high and other inputs low. From table 1.4 we see that the output of the encoder for this case is $(001)_2$. If you recall from the discussion on encoding, this is the desired output for the mentioned input voltage. The circuit shown in figure 1.5 is however, not the only possible Flash ADC. Depending on the quantization scheme used, it may be modified. For instance, if we had used mid-tread quantization instead for our example, the circuit would look like this:

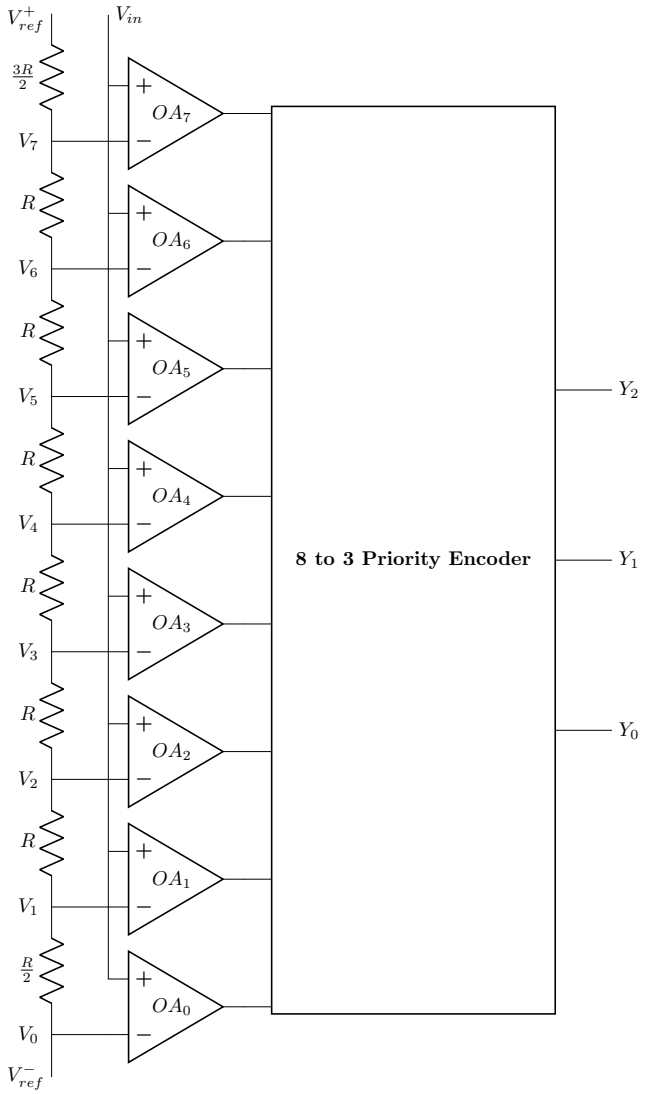


Figure 1.6: 3-bit Flash ADC (Mid-tread Quantization)

Through a similar analysis as in the mid-rise case on figure 1.6 should lead you to concluding

that the inverting terminal voltages are again equal to the lower boundaries of the quantization intervals of table 1.2.

Some interesting facts to note here:

1. **Redundancy of the 0^{th} Op Amp:** The input signal is always greater than or equal to its minimum value, which corresponds to the V_- of the 0^{th} Op Amp. Therefore, it will always output high. Instead of using OA_0, we can directly apply a high voltage at I_0 of the encoder. Hence, the *Op Amp count* in a Flash ADC is either 2^n or $2^n - 1$.
2. **Why the name 'Flash' ADC?** Because its *conversion speed is very high*—it can convert a sampled value in a *single clock cycle*.
3. **Disadvantage:** A Flash ADC uses a large number of components (resistors and Op Amps), which makes it costly and power-hungry.

Dual Slope ADC

To overcome the disadvantages of a Flash ADC, we introduce Dual Slope ADC, a cheaper but slow alternative. A generalized diagram of the Dual Slope ADC is given below:

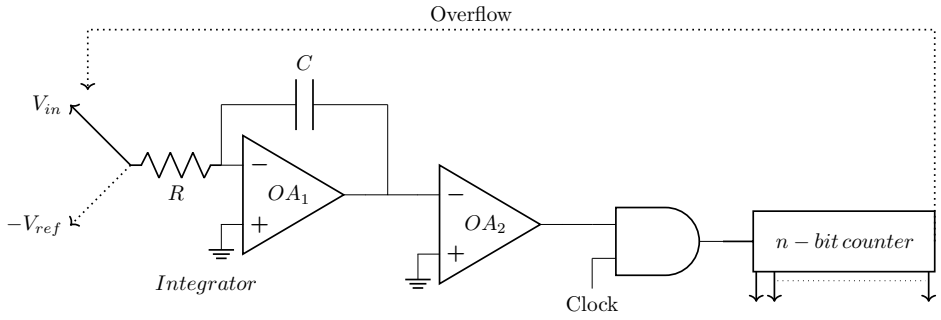


Figure 1.7: Dual Slope ADC

Let's discuss the components one by one.

Integrator: OA_1, R & C form an integrator, input to which switches between $-V_{ref}$ & V_{in}. From CSE251, we should know that if the input voltage to the integrator is V_i, then the output is,

$$V_o(t) = -\frac{1}{RC}\int_0^t V_i\,dt + V_o(0) \tag{1.2}$$

Comparator: OA_2 is a simple comparator to which, the output from the integrator is connected, at its inverting terminal. The non-inverting terminal is grounded. Thus, it will output high, when the integrator's output is negative.

AND gate & Clock: The output from the comparator is fed to an AND gate along with a clock signal of high frequency. The AND gate will give a high output if both the clock pulse and the comparator's output are high.

n-bit counter: An n-bit counter counts from 0 to 2^n-1, i.e. 2^n times, for each high input. The output from this counter is the binary of the current serial (between 0 to 2^n-1) it has counted up to. For example, consider a 3-bit counter. It counts from 0 to 7. So, its output will change from $(000)_2$ to $(111)_2$ by one step at each high input to the counter. Thus, if we say the counter has counted 4 times since the start, it has actually counted from 0 up to 3, and its current output will be $(011)_2$. Once it reaches 2^n-1, the next high input causes it to overflow, and the counter resets to 0.

Analysis of Operation: We will take a step by step approach to understand the function of the Dual Slope ADC.

1. **Integration:** We discussed earlier that the input to the integrator switches between input & a reference voltage. In each separate conversion of a sampled analog input, the input voltage is connected to the integrator input for a fixed amount of time t_1. As we said that we use high sampling frequencies, which effectively makes the sampled values a single constant voltage. We can observe from equation 1.2, that a constant input voltage would cause the output of the integrator to be as follows(assuming 0 initial voltage):

$$V_o(t) = -\frac{1}{RC} \times V_{in} \times t$$

This is a straight line equation with respect to time, for which the slope is $-\frac{V_{in}}{RC}$. Let the voltage output from the integrator, after t_1 is V_1. Then we have,

$$V_1 = -\frac{V_{in} t_1}{RC} \tag{1.3}$$

The time t_1 depends on the number of bits used in the output digital signal, and on the frequency of the clock pulse in the following manner,

$$t_1 = \frac{2^n}{f_{CLK}} \tag{1.4}$$

The time t_1 is actually the time taken for the n-bit counter to count 2^n times starting from 0 to $2^n - 1$. Its expression can be easily drived by unitary method. As we said the counter counts for every high clock pulse, number of pulses thus needed for counting 2^n times is also 2^n. If the clock frequency is f_{CLK}, time taken for 2^n pulses $= 2^n \times f_{CLK}$. This process is showed in the following graph:

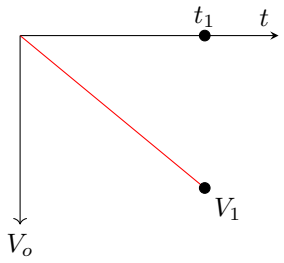


Figure 1.8: Integrator output after t_1

2. **De-integration:** Next, the switch at the input of the integrator connects to the negative reference voltage $-V_{ref}$. This is also a constant voltage. Thus, we will again get a straight

line output from the integrator, but this time the slope will be positive. Also, the initial output voltage is not 0 this time, rather, V_1. This rising (positive slope) nature of the output causes the value to increase from V_1 to 0. The time taken for the output of the integrator to become 0 from V_1 is t_2. Using equation 1.2 again, we can write for this case,

$$
\begin{aligned}
& V_o(t_1+t_2) = -\frac{V_{ref}}{RC}\int_{t_1}^{t_1+t_2} dt + V_o(t_1) \\
& \Rightarrow 0 = \frac{V_{ref}}{RC}(t_2+t_1-t_1) + V_1 \\
& \Rightarrow \frac{V_{ref}}{RC}t_2 - \frac{V_{in}t_1}{RC} = 0 \\
& \Rightarrow t_2 = \frac{V_{in}t_1}{V_{ref}} \\
& \Rightarrow t_2 = \frac{2^n}{f_{CLK}} \cdot \frac{V_{in}}{V_{ref}}
\end{aligned} \tag{1.5}
$$

Since all other parameters in equation 1.5 are constants, t_2 is proportional to the input voltage V_{in}. Which means, the larger the sampled value, the longer is t_2.

The output of the integrator, after this process would look like the following:

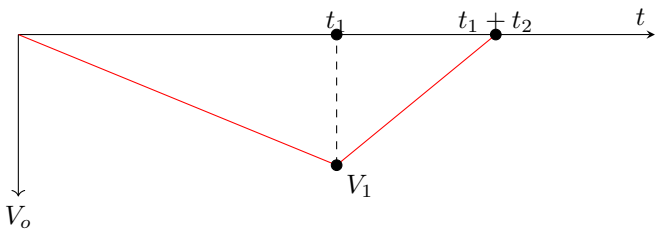


Figure 1.9: Integrator output after t_2

3. **Comparator AND Clock:** We see that the integrator output in figure 1.9 is always negative, during the whole conversion process (t_1+t_2). Since this output is fed to the inverting terminal of the comparator (OA_2), the output of OA_2 will always be high. Consequently, the AND gate function reducess from Comparator AND Clock to Clock (1 AND A = A). This means, the AND gate will output high value whenever the clock pulse is high. Only after t_2, when the integrator's output becomes 0, the comparator will give low output. Then the AND gate will block the clock pulse from the counter, marking an end to the counting.

4. **Counting of the counter:** The n-bit counter is effectively receiving the clock as its input. At each clock pulse, it counts one by one. During 0 to t_1, it counts from 0, up to 2^n-1. Then it overflows, and this causes the input of the integrator to switch from V_{in} to V_{ref}. Then the counter resets to 0, and begins counting for the 'De-integration' phase. The formula of t_1 we showed in equation 1.4, can be derived using unitary method with the help of this

concept.

The counter counts once every T_{CLK} time
The counter counts 2^n times in $T_{\text{CLK}} \times 2^n$ time
$$\therefore t_1 = 2^n \times T_{\text{CLK}} = \frac{2^n}{f_{CLK}}$$

Here, T_{CLK} is the period of the clock pulse.

As we saw back in equation 1.5, that t_2 is proportional to the input sampled signal, the counter counts up to a value proportional to this input voltage within t_2 ($t_2 \times f_{CLK} = \frac{V_{in}}{V_{ref}} \propto V_{in}$).

Hence, the output of the counter after t_2 is the binary of $N = (t_2 \times f_{CLK} - 1)$ (since the counter counts from 0 and $t_2 \times f_{CLK}$ times).

In a word, we get a digital output from the n-bit counter proportional to the input sampled signal. The bit count of the counter depends on the number of quantization levels we use. For 2^n quantization levels, we need an n-bit counter. For instance, if we want 8 quantization levels, we need a 3-bit counter. One thing to note here, is that, t_1 is the same for different sampled inputs. However, t_2 varies. Thus, we will have different V_1 values after the same t_1, while the conversion for each finishes at different instants ($t_1 + t_2$). All these are visualized below for multiple samples:

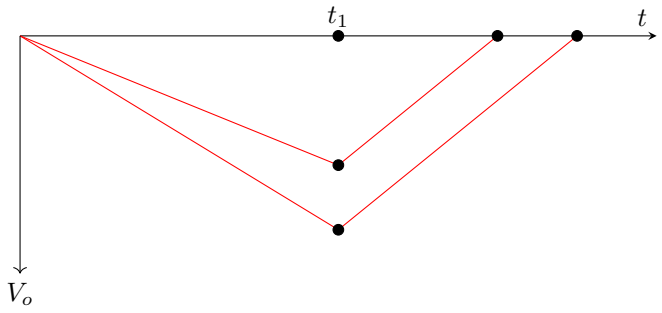


Figure 1.10: Integrator output for different sampled inputs

Let's discuss some important facts regarding Dual Slope ADCs.

1. Let's consider the decimal of the output, N. As we said, $N = (t_2 \times f_{CLK}) - 1$. From which we can write, $t_2 = \frac{N+1}{f_{CLK}}$. Comparing this with equation 1.5,

$$V_{in} = \frac{N+1}{2^n} \cdot V_{ref} \tag{1.6}$$

2. This is not the only possible Dual Slope ADC circuit. There is a common modification to this— the input voltage is applied in opposite polarity, and the reference voltage used is then positive. This then causes the *integration* phase to have a positive slope, and the *de-integration* phase takes a negative slope. However, the analysis and other formulas remain the same. Just, the whole output from the integrator is mirrored with respect to x-axis. The integrator's output is then as shown:

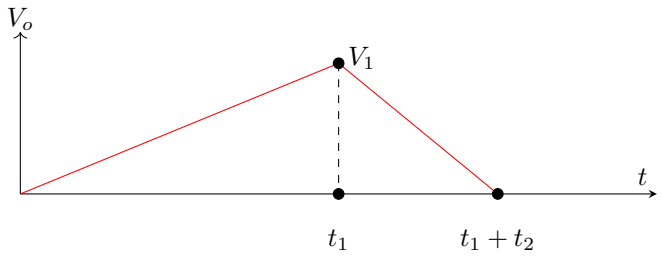


Figure 1.11: Integrator output if V_{in} & V_{ref} are reversed

Note: However, we must swap the connections of the *comparator* to achieve this though. This is because, the integrator's output will always be positive now. So, it should be applied to the non-inverting terminal of the Op Amp instead. Consequently, the inverting terminal of the Op Amp needs to be grounded. This will again cause the Op Amp to always output high, during the processing of a sampled input.

3. Well we haven't discussed the context behind the name 'Dual Slope' yet, but you should have guessed it by now. As we see in both figures 1.9 & 1.11, the slope of the integration, and de-integration phases are different. First one depends on the value of the sampled input, while the second one is the same for all samples, and depends on the reference voltage instead.

4. The number of *components* used are significantly lower than the equivalent Flash ADC circuit. For instance, a 4-bit Flash ADC would require at least 2^4 or 16 resistors, and $2^4 - 1$ or 15 Op Amps. Whereas, the Dual Slope ADC needs two Op Amps and only one resistor & capacitor irrespective of the resolution or bit count.

5. Dual Slope ADCs are really slow, and take a lot of time for conversion compared to Flash ADCs.

Formulas Roster		
Quantization		
Topic	**n-bit**	**3-bit**
Step Size (Δ)	$\Delta = \frac{V_{max}-V_{min}}{2^n}$	$\Delta = \frac{V_{max}-V_{min}}{8}$
Flash ADC		
Topic	**n-bit**	**3-bit**
Number of Resistors	$N_R = 2^n$	$N_R = 8$
Number of Op Amps	$N_{OA} = 2^n/2^n - 1$	$N_{OA} = 8/7$
Inverting Terminal Voltage of Op Amps	$V_i = V_{ref}^- + i \times \Delta$	
Dual Slope ADC		
Topic	**n-bit**	
Integration Phase Duration	$t_1 = \frac{2^n}{f_{CLK}}$	
De-Integration Phase Duration	$t_2 = \frac{V_{in}}{V_{ref}} t_1$	
Output Voltage of Integrator after Integration Phase	$V_1 = -\frac{V_{in}}{RC} t_1$	
Number of Counts during De-Integration Phase	$m = N + 1 = t_2 \times f_{CLK}$	
Maximum Allowable Sampling Frequency	$f_{s_{max}} = \frac{1}{2t_1}$	
Slope of Integration Phase	$-\frac{V_{in}}{RC}$	
Slope of De-Integration Phase	$\frac{V_{ref}}{RC}$	

Problems Roster

Problem 1: Design a 3-bit Flash ADC for a signal with maximum & minimum value of 10 V & 0 V respectively. The quantized levels of the ADC should be uniform (equal step-size). Answer the following:

(a)	Calculate the total number of resistors & Op Amps required.
(b)	Calculate the **1LSB** value or step size.
(c)	Find the quantization levels & plot the D_{out} (digital output) vs V_{in} plot.
(d)	If the input is 7 V: (i) Find the quantization interval the input lies in. (ii) What is the digital output for this input?
(e)	If the digital output is 110_2, what are the maximum & minimum values of input that would produce this result?
(f)	If an additional bit was desired at the output, what would be the required number of components?

Solution:

(a) $N_R = 2^n = 2^3 = 8$
$N_{OA} = 2^n$ or 2^n -1 = 8 or 7
(b) $V_{1LSB} = \Delta = \frac{V_{max} - V_{min}}{2^n} = \frac{10-0}{8} = 1.25\,V$
(c) The quantization levles are as follows:

Quantization Interval	Quantization Level
0-1.25	0.625
1.25-2.5	1.875
2.5-3.75	3.125
3.75-5	4.375
5-6.25	5.625
6.25-7.5	6.875
7.5-8.75	8.125
8.75-10	9.375

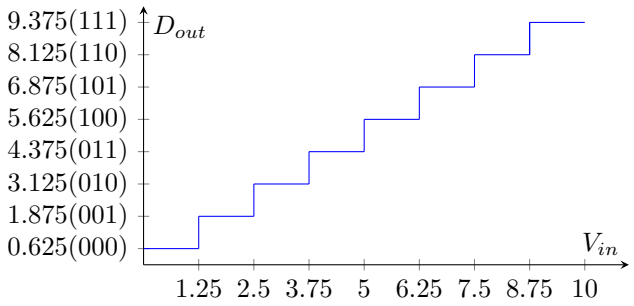


Figure: D_{out} vs V_{in} graph

(d)

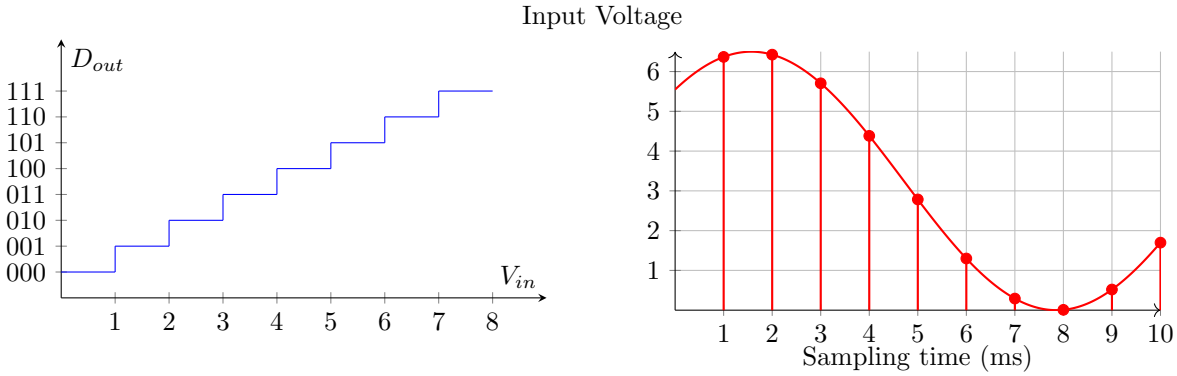
(i) 6.25-7.5

(ii) 101

(e) Maximum = 8.75 V & minimum = 7.5 V.

(f) For 4-bit Flash ADC, $N_{OP\,AMP} = 2^4$ or $2^4 - 1$. $N_R = 2^4$.

Problem 2:



(a)	Design a 3-bit Flash ADC for the given input-output characteristics.
(b)	An unknown signal is passed to the ADC as input. The ADC takes samples at a rate of 1 kHz. In the graph, the input signal is shown where the x-axis represents the time, and the y-axis represents voltage at any specific time. The sampling instances are given in the figure. Find the encoded output that represents the analog sigal inside the given time frame.

Solution:

(a)

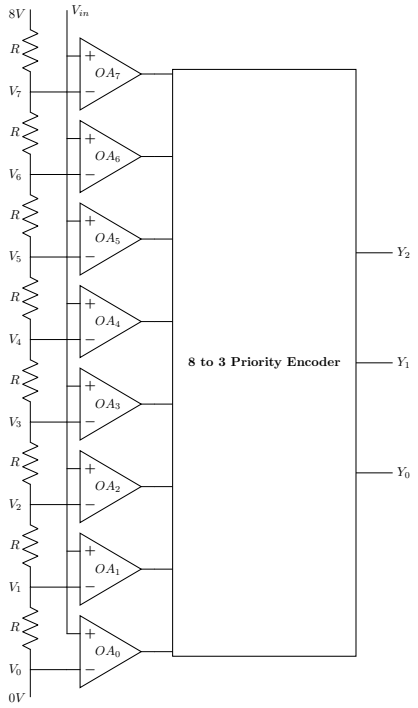


Figure 1.12: 3-bit Flash ADC for Problem 2(a)

(b)

Sampling Instances	Input Voltage	Quantization Interval	Encoded Value
1 ms	6.3 V	6 V - 7 V	110
2 ms	6.4 V	6 V - 7 V	110
3 ms	5.7 V	5 V - 6 V	101
4 ms	4.4 V	4 V - 5 V	100
5 ms	2.8 V	2 V - 3 V	010
6 ms	1.3 V	1 V - 2 V	001
7 ms	0.3 V	0 V - 1 V	000
8 ms	0 V	0 V - 1 V	000
9 ms	0.5 V	0 V - 1 V	000
10 ms	1.7 V	1 V - 2 V	001

Problem 3:

A Dual Slope ADC has $V_{ref} = 5$ V, and an 8 bit counter that outputs an 8-bit representation of the input signal. A 1 MHz clock is used for the clock and counter circuits.

(a)	Determine the input voltage range, number of steps and step size (resolution) of the ADC.
(b)	For a specific input voltage, the ADC outputs a count of m=100. Determine the input voltage.
(c)	Determine the total time required to get the reading in (b).
(d)	Calculate the maximum sampling rate of the ADC.
(e)	A person wishes to get a sampling rate 4 times that of the current circuit. Determine how many bits should be used for the counter without changing any other system parameters.

Solution:

(a) Input voltage range: 0 V - 5 V

Number of steps $= 2^8 = 256$

Step size, $\Delta = \frac{V_{ref}}{2^n} = \frac{5}{256} = 0.0195\,V$

(b) We know from equation 1.6, $V_{in} = \frac{N+1}{2^n} V_{ref}$

$$\therefore V_{in} = \frac{100+1}{256} \times 5 = 1.973\,V$$

(c) We know from equation 1.4, $t_1 = \frac{2^n}{f_{CLK}}$

$$\therefore t_1 = \frac{2^8}{1 \times 10^6}\,s = 0.256\,ms$$

From equation 1.5, $t_2 = \frac{2^n}{f_{CLK}} \cdot \frac{V_{in}}{V_{ref}}$

$$\therefore t_2 = \frac{2^8}{1 \times 10^6} \cdot \frac{1.973}{5}\,s = 0.101\,ms$$

Therefore, total conversion time, $t = t_1 + t_2 = 0.256 + 0.101 = 0.357\,ms$

(d) Maximum conversion time is limited by the time required for worst case conversion of input $= V_{ref} = 5$ V. For this case $t_1 = t_2 = 0.256\,ms$.
Thus, worst case conversion time,$t_{max} = 2 \times t_1 = 2 \times 0.256 = 0.512\,ms$.

$$\therefore \text{Maximum sampling rate} = \frac{1}{t_{max}} = \frac{1}{0.512 \times 10^{-3}}\,Hz = 1953.125\,Hz$$

(e) From (d) we see, maximum sampling rate $\propto \frac{1}{2^n}$. Thus,

$$\frac{f_{samp_1}}{f_{samp_2}} = \frac{2^{n_2}}{2^{n_1}} \Rightarrow \frac{2^{n_2}}{2^8} = \frac{1}{4} \Rightarrow n_2 = 6$$

Problem 4:
Suppose a sinusoidal signal with peak-to-peak value of 6 V & frequency of 1 kHz needs to be encoded using Dual Slope ADC. What changes are necessary to the Dual Slope ADC in *Problem*

3 to get a successful conversion?

Solution: If we closely observe, there is another limitation of the Dual Slope ADC of figure 1.7—it cannot deal with bipolar input signals (i.e. signals with both positive & negative values).

The sinusoidal signal mentioned in the question ranges between -3 to 3. To handle this signal and to get a successful conversion using the Dual Slope ADC, we first need to make all of its values positive. This can be done by adding an *appropriate offset* to the sine wave. The goal is to get all of its values within the range of 0 to a maximum value, which is the requirement for our Dual Slope ADC.

So, for a sine wave of amplitude 3 V (peak-to-peak value of 6 V), we need to add 3 V of offset. This will lift all the values of the sine wave between 0 V to 6 V. This is illustrated in the following figure:

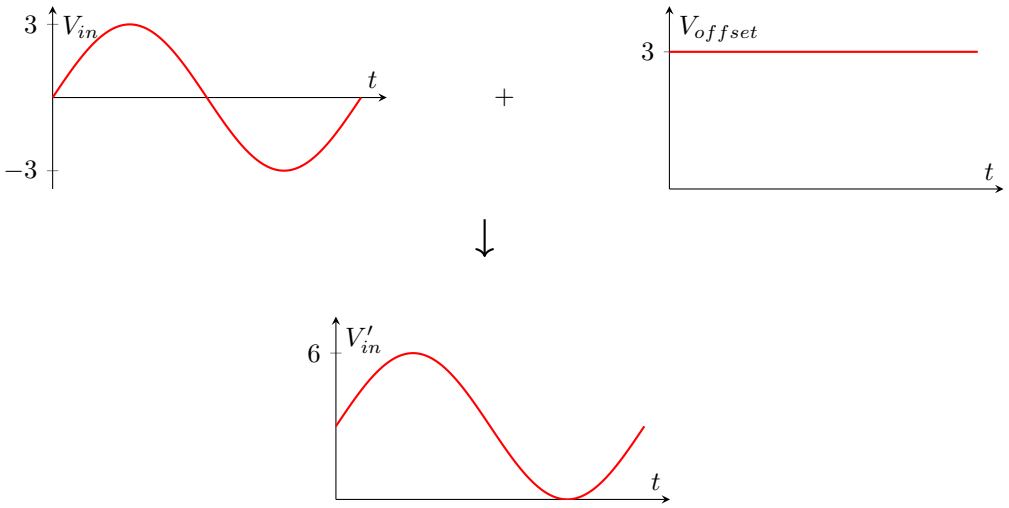


Figure 1.13: Adding offset to input signal

But the question is, how do we achieve this addition of offset? Well, it's easier than doing the ADC. Recall from CSE251, we studied inverting adders. If we simply apply the sinusoidal input to one input of an inverting adder, and a DC voltage of -3 V to another, we can get V'_{in} as in figure 1.13. Thus the full circuit including this adder would be:

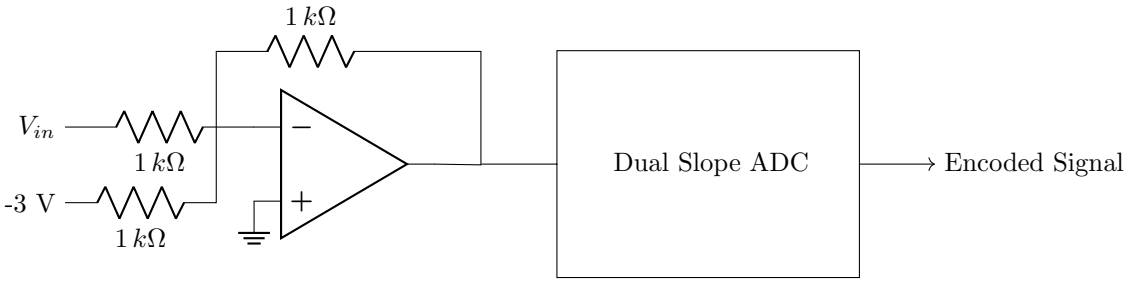


Figure 1.14: Modified Dual Slope ADC for handlinig bipolar input

Notice that we do not need to invert the input sinusoidal signal here, because it is bipolar.
Two important jobs are still to be done. The reference voltage of the Dual Slope ADC also needs to be changed. As the input signal ranges between 0 V to 6 V now, the new reference voltage $V'_{ref} = 6$ V.
Also, we know that the minimum sampling frequency (Nyquist rate) must be twice of the input signal. So, we need to make sure that the maximum sampling rate of the Dual Slope ADC be at least 2 kHz. Thus, we need to modify the clock frequency.

$$\text{Worst conversion time}, t = 2 \times t_1 = 2 \times \frac{256}{f'_{CLK}}$$

$$\therefore f'_{CLK} = \frac{512}{t} = \frac{512}{\frac{1}{f_{Nyquist}}} = \frac{512}{\frac{1}{2\times10^3}} = 1.024\,MHz$$

Problem 5:

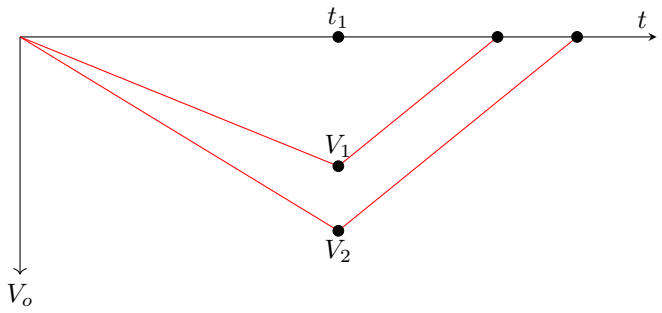


Figure 1.15: Integrator output vs time

For a 6-bit Dual Slope ADC V_1 = -6 V, V_2 = -8 V in figure 1.15 and the maximum allowable sampling frequency is 1.5625 kHz. The time constant τ of the integrator is 0.5 ms.

(a)	Find the two input voltages.
(b)	If the reference voltage is 15 V, find the digital outputs for the inputs found in (a).
(c)	Find the encoded output for which the slope of the integration phase of the integrator would be the average of the two given.

Solution:

(a)

$$V_{in_1} = V_1 \times \frac{RC}{t_1} = -(-6) \times \frac{0.5 \times 10^{-3}}{t_1}$$

Now, worst case conversion time, $2t_1 = \frac{1}{1.5625\times10^3} = 0.64\,ms$, $\therefore t_1 = 0.32\,ms$.

$$\therefore V_{in_1} = \frac{3 \times 10^{-3}}{0.32 \times 10^{-3}} = 9.375V$$

Similarly,

$$V_{in_2} = \frac{-(-8) \times 0.5 \times 10^{-3}}{0.32 \times 10^{-3}} = 12.5V$$

(b)

$$N_1 + 1 = \frac{V_{in_1}}{V_{ref}} \times 2^6 = \frac{9.375}{15} \times 64 = 40 \Rightarrow N_1 = 39$$

$$N_2 + 1 = \frac{V_{in_2}}{V_{ref}} \times 2^6 = \frac{12.5}{15} \times 64 = 53(\text{floored value}) \Rightarrow N_2 = 52$$

$\therefore D_1 =$ binary of $N_1 = 100111$

$\therefore D_2 =$ binary of $N_2 = 110100$

(c) Let slopes of integration for V_{in_1} & V_{in_2} are m_1 & m_2 respectively.

$$m_1 = -\frac{V_{in_1}}{RC} = -\frac{9.375}{0.5} = -18.75\, V/ms$$

$$m_2 = -\frac{V_{in_2}}{RC} = -\frac{12.5}{0.5} = -25\, V/ms$$

$$\therefore m = \frac{m_1 + m_2}{2} = -21.875\, V/ms \Rightarrow -\frac{V_{in}}{RC} = -21.875 \Rightarrow V_{in} = 0.5 \times 21.875 = 10.9375V$$

$$\therefore N + 1 = \frac{V_{in}}{V_{ref}} \times 2^6 = \frac{10.9375}{15} \times 64 = 46(\text{floored value}) \Rightarrow N = 45$$

$\therefore D =$ binary of $45 = 101101$

Problem 6:
If for the 3-bit Flash ADC shown in figure 1.6, V_2 = -1 V and V_6 = 7 V—

(a)	Find the reference voltages V_{ref}^+ & V_{ref}^-.
(b)	What value of offset needs to be added to the input signal, for which the Flash ADC in (a) is designed, so that it can be implemented using an 8-bit Dual Slope ADC with a 2.5 MHz clock? What will be the reference voltage of the Dual Slope ADC?
(c)	Find the average conversion time of the Dual Slope ADC mentioned in (b), for the highest quantization interval in (a).

Solution:

(a) We see in figure 1.6, $V_2 = V_{ref}^- + I \times 1.5R$. Also, $V_6 = V_{ref}^- + I \times 5.5R$.

$$V_{ref}^- + 1.5 \times IR = -1$$

$$V_{ref}^- + 5.5 \times IR = 7$$

Solving the above two equations, $V_{ref}^{-} = -4\,V$, $IR = 2\,V$.

$$V_{ref}^{+} = V_{ref}^{-} + 0.5IR + 6IR + 1.5IR = -4 + 8IR = -4 + 8 \times 2 = 12\,V$$

(b) $V_{offset} = 4\,V$.
$V_{ref} = (V_{ref}^{+} + V_{offset}) = (12 + -4) = 16\,V$

(c) Highest quantization interval in (a): 9 V - 12 V.
Total conversion time for input of 9 V,

$$t_{9\,V} = \frac{2^n}{f_{CLK}} + \frac{9 + V_{offset}}{V_{ref}} \times \frac{2^n}{f_{CLK}} = \frac{2^8}{2.5 \times 10^6}(1 + \frac{9+4}{16}) = 0.1856\,ms$$

Total conversion time for input of 12 V,

$$t_{12\,V} = \frac{2^n}{f_{CLK}} + \frac{12 + V_{offset}}{V_{ref}} \times \frac{2^n}{f_{CLK}} = \frac{2^8}{2.5 \times 10^6}(1 + \frac{12+4}{16}) = 0.2048\,ms$$

Thus, the average conversion time for this quantization interval, $t_{avg} = \frac{0.1856+0.2048}{2} = 0.1952\,ms$

Problem 7: For an 8-bit Dual Slope ADC, the maximum conversion time was found to be $512\,\mu s$.

(a)	Find the clock frequency.
(b)	Find the maximum allowable samplign frequency.
(c)	Find the conversion time for the output '10110110'.

Solution:

(a) We have,

$$2t_1 = 512\,\mu s \Rightarrow 2\frac{2^n}{f_{CLK}} = 512\,\mu s \Rightarrow f_{CLK} = 1\,MHz$$

(b)

$$f_{s_{max}} = \frac{1}{2t_1} = 1953.125\,Hz$$

(c)

$$t_{10110110} = t_1 + t_{2_{10110110}} = 256 + \frac{N+1}{2^n}t_1 = 256 + \frac{182+1}{256}256 = 439\,\mu s$$

Chapter 2

DAC (Digital to Analog Conversion)

DAC is the process of converting a digital signal or bit stream to an analog signal. The whole DAC process can be summarized as follows:

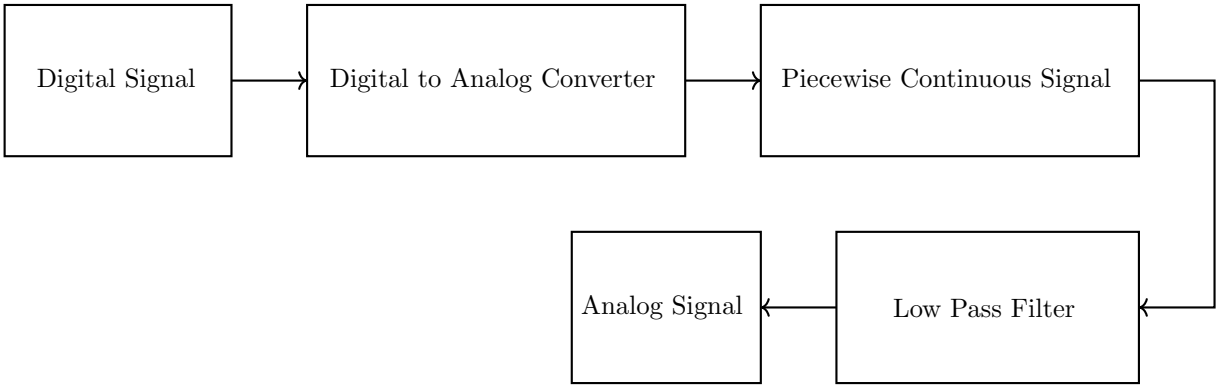


Figure 2.1: A flow chart of DAC process

As like ADC, we will be studying the Digital to Analog Converter in this course. We discuss the following two DACs.

Binary Weighted Resistors (BWR) DAC

A 3-bit Binary Weighted Resistors DAC looks like this:

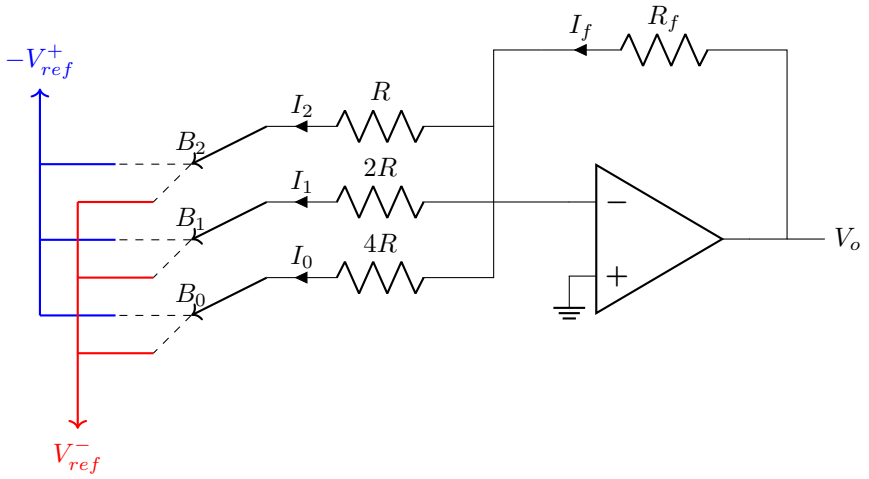


Figure 2.2: A 3-bit Binary Weighted Resistor DAC

As we can see, it is effectively a 3-input *inverting adder*, with different gains on each branches, and the input can switch between two separate reference voltages.

Analysis of Operation: The conversion from digital to analog follows a simple concept of binary to decimal number conversion. We know, that to convert a binary number to its decimal equivalent, we need to multiply each bit with the appropriate power of 2 and then sum the products. The circuit in figure 2.2, is implementing this through its input branches with successively doubled resistors. The switches of the input branches connect to the appropriate reference voltage according to the bit of the digital input signal they represent.

Here, B_2 is the MSB & B_0 is the LSB. Let the currents through the input branches be I_2, I_1 & I_0. While, the current through the feedback resistor, R_f be I_f. As the Op Amp's input terminals are virtually shorted and the non-inverting terminal is grounded, voltage at the inverting terminal, $V_- = 0$ V. Applying KCL at V_- and expressing the currents using Ohm's law,

$$I_f = I_2 + I_1 + I_0 \Rightarrow \frac{V_o - V_-}{R_f} = \frac{V_- - V_{B_2}}{R} + \frac{V_- - V_{B_1}}{2R} + \frac{V_- - V_{B_0}}{4R}$$

$$\Rightarrow V_0 = -\frac{R_f}{R}(V_{B_2} + \frac{V_{B_1}}{2} + \frac{V_{B_0}}{4})$$

As we can see, the contributions to the output voltage of the input branches doubles from LSB to MSB, just like in binary to decimal conversion.

Now, the switches at the inputs function like this— when the input bit is high, it connects to $-V_{ref}^{+}$, and when the bit is low, it connects to V_{ref}^{-}. The idea of two reference voltages for the

two bits (1 & 0) comes from the fact that, each bit represent a certain voltage. As the 3 input branches can all have either 1 or 0 as inputs, we can convert 2^3 digital inputs to analog voltage (V_o). Well, the question is, how do we select these reference voltages?

Let's consider two extreme inputs two answer this. The lowest member of the possible 2^3 input bit streams is the one with all bits set to 0, '000'. So, all input branches will connect to V_{ref}^-. The output voltage for this case is,

$$V_{o_{000}} = -\frac{R_f}{R} \times V_{ref}^-(1 + \frac{1}{2} + \frac{1}{4}) = -\frac{R_f}{R} \times V_{ref}^- \times \frac{7}{4}$$

Similarly, the other extreme input is when all bits are set to 1, '111'. The output voltage for this case can be found in a same manner,

$$V_{o_{111}} = -\frac{R_f}{R} \times -V_{ref}^+ \times \frac{7}{4}$$

If we recall our knowledge on ADC, '000' was used to encode the lowest quantization level, and '111' for the highest level. Thus, we select reference voltages, feedback resistance & branch resistances in accordance with the highest & lowest quantization levels, such that $V_{o_{000}}$ & $V_{o_{111}}$ are equal to them. The outputs of the other inputs then automatically matches with the respective quantization levels.

Some important terminologies & facts of Binary Weighted Resistors DAC:

1. **LSB Voltage and Step Size:** LSB voltage is the output voltage when only the LSB is set to 1 and all other bits are set to 0.

   $$V_{LSB} = V_{o_{001}} = -\frac{R_f}{R}(V_{ref}^- + \frac{V_{ref}^-}{2} + \frac{-V_{ref}^+}{4}) \tag{2.1}$$

   The step size is the difference between two successive quantization levels. So we can write,

   $$\Delta = V_{o_{001}} - V_{o_{000}} = -\frac{R_f}{R}\frac{-V_{ref}^+ - V_{ref}^-}{4} = \frac{R_f}{R}\frac{V_{ref}^+ + V_{ref}^-}{4} \tag{2.2}$$

   However, one thing to note here is that, this equation is *specifically* for a 3-bit DAC. For an **n-bit DAC**, the step size formula can be generalized as follows:

   $$\Delta = \frac{R_f}{R}\frac{V_{ref}^+ + V_{ref}^-}{2^{n-1}} \tag{2.3}$$

2. This DAC only matches the quantization levels for an encoding using *mid-rise* quantization, since the step size is uniform throughout. Try it yourself and verify that any two successive input bit streams' output voltage differ by the same amount.

3. **MSB Voltage:** Just like LSB voltage, MSB voltage is the output voltage when only the MSB is set to 1.

   $$V_{MSB} = V_{o_{100}} = -\frac{R_f}{R}(-V_{ref}^+ + \frac{V_{ref}^-}{2} + \frac{V_{ref}^-}{4}) \tag{2.4}$$

4. One of the disadvantages of Binary Weighted Resistors is that, a lot of different resistors are used. Hence, fluctuations in their values can cause errors in output voltage.

R2R Ladder DAC

Variant 1

To overcome the problem of too many different resistors of the previous DAC, we bring in the R2R Ladder. For a 3-bit input the circuit is shown below:

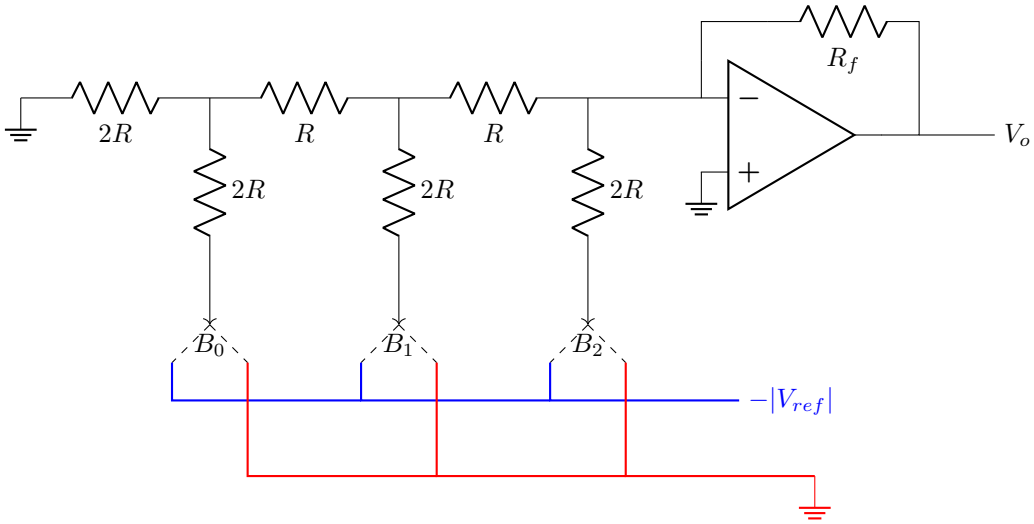


Figure 2.3: A 3-bit R2R Ladder DAC (Variant 1)

Analysis of Operation: A lot of things in figure 2.3 looks familiar, don't they? They function actually the same for this DAC too, as in Binary Weighted Resistors. The main difference here is that the input branches have *the same* resistance, 2R each. Also, there are resistors of value R in between input branches. Finally, after the LSB branch, the ladder ends with a 2R resistor, to the ground. The input branches are like the steps of the ladder like structure. Let's now get mathematical.

To determine the output voltage, we will first find the effects of each input bit branch to the output and then use *superposition* to get their combined effect. Let's start with B_0.

Consider the case when $B_0 = 1$, and the other two bits are 0. The B_0 switch connects to $-|V_{ref}|$, and the other two switches to the ground. Refer to figure 2.4. Since $V_- = 0$ V, the voltage across the 2R resistance in the B_2 branch is 0-0 = 0 V. Thus, no current will flow. Let's perform Node Analysis on nodes n_1 & n_0. For n_0,

$$\frac{V_{n_0} - (-|V_{ref}|)}{2R} + \frac{V_{n_0} - 0}{2R} + \frac{V_{n_0} - V_{n_1}}{R} = 0 \Rightarrow \frac{V_{n_0}}{2} + \frac{V_{n_0} + |V_{ref}|}{2} + V_{n_0} - V_{n_1} = 0$$

For n_1,

$$\frac{V_{n_1} - 0}{2R} + \frac{V_{n_1} - 0}{R} + \frac{V_{n_1} - V_{n_0}}{R} = 0 \Rightarrow \frac{V_{n_1}}{2} + V_{n_1} + V_{n_1} - V_{n_0} = 0$$

Solving the two equations, $V_{n_0} = -\frac{5}{16}|V_{ref}|$, $V_{n_1} = -\frac{1}{8}|V_{ref}|$

Now applying KCL at the inverting terminal,

$$\frac{V_o^0 - 0}{R_f} = \frac{0 - V_{n_1}}{R} \Rightarrow V_o^0 = R_f \times \frac{|V_{ref}|}{8R}$$

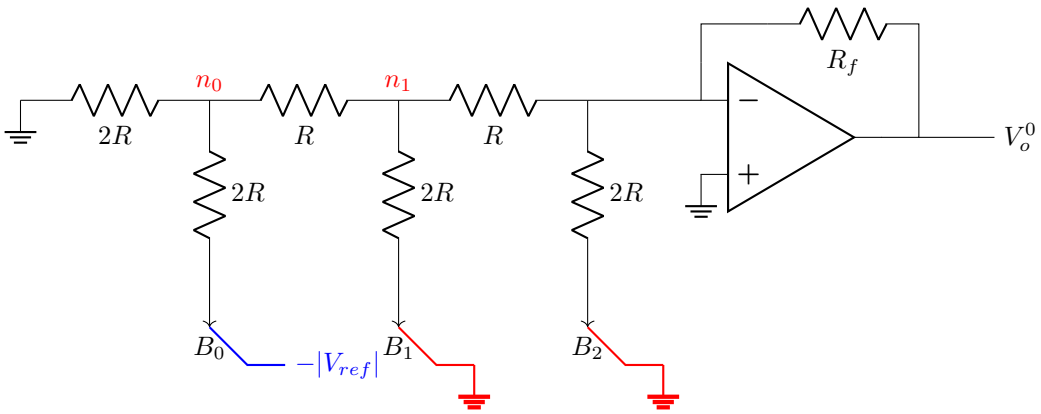


Figure 2.4: Case 001

Similarly for the case when only B_1 is 1:

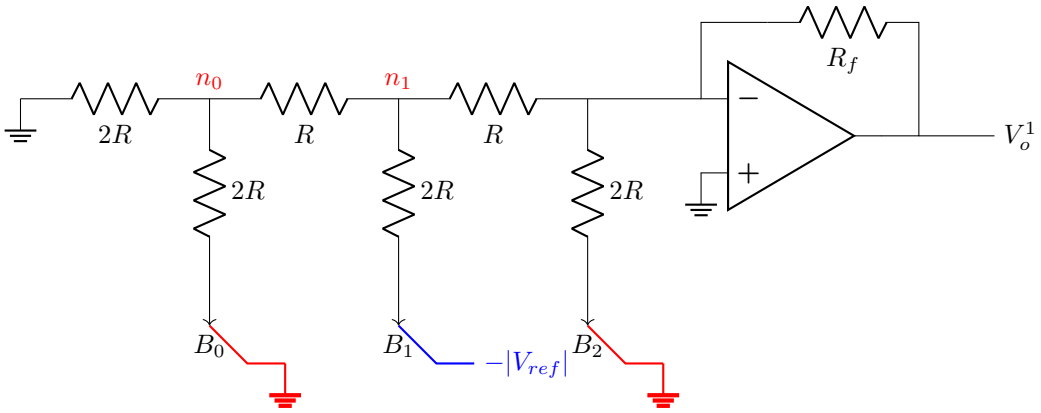


Figure 2.5: Case 010

Again, applying Node Analysis to n_0 & n_1 in figure 2.5, for n_0,

$$\frac{V_{n_0} - 0}{2R} \times 2 + \frac{V_{n_0} - V_{n_1}}{R} = 0$$

For n_1,

$$\frac{V_{n_1} - (-|V_{ref}|)}{2R} + \frac{V_{n_1} - 0}{R} + \frac{V_{n_1} - V_{n_0}}{R} = 0$$

Solving, $V_{n_0} = -\frac{1}{8}|V_{ref}|$, $V_{n_1} = -\frac{1}{4}|V_{ref}|$. Now, applying KCL at the inverting terminal,

$$\frac{V_o^1 - 0}{R_f} = \frac{0 - V_{n_1}}{R} \Rightarrow V_o^1 = R_f \times \frac{|V_{ref}|}{4}$$

Finally for the case when $B_2 = 1$:

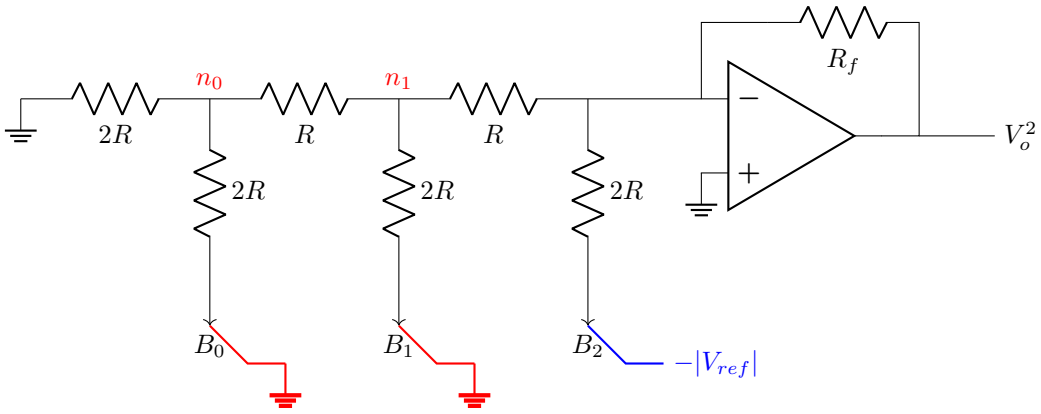


Figure 2.6: Case 100

Node Analysis gives,

$$\frac{V_{n_0} - 0}{2R} \times 2 + \frac{V_{n_0} - V_{n_1}}{R} = 0$$

$$\frac{V_{n_1} - V_{n_0}}{R} + \frac{V_{n_1} - 0}{2R} + \frac{V_{n_1} - 0}{R} = 0$$

Solving, $V_{n_0} = V_{n_1} = 0$. Now applying KCL at the inverting terminal,

$$\frac{V_o^2 - 0}{R_f} = \frac{0 - (-|V_{ref}|)}{2R} \Rightarrow V_o^2 = R_f \times \frac{|V_{ref}|}{2R}$$

One thing to note for this case is that the current through the B_2 branch is not 0 this time since the B_2 switch is connected to $-|V_{ref}|$ instead of ground.

Let's now combine the results using superposition,

$$V_o = V_o^0 + V_o^1 + V_o^2 = \frac{R_f|V_{ref}|}{2R}(B_2 + \frac{B_1}{2} + \frac{B_0}{4})$$

As we can see, the effect of doubled weightage for higher order bits is also effective for this DAC circuit. So, it follows the similar concept of binary to decimal conversion.

Variant 2

Another possible variant of the R2R DAC is shown below:

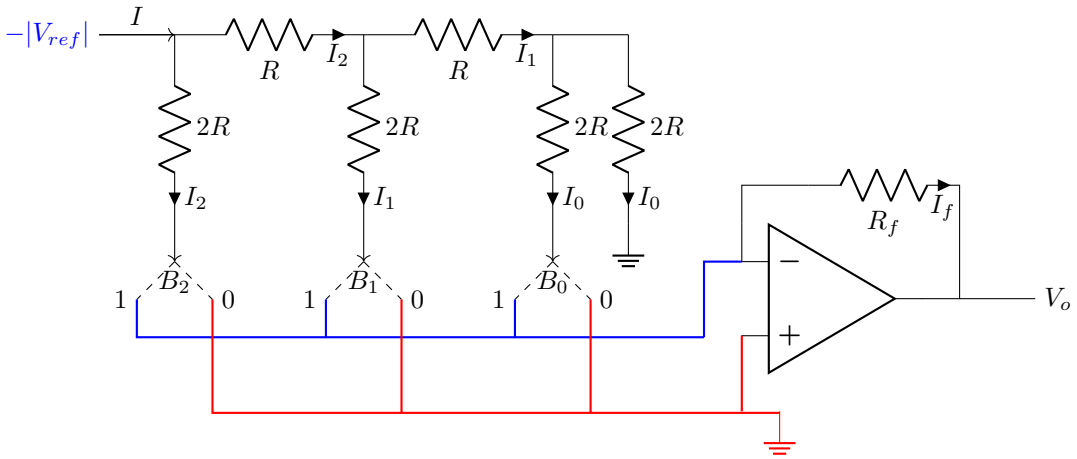


Figure 2.7: A 3-bit R2R Ladder DAC (Variant 2)

One of the main differences of this variant is that the switches connect to ground for both bits (1 & 0). However, these two grounds connect to the two different terminals of the Op Amp. The reference voltage this time is applied in between an R & a 2R valued resistance.

Analysis of Operation: Since the input branches & the rightmost 2R resistance are always grounded at one end irrespective of the inputs to the switches— we can derive the configuration of the resistances in the ladder. Let's start with the rightmost two 2R resistances. They are in parallel combination and their equivalent resistance (let R_{P_1}) is R. Now, R_{P_1} is in series with the rightmost R. Their equivalent will be R+R=2R (let R_{S_1}). R_{S_2} is in parallel with the 2R resistance of input branch B_1. Their equivalent will again be R (let R_{P_2}). The leftmost R & R_{P_2} are in series. For the same reason, their equivalent (let R_{S_2}) will be 2R. Finally, R_{S_2} & the leftmost 2R (of branch B_2) are in parallel.

Now let's verify the currents marked on different branches. We start by assigning notations for the currents of the input branches (I_0 to I_2). Since the two rightmost 2R resistances are in parallel, they will get the same currents through them (I_0). For this very logic the current through (R+R_{S_1}) will also be I_1. And finally, the current through (R+R_{S_2}) will be I_2. Tracing back from the rightmost node using KCL, $I_1 = I_0 + I_0 = 2I_0$. Then, $I_2 = I_1 + I_1 = 2I_1 = 4I_0$. Finally, $I = I_2 + I_2 = 2I_2 = 4I_1 = 8I_0$.

Consider the case when all input bits are high. All the input switches are connected to the inverting terminal of the Op Amp. So, applying KCL at this terminal,

$$I_f = I_2 + I_1 + I_0 = I_2 + \frac{I_2}{2} + \frac{I_2}{4} = \frac{-|V_{ref}| - 0}{2R}(1 + \frac{1}{2} + \frac{1}{4})$$

But $I_f = \frac{0-V_o}{R_f}$. So,

$$-\frac{V_o}{R_f} = -\frac{|V_{ref}|}{2R}(1 + \frac{1}{2} + \frac{1}{4}) \Rightarrow V_o = R_f \frac{|V_{ref}|}{2R}(1 + \frac{1}{2} + \frac{1}{4})$$

Generalizing for both the bits,

$$V_o = R_f \frac{|V_{ref}|}{2R}(B_2 + \frac{B_1}{2} + \frac{B_0}{4}) \tag{2.5}$$

So, we got the same formula for the output voltage. The difference is thus in the structure, not the result.

Important terminologies & facts of R2R Ladder DAC:

1. Uses only two values of resistors— easy and accurate fabrication is possible.
2. Easily scalable to desired number of bits.
3. Unable to convert to bipolar analog signals. Thus requires offset addition after conversion, to achieve bipolarity.
4. **MSB & LSB Voltages:**

$$V_{MSB} = V_{o_{100}} = \frac{R_f|V_{ref}|}{2R}(1 + 0 + 0) = \frac{R_f|V_{ref}|}{2R} \tag{2.6}$$

$$V_{LSB} = V_{o_{001}} = \frac{R_f|V_{ref}|}{2R}(0 + 0 + \frac{1}{4}) = \frac{R_f|V_{ref}|}{8R} \tag{2.7}$$

   The LSB voltage is also the *step size* or Δ.

5. One disadvantage of *variant 2* is that there is always a current flowing through the resistors even if the input bits are 0. This causes more power dissipation.

Formulas Roster		
Binary Weighted Resistors DAC (BWR)		
Topic	**n-bit**	**3-bit**
Output Voltage (V_o)	$V_o = -\frac{R_f}{R}\sum_{i=0}^{n-1}\frac{V_{B_i}}{2^{n-1-i}}$	$V_o = -\frac{R_f}{R}(V_{B_2} + \frac{V_{B_1}}{2} + \frac{V_{B_0}}{4})$
Step Size (Δ)	$\Delta = \frac{R_f}{R}\frac{V_{ref}^+ + V_{ref}^-}{2^{n-1}}$	$\frac{R_f}{R}\frac{V_{ref}^+ + V_{ref}^-}{4}$
LSB Voltage (V_{LSB})	$V_{LSB} = \frac{R_f}{R}(\sum_{i=0}^{n-2}\frac{-V_{ref}^-}{2^i} + \frac{V_{ref}^+}{2^{n-1}})$	$V_{LSB} = \frac{R_f}{R}(-V_{ref}^- + \frac{-V_{ref}^-}{2} + \frac{V_{ref}^+}{4})$
MSB Voltage (V_{MSB})	$V_{MSB} = \frac{R_f}{R}(\sum_{i=1}^{n-1}\frac{-V_{ref}^-}{2^i} + V_{ref}^+)$	$V_{MSB} = \frac{R_f}{R}(V_{ref}^+ + \frac{-V_{ref}^-}{2} + \frac{-V_{ref}^-}{4})$
Input Branch Currents (I_i)	$I_i = -\frac{V_{B_i}}{2^{n-1-i}R}$	$I_2 = -\frac{V_{B_2}}{R}$ $I_1 = -\frac{I_{V_{B_1}}}{2R}$ $I_0 = -\frac{V_{B_0}}{4R}$
R2R Ladder DAC		
Topic	**n-bit**	**3-bit**
Output Voltage (V_o)	$V_o = \frac{R_f\lvert V_{ref}\rvert}{2R}\sum_{i=0}^{n-1}\frac{B_i}{2^{n-1-i}}$	$V_o = \frac{R_f\lvert V_{ref}\rvert}{2R}(B_2 + \frac{B_1}{2} + \frac{B_0}{4})$
Step Size (Δ)	$\Delta = \frac{R_f}{2R}\frac{\lvert V_{ref}\rvert}{2^{n-1}}$	$\Delta = \frac{R_f}{2R}\frac{\lvert V_{ref}\rvert}{4}$
LSB Voltage (V_{LSB})	$V_{LSB} = \frac{R_f}{2R}\frac{\lvert V_{ref}\rvert}{2^{n-1}}$	$V_{LSB} = \frac{R_f}{2R}\frac{\lvert V_{ref}\rvert}{4}$
MSB Voltage (V_{MSB})	$V_{MSB} = \frac{R_f}{2R}\lvert V_{ref}\rvert$	$V_{MSB} = \frac{R_f}{2R}\lvert V_{ref}\rvert$
Input Branch Currents (I_i) (Variant 2)	$-\frac{\lvert V_{ref}\rvert}{2^{n-i}R}$	$I_2 = -\frac{\lvert V_{ref}\rvert}{2R}$ $I_1 = -\frac{\lvert V_{ref}\rvert}{4R}$ $I_0 = -\frac{\lvert V_{ref}\rvert}{8R}$

Problems Roster

Problem 1:

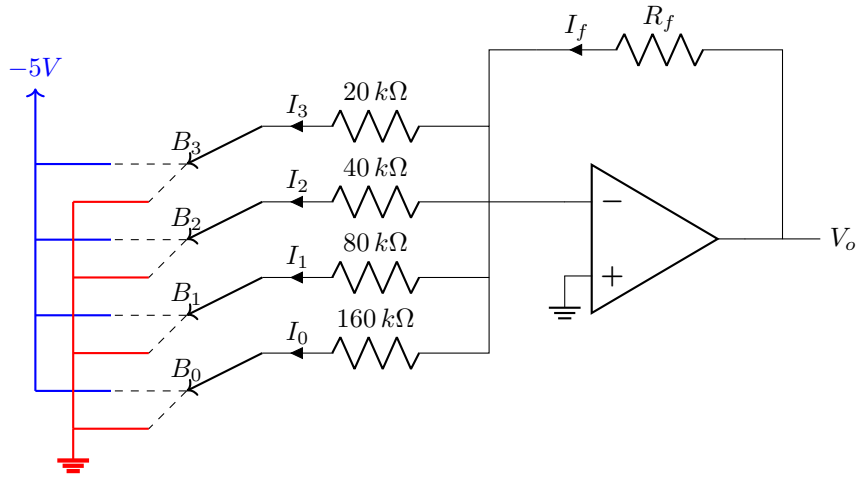


Figure 2.8: A 4-bit Binary Weighted Resistor DAC

For the 4-bit DAC circuit shown in figure 2.8, assume $R_f = 5\,k\Omega$

(a)	Determine the output voltage for the inputs— (i) 1100 (ii) 1010.
(b)	Find the *MSB* & *LSB* voltages. What is the maximum possible output from the DAC?
(c)	What are the values of the input branch currents when they conduct?

Solution:

(a)

(i)

$$V_{o_{1100}} = -\frac{R_f}{R}(-V_{ref}^{+} + \frac{-V_{ref}^{+}}{2} + \frac{V_{ref}^{-}}{4} + \frac{V_{ref}^{-}}{8}) = -\frac{5}{20}(-5 + \frac{-5}{2} + \frac{0}{4} + \frac{0}{8}) = 1.875\,V$$

(ii)

$$V_{o_{1010}} = -\frac{5}{20}(-5 + 0 + \frac{-5}{4} + 0) = 1.5625\,V$$

(b)

$$V_{MSB} = V_{o_{1000}} = -\frac{5}{20}(-5 + 0 + 0 + 0) = 1.25\,V$$

$$V_{LSB} = V_{o_{0001}} = -\frac{5}{20}(0 + 0 + 0 + \frac{-5}{8}) = 0.15625\,V$$

(c) The input branches conduct whenever their respective bits are "1". Thus,

$$I_3 = \frac{0-(-5)}{20} = 0.25\,mA$$

$$I_2 = \frac{0-(-5)}{40} = 0.125\,mA$$

$$I_1 = \frac{0-(-5)}{80} = 0.0625\,mA$$

$$I_0 = \frac{0-(-5)}{160} = 0.03125\,mA$$

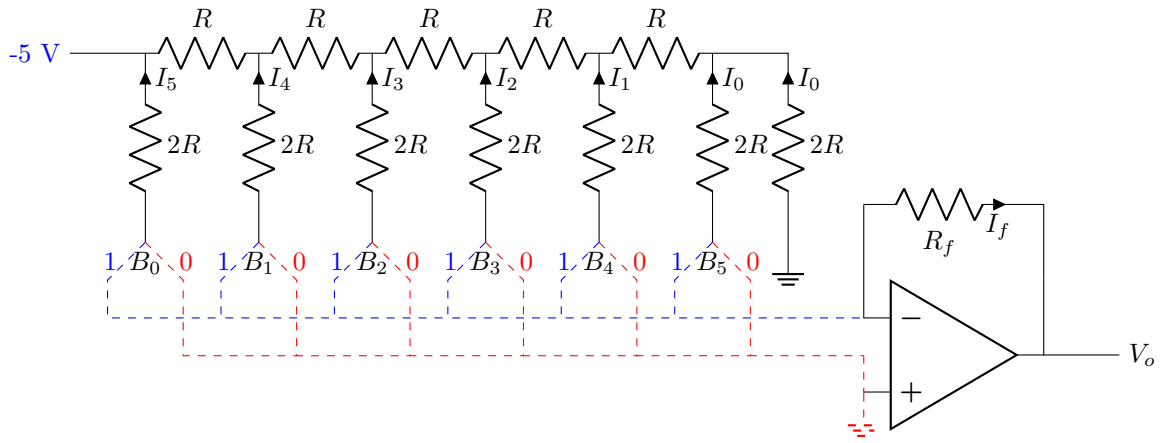
Problem 2:

Consider a 6-bit R2R DAC (variant 2). Assume $R_f = R = 5\,k\Omega$ & $|V_{ref}|$=5 V.

(a)	Draw the DAC circuit with proper labelings.
(b)	Find the input branch currents I_0 to I_5.
(c)	What is the output for the input "010011"? What is the change in output voltage if the input changes from "101010" to "010101".

Solution:

(a)



(b)

$$I_5 = \frac{0-(-5)}{2\times 5} = 0.5\,mA$$

$$I_4 = \frac{1}{2}I_5 = 0.25\,mA$$

$$I_3 = \frac{1}{2}I_4 = 0.125\,mA$$

$$I_2 = \frac{1}{2}I_3 = 0.0625\,mA$$

$$I_1 = \frac{1}{2}I_2 = 0.03125\,mA$$

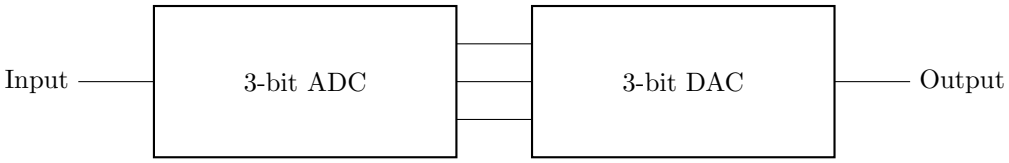
$$I_0 = \frac{1}{2}I_1 = 0.15625\,mA$$

(c)

$$V_{o_{010011}} = \frac{R_f|V_{ref}|}{2R}(0 + \frac{1}{2} + 0 + 0 + \frac{1}{16} + \frac{1}{32}) = \frac{5 \times 5}{2 \times 5} \times \frac{19}{32} = 1.484375\,V$$

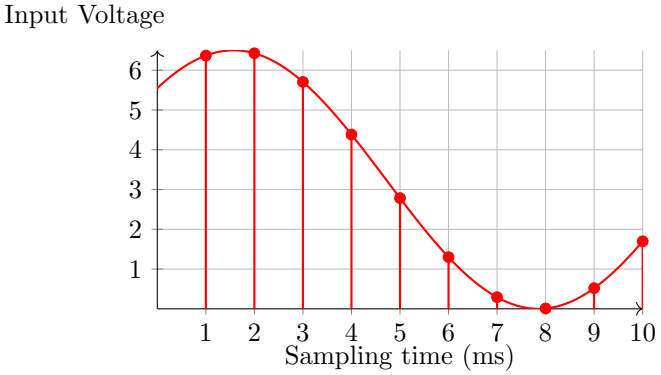
$$\Delta V_o = V_{o_{101010}} - V_{o_{010101}} = \frac{R_f|V_{ref}|}{2R}[(1+0+\frac{1}{4}+0+\frac{1}{16}+0)-(0+\frac{1}{2}+0+\frac{1}{8}+0+\frac{1}{32})] = \frac{5 \times 5}{2 \times 5} \times \frac{21}{32} = 1.640625\,V$$

Problem 3:



ADC Input Voltage	Encoding	DAC Output Voltage
0-1	000	0.5
1-2	001	1.5
2-3	010	2.5
3-4	011	3.5
4-5	100	4.5
5-6	101	5.5
6-7	110	6.5
7-8	111	7.5

(a)	For the following input waveshape, draw the reconstructed output by the DAC. The sampling instances are marked on the input waveshape.
(b)	Comment on the quality of the reconstructed signal and how the quality would be affected if additional bits were used for both the ADC and DAC.

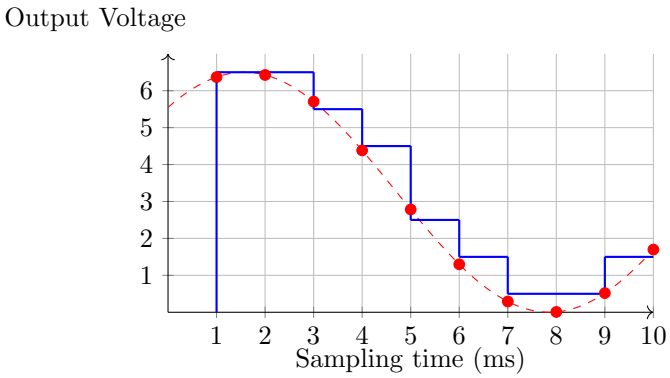


Solution:

(a) Using the table given, let's first find the output voltages for the sampled inputs.

Sampling Instances	Sampled Input	Encoding	DAC Output Voltage
1	6.3	110	6.5
2	6.4	110	6.5
3	5.7	101	5.5
4	4.4	100	4.5
5	2.8	010	2.5
6	1.3	001	1.5
7	0.3	000	0.5
8	0	000	0.5
9	0.5	000	0.5
10	1.7	001	1.5

Reconstructed Signal (in blue):



(b) Reconstructed signal roughly estimates the original input, and the quality is not very good.

Using higher number of bits for both the ADC and DAC will give a better voltage resolution. The reconstructed voltage levels would be closer to that of the originally sampled value.

Problem 4:

Let for a 4-bit BWR DAC, the output of the two inputs '0110' & '1001' are -0.5 V & 2.5 V respectively. Assume $R_f = R$ (MSB branch resistance).

(a)	Find the two reference voltages.
(b)	What are the maximum & minimum values of the actual analog signal?
(c)	If an R2R DAC were to be used instead, what modifications are needed to get the desired quantization levels as output?

Solution:

(a) We have,

$$V_{o_{0110}} = -\frac{R_f}{R}(V_{ref}^- + \frac{-V_{ref}^+}{2} + \frac{-V_{ref}^+}{4} + \frac{V_{ref}^-}{8})$$

$$\Rightarrow -0.5 = 0.75V_{ref}^+ - 1.125V_{ref}^- \tag{2.8}$$

Similarly, for '1001',

$$2.5 = 1.125V_{ref}^+ - 0.75V_{ref}^- \tag{2.9}$$

Solving equations 2.8 & 2.9,

$$V_{ref}^+ = \frac{68}{15}, V_{ref}^- = \frac{52}{15}$$

(b) Step size,

$$\Delta = \frac{V_{ref}^+ + V_{ref}^-}{2^{n-1}} = \frac{\frac{68}{15} + \frac{52}{15}}{2^{4-1}} = 1\,V$$

Now, the *highest* quantization level is the output for the input '1111',

$$V_{o_{1111}} = -\frac{R_f}{R}(-V_{ref}^+ + \frac{-V_{ref}^+}{2} + \frac{-V_{ref}^+}{4} + \frac{-V_{ref}^+}{8}) = V_{ref}^+(1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}) = \frac{68}{15} \times \frac{15}{8} = 8.5$$

Similarly, the *lowest* quantization level is the output for the input '0000',

$$V_{o_{0000}} = -\frac{R_f}{R}(V_{ref}^- + \frac{V_{ref}^-}{2} + \frac{V_{ref}^-}{4} + \frac{V_{ref}^-}{8}) = -\frac{52}{15} \times \frac{15}{8} = -6.5\,V$$

Now, we know, these quantization levels are the midpoints of respective quantization intervals. So, the maximum value of the actual analog signal should be $\frac{\Delta}{2}$ higher than the highest quantization level.

$$\therefore V_{max} = V_{o_{1111}} + \frac{\Delta}{2} = 8.5 + \frac{1}{2} = 9\,V$$

Similarly, the minimum value of the actual analog signal, should be $\frac{\Delta}{2}$ lower than the lowest quantization level.

$$\therefore V_{min} = V_{o_{0000}} - \frac{\Delta}{2} = -6.5 - \frac{1}{2} = -7\,V$$

(c) The quantization levels have both positive & negative values. This cannot be produced by the R2R DAC, since it can only produce outputs of a certain polarity (either all positives or all negatives). So, we can produce a shifted version of the quantization levels using the R2R DAC, then we can obtain the actual quantization levels by subtracting the shifted amount from the output of the DAC.

The lowest quantization level we found in (b) was -6.5 V & the highest was 8.5 V. So, the range of outputs from the BWR DAC was [-6.5,8.5]. So, the shifted version of this range, which can be generated from the R2R DAC would be [0,8.5+6.5] or [0,15], with a shift amount of 6.5 V.

In that case, the reference voltage for the R2R DAC would be, 15 V. Then we must subtract the shift amount (6.5 V) from the output of the R2R DAC. The whole modified process would be as follows:

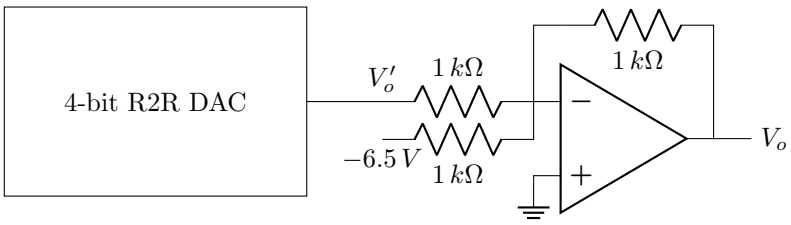


Figure 2.9: Modifications for handling bipolar quantization levels in an R2R DAC

As we can see in figure 2.8, the output V_o' from the 4-bit R2R DAC, is fed to an inverting adder with the voltage -6.5 V. The output from the adder, V_o is thus,

$$V_o = -(\frac{1}{1}V_o' + \frac{1}{1} \times -6.5) = -(V_o' - 6.5)$$

Here, the output range of V_o' is [0,15]. Thus, the output range of $V_o' - 6.5$ is [-6.5,8.5]. So, V_o is just the inverted version of our desired output. We can simply take it in an inverted manner to deal with this reversed nature.

Problem 5:

Let a sender wishes to convert the analog signal $3.5 + 4cos(\omega t)$ in a digital signal, and then transmit it to a receiver. The receiver will then back convert the received digital signal into an analog signal. But the receiver has a 3-bit R2R DAC, for which $R_f = R = 2\,k\Omega$.

(a)	What should be the value of reference voltage for the receiver's DAC?
(b)	If the output from the DAC of the receiver at a certain instant is '3 V', what are the possible values of the input sampled value at the sender's end?
(c)	Calculate the step size of the DAC.

Solution:

(a) The minimum & maximum value of the input analog signal at the sender's end is $3.5 - 4 = -0.5$ & $3.5 + 4 = 7.5$ respectively. Considering mid-rise quantization, the quantization levels & encoded outputs for the ADC of this signal would be:

Quantization Levels	Encoded Outputs
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Thus, the highest quantization interval is 6.5 V. This should be the output from the receiver's DAC for the input '111'. So, using the output voltage formula of R2R DAC,

$$V_{o_{111}} = \frac{R_f |V_{ref}|}{2R}(1 + \frac{1}{2} + \frac{1}{4}) \Rightarrow 7 = \frac{|V_{ref}|}{2} \times \frac{7}{4}$$

$$\Rightarrow |V_{ref}| = 8\,V$$

(b) From the table in (a), we see, the quantization level 3 was encoded into '011'. Thus, this should be the input at the receiver's DAC for an output of 3 V.

(c)

$$\Delta = \frac{R_f}{2R}\frac{|V_{ref}|}{2^{n-1}} = \frac{1}{2}\frac{8}{2^{3-1}} = 1\,V$$

Chapter 3

Schmitt Trigger

Review of Op Amp

We will need to recall our knowledge from CSE251 on Op Amps first. Op Amps operate in two modes: i) Open Loop ii) Closed loop. In open loop configuration, it behaves as a comparator, and as we have said it in multiple occasions, it outputs the high bias voltage when $V_+ > V_-$ & low bias voltage in the opposite scenario. Now let's review the behaviors of an Op Amp with feedback.

In **negative feedback**, an important characteristics of the Op Amp is that its terminals are virtually shorted. Meaning, $V_+ = V_-$. This is *not* the case in positive feedback though. In positive feedback the Op Amps behave as comparators too. However, due to its feedback configuration, we get a special type of comparators. Let us observe the VTC (Voltage Transfer Characteristics) of an Op Amp in different configurations first.

VTC of an Op Amp in Open Loop Configuration:

1. **Input applied to inverting terminal:**

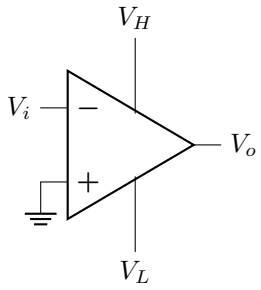


Figure 3.1: Op Amp as a comparator with input at inverting terminal

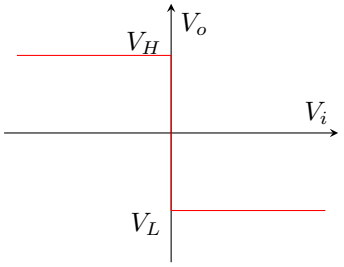


Figure 3.2: VTC of an inverting comparator when non-inverting terminal is grounded

When there is a **non-zero** (assuming positive value) reference voltage applied to the non-inverting terminal:

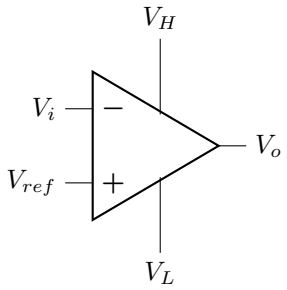


Figure 3.3: Op Amp as a comparator with input at inverting terminal with applied reference voltage

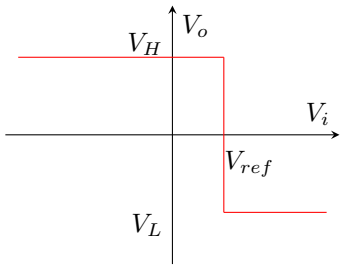


Figure 3.4: VTC of an inverting comparator when a non-zero reference is applied to the non-inverting

The condition of the above two comparators are $V_i < 0$ & $V_i < V_{ref}$ respectively.

2. **Input applied to non-inverting terminal:**

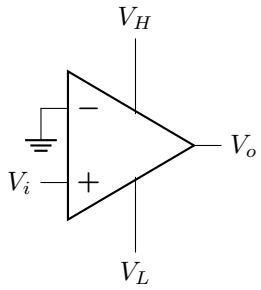


Figure 3.5: Op Amp as a comparator with input at non-inverting terminal

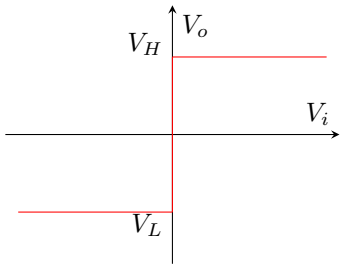


Figure 3.6: VTC of a non-inverting comparator when inverting terminal is grounded

When there is a **non-zero** (assuming positive value) reference voltage applied to the non-inverting terminal:

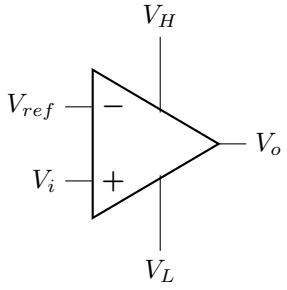


Figure 3.7: Op Amp as a comparator with input at non-inverting terminal with applied reference voltage

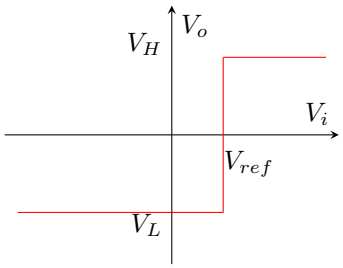


Figure 3.8: VTC of a non-inverting comparator when a non-zero reference voltage is applied to the inverting terminal

The condition of the above two comparators are $V_i > 0$ & $V_i >> V_{ref}$ respectively.

All the four cases above produces output on the basis of the principle if $V_+ > V_-$ then $V_o = V_H$, otherwise, $V_o = V_L$. If we want a bit of control on the VTCs, alongside the option to change the reference voltage, then we can implement the following methods:

3. **Comparator with resistive tuning of reference voltage:**

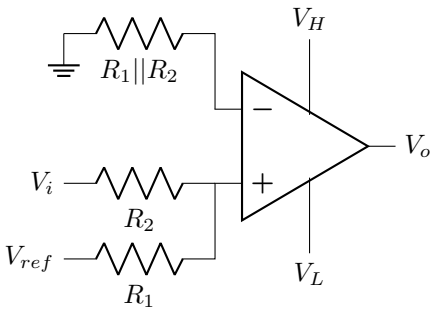


Figure 3.9: Op Amp as a comparator with input at non-inverting terminal with applied reference voltage & resistive tuning

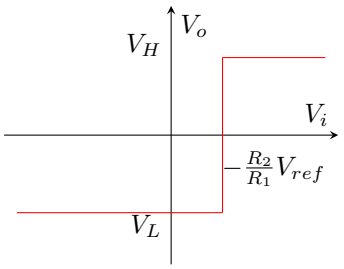


Figure 3.10: VTC of a non-inverting comparator when a non-zero reference voltage is applied to the inverting terminal (with resistive tuning)

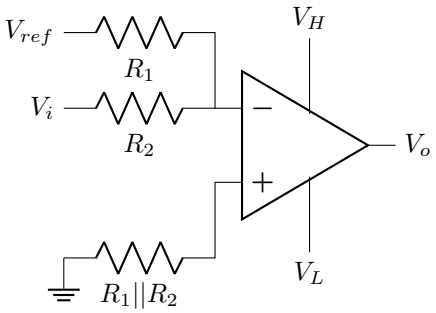


Figure 3.11: Op Amp as a comparator with input at non-inverting terminal with applied reference voltage & resistive tuning

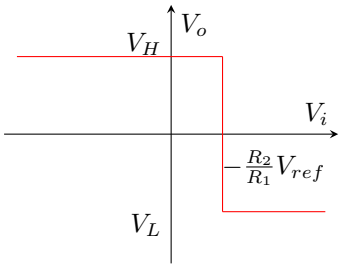


Figure 3.12: VTC of an inverting comparator when a non-zero reference voltage is applied to the non-inverting terminal (with resistive tuning)

Here, the condition for switching of output voltage from one bias voltage to the other is not simple as before. To get this relation, we need to find the voltage of the two terminals. This is because, they are not simply the input or reference voltage as like before. Also, the main condition remains the same ($V_+ > V_-$ leads to $V_o = V_H$ and V_L otherwise).

In both cases, the terminal other than the one at which the input & reference voltage are being applied, is grounded through a resistance of the value $R_1||R_2$. Since the Op Amp terminals don't draw any current, there is no voltage drop across this resistance. Thus, we can say that in both cases, the voltage of this terminal is 0 V. To find the voltage of the terminal at which the input & reference are being applied, we have to apply KCL at that

terminal. For the case in figure 3.9, we can write using KCL at the non-inverting terminal,

$$\frac{V_+ - V_i}{R_2} + \frac{V_+ - V_{ref}}{R_1} = 0 \Rightarrow V_+ = \frac{R_1}{R_1 + R_2} V_i + \frac{R_2}{R_1 + R_2} V_{ref}$$

Replacing this expression of V_+ in the condition of the comparator,

$$V_+ > V_- \Rightarrow \frac{R_1}{R_1 + R_2} V_i + \frac{R_2}{R_1 + R_2} V_{ref} > 0 \Rightarrow V_i > -\frac{R_2}{R_1} V_{ref}$$

For the case in figure 3.11, $V_+ = 0\,V$. Applying KCL at the inverting terminal,

$$\frac{V_- - V_i}{R_1} + \frac{V_- - V_{ref}}{R_2} = 0 \Rightarrow V_- = \frac{R_1}{R_1 + R_2} V_i + \frac{R_2}{R_1 + R_2} V_{ref}$$

Again, replacing this in the condition,

$$V_+ > V_- \Rightarrow 0 > \frac{R_1}{R_1 + R_2} V_i + \frac{R_2}{R_1 + R_2} V_{ref} \Rightarrow V_i < -\frac{R_2}{R_1} V_{ref}$$

We are done for the moment with open loop Op Amps. As we now go in to discussing Op Amps with feedbacks, the knowledge on open loop comparators shown above will help greatly. If we summarize the outcome of the discussions on open loop operation of Op Amps, there can be *two* types of comparators— **inverting & non-inverting**. It all depends on which terminal the input is being applied to.

Schmitt Triggers

They are just Op Amps with positive feedbacks which act like comparators. The difference is that due to the feedback network, the switching of the output voltage between the two bias voltages do not just occur at a single value. Rather, there are two thresholds (high, V_{TH} & low, V_{TL}). Depending on which terminal the input is being applied, there can also be two types of Schmitt Triggers— inverting & non-inverting. Also, like the open loop, there is option to use a reference voltage.

Without Applied Reference Voltage:

1. **Inverting Schmitt Trigger:**

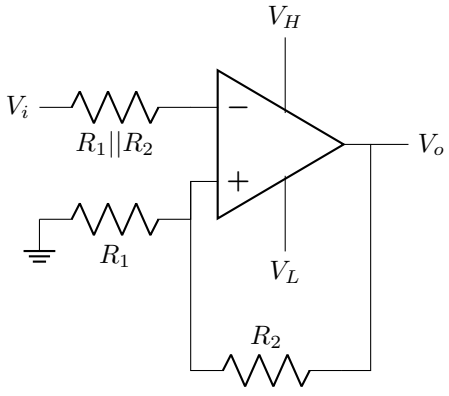


Figure 3.13: An Inverting Schmitt Trigger without reference voltage

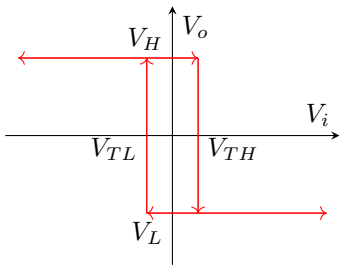


Figure 3.14: VTC of an Inverting Schmitt Trigger (without applied reference voltage)

As we can see in figure 3.14, the output voltage can change at two values of the input. These are called the *thresholds* of the Schmitt Trigger. This occurs due to the feedback network, which makes the next output voltage of the Op Amp to depend on its previous output too, alongside the present input. Let's explain how.

Suppose, the output voltage initially was V_H. This a possible output if either the input voltage was *lower* than V_{TL}, or, between the two thresholds. If indeed it was the first case, then if the input increases beyond V_{TL} now, but does not yet exceed V_{TH}, then the output will *not* change to V_L. It will only switch to V_H if the input crosses V_{TH}. Now suppose the input was in between the two thresholds. This can lead to $V_o = V_H$ *only* if the output was previously high. It is not possible for the Op Amp to switch to V_H from V_L, unless the input goes lower than V_{TL}. Thus, for input in between thresholds, the output of the Schmitt Trigger depends on the previous output.

A similar analysis can be done for the case when the output voltage is V_L. The summary of the operation of inverting Schmitt Trigger is as follows:

If $V_i > V_{TH}$ then $V_o = V_L$

If $V_i < V_{TL}$ then $V_o = V_H$

If $V_{TL} < V_i < V_{TH}$ then $V_o = V_H$ if the previous output $= V_H$ otherwise $V_o = V_L$

We now wish to determine the expressions of V_{TH} & V_{TL} in terms of circuit parameters. If we observe figure 3.13, as Op Amps don't draw current, we can say $V_- = V_i$. Now applying KCL at the non-inverting terminal,

$$\frac{V_+ - V_o}{R_2} + \frac{V_+ - 0}{R_1} = 0 \Rightarrow V_+ = \frac{R_1}{R_1 + R_2} V_o$$

We need to know a previous value of V_o to predict the current result. Assuming V_o was previously high (V_H), the next switching of V_o will occur when $V_+ < V_-$ (output of a comparator goes low if this happens). Thus, the marginal point is when $V_+ = V_- = V_i = V_{TH}$ (from the VTC). We have,

$$\frac{R_1}{R_1 + R_2} V_o = V_i \Rightarrow V_{TH} = \frac{R_1}{R_1 + R_2} V_H \tag{3.1}$$

A similar analysis with the initial assumption of $V_o = V_L$, we can find the value of V_{TL}. The switching from V_L to V_H occurs when $V_i = V_{TL}$. And this time $V_+ = \frac{R_1}{R_1+R_2} V_o = \frac{R_1}{R_1+R_2} V_L$. We thus have,

$$V_{TL} = \frac{R_1}{R_1 + R_2} V_L \tag{3.2}$$

2. **Non-Inverting Schmitt Trigger:**

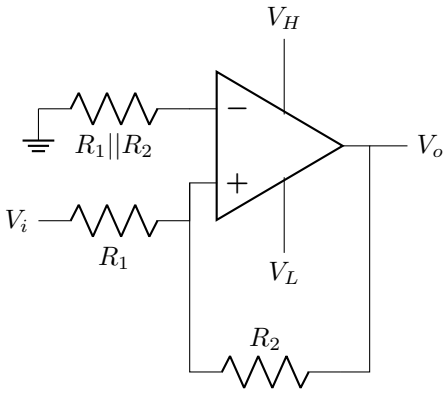


Figure 3.15: A Non-Inverting Schmitt Trigger without reference voltage

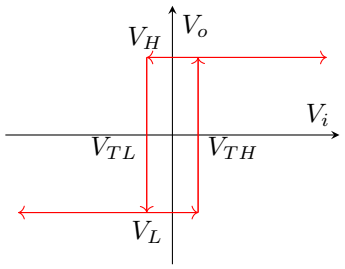


Figure 3.16: VTC of a Non-Inverting Schmitt Trigger (without applied reference voltage)

The difference here is that the input is applied at the non-inverting terminal through R_1. The inverting terminal is grounded throught the parallel equivalent resistance. Thus, $V_- = 0\,V$. To find V_+, we apply KCL at the non-inverting terminal.

$$\frac{V_+ - V_i}{R_1} + \frac{V_+ - V_o}{R_2} = 0 \Rightarrow V_+ = \frac{R_2}{R_1 + R_2} V_i + \frac{R_1}{R_1 + R_2} V_o$$

Now, from the VTC in figure 3.16, we see that if $V_o = V_L$ initially, then it will switch to V_H if V_i crosses V_{TH}. Considering the marginal case,

$$V_+ = V_- \Rightarrow \frac{R_2}{R_1 + R_2} V_i + \frac{R_1}{R_1 + R_2} V_o = 0 \Rightarrow \frac{R_2}{R_1 + R_2} V_{TH} = -\frac{R_1}{R_1 + R_2} V_L$$

$$\Rightarrow V_{TH} = -\frac{R_1}{R_2} V_L \tag{3.3}$$

Again, from the VTC in figure 3.16, if the initial output was V_H, then it would switch to V_L when V_i falls lower than V_{TL}. Thus we have,

$$\frac{R_2}{R_1 + R_2} V_{TL} = -\frac{R_1}{R_1 + R_2} V_H \Rightarrow V_{TL} = -\frac{R_1}{R_2} V_H \tag{3.4}$$

Till now, the Schmitt Triggers we have studied have the property that the threshold voltages depend solely on the circuit parameters, bias voltages and resistances. These offer seldom flexibility and scope of tuning. If we want more control on our thresholds, we need to apply an external reference voltage just like in figures 3.9 & 3.11.

With Applied Reference Voltage:

1. **Inverting Schmitt Trigger with Reference Voltage:**

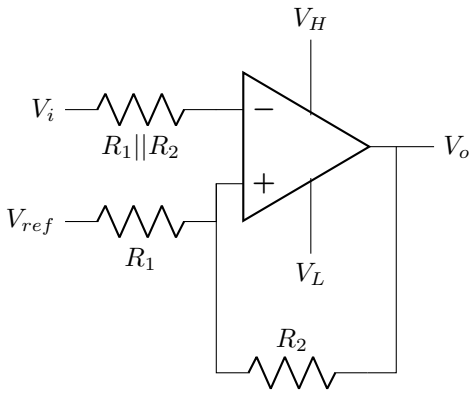


Figure 3.17: An Inverting Schmitt Trigger with reference voltage

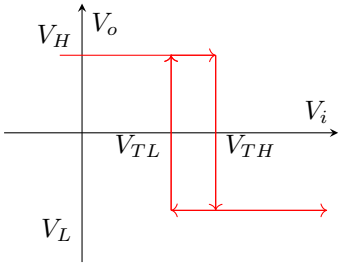


Figure 3.18: VTC of an Inverting Schmitt Trigger (with applied reference voltage)

As we can see, the inverting nature of the VTC is still the same. The change is that the whole VTC has shifted along the V_i axis. Let's find the new values of the thresholds.

Like before, $V_- = V_i$. Applying KCL at the non-inverting terminal,

$$\frac{V_+ - V_{ref}}{R_1} + \frac{V_+ - V_o}{R_2} = 0 \Rightarrow V_+ = \frac{R_1}{R_1 + R_2} V_o + \frac{R_2}{R_1 + R_2} V_{ref}$$

Assuming $V_o = V_H$ initially, the output will switch when V_i crosses the new V_{TH}. Thus,

$$V_+ = V_- \Rightarrow \frac{R_1}{R_1 + R_2} V_o + \frac{R_2}{R_1 + R_2} V_{ref} = V_i$$

$$\Rightarrow V_{TH} = \frac{R_1}{R_1 + R_2} V_H + \frac{R_2}{R_1 + R_2} V_{ref} \tag{3.5}$$

If we compare equation 3.5 with equation 3.1, we see that the change in the value of V_{TH} is $\frac{R_2}{R_1+R_2} V_{ref}$. A similar analysis assuming $V_o = V_L$ initially gives,

$$V_{TL} = \frac{R_1}{R_1 + R_2} V_L + \frac{R_2}{R_1 + R_2} V_{ref} \tag{3.6}$$

Comparing 3.6 with 3.2, we see the same amount of shift in its value. This amount of shift is known as ***Shift Voltage***, V_S. So,

$$V_S = \frac{R_2}{R_1 + R_2} V_{ref} \tag{3.7}$$

The VTC of the Inverting Schmitt Trigger has been shifted by an amount as indicated in 3.7 due to the application of a reference voltage.

2. **Non-Inverting Schmitt Trigger with Reference Voltage:**

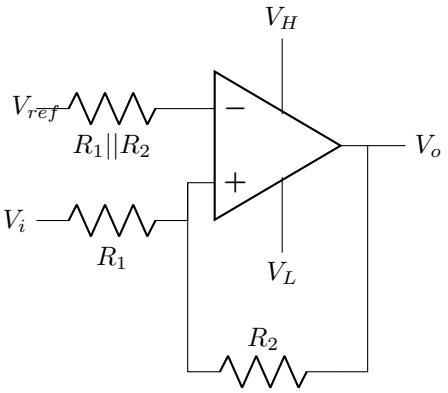


Figure 3.19: A Non-Inverting Schmitt Trigger with reference voltage

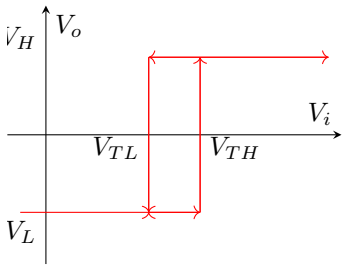


Figure 3.20: VTC of a Non-Inverting Schmitt Trigger (without applied reference voltage)

A similar analysis for figure 3.19, would give the shifted thresholds for this Non-Inverting Schmitt Trigger with applied reference voltage. For this circuit, we see, $V_- = V_{ref}$. Applying KCL at the non-inverting terminal,

$$\frac{V_+ - V_i}{R_1} + \frac{V_+ - V_o}{R_2} = 0 \Rightarrow V_+ = \frac{R_2}{R_1 + R_2} V_i + \frac{R_1}{R_1 + R_2} V_o$$

Now, assuming initially the output was V_L, it will switch to V_H when $V_i = V_{TH}$. Considering the marginal condition,

$$V_+ = V_- \Rightarrow \frac{R_2}{R_1 + R_2} V_i + \frac{R_1}{R_1 + R_2} V_o = V_{ref}$$

$$\Rightarrow \frac{R_2}{R_1 + R_2} V_{TH} + \frac{R_1}{R_1 + R_2} V_L = V_{ref} \Rightarrow V_{TH} = -\frac{R_1}{R_2} V_L + \frac{R_1 + R_2}{R_2} V_{ref} \tag{3.8}$$

Similarly, assuming the initial output to be V_H, we can find V_{TL}—

$$\frac{R_2}{R_1 + R_2} V_{TL} + \frac{R_1}{R_1 + R_2} V_H = V_{ref}$$

$$\Rightarrow V_{TL} = -\frac{R_1}{R_2} V_H + \frac{R_1 + R_2}{R_2} V_{ref} \tag{3.9}$$

Thus, the *shift voltage* for Non-inverting Schmitt Trigger with applied reference voltage is,

$$V_S = \frac{R_1 + R_2}{R_2} V_{ref} \tag{3.10}$$

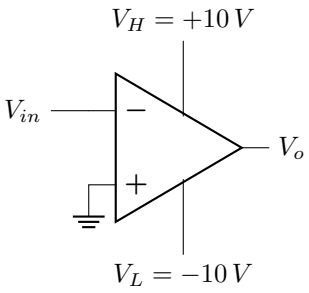
Now let's talk about some applications & facts of Schmitt Trigger.

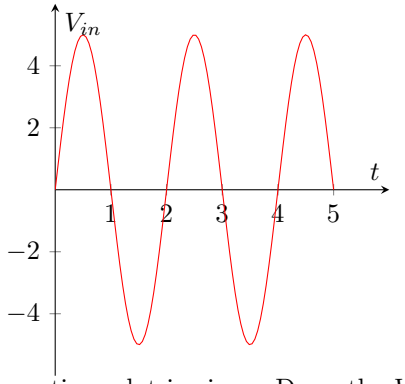
1. **Hysteresis Width:** For *all* the Schmitt Triggers shown till now, Hysteresis Width is the difference between the two thresholds. So, $V_h = V_{TH} - V_{TL}$.
2. Schmitt Triggers are just enhanced comparators with memory. They operate on the basis of both current input & past output state.
3. Some notable applications of Schmitt Trigger are— noise reduction, level detection based control systems.

Formulas Roster	
Topic	**Formula**
Inverting Comparator with Resistive Tuning	
Condition of Output Voltage	$V_i < -\frac{R_2}{R_1}V_{ref} \Rightarrow V_o = V_H$ $V_i > -\frac{R_2}{R_1}V_{ref} \Rightarrow V_o = V_L$
Non-Inverting Comparator with Resistive Tuning	
Condition of Output Voltage	$V_i > -\frac{R_2}{R_1}V_{ref} \Rightarrow V_o = V_H$ $V_i < -\frac{R_2}{R_1}V_{ref} \Rightarrow V_o = V_L$
Inverting Schmitt Trigger without Reference Voltage	
Thresholds	$V_{TH} = \frac{R_1}{R_1+R_2}V_H$ $V_{TL} = \frac{R_1}{R_1+R_2}V_L$
Non-Inverting Schmitt Trigger without Reference Voltage	
Thresholds	$V_{TH} = -\frac{R_1}{R_2}V_L$ $V_{TL} = -\frac{R_1}{R_2}V_H$
Inverting Schmitt Trigger with Reference Voltage	
Thresholds	$V_{TH} = \frac{R_1}{R_1+R_2}V_H + \frac{R_2}{R_1+R_2}V_{ref}$ $V_{TL} = \frac{R_1}{R_1+R_2}V_L + \frac{R_2}{R_1+R_2}V_{ref}$
Shift Voltage	$V_s = \frac{R_2}{R_1+R_2}V_{ref}$
Non-Inverting Schmitt Trigger with Reference Voltage	
Thresholds	$V_{TH} = -\frac{R_1}{R_2}V_L + \frac{R_1+R_2}{R_2}V_{ref}$ $V_{TL} = -\frac{R_1}{R_2}V_H + \frac{R_1+R_2}{R_2}V_{ref}$
Shift Voltage	$V_s = \frac{R_1+R_2}{R_2}V_{ref}$
General Topics for All Schmitt Triggers	
Hysteresis Width	$V_h = V_{TH} - V_{TL}$

Problems Roster

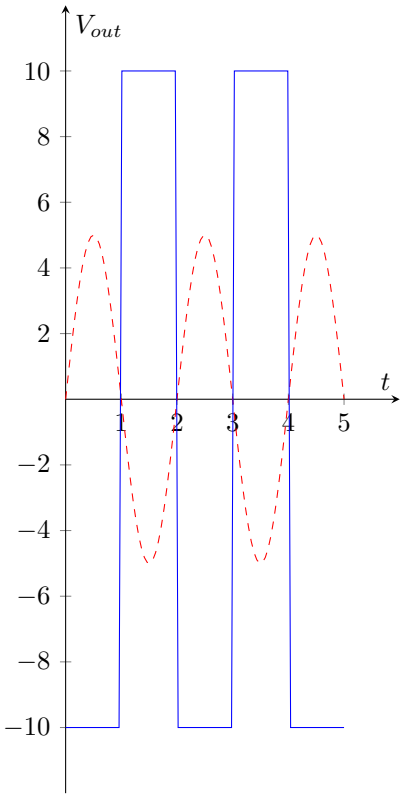
Problem 1:



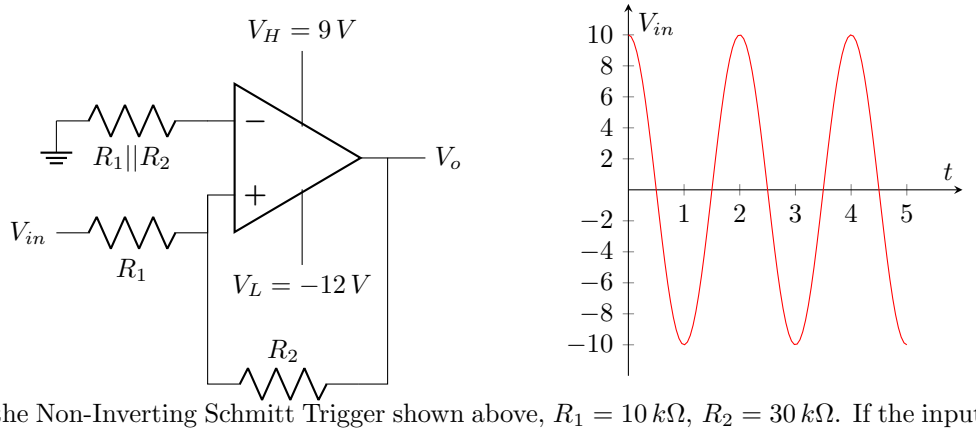


For the Op Amp Comparator circuit given above, the V_{in} vs time plot is given. Draw the V_{out} vs time plot for the given input.

Solution:



Problem 2:



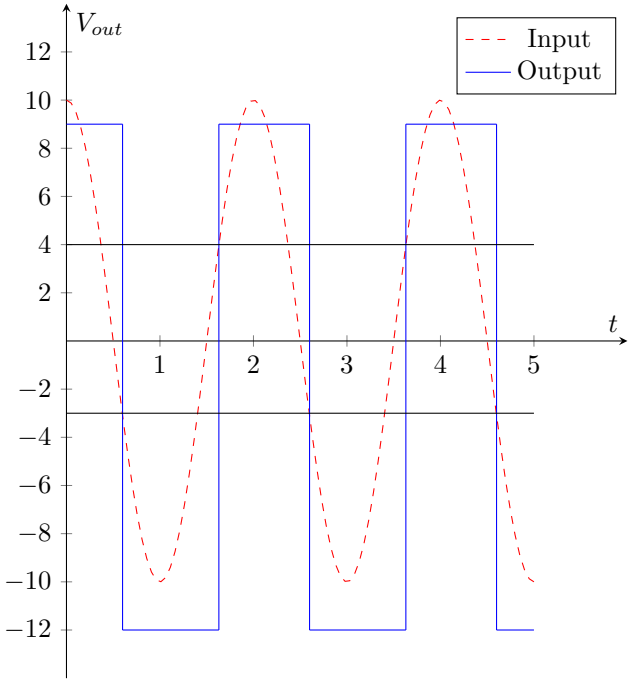
For the Non-Inverting Schmitt Trigger shown above, $R_1 = 10\,k\Omega$, $R_2 = 30\,k\Omega$. If the input signal shown is applied to the Schmitt Trigger, draw the output.

Solution:

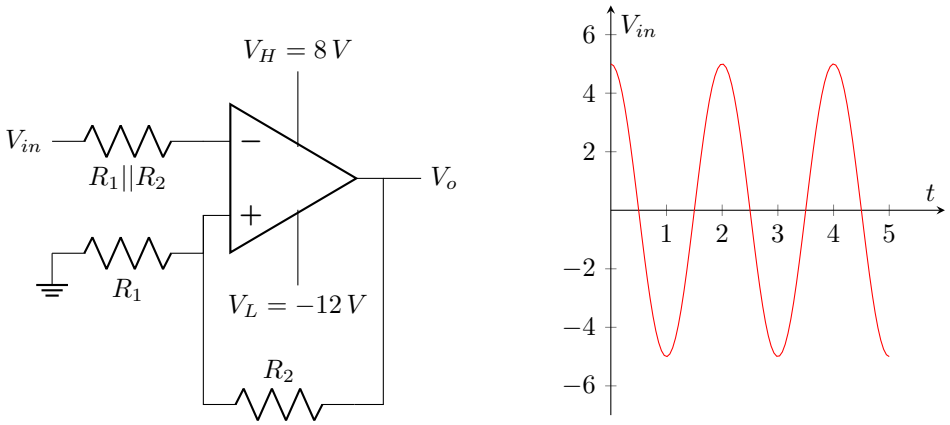
Calculation of Thresholds:

$$V_{TH} = -\frac{R_1}{R_2}V_L = -\frac{10}{30}(-12) = 4\,V$$

$$V_{TL} = -\frac{R_1}{R_2}V_H = -\frac{10}{30}(9) = -3\,V$$



Problem 3:



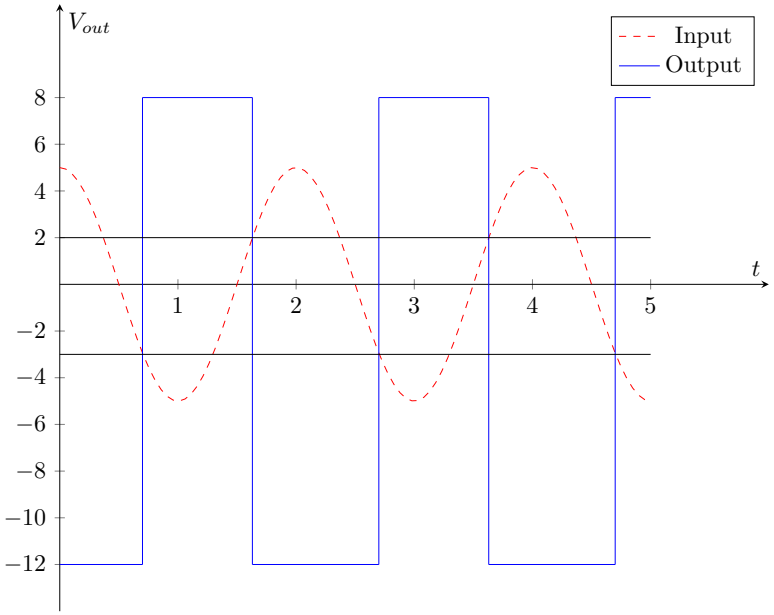
For the Inverting Schmitt Trigger shown above, $R_1 = 10\,k\Omega$, $R_2 = 30\,k\Omega$. If the input signal shown is applied to the Schmitt Trigger, draw the output.

Solution:

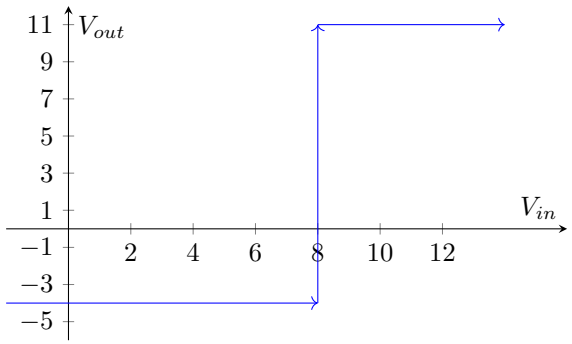
Calculation of Thresholds:

$$V_{TH} = \frac{R_1}{R_1 + R_2} V_H = \frac{10}{10 + 30}(8) = 2\,V$$

$$V_{TL} = \frac{R_1}{R_1 + R_2} V_H = \frac{10}{10 + 30}(-12) = -3\,V$$



Problem 4:

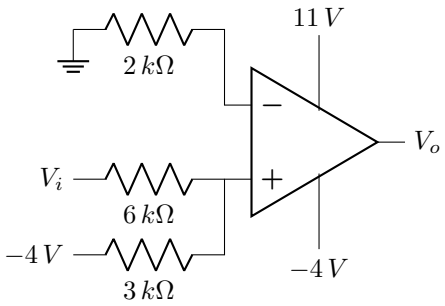


For the VTC given, design a comparator with a reference voltage of -4 V.

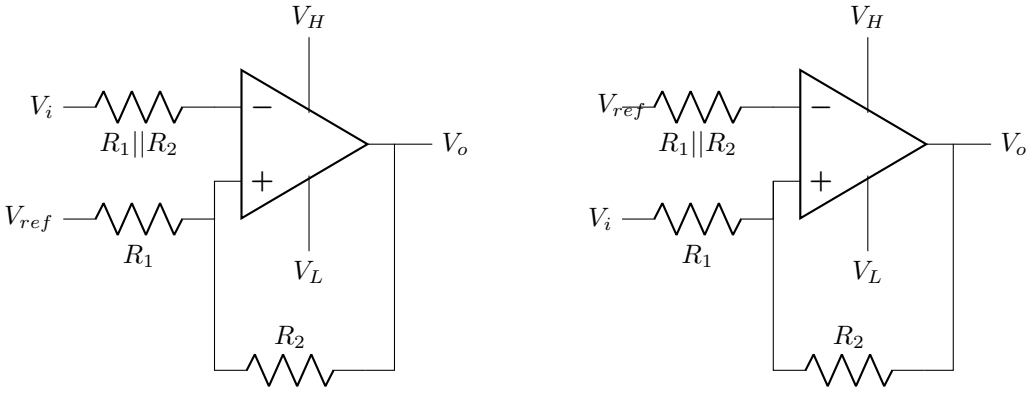
Solution:
We know, for a Non-Inverting Comparator with resistive tuning, $V_+ > -\frac{R_2}{R_1}V_{ref}$ results in $V_o = V_H$. From the given VTC, $V_H = 11\,V$, $V_L = -4\,V$. Now since $V_{ref} = -4\,V$,

$$-\frac{R_2}{R_1}V_{ref} = 8 \Rightarrow \frac{R_2}{R_1} = \frac{8}{4} = 2 \Rightarrow R_2 = 2R_1$$

Thus a possible design would be:



Problem 5:



For the above two Schmitt Triggers, $R_1 = 5\,k\Omega \quad R_2 = 20\,k\Omega, \quad V_{ref} = 3\,V, \quad V_H = 12\,V, \quad V_L = -10\,V$.

(a)	Find the threshold voltages.
(b)	Find the hysteresis widths & shift voltages.
(c)	Draw their VTCs.

Solution:

(a) For the inverting Schmitt Trigger,

$$V_{TH} = \frac{R_1}{R_1 + R_2} V_H + \frac{R_2}{R_1 + R_2} V_{ref} = \frac{5}{5+20} 12 + \frac{20}{20+5} 3 = 4.8\,V$$

$$V_{TL} = \frac{R_1}{R_1 + R_2} V_L + \frac{R_2}{R_1 + R_2} V_{ref} = \frac{5}{5+20} (-10) + \frac{20}{20+5} 3 = 0.4\,V$$

For the non-inverting Schmitt Trigger,

$$V_{TH} = -\frac{R_1}{R_2} V_L + \frac{R_1 + R_2}{R_2} V_{ref} = -\frac{5}{20} (-10) + \frac{5+20}{20} 3 = 6.25\,V$$

$$V_{TL} = -\frac{R_1}{R_2} V_H + \frac{R_1 + R_2}{R_2} V_{ref} = -\frac{5}{20} (12) + \frac{5+20}{20} 3 = 0.75\,V$$

(b) For the inverting Schmitt Trigger,

$$V_H = V_{TH} - V_{TL} = 4.8 - 0.4 = 4.4\,V$$

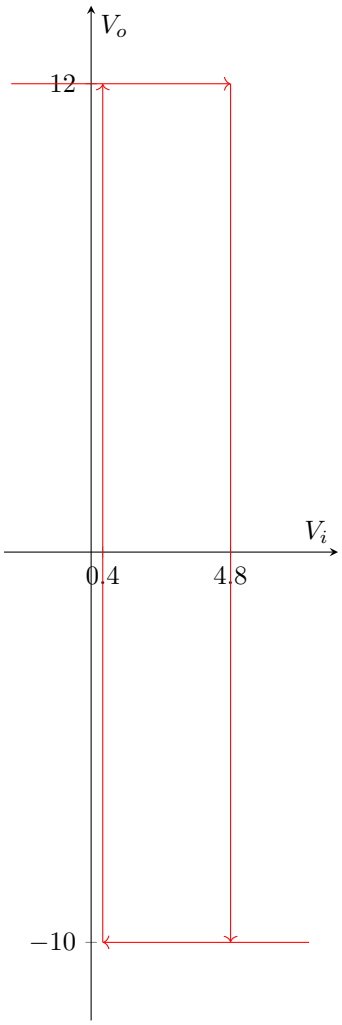
$$V_S = \frac{R_2}{R_1 + R_2} V_{ref} = 2.4\,V$$

For the non-inverting Schmitt Trigger,

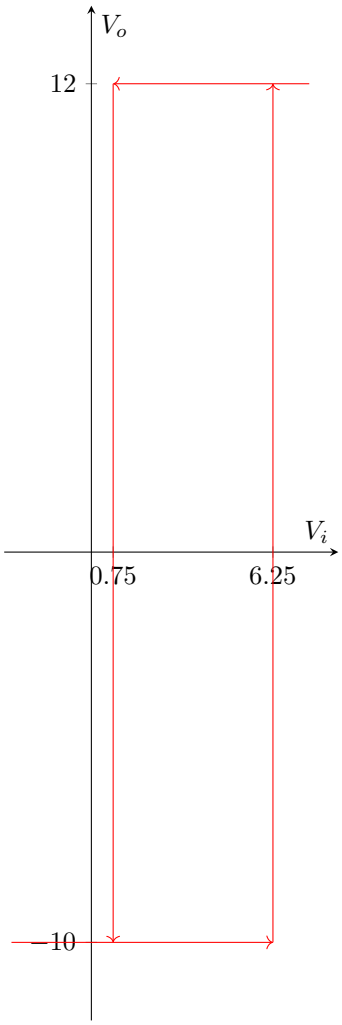
$$V_H = V_{TH} - V_{TL} = 6.25 - 0.75 = 5.5\,V$$

$$V_S = \frac{R_1 + R_2}{R_2} V_{ref} = 3.75\,V$$

(c)

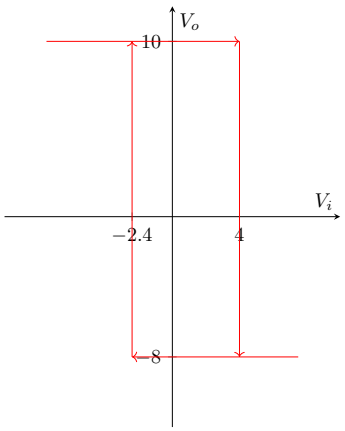


Inverting Schmitt Trigger



Non-Inverting Schmitt Trigger

Problem 6:



For the VTC given—

(a)	Find the shift voltage.
(b)	If $R_1 = 2\,k\Omega$, design the Schmitt Trigger circuit.

Solution:

(a) From the VTC, $V_H = 10\,V, \quad V_L = -8\,V, \quad V_{TH} = 4\,V, \quad V_{TL} = -2.4\,V$. Now,

$$V_{TH} = \frac{R_1}{R_1 + R_2} V_H + V_S \Rightarrow 4 = 10k + V_S [\text{Let } \frac{R_1}{R_1 + R_2} = k]$$

$$V_{TL} = kV_L + V_S \Rightarrow -2.4 = -8k + V_S$$

Solving the above two equations, $V_S = \frac{4}{9}\,V, \quad k = \frac{16}{45}$

(b) From (a),

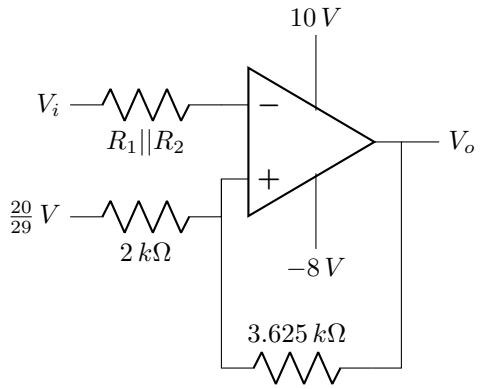
$$k = \frac{16}{45} \Rightarrow \frac{R_1}{R_1 + R_2} = \frac{16}{45} \Rightarrow \frac{2}{2 + R_2} = \frac{16}{45}$$

$$\Rightarrow R_2 = 3.625\,k\Omega$$

Now, $V_S = \frac{R_2}{R_1 + R_2} V_{ref}$. So,

$$\frac{4}{9} = \frac{3.625}{2 + 3.625} V_{ref} \Rightarrow V_{ref} = \frac{20}{29}\,V$$

Thus, the designed Schmitt Trigger will be:


10 V
V_i
R_1||R_2
V_o
20/29 V
2 kΩ
−8 V
3.625 kΩ

Chapter 4

Signal Generators

Square Wave Generator

A square wave is a *periodic* wave that has two distinct and fixed levels, and oscillates between these two values. They do not necessarily have to be of opposite polarity. The amount of time allocated for the two levels may also vary. A few examples are as follows:

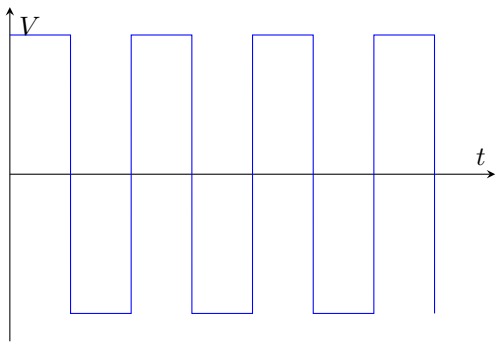


Figure 4.1: A symmetric square wave

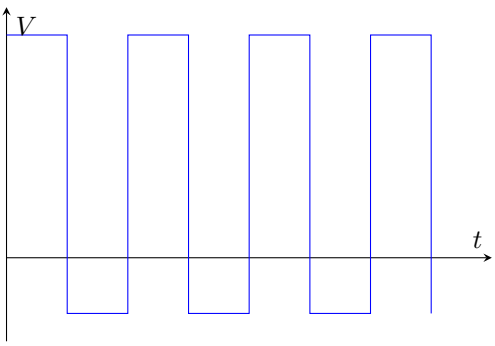


Figure 4.2: A square wave with offset

Now, to produce such a signal, we first need two distinct voltage levels. Can you recall any such components that only outputs two voltages? Yes, it's the Op Amp, when acting as a comparator or Schmitt Trigger. Which one should we use? Well, as we can see in the above figures, we need switching between the voltage levels at multiple instances, which means varying thresholds. So, the comparator is not of much use here. We will need to use the Schmitt Trigger, but with some modifications. One of the terminal voltage needs to oscillate between the thresholds, so that we get switching between V_H & V_L at the output. Let's see the circuit without further trailers.

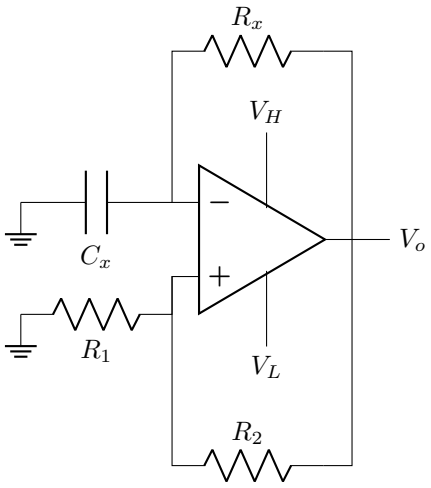


Figure 4.3: A Square Wave Generator

Although the circuit in figure 4.3 seem to have both feedback networks, the output behaviour is dictated by the positive feedback. Hence, it is effectively an *inverting Schmitt Trigger*. The input voltage of it is the voltage across the capacitor C_x. Let's now see in details how does this produce a square wave.

Analysis of Operation: Since no current is drawn at any terminals of the Op Amp, we can isolate the negative feedback network and perform a separate analysis. It is an *RC circuit* as shown below:

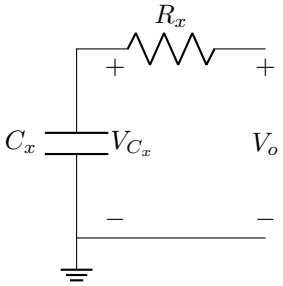


Figure 4.4: RC circuit of the negative feedback network

Since the output voltage, V_o has only two possible distinct DC values (V_H & V_L), the RC circuit in figure 4.4 will always have a DC voltage applied across it, irrespective of the value of V_o.

Now recall from CSE250, for a simple series RC circuit, if a DC voltage of V_s is applied, the voltage response of the capacitor is as follows:

$$V_c(t) = V_s + [V_c(t_i) - V_s]e^{-\frac{t-t_i}{\tau}}$$

For our circuit in figure 4.4, we can write,

$$V_{C_x} = V_o + [V_{C_x}(t_i) - V_o]e^{-\frac{t-t_i}{\tau}} \tag{4.1}$$

Here, $\tau = R_x C_x$

We have already said that due to positive feedback, the output voltage can only have the values V_H & V_L. And since it's an inverting Schmitt Trigger, assuming V_o to be V_H initially, it will switch from V_H to V_L, when the inverting terminal voltage rises above V_{TH}. Let the switching instant is T_1. Also, we may assume the initial voltage across the capacitor to be V_{TL}. Since this is the highest possible value up to which the output would stay V_L. So, basically we are considering the starting point of our analysis the moment when the output has just switched

from V_L to V_H because the capacitor has reached V_{TL}. Assuming $t_i = 0$, these informations can be put together in equation 4.1 in the following manner:

$$V_{TH} = V_H + [V_{TL} - V_H]e^{-\frac{T_1 - 0}{R_x C_x}}$$

$$\Rightarrow e^{-\frac{T_1}{R_x C_x}} = \frac{V_{TH} - V_H}{V_{TL} - V_H} \Rightarrow -\frac{T_1}{R_x C_x} = ln(\frac{V_{TH} - V_H}{V_{TL} - V_H})$$

$$\Rightarrow T_1 = R_x C_x ln(\frac{V_{TL} - V_H}{V_{TH} - V_H}) = R_x C_x ln(\frac{V_{TL} - V_H}{V_{TH} - V_H}) \tag{4.2}$$

Let's get a visual representation of what has happened till now.

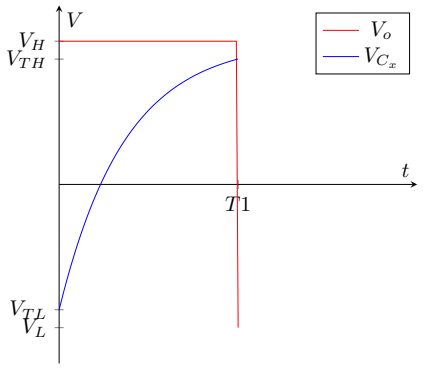


Figure 4.5: Response of Square Wave Generator(half period)

Does figure 4.5 ring any bell? The output voltage has covered the half period of a square wave. At T_1, V_o has switched to V_L since, the inverting terminal input, V_{C_x} has reached V_{TH}. Let's complete our analysis for the second half.

The next switching will occur when V_{C_x} reaches V_{TL} again. Then the output will switch back to V_H. Let this happens at $t = T_1 + T_2$. Using equation 4.1, we can write,

$$V_{TL} = V_L + [V_{TH} - V_L]e^{-\frac{T_1 + T_2 - T_1}{R_x C_x}}$$

$$\Rightarrow e^{-\frac{T_2}{R_x C_x}} = \frac{V_{TL} - V_L}{V_{TH} - V_L} \Rightarrow -\frac{T_2}{R_x C_x} = ln(\frac{V_{TL} - V_L}{V_{TH} - V_L})$$

$$\Rightarrow T_2 = R_x C_x ln(\frac{V_{TH} - V_L}{V_{TL} - V_L}) \tag{4.3}$$

Now let's complete our square wave:

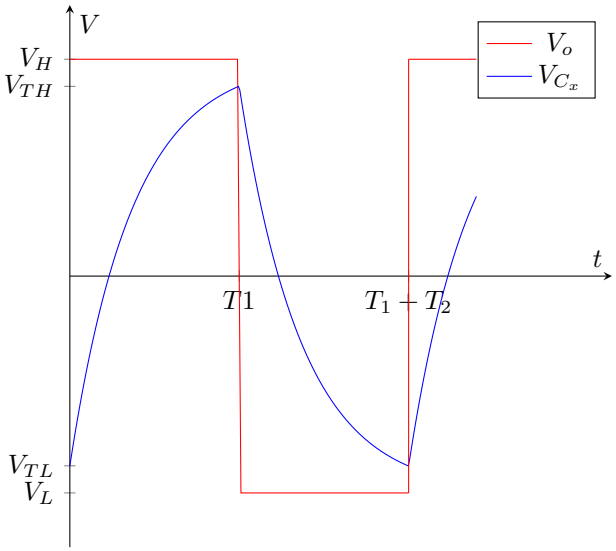


Figure 4.6: Response of Square Wave Generator

Thus, the capacitor voltage V_{C_x} oscillates between V_{TL} & V_{TH} and the output voltage changes accordingly between V_L & V_H. The result is the square wave with high peak of V_H and low peak of V_L.
Some important parameters & facts of Square Wave Generator:

1. **Time Period:** The time period of the generated square wave is $T = T_1 + T_2$.
2. **Duty Cycle:** Duty cycle for the square wave is considered to be the fraction of the period it attains the high peak. Thus,

$$D = \frac{T_1}{T_1 + T_2} \times 100 \tag{4.4}$$

3. From the default circuit in figure 4.2, it is an inverting Schmitt Trigger without any applied reference voltage. Thus, its thresholds will be, $V_{TH} = \frac{R_1}{R_1+R_2}V_H$ & $V_{TL} = \frac{R_1}{R_1+R_2}V_L$.
4. To get a **50%** duty cycle, we need $T_1 = T_2$. For that to happen,

$$R_xC_xln\left(\frac{V_{TL} - V_H}{V_{TH} - V_H}\right) = R_xC_xln\left(\frac{V_{TH} - V_L}{V_{TL} - V_L}\right)$$

$$\Rightarrow \frac{V_{TL} - V_H}{V_{TH} - V_H} = \frac{V_{TH} - V_L}{V_{TL} - V_L} \quad \Rightarrow \quad \frac{\left(\frac{R_1}{R_1+R_2}V_L\right) - V_H}{\left(\frac{R_1}{R_1+R_2}V_H\right) - V_H} = \frac{\left(\frac{R_1}{R_1+R_2}V_H\right) - V_L}{\left(\frac{R_1}{R_1+R_2}V_L\right) - V_L}$$

$$\Rightarrow \frac{\frac{R_1}{R_1+R_2}V_L - V_H}{V_H} = \frac{\frac{R_1}{R_1+R_2}V_H - V_L}{V_L}$$

$$\Rightarrow \frac{R_1}{R_1+R_2}\left(\frac{V_L}{V_H} - \frac{V_H}{V_L}\right) = 0 \Rightarrow |V_H| = |V_L|$$

Triangular Wave Generator

Like the square wave, a triangular wave also has two peaks. However, it switches between these two peaks with a finite slope, unlike the vertical switching of the square wave.

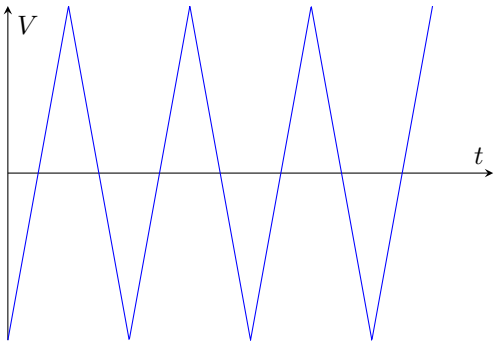


Figure 4.7: A symmetric triangular wave

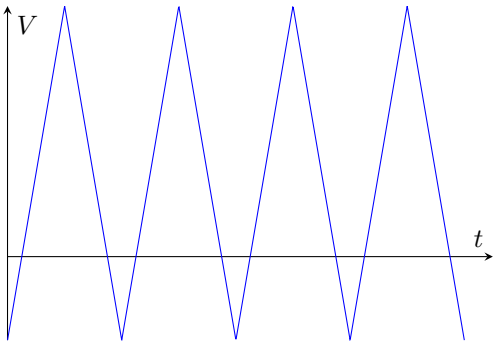


Figure 4.8: A triangular wave with offset

So, how do we generate such signals? The straight forward answer is by integrating a square wave. How? Well, we know that the integral of a constant value is a straight line with a slope proportional to that value. Sounds tough to understand? Just have a look below:

$$\int c\,dx = cx$$

Since the square wave is made up of two constant peaks, they intigrate to straight lines proportional to their peaks. So, do we simply pass the output of our previously studied square wave generator to an integrator? Well, we can, but there is a better method. Let's look at the better circuit, the triangular wave generator:

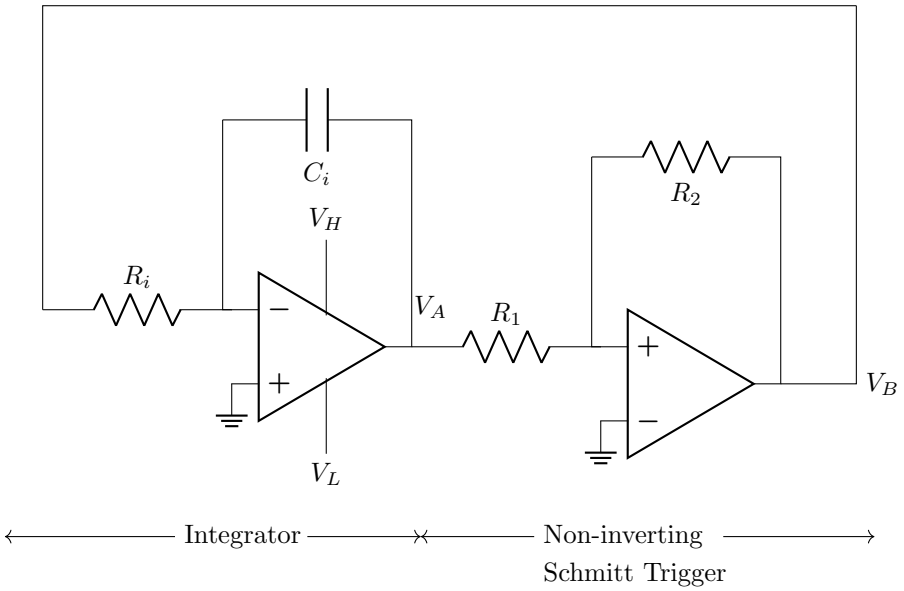


Figure 4.9: A Triangular Wave Generator

As we can see, an integrator's output is fed to a non-inverting Schmitt Trigger. The Schmitt Trigger's output is also fed back to the integrator. Let's go in details.

Analysis of Operation: The output of the non-inverting Schmitt Trigger is either V_H or V_L. Thus, the integrator gets constant inputs in both cases. We have already discussed the integrator's output formula in Dual Slope ADC. So, we can write,

$$V_A = -\frac{1}{R_i C_i}\int_{t_i}^{t} V_B\, dt + V_A(t_i)$$

Let's consider the case when the initial output from the Schmitt Trigger is V_H. The output of the Schmitt Trigger switches to V_H from V_L when the input equals V_{TH}. Thus, for this initial case, we may assume that the integrator's output has just reached V_{TH}, and caused the Schmitt Trigger to switch its output to V_H. So, $V_B = V_H$, $V_A(t_i) = V_{TH}$. Assuming $t_i = 0$,

$$V_A = -\frac{1}{R_i C_i}\int_{0}^{t} V_H\, dt + V_{TH} \Rightarrow V_A = -\frac{1}{R_i C_i} V_H t + V_{TH}$$

This is a straight line with a slope of $-\frac{V_H}{R_i C_i}$, and a y-axis intercept of V_{TH}. Let after time T_1, it reduces to V_{TL} from V_{TH}, due to the negative slope. We get,

$$V_{TL} = -\frac{V_H}{R_i C_i} T_1 + V_{TH} \Rightarrow T_1 = R_i C_i \frac{V_{TH} - V_{TL}}{V_H} = \tau \frac{V_{TH} - V_{TL}}{V_H} \tag{4.5}$$

The graphical view of the incidents till now would be as follows:

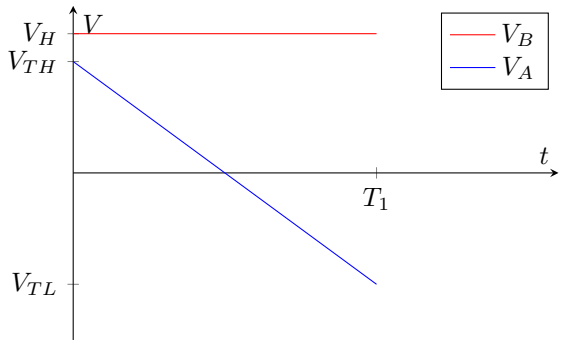


Figure 4.10: Triangular Wave Generator Responses (first half)

Now that the output of the integrator (i.e. the input to the Schmitt Trigger) is V_{TL}, the output of the Schmitt Trigger will switch to V_L. This causes the slope of the integrator to change—

$$V_A = -\frac{1}{R_i C_i}\int_{T_1}^{t} V_L\, dt + V_A(T_1) \Rightarrow V_A = -\frac{V_L}{R_i C_i}(t - T_1) + V_{TL}$$

This is a positive slope, because V_L is usually negative. So, now the output of the integrator will rise from V_{TL} to V_{TH}, and throughout the output from the Schmitt Trigger will remain V_L. Let the output from the integrator reaches V_{TH} again at $t = T$, where $T - T_1 = T_2$. Then we have,

$$V_{TH} = -\frac{V_L}{R_i C_i}(T - T_1) + V_{TL} \Rightarrow T_2 = R_i C_i \frac{V_{TL} - V_{TH}}{V_L} = \tau \frac{V_{TL} - V_{TH}}{V_L} \tag{4.6}$$

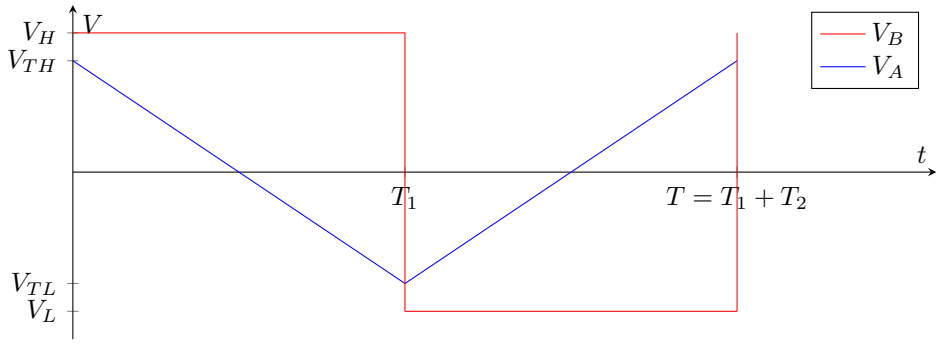


Figure 4.11: Triangular Wave Generator Responses (full)

Thus, the output from the integrator is the triangular wave. To summarize, the output of the integrator changes linearly between V_{TH} & V_{TL}, which in turn causes the non-inverting Schmitt Trigger to periodically change its output between V_H & V_L.

Some important facts and terminologies regarding Triangular Wave Generators:

1. **Duty Cycle:** Unlike the square wave, the duty cycle for a triangular wave is the fraction of time its slope remains positive. So,

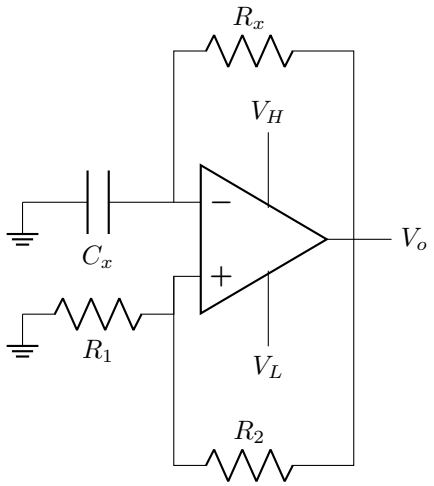
$$D = \frac{T_2}{T_1 + T_2} \times 100 \tag{4.7}$$

2. Since the Schmitt Trigger used is non-inverting, its thresholds will be, $V_{TH} = -\frac{R_1}{R_2} V_L$ & $V_{TL} = -\frac{R_1}{R_2} V_H$.
3. We can use the output of the non-inverting Schmitt Trigger as a square wave as well.

Formulas Roster	
Topic	**Formula**
Square Wave Generator	
Higher Peak Duration	$T_1 = R_x C_x \ln\left(\frac{V_{TL} - V_H}{V_{TH} - V_H}\right)$
Lower Peak Duration	$T_2 = R_x C_x \ln\left(\frac{V_{TH} - V_L}{V_{TL} - V_L}\right)$
Time Constant	$\tau = R_x C_x$
Duty Cycle	$D = \frac{T_1}{T_1 + T_2} \times 100$
Triangular Wave Generator	
Negative Slope Duration	$T_1 = R_i C_i \left(\frac{V_{TH} - V_{TL}}{V_H}\right)$
Positive Slope Duration	$T_2 = R_i C_i \left(\frac{V_{TL} - V_{TH}}{V_L}\right)$
Time Constant	$\tau = R_i C_i$
Duty Cycle	$D = \frac{T_2}{T_1 + T_2} \times 100$

Problems Roster

Problem 1:



Let for the square wave generator shown, $|V_H|=|V_L|$. Also, the generated square wave has a frequency of 1 MHz.

(a)	Calculate the duty cycle.
(b)	Derive the expression of time period T, in terms of circuit parameters.
(c)	Design the circuit by choosing reasonable resistor & capacitor values to achieve the time period found in (b).

Solution:

(a) Since, $|V_H|=|V_L|$, $V_H = -V_L$.

$$T_1 = R_x C_x \ln\left(\frac{V_{TL} - V_H}{V_{TH} - V_H}\right) = R_x C_x \ln\left(\frac{\frac{R_1}{R_1+R_2}V_L - V_H}{\frac{R_1}{R_1+R_2}V_H - V_H}\right)$$

$$= R_x C_x \ln\left(\frac{\frac{R_1}{R_1+R_2}(-V_H) - V_H}{\left(\frac{R_1}{R_1+R_2} - 1\right)V_H}\right) = R_x C_x \ln\left(\frac{-\left(\frac{R_1}{R_1+R_2}+1\right)}{\frac{R_1}{R_1+R_2} - 1}\right)$$

Similarly,

$$T_2 = R_x C_x \ln\left(\frac{V_{TH} - V_L}{V_{TL} - V_L}\right) = R_x C_x \ln\left(\frac{\frac{R_1}{R_1+R_2}(-V_L) - V_L}{\frac{R_1}{R_1+R_2}V_L - V_L}\right)$$

$$= R_x C_x \ln\left(\frac{-\left(\frac{R_1}{R_1+R_2}+1\right)}{\frac{R_1}{R_1+R_2}-1}\right) = T_1$$

$$\therefore T = T_1 + T_2 = 2T_1$$

$$\therefore D = \frac{T_1}{T}\times = \frac{T_1}{2T_1} \times 100 = 50\%$$

(b)

$$T = 2T_1 = 2R_x C_x \ln\left(\frac{-\left(\frac{R_1}{R_1+R_2}+1\right)}{\frac{R_1}{R_1+R_2}-1}\right) = 2R_x C_x \ln\left(\frac{-(2R_1+R_2)}{-R_2}\right) = 2R_x C_x \ln\left(\frac{2R_1+R_2}{R_2}\right)$$

(c) As, $f = 1\,MHz$, $T = 1\,\mu s$. Let, $C_x = 1\,nF$, $R_1 = 1\,k\Omega = R_2$. Then,

$$1\times10^{-6} = 2R_x \times 1\times10^{-9} \ln\left(\frac{2\times1\times10^3+1\times10^3}{1\times10^3}\right) \Rightarrow R_x = 455.12\,\Omega$$

Problem 2:

If $R_1 = 0.86R_2$ & $|V_H| = |V_L|$ for a square wave generator, prove that $T = 2R_xC_x$.

Solution:

Using the derivation in Problem 1, (you must show the entire derivation in exam)

$$T = 2R_xC_x \ln\left(\frac{2R_1+R_2}{R_2}\right) = 2R_xC_x \ln\left(\frac{2\times0.86R_2+R_2}{R_2}\right) = 2R_xC_x \ln(2.72) = 2R_xC_x$$

Problem 3:

Assume for a triangular wave generator, $R_2 = P\,R_1$ & $|V_H| = |V_L|$. Prove that, $f = \frac{P}{4R_iC_i}$.

Solution:

As $|V_H| = |V_L|$, $V_H = -V_L$

$$T_1 = R_iC_i\frac{V_{TH}-V_{TL}}{V_H} = R_iC_i\frac{-\frac{R_1}{R_2}V_L - \left(-\frac{R_1}{R_2}V_H\right)}{V_H} = R_iC_i\frac{\frac{R_1}{P\,R_1}(V_H+V_H)}{V_H}$$

$$= \frac{2R_iC_i}{P}$$

Similarly,

$$T_2 = R_iC_i\frac{V_{TL} - V_{TH}}{V_L} = R_iC_i\frac{-\frac{R_1}{R_2}V_H - \left(-\frac{R_1}{R_2}V_L\right)}{V_L} = R_iC_i\frac{\frac{R_1}{P\,R_1}(V_L + V_L)}{V_L}$$

$$= \frac{2R_iC_i}{P}$$

$$\therefore T = T_1 + T_2 = \frac{4R_iC_i}{P} \Rightarrow f = \frac{1}{T} = \frac{P}{4R_iC_i}$$

Problem 4:

If for a triangular wave generator, $V_H = -nV_L$, prove that its duty cycle will be $\frac{100n}{n+1}$.

Solution:

$$T = T_1 + T_2 = R_iC_i\left(\frac{V_{TH} - V_{TL}}{V_H} + \frac{V_{TL} - V_{TH}}{V_L}\right) = R_iC_i\left((V_{TH} - V_{TL})\left(\frac{1}{V_H} - \frac{1}{V_L}\right)\right)$$

$$\therefore D = \frac{T_2}{T} \times 100 = \frac{R_iC_i\frac{V_{TL} - V_{TH}}{V_L}}{R_iC_i\left((V_{TL} - V_{TH})\left(\frac{1}{V_H} + \frac{1}{\frac{V_H}{n}}\right)\right)}100 = \frac{\frac{n}{V_H}}{\frac{n+1}{V_H}}100 = \frac{100n}{n+1}$$

Problem 5:

Find the required ratio between R_1 & R_2, for the time period of a square wave generator to be nR_xC_x, when $|V_H| = |V_L|$

Solution:

Using the derivation in Problem 1, (You must show the entire derivation in exam)

$$T = 2R_xC_x \ln\left(\frac{2R_1 + R_2}{R_2}\right) \Rightarrow nR_xC_x = 2R_xC_x \ln\left(\frac{2R_1 + R_2}{R_2}\right) \Rightarrow \ln\left(1 + 2\frac{R_1}{R_2}\right) = \frac{n}{2}$$

$$\Rightarrow 1 + 2\frac{R_1}{R_2} = e^{\frac{n}{2}} \Rightarrow \frac{R_1}{R_2} = \frac{e^{\frac{n}{2}} - 1}{2}$$

Problem 6:

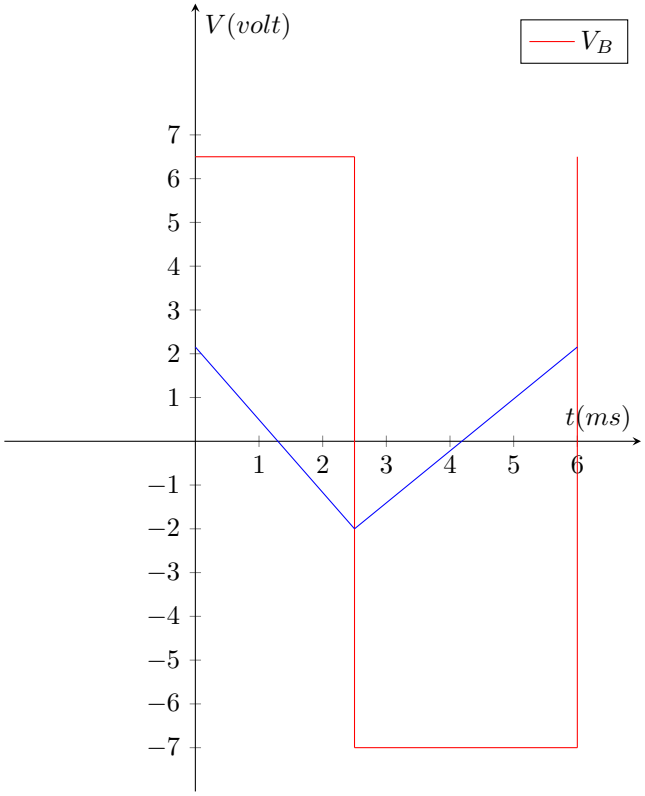


Figure 4.12: Response of a Triangular Wave Generator

The outputs of a triangular wave generator are given in figure 4.12.

(a)	Find the duty cycle of the triangular wave.
(b)	Find the ratio of the resistances of the non-inverting Schmitt Trigger.

Solution:

(a) $D = \dfrac{T_2}{T_1 + T_2} \times 100 = \dfrac{3.5}{6} \times 100 = 58.33\%$

(b) We can see from the graph, $V_H = 6.5\,V$, $V_L = -7\,V$, $V_{TL} = -2\,V$. Thus,

$$-2 = -\frac{R_1}{R_2} \times 6.5 \Rightarrow \frac{R_1}{R_2} = \frac{1}{3.25}$$

Chapter 5

Diode Logic

Welcome to Digital Electronics part of the course. Here, we study the in depth circuitry involved with the logic gates we know (e.g. OR, AND, NOT, NAND, NOR etc.). We will mainly learn how to implement digital logic with electronic circuits using diode, BJT & MOSFET. Let's start by the simplest— diodes.

We can implement two logic gates using diodes— **OR & AND**. Let's first review some basics of the diode.

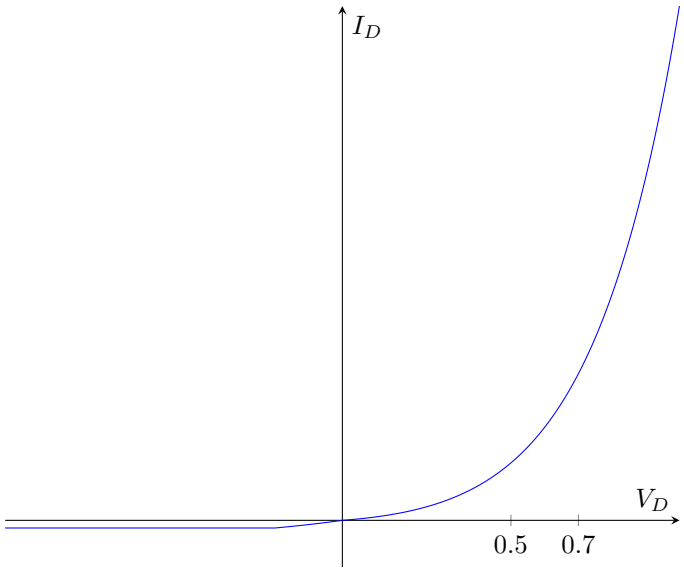


Figure 5.1: Diode I–V Characteristics

The I-V characteristics of a silicon diode is showed in 5.1. From the figure, we can see, the diode starts conducting well enough at approximately '0.7 V'. However, the current through it (I_D) starts rising appreciably after '0.5 V'. We consider the average of these two values, **'0.6 V'**, to be the **'cut-in' voltage** of the diode. This is the minimum voltage which must be applied across a diode in **forward bias** for it to be on. However, like in CSE251, once we know for sure that

the diode is in forward bias and has enough voltage across it to turn on (i.e. a voltage more than the cut-in voltage is available), we will replace the diode using the **Constant Voltage Drop(CVD)** model for a silicon diode. According to which, the voltage drop across a silicon diode in forward bias is '0.7 V'. To sum up—

1. **Cut-in Voltage:** The minimum voltage required in forward bias for a diode to turn on. Often it is denoted by V_γ. So, $V_\gamma = 0.6\,V$.
2. Once we know for sure that (1) is satisfied, and the diode will conduct, we replace the diode with a **'0.7 V'** voltage drop using the **CVD** model. This voltage is usually denoted by V_D.
3. In reverse bias, the diode will be off and will be replaced by an **open circuit**, as per the CVD model.

Let's now get introduced with the logic circuits.

Diode OR Gate

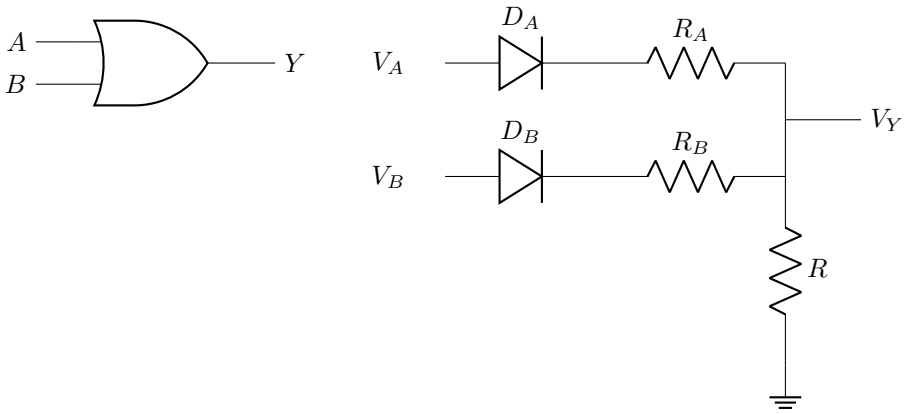


Figure 5.2: A two input OR gate implemented using Diode Logic

Analysis of Operation: Figure 5.2 depicts how a two input OR gate can be built using diodes and resistors. The inputs of this logic circuit are the the two input voltages V_A & V_B. When they are high (a value greater than V_γ, let 5 V), the diodes D_A & D_B will be in forward bias and will turn on. We can then replace them by a 0.7 V drop. When any of the input voltages are low (lower than V_γ, say 0 V), the corresponding diode will be in reverse bias, and can be replaced by an open circuit. Since there are two inputs, there can be four input logic combinations((0,0), (0,1), (1,0), (1,1)). Let's discuss each case one by one.

Case (1,1):

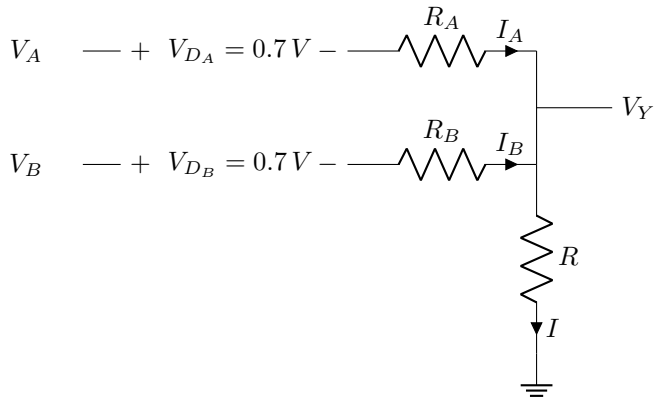


Figure 5.3: Case (1,1)

Applying KCL at 'Y' in figure 5.2,

$$I_A + I_B = I$$

$$\Rightarrow \frac{V_A - 0.7 - V_Y}{R_A} + \frac{V_B - 0.7 - V_Y}{R_B} = \frac{V_Y - 0}{R}$$

Since, both inputs are high, we can say, $V_A = V_B$. For simplicity, let us assume for the moment, $R_A = R_B$. We then have,

$$2 \times \frac{(V_A - 0.7 - V_Y)}{R_A} = \frac{V_Y}{R}$$

$$\Rightarrow \left(\frac{R_A + 2R}{RR_A}\right) V_Y = 2 \times \frac{(V_A - 0.7)}{R_A}$$

If we take $\boldsymbol{R >> R_A}$, we can ignore R_A and then,

$$\Rightarrow V_Y \approx (V_A - 0.7)$$

Which is also a high enough voltage to be treated as logically high. If at the output end the threshold for high logic is lower enough than $V_A - 0.7$, then this value will be treated as high (bitwise '1'). This is also the desired result for input case (1,1) of an OR gate.

Case(0,1) or (1,0):

Let us hold on to our assumption of $R_A = R_B$. Then both case (1,0) and (0,1) would give the same results, as there are no differnce between the input branches. So, we will analyze (0,1) here.

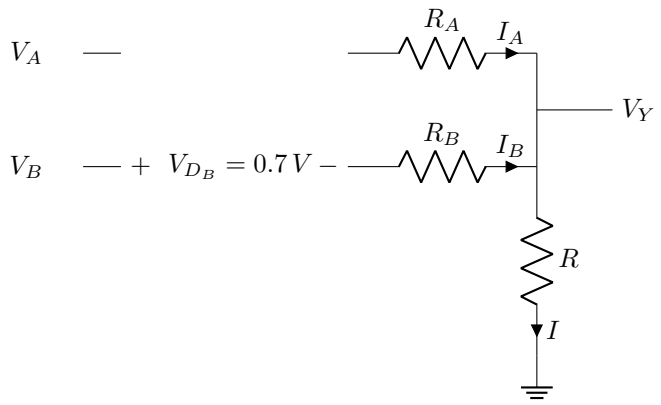


Figure 5.4: Case (0,1)

As V_A is low, D_A will be reverse biased, and can be replaced by by an open circuit. On the other hand, V_B is high, and will thus be replaced by a 0.7 V drop. Here, due to open circuit, $I_A = 0$. Thus, from KCL we have,

$$I_A + I_B = I$$

$$\Rightarrow 0 + \frac{V_B - 0.7 - V_Y}{R_B} = \frac{V_Y - 0}{R}$$

$$\Rightarrow V_Y \approx V_B - 0.7$$

Thus, we again get a high output voltage. The output logic for input cases (0,1) and (1,0) is high too.

Case (0,0):

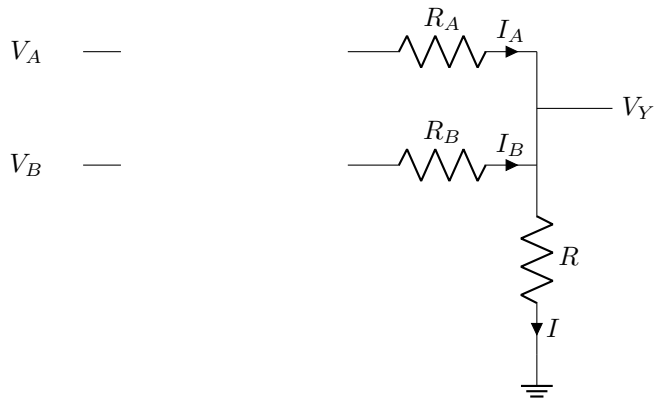


Figure 5.5: Case (0,0)

As both the input voltages are low, both diodes will be off and can be replaced by an open circuit. Thus, $I_A = I_B = 0$. Consequently, $I = I_A + I_B = 0$. This means there will be no voltage drop

across the resistor 'R'. We will then get, $V_Y = 0$, since the ground voltage will directly appear at the output terminal. This is also the required output for the (0,0) case of an OR gate.

One cruical thing to note here, that for all these to be true, we must design the circuit as per our assumption. So, R should be very large compared to R_A & R_B. The assumption of $R_A = R_B$ helped simplify the analysis, but is not a necessity. However, it is a good practice and preference that they are kept as equal as possible.

Also, while solving mathematical problems, we do not need to ignore R_A if the values of the resistors are given. We can find the exact value of the output voltage from the KCL equations, instead of approximate ones.

Power Dissipation Calculation: One important part of logic circuit design is the amount of power consumption of the circuit. We know that power consumption of any electrical element can be calculated using $P = VI$ formula. We will be using this throughout the remaining part of the course to find power dissipations.

To find the dissipated power using the stated formula, we need to know the voltage across a path or element and the current flowing through it. Once these two values are available, we can ignore what is happening inside the path. Using this concept, the power dissipation calculation diagrams for the four cases of the OR gate can be simplified as the followings:

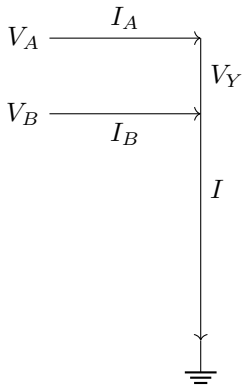


Figure 5.6: Power Calculation Diagram for Case (1,1)

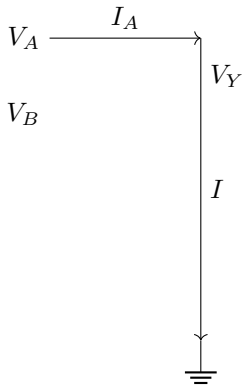


Figure 5.7: Power Calculation Diagram for Case (1,0)

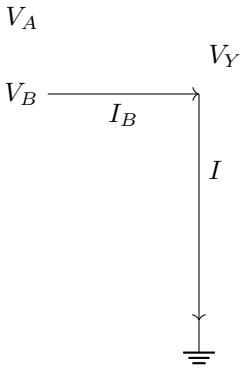


Figure 5.8: Power Calculation Diagram for Case (0,1)

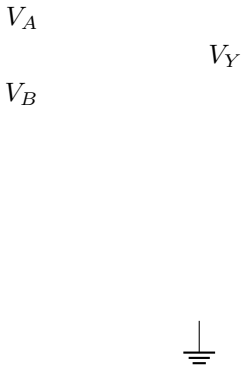


Figure 5.9: Power Calculation Diagram for Case (0,0)

From figure 5.6, we see, I_A & I_B both flows between corresponding input voltages & V_Y. While, I flows between V_Y & ground. So, the consumed power of the circuit for case(1,1):

$$P_{(1,1)} = (V_A - V_Y) \times I_A + (V_B - V_Y) \times I_B + (V_Y - 0) \times I$$

With a similar analysis, the power dissipations for the other three cases can be found to be as follows:

$$P_{(1,0)} = (V_A - V_Y) \times I_A + (V_Y - 0) \times I$$

$$P_{(0,1)} = (V_B - V_Y) \times I_B + (V_Y - 0) \times I$$

$$P_{(0,0)} = 0$$

Diode AND Gate

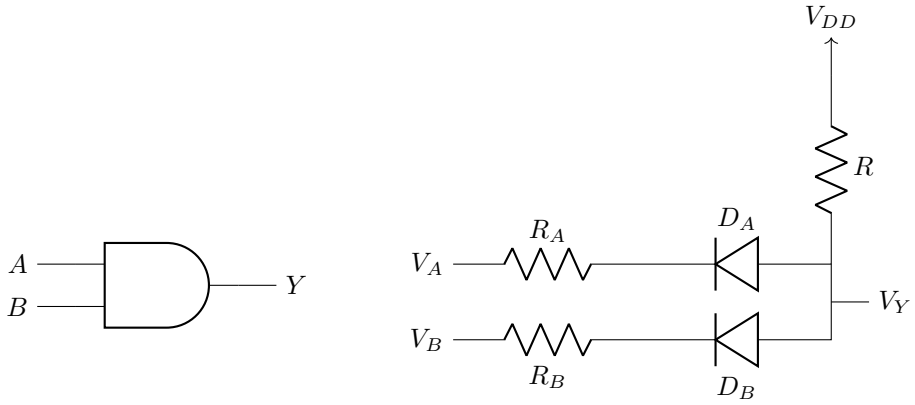


Figure 5.10: A two input AND Gate implemented using Diode Logic

Analysis of Operation: The AND gate circuit shown in figure 5.10, has a source voltage V_{DD}, which is much greater than the V_γ of the diodes (e.g. 5 V). So, when the input voltages V_A & V_B are low, their corresponding diodes D_A & D_B are forward biased. This is the opposite scenario as in the case of OR gate. If any of the inputs is high, the diode is reverse biased due to not having more than its cut-in voltage available across it. Thus, the corresponding input branch becomes open. When both diodes are off due to both inputs being high, no current flows in the circuit, due to all the paths being open. Then the source voltage appears at the output 'Y'. Let's now analyze case by case.

Case (0,0):

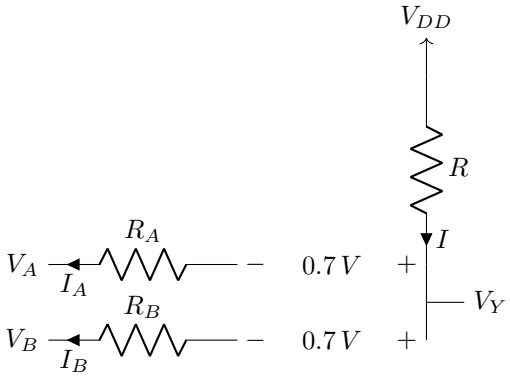


Figure 5.11: Case (0,0)

Since both V_A & V_B are low, both D_A & D_B conduct. Applying KCL at 'Y',

$$I = I_A + I_B$$

$$\Rightarrow \frac{V_{DD} - V_Y}{R} = \frac{V_Y - 0.7 - V_A}{R_A} + \frac{V_Y - 0.7 - V_B}{R_B}$$

Assuming again for simplicity, $R_A = R_B$,

$$\Rightarrow \frac{V_{DD} - V_Y}{R} = 2\frac{V_Y - 0.7 - V_A}{R_A}$$

We further simplify things by assuming the low input voltages to be '0 V'—

$$\frac{V_{DD}}{R} + 2\frac{0.7}{R_A} = V_Y \left(\frac{1}{R} + \frac{2}{R_A}\right)$$

Again, if we choose $R >> R_A$, we can ignore the fractions with 'R' in the denominator—

$$V_Y \approx 0.7\,V$$

Which is sufficiently a low voltage compared to V_{DD} or the high input voltages. Like in the case of OR gates, we can get the exact value of V_Y from the KCL equation. Also, $R_A = R_B$ is not a necessity but a good practice.

Case (0,1) or (1,0):

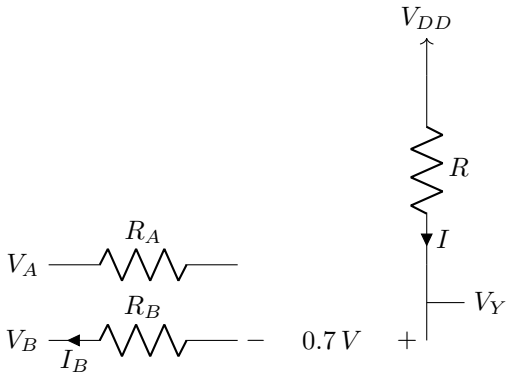


Figure 5.12: Case (1,0)

Since V_A is high, D_A will be reverse biased and can be replaced by an open circuit and so, $I_A = 0$. The KCL equation then becomes,

$$I = I_B$$

$$\frac{V_{DD} - V_Y}{R} = \frac{V_Y - 0.7}{R_B}$$

Using the similar assumption of $R >> R_B$,

$$V_Y \approx 0.7\,V$$

Which is again a low voltage and the desired result for the input case of (1,0) of an AND gate.

Case (1,1):

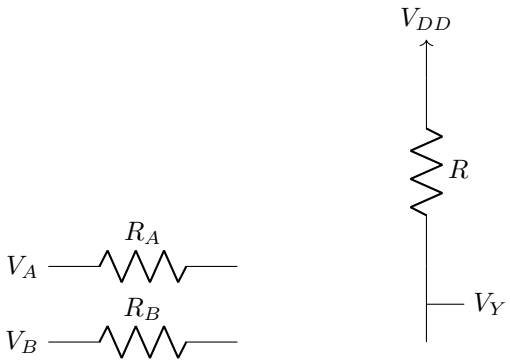


Figure 5.13: Case (1,1)

In this case, as both inputs are high, both the diodes are reverse biased and off. Thus, no current flows in the circuit and the source voltage (V_{DD}) appears at 'Y'. So, $V_Y = V_{DD}$. And we have already mentioned, V_{DD} is a high voltage. Thus, we end up with a high output, which was the requirement for this input case.

Power Dissipation Calculation:

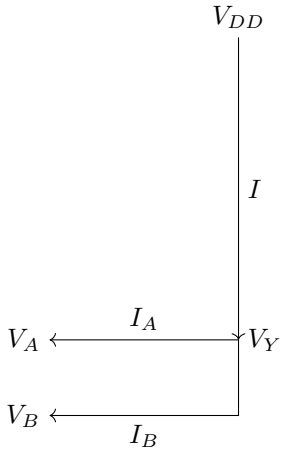


Figure 5.14: Case (0,0)

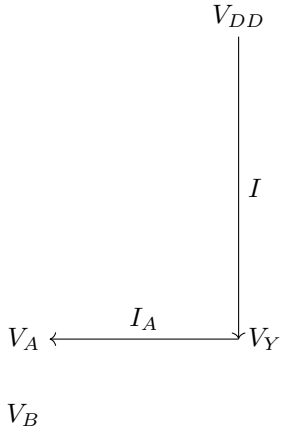


Figure 5.15: Case (0,1)

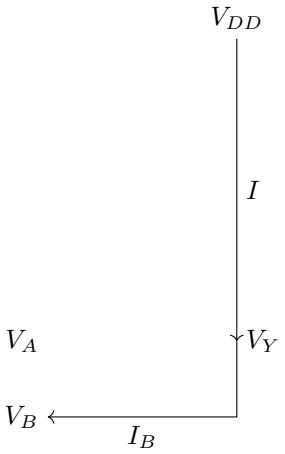


Figure 5.16: Case (1,0)

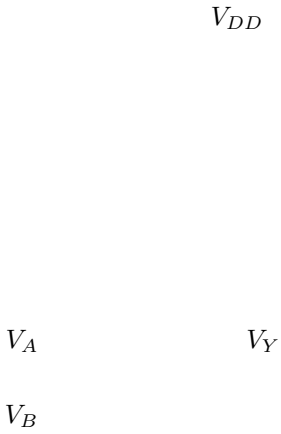


Figure 5.17: Case (1,1)

$$P_{(0,0)} = (V_{DD} - V_Y) \times I + (V_Y - V_A) \times I_A + (V_Y - V_B) \times I_B$$

$$P_{(0,1)} = (V_{DD} - V_Y) \times I + (V_Y - V_A) \times I_A$$

$$P_{(1,0)} = (V_{DD} - V_Y) \times I + (V_Y - V_B) \times I_B$$

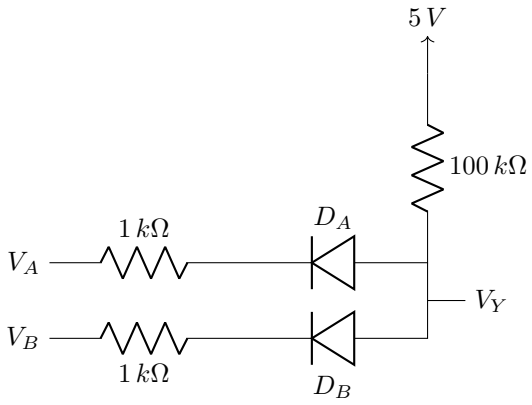
$$P_{(1,1)} = 0$$

Some things to keep in mind when solving diode logic problems:

1. While evaluating the possible operating mode of the diode for a particular input case of the logic circuit, consider whether at least '0.6 V' will be available in forward bias across the diode.
2. When an assumption of forward bias is made, replace the diode with '0.7 V' for analysis of the logic circuit. If results come accordingly, then the assumption will be verified.
3. If values of high & low input voltages are not provided, you may assume the source voltage V_{DD} to be the high voltage, and '0 V' to be the low one.

Problems Roster

Problem 1:



For the AND gate shown—

(a)	For the input logic case (1,0) find the output voltage V_Y, and verify your assumption of the diode model used.
(b)	Find the current through $100\,k\Omega$ for logic case (0,1).
(c)	Find the lower threshold of output.
(d)	If R_B is doubled, find the currents through the diodes for logic case (0,0).

Solution:

(a) Assuming high input = 5 V and low input = 0 V, KCL at 'Y' for case (1,0) gives—

$$\frac{5 - V_Y}{100} = \frac{V_Y - 0.7 - 0}{1} \Rightarrow V_Y = 0.743\,V$$

Verification: Voltage across $D_A = V_Y - (V_A + I_A R_A) = 0.743 - (5 + 0) = -4.267 < 0.7\,V$
So, our assumption of D_A being off was correct. Voltage across D_B is 0.7 V and the results from this were satisfactory. Hence, this assumption was right too.

(b) KCL for case (0,1) gives—

$$\frac{5 - V_Y}{100} = \frac{V_Y - 0.7 - 0}{1} \Rightarrow V_Y = 0.743\,V$$

$$\therefore I_{100\,k\Omega} = \frac{5 - V_Y}{100} = 0.043\,mA$$

(c) Since, $R_A = R_B$, V_Y is the same for case (0,1) and (1,0). The output voltage for the case (0,0) can be found from the KCL equation below—

$$\frac{5 - V_Y}{100} = 2 \times \frac{V_Y - 0.7 - 0}{1} \Rightarrow V_Y = 0.742\,V$$

$$\therefore V_{OL} = max(0.742,\, 0.743) = 0.743\,V$$

(d) KCL at 'Y' for this changed circuit for the case (0,0) gives—

$$\frac{5 - V_Y}{100} = \frac{V_Y - 0.7 - 0}{1} + \frac{V_Y - 0.7 - 0}{2} \Rightarrow V_Y = 0.728\,V$$

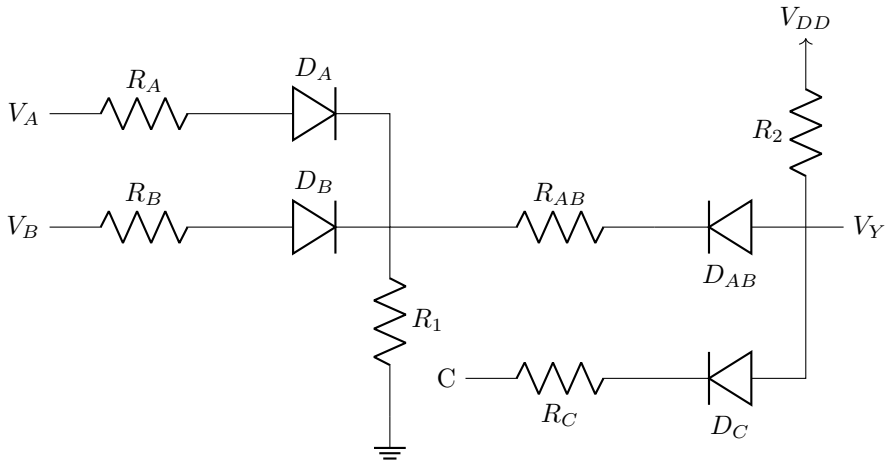
$$\therefore I_{D_A} = \frac{V_Y - 0.7}{1} = 0.028\,mA$$

$$\therefore I_{D_B} = \frac{V_Y - 0.7}{2} = 0.014\,mA$$

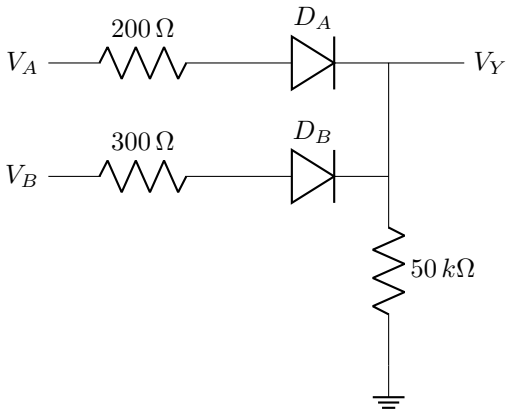
Problem 2:

Implement the boolean function, Y=(A+B)C using diode logic.

Solution:



Problem 3:



(a)	Find power dissipation for all cases.
(b)	Find the maximum & average power dissipation.

Solution:

(a) Case (0,0): $P_{(0,0)} = 0\,W$

Case (0,1): $V_A = 0\,V$, $V_B = 5\,V$. KCL equation,

$$\frac{V_B - 0.7 - V_Y}{300} + 0 = \frac{V_Y - 0}{50 \times 10^3} \Rightarrow V_Y = 4.27\,V$$

$$\therefore P_{(0,1)} = (5 - 4.27) \times \frac{5 - 0.7 - 4.27}{300} + (4.27 - 0) \times \frac{5 - 0.7 - 4.27}{300} = 0.5\,mW$$

Case (1,0): $V_A = 5\,V, V_B = 0\,V$. KCL equation,

$$\frac{V_A - 0.7 - V_Y}{200} + 0 = \frac{V_Y - 0}{50 \times 10^3} \Rightarrow V_Y = 4.28\,V$$

$$\therefore P_{(1,0)} = (5 - 0) \times \frac{5 - 0.7 - 4.28}{200} = 0.5\,mW$$

Case (1,1): $V_A = V_B = 5\,V$. KCL equation,

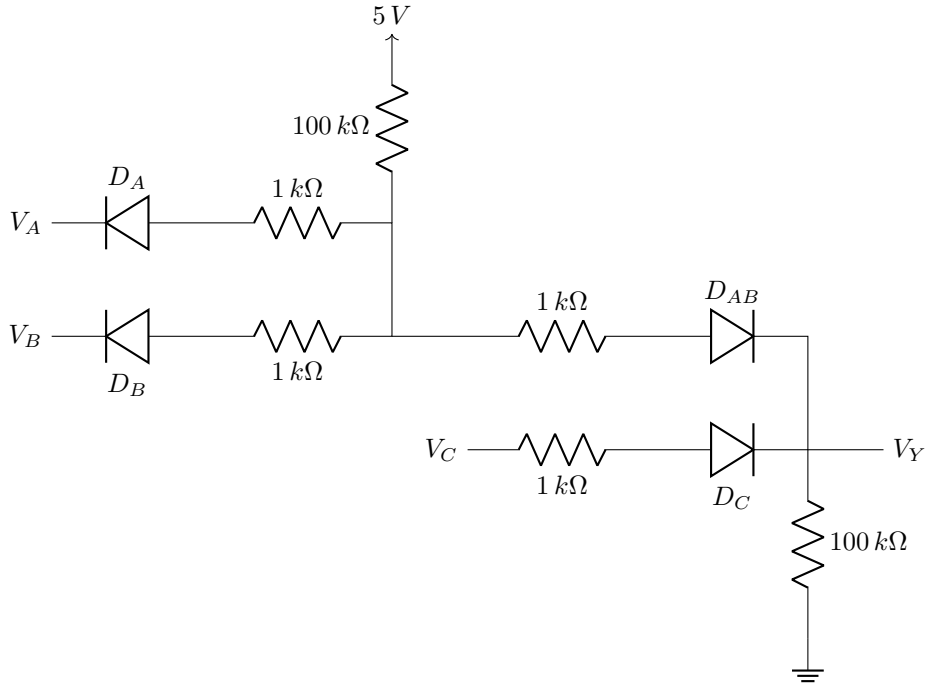
$$\frac{5 - 0.7 - V_Y}{200} + \frac{5 - 0.7 - V_Y}{300} = \frac{V_Y - 0}{50 \times 100} \Rightarrow V_Y = 4.29\,V$$

$$\therefore P_{(1,1)} = (5 - 0) \times \frac{4.29 - 0}{50 \times 10^3} = 0.42\,mW$$

(b) $P_{max} = 0.5\,mW$

$$P_{avg} = \frac{0 + 0.5 + 0.5 + 0.42}{4} = 0.355\,mW$$

Problem 4:



(a)	Find the Boolean expression of 'Y'.
(b)	Determine the higher & lower threshold of output voltage.
(c)	Find the maximum & average dissipation of the full circuit.

Solution:

(a) Y = AB + C

(b) Case (0,0,0): D_A, D_B on. Output of the AND gate will be low. So, D_{AB} will be off. D_C is off. $\therefore V_Y = 0\,V$.

Case (0,0,1): D_A, D_B on. Output of the AND gate will be low. So, D_{AB} will be off. D_C is on. KCL at 'Y',

$$\frac{5-(V_Y+0.7)}{1} = \frac{V_Y-0}{100} \Rightarrow V_Y = 4.26\,V$$

Case (0,1,0): D_A on, D_B off. Output of the AND gate will be low. So, D_{AB} will be off. D_C is off. So, $V_Y = 0\,V$.

Case (0,1,1): D_A on, D_B off. Output of the AND gate will be low. So, D_{AB} will be off. D_C is on. KCL at 'Y',

$$\frac{5-(V_Y+0.7)}{1} = \frac{V_Y-0}{100} \Rightarrow V_Y = 4.26\,V$$

Case (1,0,0): D_A is off, D_B is on. Output of the AND gate will be low. So, D_{AB} will be off. D_C is off. So, $V_Y = 0\,V$.

Case (1,0,1): D_A is off, D_B is on. Output of the AND gate will be low. So, D_{AB} will be off. D_C is on. KCL at 'Y',

$$\frac{5-(V_Y+0.7)}{1} = \frac{V_Y-0}{100} \Rightarrow V_Y = 4.26\,V$$

Case (1,1,0): D_A and D_B off. Let the output voltage of the AND gate is V_X. D_C is off. So, KCL at 'X',

$$\frac{5-V_X}{100} = \frac{V_X-(V_Y+0.7)}{1}$$

KCL at 'Y',

$$\frac{V_X-(V_Y+0.7)}{1} = \frac{V_Y-0}{100}$$

Solving the equation pair, $V_X = 2.14\,V$ & $V_Y = 2.86\,V$.

Case (1,1,1): D_A and D_B off. Let the output voltage of the AND gate is V_X. D_C is on. So, KCL at 'X',

$$\frac{5-V_X}{100} = \frac{V_X-(V_Y+0.7)}{1}$$

KCL at 'Y',

$$\frac{V_X-(V_Y+0.7)}{1} + \frac{5-(V_Y+0.7)}{1} = \frac{V_Y-0}{100}$$

Solving the equation pair, $V_X = 4.96\,V$ & $V_Y = 4.26\,V$.
$\therefore V_{OH} = min(2.86, 4.26) = 2.86\,V$
$\therefore V_{OL} = max(0) = 0\,V$

(c) Case (0,0,0): KCL at 'X',

$$\frac{5-V_X}{100} = \frac{V_x-0.7}{1} \times 2 \Rightarrow V_X = 0.72\,V$$

$$\therefore P_{(0,0,0)} = (5-0) \times \frac{5-0.72}{100} = 0.214\,mW$$

Case (0,0,1): KCL at 'X' will be same as (0,0,0). So, $V_X = 0.72\,V$. From (b), $V_Y = 4.26\,V$. So,

$$\therefore P_{(0,0,1)} = (5-0) \times \frac{5-0.72}{100} + (5-0) \times \frac{5-0.7-4.26}{1} = 0.41\,mW$$

Case (0,1,0): KCL at 'X',

$$\frac{5-V_X}{100} = \frac{V_X-0.7}{1} \Rightarrow V_X = 0.74\,V$$

$$\therefore P_{(0,1,0)} = (5-0) \times \frac{5-0.74}{100} = 0.213\,mW$$

Case (0,1,1): KCL at 'X' will be same as (0,1,0). So, $V_X = 0.74\,V$. From (b) $V_Y = 4.26\,V$. So,

$$\therefore P_{(0,1,1)} = (5-0) \times \frac{5-0.74}{100} + (5-0) \times \frac{5-0.7-4.26}{1} = 0.413\,mW$$

Case (1,0,0): KCL at 'X' will be the same as (0,1,0). So, $V_X = 0.74\,V$. From (b), $V_Y = 0\,V$. So,

$$\therefore P_{(1,0,0)} = (5-0) \times \frac{5-0.74}{100} = 0.213\,mW$$

Case (1,0,1): KCL at 'X' will be the same as (0,1,0). So, $V_X = 0.74\,V$. From (b), $V_Y = 4.26\,V$. So,

$$\therefore P_{(1,0,1)} = P_{(0,1,1)} = 0.413\,mW$$

Case (1,1,0): From (b), $V_X = 2.14\,V$. So,

$$\therefore P_{(1,1,0)} = (5-0) \times \frac{5-2.14}{100} = 0.143\,mW$$

Case (1,1,1): From (b), $V_X = 4.96\,V$ & $V_Y = 4.26\,V$. So,

$$\therefore P_{(1,1,1)} = (5-0) \times \frac{5-4.96}{100} + (5-0) \times \frac{5-0.7-4.26}{1} = 0.202\,mW$$

$$\therefore P_{max} = 0.413\,mW$$

$$\therefore P_{avg} = \frac{0.413 \times 2 + 0.213 \times 2 + 0.41 + 0.143 + 0.202 + 0.214}{8} = 0.278\,mW$$

Chapter 6

Resistor Transistor Logic (RTL)

Till now, we have been able to construct OR & AND gates using diode logic. However, they are not an efficient method of implementing logic. Diodes are the least controllable electronic device. Also, without a NOT gate, we cannot implement any logic function we want. So, we will move forward to RTL, Resistor Transistor Logic. It will give us the NOT gate circuit and many more. But befor going into RTLs, we need to review and know a bit more about BJTs from CSE251.

Back to BJTs

We know that an n-p-n BJT has two p-n junctions— the base-emitter junction (B-E) and the base-collector junction (B-C). The operating mode of the BJT can thus be of the following four types, depending on the bias type of the two junctions. Let's talk about these modes one by one.

B-E junction bias	B-C junction bias	Operating mode
Forward	Reverse	Active
Reverse	Reverse	Cut-off
Forward	Forward	Saturation
Reverse	Forward	Reverse Active

Table 6.1: Operating Modes of a BJT

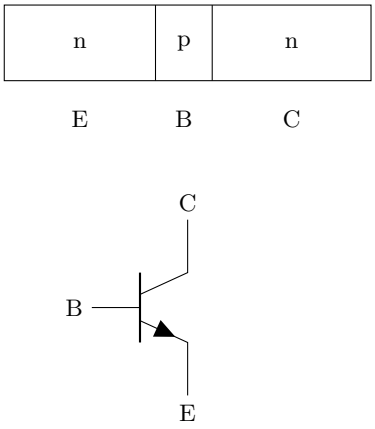


Figure 6.1: An n-p-n BJT

Active Mode: The B-E junction is forward biased by applying a higher voltage at the base with respect to the emitter. This causes the majority charge carrier of the n-type emitter (electrons) to drift to the p-type region, the base, as it should for a p-n junction in forward bias. Now, we know that the base is relatively doped at a lower concentration compared to the emitter & collector. So, only a few of the electrons arriving from the emitter (about 5%) recombine with the majority charge carrier of the base (holes). The rest? Well they continue to move through the base-collector junction towards the collector, as to the base, these electrons are minority carrier, and the B-C junction is reverse biased. Recall that in reverse bias if any current flows, they are caused by the minority carriers. So, we get a continued electron flow starting at the emitter, crossing the base and through the collector. As the direction of current flow is opposite to that of the electrons, the currents involved in the three regions will have a direction in the reverse of the electron flow. The current flow diagram of an n-p-n BJT in active mode will be as follows:

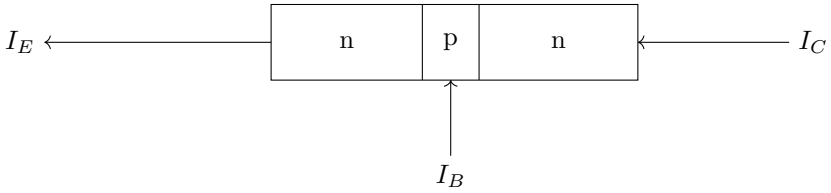


Figure 6.2: Current flow diagram in active mode of an n-p-n BJT

From figure 6.2, $I_E = I_C + I_B$. As the B-E junction is forward biased, $V_{BE} > 0$. The exact requirement varies with temperature, '0.6-0.7 V' is a common value. Also, $V_{BC} < 0$. The ratio of I_C & I_B is called the 'forward beta' of the BJT. So, $\beta_F = \frac{I_C}{I_B}$. β_F usually has a high value (e.g. 30, 50, 100 etc.).

Cut-off Mode: In this mode, both the junctions are reverse biased. So, no currents flow. The whole BJT can simply be replaced by an open circuit. Note that as the p-n junction activates when the applied voltage is at least 0.5 V, in cut-off, $V_{BE} < 0.5$ is enough to keep the B-E junction reverse biased.

Saturation Mode: With both the junctions forward biased, not only electrons drift from the emitter to the base, but also from the collector as well. This increases the amount of electrons in the base compared to the active mode. Consequently the amount of recombination rises, causing an increase in the base current with it. The collector current cannot follow $\beta_F I_B$ anymore, rather is dictated by the external circuit. However, it still follows the same direction as in forward active mode. Due to the external circuit, the emitter electrons that did not recombine in the base, manage to reach the collector. They are still in a higher number than the amount of electrons going to the base from the collector. So, the net collector current is still has the same direction. Since this effect is forced by the external circuit, the ratio of I_C & I_B for this operating mode is called the forced beta (β_{forced}). It has a lower value compared to β_F, due to the reduced collector current, and can change depending on the external circuitry.

For this mode, $V_{BE} = 0.8\,V$ and $V_{BC} = 0.6 - 0.7\,V$ as both the junctions are forward biased. This means $V_{CE} = V_{CB} - V_{EB} = 0.1 - 0.2\,V$.

Reverse Active Mode: In this mode, the emitter & the collector swap their roles. So, now the B-C junction being forward biased, pushes electrons towards the base. Among these, a few recombine with holes and the rest continue to move throught the B-E junction to the emitter due to this junction being reverse biased. Well, if we still call the regions with their old names, then the current flow diagram would look like the following:

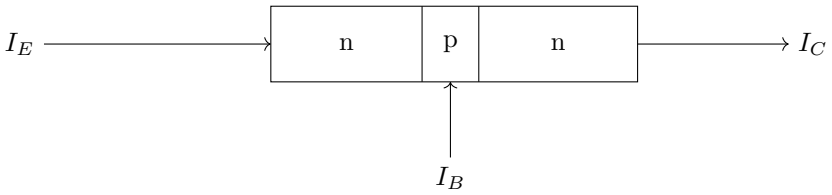


Figure 6.3: Current flow diagram in reverse active mode of an n-p-n BJT

The beta of the BJT for this mode is thus, $\beta_R = \dfrac{I_E}{I_B}$, as the emitter is playing the role of the collector now. Also, from figure 6.3, $I_C = I_E + I_B$. The value of reverse beta, β_R is typically 0.1-0.3 V. This low value is due to the fact that, emitters are highly doped compared to collectors. So, when a collector plays the role of an emitter, it cannot inject the same amount of electrons as the emitter could have done in forward active mode. This reduces the I_E and results in a smaller beta. For this mode, $V_{BC} = 0.7\,V$ and $V_E > V_B > V_C$. This can be easily anticipated from the fact that B-E junction is reverse biased, and B-C junction is forward biased.

We can summarize all the key informations of the four operating modes of the BJT in the diagram shown in the next page. Here, we have used the two junction voltages V_{BE} & V_{BC} as the axes variables, since their value determines the operating region.

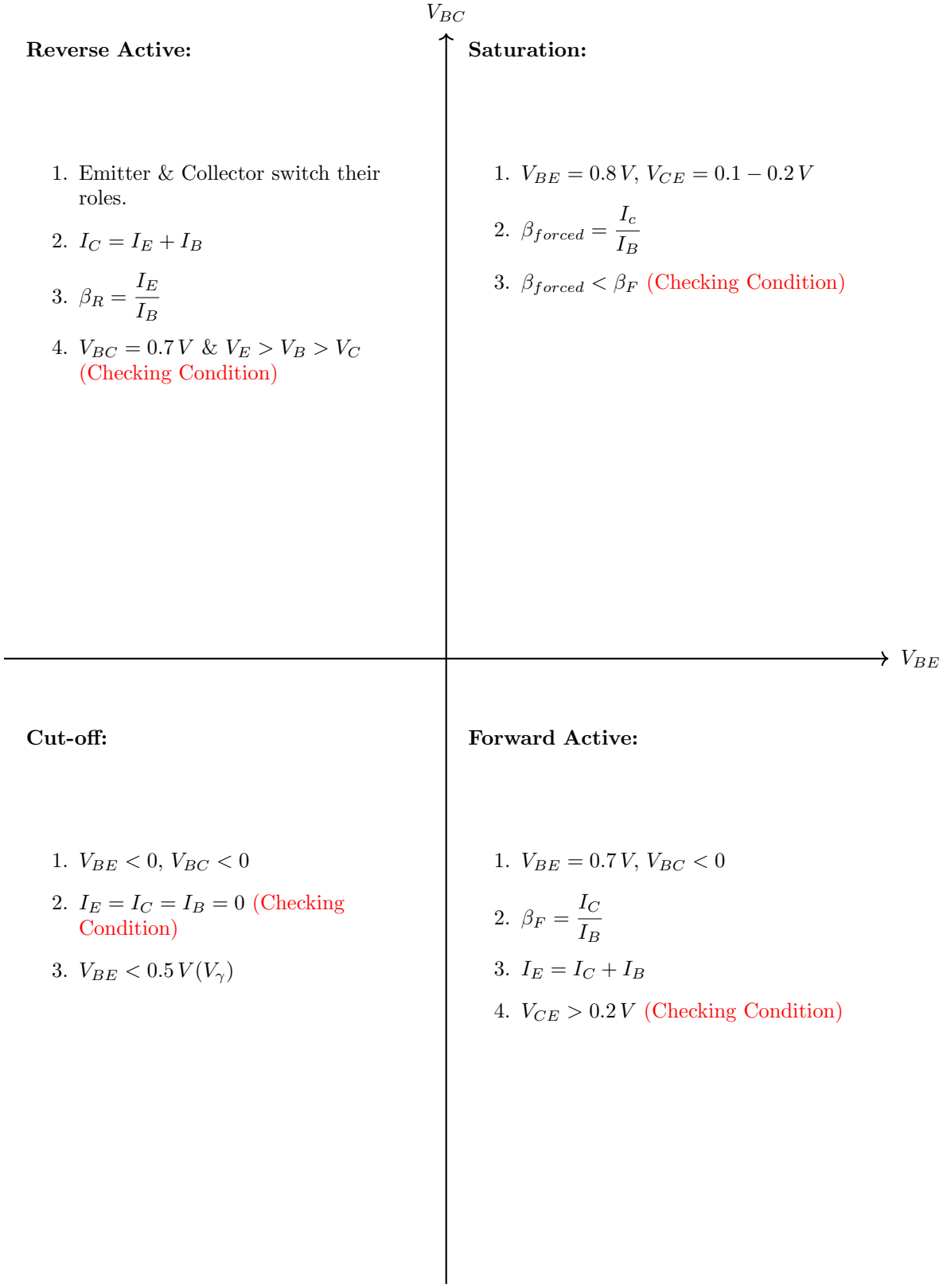


Figure 6.4: Operating Modes of an n-p-n BJT

RTL NOT Gate

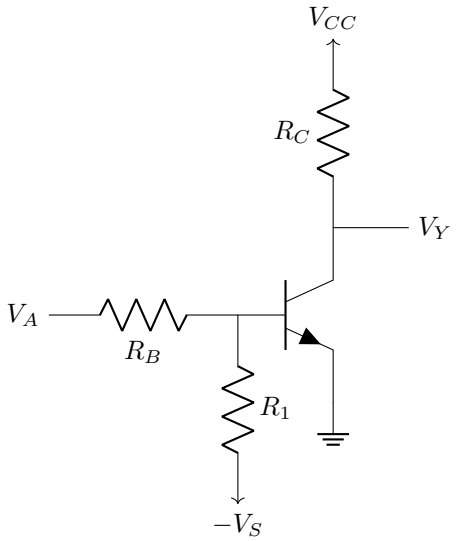


Figure 6.5: A typical RTL NOT gate

Figure 6.5 shows an usual RTL NOT gate circuit. The input to which is V_A and V_Y is the output. R_1 limits I_B to prevent damage of the BJT. To achieve these, $R_1 >> R_B$ must be maintained. $-V_S$ enhances the current drawn by R_1, reducing I_B further. However, it is not a necessity and it can be 0 too (i.e. grounded). Now let's look at how this circuit acts as a NOT gate.

Analysis of Operation:

Case(0)(V_A = *Low*): Due to the input voltage being low, the base of the BJT does not gate enough voltage (less than 0.5 V) to turn the B-E junction on (i.e. forward bias it). This is because, the emitter is grounded. So, $V_E = 0\,V$. Say our low input voltage is 0 V. Then $V_{BE} = 0 - 0 = 0\,V$. Thus, B-E junction remains in reverse bias. Since the collector is connected to a high voltage source V_{CC}, its voltage is also greater than that of the base. Consequently, B-C junction also remains in reverse bias. This indicates that the BJT is in cut-off mode. So, it acts as an effective open circuit—

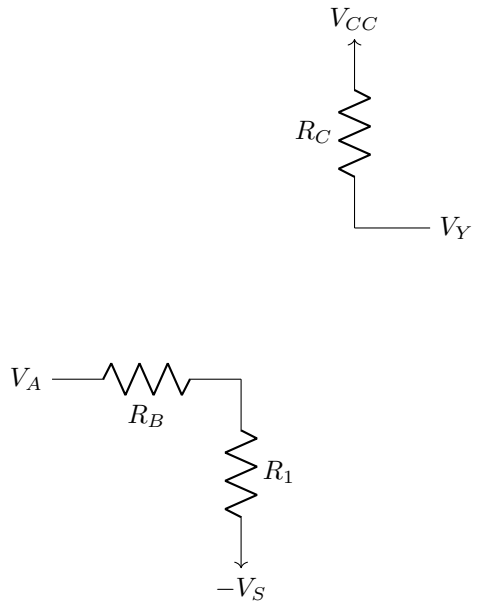


Figure 6.6: Case (0) of the RTL NOT gate

Now, since the BJT is an open circuit, no current flows through R_C. As can be seen from figure 6.6. Thus, $V_Y = V_{CC}$, which is a high voltage. So, we get a high output voltage for a low input voltage, as we should for a NOT gate.

Case(1)($V_A = High$): When the input voltage V_A is high (say equal to V_{CC}), there is enough voltage at base to drive the B-E junction in forward bias (i.e. $V_{BE} > 0.5\,V$). Now, the B-C junction is also forward biased, since the collector is again connected to a high voltage source, V_{CC}. Since, there will be a voltage drop across R_B, V_B will never get the full V_A. So, both junctions being forward biased, leads to the BJT operating in saturation mode. Now, from figure 6.4, we know that in saturation, $V_{CE} = 0.2\,V$ & $V_{BE} = 0.8\,V$. As $V_E = 0\,V$, this leads to $V_C = 0.2\,V$ & $V_B = 0.8\,V$. So, $V_Y = V_C = 0.2\,V$. Consequently, we get a low output voltage from a high input voltage. Here, the three currents (I_E, I_C & I_B) are not zero, rather follow $I_E = I_C + I_B$ & $I_C = \beta_{forced} I_B$. To verify our assumption of the BJT operating in saturation, we can find β_{forced} and show that it is lower than the forward beta β_F of the BJT.

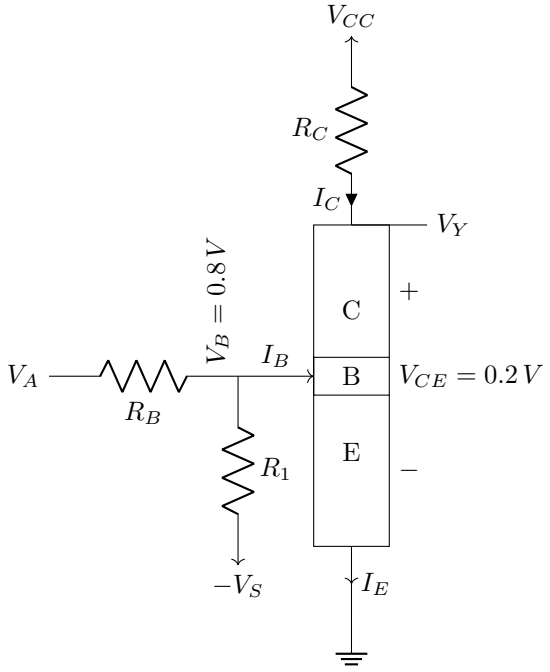


Figure 6.7: Case (1) of the RTL NOT gate

Let's look at the power dissipation diagrams and calculations for the two cases:

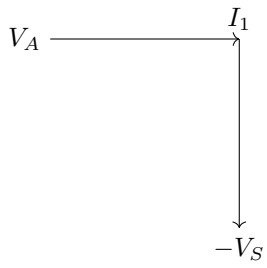


Figure 6.8: Power dissipation diagram for Case(0)

$\therefore P_0 = (V_A - (-V_S)) \times I_1$

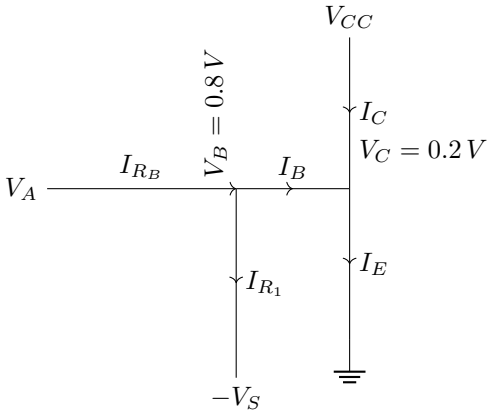


Figure 6.9: Power dissipation diagram for Case(1)

$\therefore P_1 = (V_A - 0.8)I_{R_B} + (0.8 - (-V_S))I_{R_1} + (0.8 - 0)I_B + (V_{CC} - 0)I_C$

RTL NOR Gate

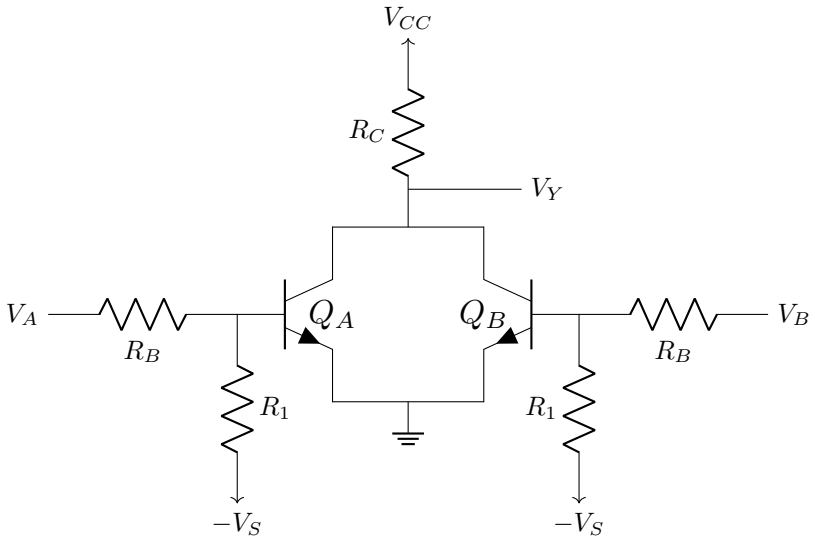


Figure 6.10: A typical RTL NOR gate

Although we have denoted the same value of R_B, V_S for the two BJTs, they can be different as well. Now that there are two inputs (V_A & V_B), there will be four input cases. Let's discuss them accordingly.

Case(0,0): When both the inputs are low, both Q_A & Q_B will be in cut-off. The result will be both of them acting as an open circuit. Then the source voltage V_{CC} appears directly at 'Y', as no current flows through R_C (as $I_{C_A} = I_{C_B} = 0$). So, $V_Y = V_{CC}$, which is a high voltage. This is the desired result for case (0,0) of a NOR gate.

Case(0,1) or (1,0): Since we have considered similar input side parameters (R_B & $-V_S$) for both the BJTs, case (1,0) & (0,1) would produce similar results. So, when one of the inputs is low, its BJT will be in cut-off and the other one's will be in saturation for the same reason as in the case of NOT gate. Now that one BJT is in saturation, its collector voltage (V_C) will be set to '0.2 V'. So, $V_Y = 0.2\,V$. Which is a low voltage. The collector current of this BJT (in saturation) will be non-zero and will depend on the external circuit (V_{CC} & R_C). Its base voltage (V_B) will be '0.8 V' too. So, the analysis will be similar to the NOT gate's case (1).

Case(1,1): When both inputs are high, both the BJTs will be in saturation. Then both their collector voltages will be set to '0.2 V'. So, again we get $V_Y = 0.2\,V$, a low output voltage. However, for this case, the current through R_C will split into two separate collector currents ($I_{R_C} = I_{C_A} + I_{C_B}$).

Let's look at the power dissipation related stuffs.

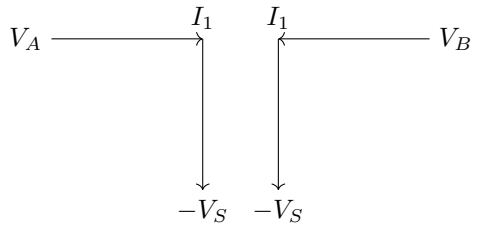


Figure 6.11: Power dissipation diagram for Case (0,0)

$P_{(0,0)} = 2 \times (V_A - (-V_S)) \times I_1$

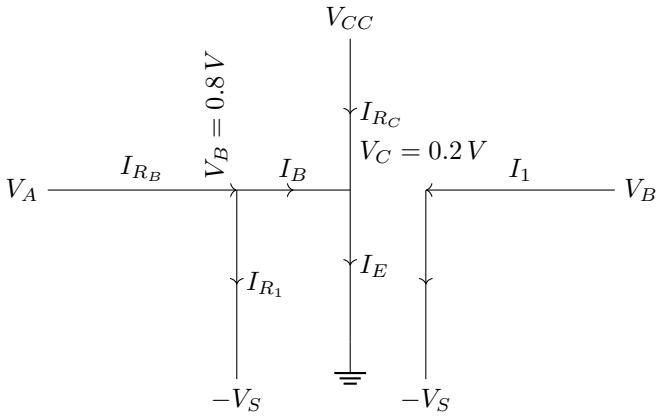


Figure 6.12: Power dissipation diagram for Case(1,0)

$P_{(1,0)} = (V_A - 0.8) \times I_{R_B} + (0.8 - (-V_S)) \times I_{R_1} + (0.8 - 0) \times I_B + (V_{CC} - 0) \times I_{R_C} + (V_B - (-V_S)) \times I_1$

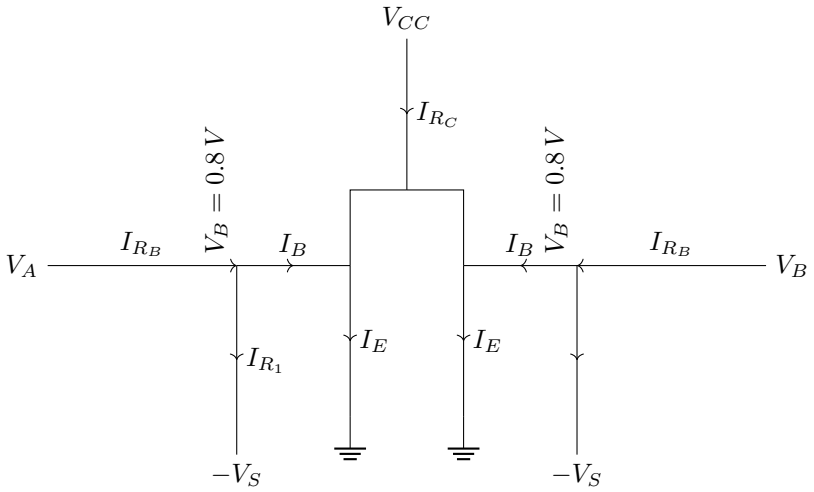


Figure 6.13: Power dissipation diagram for Case(1,1)

$P_{(1,1)} = 2 \times [(V_A - (-V_S)) \times I_{R_B} + (V_B - 0) \times I_B] + (V_{CC} - 0) \times I_{R_C}$

Noise Margin

The maximum amount of noise voltage that can be tolerated by a logic circuit while completing a successful transmission of signal from output to input. It occurs due to the unwanted interference of random voltages or signals in the transmission line between output of one logic circuit and input of another consequent one. Noise margin is the protective measure maintained in digital communication to prevent the effect of these noises.

Recall from Diode Logic, we had two thresholds of the output of a logic circuit— the upper & lower thresholds (V_{OH} & V_{OL}). These are selected keeping in mind the minimum value of high output & maximum value of low output possible from that circuit respectively. We have similar thresholds at the input of a logic circuit as well. These are denoted by V_{IH} & V_{IL}. These are the values of the minimum value of the input voltage, that we want our logic circuit to treat as 'high' logic, and the maximum value which we would consider to be a 'low' logic respectively.

Consider the case of two logic circuits cascaded, i.e. one's output is fed to the input of the other. We call the first stage in such a cascaded connection **the driver**. The circuits (if there are multiple) which are fed the output of this driver are called **loads**.

Now, the lowest possible high output from the driver is V_{OH} of that circuit. This has to be greater than the V_{IH} of the loads, otherwise, the load circuits will not recognize it as a high input. But should V_{OH} & V_{IH} be equal?

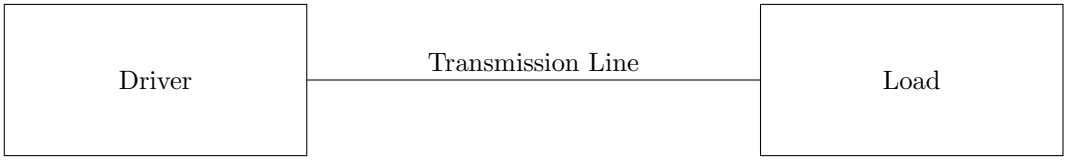


Figure 6.14: A cascaded two stage digital communication system

The problem of doing so, is the noise in the transmission line. Let a negative voltage is present as a noise in the line. Then it will reduce the output voltage from the driver below V_{OH} ($V_o' = V_{OH} - V_N$). Thus, if we make $V_{IH} = V_{OH}$, this reduced value (V_o') will not be treated as a high input at the loads. Similar reasoning can be done for the case of low output. Noise voltage can be positive and increase an output near the value of V_{OL}. This, then cannot be determined as a low input at the load, if we had set $V_{IL} = V_{OL}$.

The above discussion should lead us to this conclusion— we need to select V_{IH} to a lower value than V_{OH} to tackle the possibility of the presence of negative noise in the transmission line. Similarly, we need to choose a V_{IL}, which is higher enough than V_{OL}, so that it can detect a low input irrespective of the presence of positive noises. All these can be depicted in the following diagram:

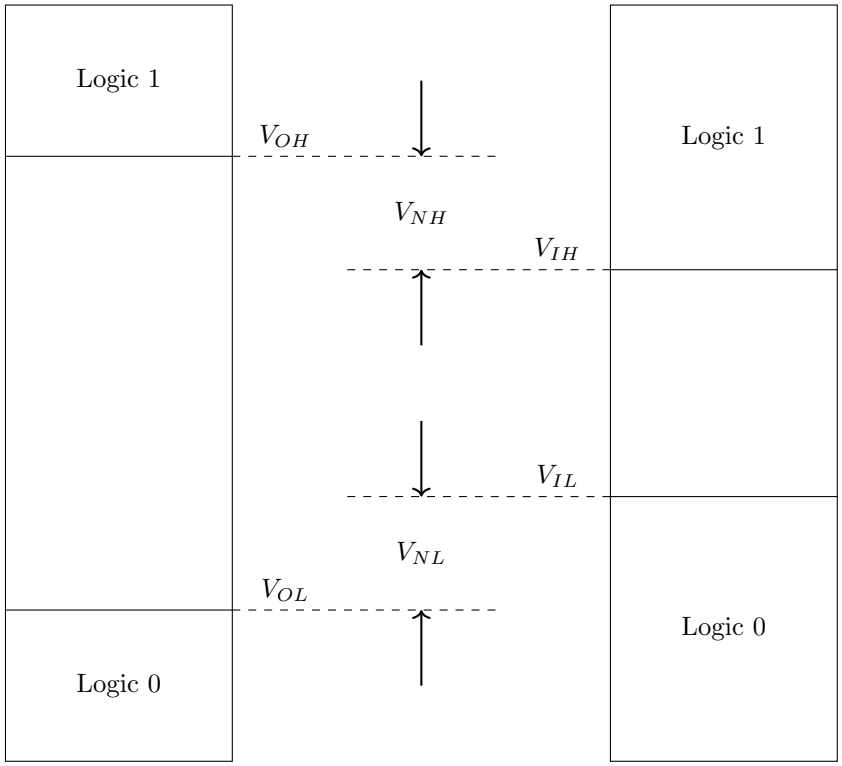


Figure 6.15: Noise Margins & Voltage Thresholds

So, there are two noise margins—

$$V_{NH} = V_{OH} - V_{IH} \tag{6.1}$$

$$V_{NL} = V_{IL} - V_{OL} \tag{6.2}$$

They are respectively called the high noise margin and the low noise margin. Well which one should be our **overall noise margin**? One thing to note here is that not necessarily V_{NH} and V_{NL} will be the same. They can and most often differ. Also, although we have discussed the noise margin introduction from the POV of we choosing the thresholds, often these are not in our hands to set. Thus, the thresholds and consequently the noise margins are often the characteristics of the logic circuits.

Now, coming back to our question. If we want to define an overall noise margin, which one should we select? Well noise margin is the amount of tolerance of a logic circuit. We must assume the worst and build other things based on this scenario. For example, if $V_{NH} > V_{NL}$, and you choose V_{NH} as your overall margin, then it will be a wrong decision. Because when the output from the driver is low, chances are that noises of positive magnitude, greater than V_{NL} can be present. It will then not be able to prevent the effect due to a smaller low noise margin. So, we construct our transmission line and other stuffs considering that the system can at best

tolerate the minimum of the two noise margins.

Overall Noise Margin, $V_N = min(V_{NH}, V_{NL})$

Now how do we calculate the noise margin for our logic circuits? Well, we need to find the output thresholds of the driver circuit and the input thresholds of the load circuits. While calculating these thresholds, we may need to perform separate analysis on driver & load circuits if needed. For example, we have already learnt how to find the output thresholds in case of diode logic circuits. Those methods can mostly be used in case of other logic circuits too if applicable. But mostly there will be exceptions.

As we have now studied RTL circuits, let's talk about how to find their thresholds. Firstly, the lower threshold V_{OL} of RTL circuits is fixed at 0.2 or 0.1 V depending on the manufacturer. This is a fixed parameter of the saturation mode of a BJT. So, we don't need to find it separately. Now, in case of V_{OH}, it mostly depends on our choice. Why? Because we have seen till now, that when operating separately, the RTL circuits output the V_{CC} (source voltage) as the high output due to the BJT being an open circuit. However, when there are are loads connected to the driver RTL circuit, the path from V_{CC} will not remain open anymore. Rather, it will supply current to the loads (for current drawing type loads, e.g. the OR gate). So, there will be a drop across R_C, resulting in a reduced voltage at the output terminal. Now, it is up to us to decide how low are we willing to accept the output voltage as a high output. That would be the V_{OH}. So, mostly the V_{OH} is given where needed.

Next, how to get the input thresholds? This is not usually a fixed parameter and needs analysis on the load circuits. The concept in finding the input thresholds is— what value of input would cause the electronic components of the load circuit to change their operating mode from the required one for that input logic. For example if we apply enough high voltage at the base such that $V_{BE} > 0.5\,V$, then the BJT would move to saturation or forward active from cut-off. Which will result in a wrong output if the desired operating mode of the BJT is cut-off for that particular logic. So, we can perform analysis to find this minimum input voltage that would turn on the BJT from cut-off. This is the input lower threshold(V_{IL}), since for low inputs, the BJT is supposed to remain in cut-off. A similar approach can be made to find V_{IH}. When the input is high, the BJT is expected to operate in saturation mode. If the input gets reduced, the base current will be smaller. However, the collector current would not change, since while in saturation, the collector voltage is fixed at '0.2 V'. This causes β_{forced} to rise. Now, we know that to remain in saturation, β_{forced} must be lower than β_F. So, due to this rise of β_{forced}, the BJT will shift to forward active mode from saturation once $\beta_{forced} = \beta_F$. So, V_{IH} is this minimum value of high input for which this occurs. Hopefully, all this will be clear once you go through examples related to noise margin in problem rosters.

Fanout

Fanout is the number of loads connected to a driver circuit. Maximum fanout is the maximum number of loads that can be connected to the driver, without malfunctioning its logic operation.

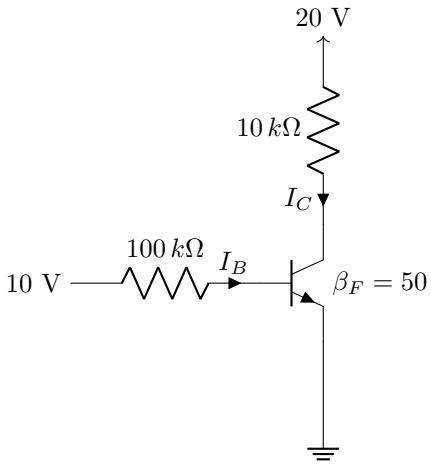
How do we find the maximum fanout of a circuit? It depends on the type of load connected. In case of RTL logic circuits, if the load is of current drawing type, we calculate the maximum suppliable current for all input cases of the driver to the loads. This is then divided by the individual current demand of a load. The floored value of this ratio is the maximum allowable fanout for the corresponding input case. The minimum of this for all input cases is the overall maximum fanout for the circuit under study.

On the other hand, if the load delivers current to the driver instead, this causes an increase in the collector current of the BJT (since loads are connected to the collector of the driver) in the input cases when the BJT is in saturation. If too many loads are connected, the rise in I_C can be sufficient enough to cause $\beta_{forced} = \beta_F$. Which will cause the circuit to malfunction. So, the maximum fanout for this input case is found from the marginal condition of $\beta_{forced} = \beta_F$.

If for any input cases, the connection between the driver and load cut out due to open circuit (typically this happens in case of loads which deliver current to the driver), then the maximum allowable fanout for those input cases is infinity. This is because as there will be no connection between driver and load, it doesn't matter how many loads are there.

Problems Roster

Problem 1:



Assuming the given BJT is in forward active mode—

(a)	Find I_B, I_C & I_E.
(b)	Find V_C.
(c)	Verify if the BJT is in forward active mode.

Solution:

(a) In forward active mode, $V_{BE} = 0.7\,V$. Since $V_E = 0\,V$, $V_B = 0.7\,V$. So,

$$I_B = \frac{10 - 0.7}{100k} = 0.093\,mA$$

$$\therefore I_C = \beta_F I_B = 50 \times 0.093 = 4.65\,mA$$

$$\therefore I_E = I_C + I_B = 4.743\,mA$$

(b) $V_C = 20 - I_C \times 10 = -26.5\,V$

(c) $V_{CE} = -26.5 - 0 = -26.5 < 0.2\,V$. So, the BJT is not operating in forward active mode and our assumption was wrong.

Problem 2:

Assuming saturation mode for the BJT in **Problem 1**—

(a)	Find I_B, I_C & I_E.
(b)	Verify if the BJT is in saturation mode.

Solution:

(a) For saturation mode, $V_{BE} = 0.8\,V$. Since $V_E = 0\,V$, $V_B = 0.8\,V$. So,

$$I_B = \frac{10 - 0.8}{100} = 0.092\,mA$$

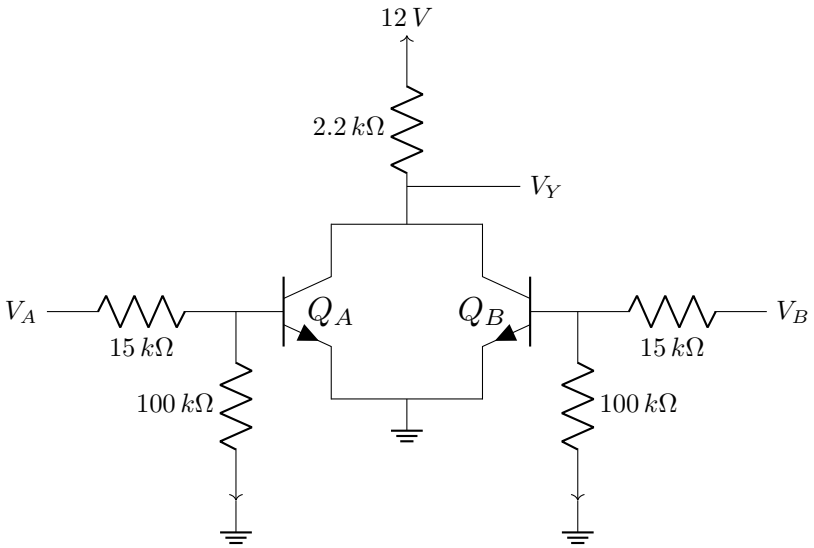
Also, $V_{CE} = 0.2\,V$. So, $V_C = 0.2\,V$.

$$\therefore I_C = \frac{20 - 0.2}{10} = 1.98\,mA$$

$$\therefore I_E = I_C + I_B = 2.072\,mA$$

(b) $\beta_{forced} = \dfrac{I_C}{I_B} = 21.52 < \beta_F$

Problem 3:



For both Q_A & Q_B, $\beta_F = 30$.

(a)	Determine the output voltage for all input cases.
(b)	What are the high & low thresholds of the output voltage?
(c)	If the '100 $k\Omega$' of 'Q_B' is doubled, find the new I_B of Q_B. Will it still satisfy saturation mode conditions for Q_B in case of (1,1) & (0,1)?

Solution:

(a) Case (0,0): Q_A & Q_B both in cut-off. So, $I_{R_C} = 0$. Thus, $V_Y = 12\,V$.

Case (0,1): Q_A in cut-off & Q_B in saturation. So, $V_Y = V_C = 0.2\,V$.

Case (1,0): Similar as case (0,1), $V_Y = 0.2\,V$.

Case (1,1): Q_A & Q_B are both in saturation. So, $V_Y = V_C = 0.2\,V$.

(b) $V_{OH} = 12\,V$, $V_{OL} = 0.2\,V$.

(c) $I_{B_{new}} = \dfrac{12 - 0.8}{15} - \dfrac{0.8}{200} = 0.743\,mA$

For (0,1): $I_{C_B} = I_{R_C} = \dfrac{12 - 0.2}{2.2} = 5.363\,mA$

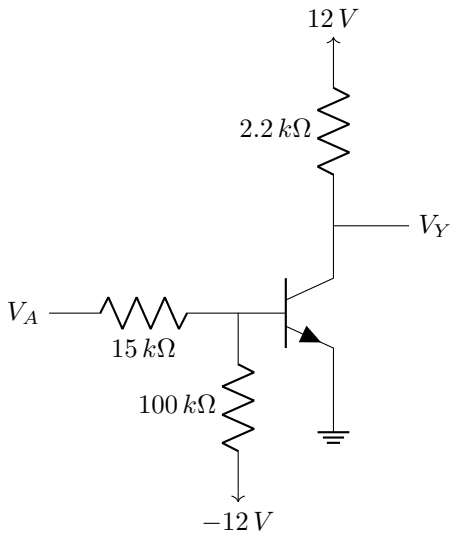
$$\beta_{forced} = \frac{5.363}{0.743} = 7.22 < \beta_F$$

For (1,1): $I_{C_B} = \dfrac{I_{R_C}}{2} = 2.682\,mA$

$$\beta_{forced} = \frac{2.682}{0.743} = 3.6 < \beta_F$$

So, saturation mode conditions are satisfied.

Problem 4:



Find the maximum & average power dissipation of the RTL NOT gate shown.[Assume low input=0.2 V, high input = 12 V]

Solution:

Case (0): $P_0 = (0.2 - (-12)) \times \dfrac{0.2 - (-12)}{15 + 100} = 1.29\,mW$

Case (1): $P_1 = (12{-}0.8) \times \dfrac{12 - 0.8}{15} + (0.8{-}(-12)) \times \dfrac{0.8 + 12}{100} + (0.8{-}0) \times \left(\dfrac{12 - 0.8}{15} - \dfrac{0.8 - (-12)}{100} \right) +$

$(12 - 0) \times \dfrac{12 - 0.2}{2.2} = 74.86\,mW$

$\therefore P_{max} = 74.86\,mW$

$\therefore P_{avg} = \dfrac{74.86 + 1.29}{2} = 38.075\,mw$

Problem 5:

For the RTL inverter in **Problem 4**, if the '-12 V' was replaced with a ground, find the ratio of maximum and minimum dissipated power.

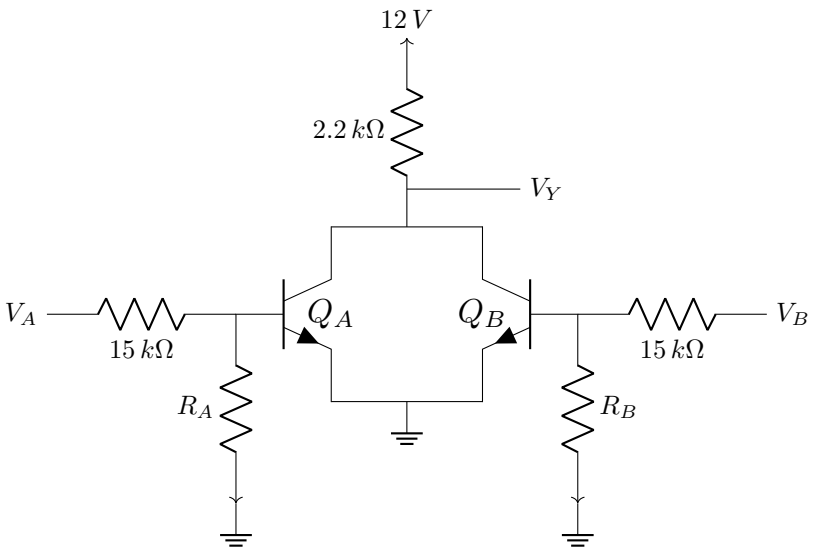
Solution:

Case (0): $P_0 = (0.2 - 0) \times \dfrac{0.2 - 0}{15 + 100} = 0.35\,\mu W$

Case (1): $P_1 = (12 - 0) \times \dfrac{12 - 0.8}{15} + (12 - 0) \times \dfrac{12 - 0.2}{2.2} = 73.32\,mW$

$\therefore \dfrac{P_{max}}{P_{min}} = \dfrac{P_1}{P_0} = 209496.1 : 1$

Problem 6:



For the given circuit, if $R_A = R_B$—

(a)	If the power dissipation for the logic case (0,0) is $0.5\,\mu W$, find the value of the resistances.
(b)	Find a new value of R_C to halve the value of maximum power dissipation of the circuit.

Solution:

(a) Case (0,0):

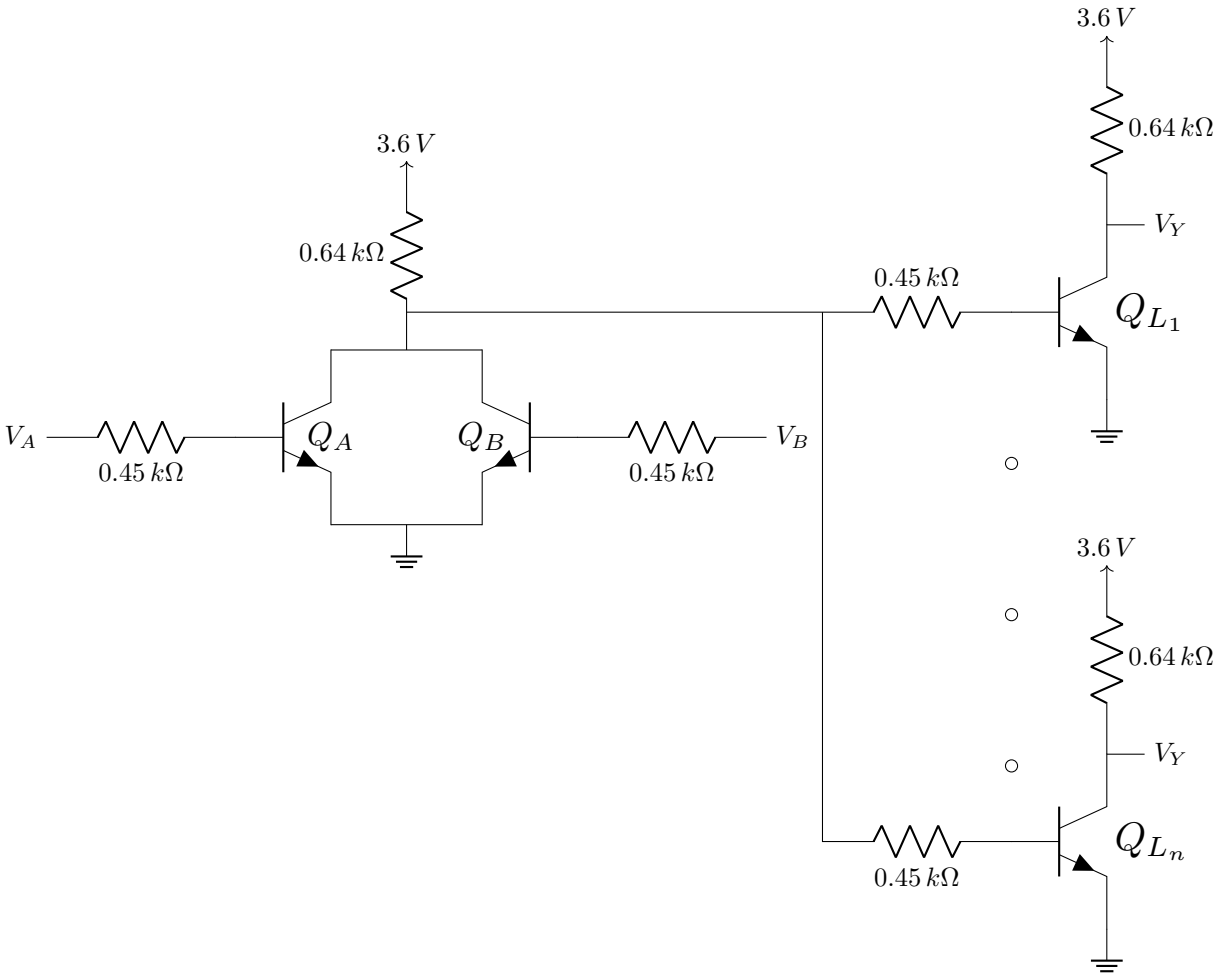
$$P_{(0,0)} = 2 \times (0.2 - 0) \times \frac{0.2 - 0}{15 + R_A} = 0.5 \times 10^{-3} \Rightarrow R_A = 145\,k\Omega$$

(b) $P_{max} = P_{(1,1)} = 2 \times (12 - 0) \times \dfrac{12 - 0.8}{15} + (12 - 0) \times \dfrac{12 - 0.2}{2.2} = 82.28\,mW$

$$P'_{max} = \frac{1}{2} \times 82.28 = 41.14\,mW$$

Now, $P'_{max} = 2 \times (12 - 0) \times \dfrac{12 - 0.8}{15} + (12 - 0) \times \dfrac{12 - 0.2}{R'_C} \Rightarrow R'_C = 6.098\,k\Omega$

Problem 7:



If for the given RTL NOR driver & RTL NOT loads, $\beta_F = 30$, $V_{OH} = 3.5\,V$ & $V_{OL} = 0.2\,V$, find the noise margin.

Solution:

Determination of V_{IH}: This is the minimum high input for which the load transistors will shift to forward active from saturation. The marginal condition is $\beta_{forced} = \beta_F$.

$$I_B = \frac{V_{IH} - 0.8}{0.45}$$

$$I_C = \frac{3.6 - 0.2}{0.64} = 5.3125\,mA$$

$$\therefore \beta_{forced} = \frac{I_C}{I_B} = \frac{5.3125}{\frac{V_{IH} - 0.8}{0.45}} = \beta_F = 30$$

$$\Rightarrow V_{IH} = 0.88\,V$$

Determination of V_{IL}: This is the maximum low input for which the load transistors will turn on from cut-off. The marginal condition is $V_{BE} = 0.5\,V$. Since $I_B = 0$ in cut-off,

$$\frac{V_{IL} - 0.5}{0.45} = 0 \Rightarrow V_{IL} = 0.5\,V$$

$$\therefore V_{NH} = V_{OH} - V_{IH} = 3.5 - 0.88 = 2.62\,V$$

$$\therefore V_{NL} = V_{IL} - V_{OL} = 0.5 - 0.2 = 0.3\,V$$

$$\therefore V_N = min(V_{NH}, V_{NL}) = 0.3\,V$$

Problem 8:

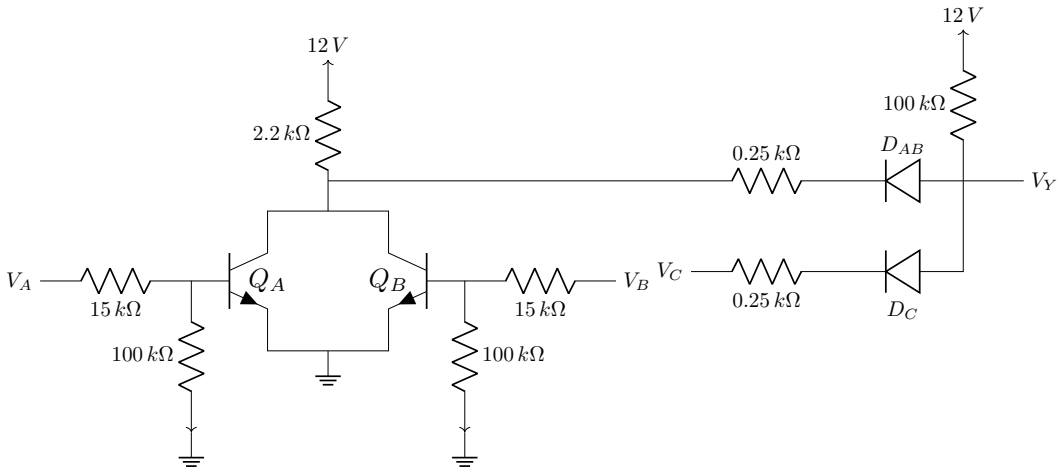
What value of the resistance connected to the base would make $V_{N_H} = V_{N_L}$?

Solution:

$$V'_{IH} = V_{OH} - V_{N_H} = 3.5 - 0.3 = 3.2\,V$$

$$\frac{V'_{IH} - 0.8}{R'_B} = \frac{I_C}{\beta_F} = \frac{5.3125}{30} \Rightarrow R'_B = 13.55\,k\Omega$$

Problem 9:



For the given circuit $V_{OH} = 11.5\,V$, $V_{OL} = 0.2\,V$, $\beta_F = 25$, high input = 12 V, low input = 0 V.

(a)	What boolean function is the circuit implementing? Which is the driver & which is the load?
(b)	Find the maximum fanout.
(c)	Find the maximum power dissipation considering maximum fanout number of loads are connected.

Solution:

(a) $Y = \overline{(A+B)}C$. Driver is a NOR gate, while load is an AND gate.

(b) There are four possible outputs of the driver NOR gate. We will split our analysis in two parts— for high & low output cases of the driver.

Case (0,0) is the only case when the output of the NOR gate will be high. Assuming the output to be V_{OH}, this high output will cause D_{AB} to be in reverse bias and thus will remain off. This results in no connection between driver and load circuit. So, the maximum fanout for this case is infinity (∞).

Case (0,1), (1,0) and (1,1): For all these cases, the output will be V_{OL}. This will cause D_{AB} to be on. Now, the maximum current that can be delivered from the load AND gate is for the case when V_C is high (since the full current from 12 V source will flow through D_{AB}). This current will cause a rise in the collector current of the driver BJTs. We will consider (0,1) or (1,0), because the full current will go through a single BJT, unlike in (1,1) when they will be split in half. So, the increased collector current for those cases would be,

$$I_c' = I_{2.2\,k\Omega} + N \times I_{D_{AB}} = \frac{12 - 0.2}{2.2} + N \times \frac{12 - V_Y}{100}$$

Now, KCL at 'Y',

$$\frac{12 - V_Y}{100} = \frac{V_Y - 0.7 - 0.2}{0.25} \Rightarrow V_Y = 0.93\,V$$

The maximum fanout for these cases can be found from the marginal condition, $\beta_{forced} = \frac{I'_C}{I_B} = \beta_F$.

$$I'_C = 25 \times I_B = 25 \times \left(\frac{12 - 0.8}{15} - \frac{0.8 - 0}{100}\right)$$

$$\Rightarrow 5.363 + N \times \frac{12 - 0.93}{100} = 25 \times 0.74 \Rightarrow N = floor(118.67) = 118$$

$\therefore$ Maximum fanout = min(∞, 118) = 118

(c) Maximum power case (1,1,0) as this turns on all BJTs and diodes of driver and loads. KCL at 'Y' for this case,

$$\frac{12 - V_Y}{100} = \frac{V_Y - 0.7 - 0.2}{0.25} + \frac{V_Y - 0.7 - 0}{0.25} \Rightarrow V_Y = 0.814\,V$$

$$P_{(1,1,0)} = (12 - 0) \times I_{R_C} + 2 \times (12 - 0) \times I_{15\,k\Omega} + 118 \times (12 - 0) \times I_{100\,k\Omega}$$

$$= 12 \times [\frac{12 - 0.2}{2.2} + 2 \times \frac{12 - 0.8}{15} + 118 \times \frac{12 - 0.814}{100}] = 240.67\,mW$$

Problem 10:

If for the driver in **Problem 7**, $V_{OH} = 1.3\,V$—

(a)	Find the maximum fanout.
(b)	Find the output voltage of the driver if number of loads, N = 5 and both inputs to the driver are low.
(c)	Find the $(\beta_F)_{min}$ (for the loads) and the power dissipation of the loads for the conditions in (b).
(d)	Find the power dissipation in the driver only when both inputs are high.
(e)	What logic function does the driver and load combination implement?

Solution:

(a) Case (0,0) when the driver output is high: the load NOT gates draw current from the driver and are in saturation. for maximum number of loads, assuming V_{OH} to be the output of the driver, each load draws a current of—

$$I_L = \frac{V_{OH} - 0.8}{0.45} = \frac{1.3 - 0.8}{0.45} = 1.11\,mA$$

Maximum suppliable current from the driver—

$$I_{supply} = \frac{3.6 - V_{OH}}{0.64} = 3.59\,mA$$

Thus, the maximum fanout for this case = floor $\left(\frac{3.59}{1.11}\right) = 3$

Case (0,1), (1,0), (1,1): For these cases, the output of the NOR gate driver is low (0.2 V). So, the load NOT gates will be in cut-off. As there is no extra resistance from the base of the loads to the ground, the loads will not draw any current as $I_B = 0$. So, any number of loads can be connected to the driver. Thus, maximum fanout for these cases is ∞.

The overall fanout = min $(\infty, 3) = 3$

(b) Since both inputs are low, the driver BJTs will be in cut-off. However, the output voltage of the driver (say V_o) will not be the source voltage, since there are loads connected to it. The load BJTs will be on, due to a high voltage at their bases. Since, N = 5, the KCL equation at the output of the driver would be,

$$\frac{3.6 - V_o}{0.64} = 5 \times \frac{V_o - 0.8}{0.45} \Rightarrow V_o = 1.15\,V$$

(c) The minimum β_F is the β_{forced} of the BJT for a certain condition. Using the results obtained in (b),

$$I_B = \frac{1.15 - 0.8}{0.45} = 0.78\,mA$$

$$I_C = \frac{3.6 - 0.2}{0.64} = 5.3125\,mA$$

$$\therefore \beta_{forced} = (\beta_F)_{min} = \frac{I_C}{I_B} = \frac{5.3125}{0.78} = 6.81$$

$$P = (1.15 - 0) \times \frac{3.6 - 1.15}{0.64} + 5 \times (3.6 - 0) \times \frac{3.6 - 0.2}{0.64} = 100.27\,mW$$

(d)

$$P = (3.6 - 0) \times \frac{3.6 - 0.2}{0.64} + 2 \times (3.6 - 0) \times \frac{3.6 - 0.8}{0.45} = 63.925\,mW$$

(e) $Y = \overline{A + B}$

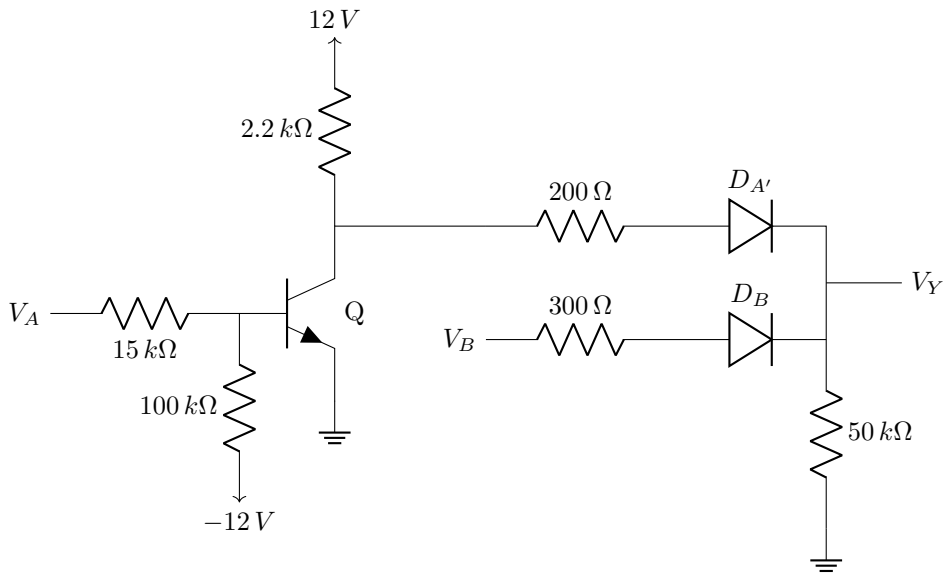
Problem 11:

Find the value of V_{OH} for which the maximum fanout in **Problem 10** would be '2'.

Solution:

$$\frac{3.6 - V'_{OH}}{0.64} = \frac{V'_{OH} - 0.8}{0.45} \times 2 \Rightarrow V'_{OH} = 1.53\,V$$

Problem 12:



For the BJT 'Q' in the above circuit, $V_{OH} = 10\,V$, $V_{OL} = 0.2\,V$, $\beta_F = 30$.

(a)	Find the maximum fanout.
(b)	Find the maximum power dissipation considering maximum fanout number of loads connected.

Solution:

(a) Case (1): Q is in saturation. Low output voltage from the driver causes $D_{A'}$ to be off. Thus, no connection between driver & load. So, maximum fanout = ∞.

Case (0): Q is in cut-off. Worst case from p.o.v. of load is when $V_B = 0$ and the $D_{A'}$ branch needs to drive the output V_Y high. However, we have the constraint that the output from the driver cannot fall below V_{OH}.

$$I_L = \frac{V_{OH} - 0.7 - 0}{0.2 + 50} = 0.185\,mA$$

$$I_{supply} = \frac{12 - V_{OH}}{2.2} = 0.91\,mA$$

So,

$$I_{supply} = N \times I_L \Rightarrow N = floor(\frac{0.91}{0.185}) = 4$$

$\therefore$ Maximum fanout = min (∞, 4) = 4

(b) Case ($V_A = 12\,V$, $V_B = 12\,V$):

$$P = (12-0)\left(\frac{12-0.8}{15} - \frac{0.8-(-12)}{100}\right) + (12-(-12)) \times \frac{0.8-(-12)}{100} + (12-0) \times \frac{12-0.2}{2.2}$$

$$+4 \times (12-0) \times \frac{12-0.7-0}{0.3+50} = 84.21\,mW$$

Case ($V_A = 12\,V$, $V_B = 0\,V$):

$$P = (12-0)\left(\frac{12-0.8}{15} - \frac{0.8-(-12)}{100}\right) + (12-(-12)) \times \frac{0.8-(-12)}{100} + (12-0) \times \frac{12-0.2}{2.2} = 73.43\,mW$$

Case ($V_A = 0\,V$, $V_B = 12\,V$):

Let output of the driver is V_o. KCL at output of the driver,

$$\frac{12 - V_o}{2.2} = \frac{V_o - 0.7 - V_Y}{0.2}$$

KCL at 'Y',

$$\frac{V_o - 0.7 - V_Y}{0.2} + \frac{12 - 0.7 - V_Y}{0.3} = \frac{V_Y}{50}$$

Solving, $V_o = 11.95\,V$, $V_Y = 11.24\,V$.

$$P = (0.2 - (-12)) \times \frac{0.2 - (-12)}{15 + 100} + (12 - 0) \times \frac{12 - 11.95}{2.2} + 4 \times (12 - 0) \times \frac{12 - 0.7 - 11.24}{0.3}$$

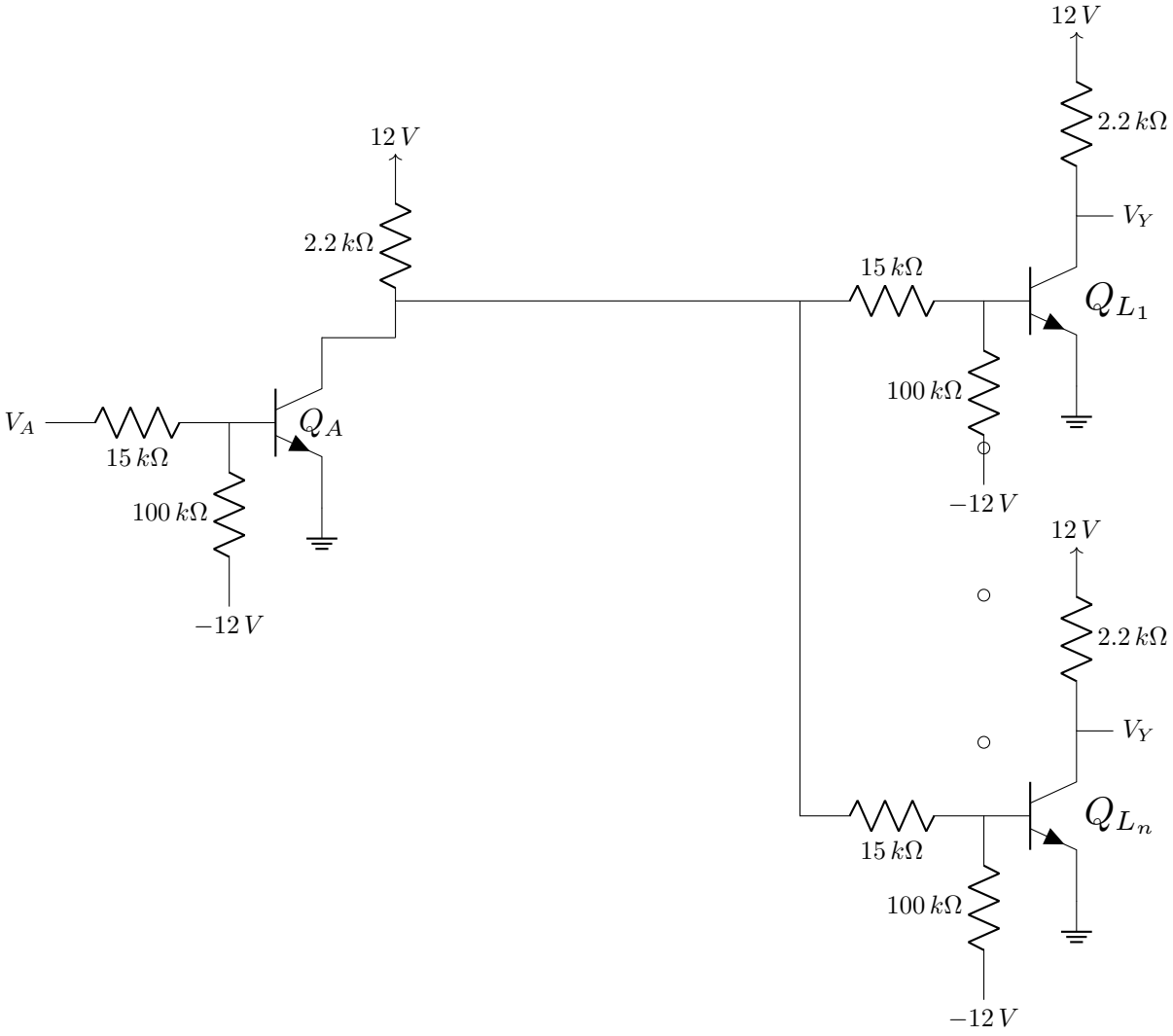
$$= 11.167\,mW$$

Case ($V_A = 0\,V$, $V_B = 0\,V$):

$$P = (0.2 - (-12)) \times \frac{0.2 - (-12)}{15 + 100} + (12 - 0) \times \frac{12 - 10}{2.2} = 65.66\,mW$$

$\therefore P_{max} = 84.21\,mW$

Problem 13:



For the given RTL inverter driver and loads, $V_{OH} = 10\,V$, $V_{OL} = 0.2\,V$, $\beta_F = 30$.

(a)	Find the maximum fanout.
(b)	Find the output of the driver, V_o, for N=2 loads, and when the input to the driver is low.
(c)	If V_A is high and the fanout is '1', find the power dissipation of the driver circuit.
(d)	If V_A is low and the fanout is '2', find the power dissipation of the total circuit.
(e)	Find the noise margin.

Solution:

(a) Case (0): Q_A in cut-off. Load BJTs will be in saturation.

$$I_{supply} = N \times I_L$$

$$\Rightarrow \frac{12 - V_{OH}}{2.2} = N \times \frac{V_{OH} - 0.8}{15}$$

$$\Rightarrow \frac{12 - 10}{2.2} = N \times \frac{10 - 0.8}{15} \Rightarrow N = floor(1.21) = 1$$

The maximum fanout for this case is 1.

Case (1): Q_A in saturation, load BJTs will be cut-off. However, the loads will still draw a current due to the '-12 V' source.

$$I_{supply} = \frac{12 - 0.2}{2.2} = 5.363\,mA$$

$$I_L = \frac{0.2 - (-12)}{15 + 100} = 0.106\,mA$$

$$\therefore N = floor\left(\frac{5.363}{0.106}\right) = 50$$

$\therefore$ The overall maximum fanout = min(1,50) = 1

(b) The driver BJT will be cut-off. However, due to the loads drawing current, the output will not be 12 V. KCL at the output of the driver,

$$\frac{12 - V_o}{2.2} = 2 \times \frac{V_o - 0.8}{15} \Rightarrow V_o = 9.46\,V$$

(c) Q_A will be in saturation. The load will be in cut-off. KCL at the output,

$$\frac{12 - 0.2}{2.2} = I_{C_A} + \frac{0.2 - (-12)}{15 + 100} \Rightarrow I_{C_A} = 5.26\,mA$$

$$P_{driver} = (12 - 0.8) \times \frac{12 - 0.8}{15} + (0.8 - 0) \times \left(\frac{12 - 0.8}{15} - \frac{0.8 - (-12)}{100}\right) +$$

$$(0.8 - (-12)) \times \frac{0.8 - (-12)}{100} + (12 - 0.2) \times \frac{12 - 0.2}{2.2} + (0.2 - 0) \times 5.26$$

$$= 74.84\,mW$$

(d) From (b), output for this scenario, $V_o = 9.46\,V$.

$$P = (0 - (-12)) \times \frac{0 - (-12)}{115} + (12 - 9.46) \times \frac{12 - 9.46}{2.2}$$

$$+2\times[(9.46-0)\times\left(\frac{9.46-0.8}{15}-\frac{0.8-(-12)}{100}\right)+(9.46-(-12))\times\frac{0.8-(-12)}{100}+(12-0)\times\frac{12-0.2}{2.2}]$$

$$= 146.91\,mW$$

(e) Determination of V_{IH}:

$$\frac{V_{IH}-0.8}{15}-\frac{0.8-(-12)}{100}=\frac{\frac{12-0.2}{2.2}}{\beta_F}$$

$$\Rightarrow V_{IH} = 5.4\,V$$

Determination of V_{IL}:

$$\frac{V_{IL}-0.5}{15}-\frac{0.5-(-12)}{100}=I_B=0$$

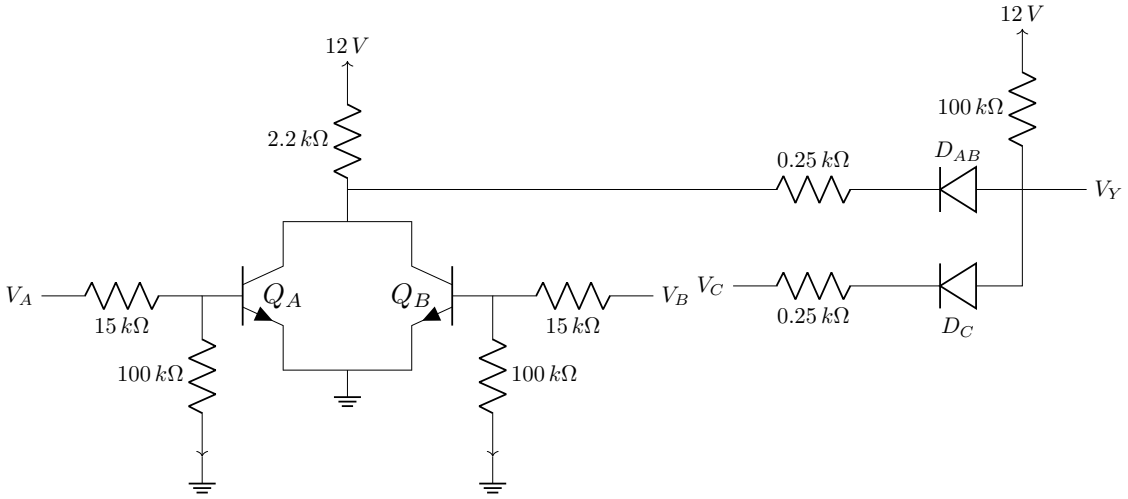
$$\Rightarrow V_{IL} = 2.375\,V$$

$$\therefore V_{NH} = V_{OH} - V_{IH} = 10 - 5.4 = 4.6\,V$$

$$\therefore V_{NL} = V_{IL} - V_{OL} = 2.375 - 0.2 = 2.175\,V$$

$$\therefore V_N = min(4.6, 2.175) = 2.175\,V$$

Problem 14:



For the given circuit, $V_{OH} = 10.5\,V$, $V_{OL} = 0.2\,V$, $\beta_F = 27.5$.

(a)	Find the maximum fanout.
(b)	Find the output voltage of the driver when **4n** number of loads are connected. Then find the average power dissipation of the **driver** for this condition.
(c)	Use additional required logic circuits to the above figure and implement the function $Y = A + B + \overline{C}$.

Solution:

(a) When driver's output is high: loads are disconnected. So, maximum fanout = ∞

When driver's output is low: Worst case is when input case of the driver is (0,1) or (1,0). When V_C is high, full current through the $100\,k\Omega$ of the loads are delivered to the driver. So,

$$I_C = I_{2.2\,k\Omega} + N \times I_L = \frac{12 - 0.2}{2.2} + N \times \frac{12 - 0.7 - 0.2}{100 + 0.25}$$

$$= 5.363 + 0.11N$$

$$I_B = \frac{12 - 0.8}{15} - \frac{0.8 - 0}{100} = 0.74\,mA$$

$$\therefore \beta_{forced} = \frac{I_C}{I_B} = \beta_F = 27.5$$

$$\Rightarrow \frac{5.363 + 0.11N}{0.74} = 27.5$$

$$\Rightarrow N = floor\left(\frac{27.5 \times 0.74 - 5.363}{0.11}\right) = 136$$

(b) For cases other than (0,0), the driver's output will be 0.2 V, due to one or both the BJTs being in saturation. So, it does not depend on the number of loads connected. For the case (0,0), the connection between the driver and the loads are cut off due to D_{AB} being off. Thus, the $2.2\,k\Omega$ of the driver will be open circuit and no current will flow. So, output voltage of the driver for this case will be 12 V.

For the cases when the driver's output is low, if V_C is low, D_C will be on. Then V_Y can be calculated from the KCL equation given below at 'Y',

$$\frac{12 - V_Y}{100} = \frac{V_Y - 0.7 - 0.2}{0.25} + \frac{V_Y - 0.7 - 0.2}{0.25} \Rightarrow V_Y = 0.91\,V$$

Power for each logic cases will be, [(A,B,C)]:

$$P_{(0,0,0)} = P_{(0,0,1)} = 2 \times (0.2 - 0) \times \frac{0.2 - 0}{15 + 100} = 0.695\,\mu W$$

$$P_{(0,1,0)} = P_{(1,0,0)} = (0.2{-}0){\times}\frac{0.2 - 0}{15 + 100}{+}(12{-}0){\times}\frac{12 - 0.8}{15 + 100}{+}(12{-}0){\times}\frac{12 - 0.2}{2.2}{+}4{\times}(0.2{-}0){\times}\frac{1}{2}{\cdot}\frac{12 - 0.91}{100}$$

$$= 65.58\,mW$$

$$P_{(0,1,1)} = P_{(1,0,1)} = (0.2-0)\times\frac{0.2-0}{15+100}+(12-0)\times\frac{12-0.8}{15+100}+(12-0)\times\frac{12-0.2}{2.2}+4\times(0.2-0)\times\frac{12-0.91}{100}$$

$$= 65.62\,mW$$

$$P_{(1,1,0)} = 2\times(12-0)\times\frac{12-0.8}{15+100}+(12-0)\times\frac{12-0.2}{2.2}+4\times(0.2-0)\times\frac{1}{2}\cdot\frac{12-0.91}{100}$$

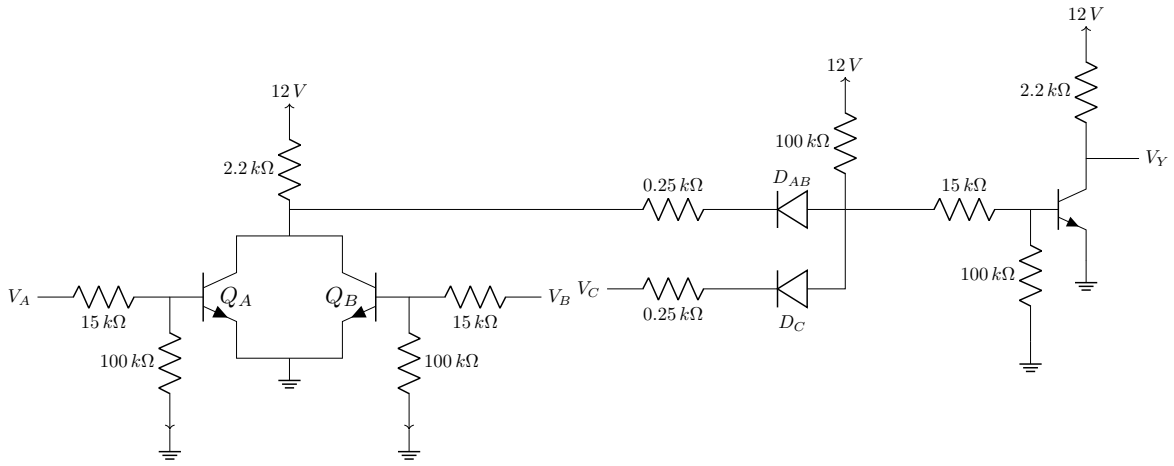
$$= 66.75\,mW$$

$$P_{(1,1,1)} = 2\times(12-0)\times\frac{12-0.8}{15+100}+(12-0)\times\frac{12-0.2}{2.2}+4\times(0.2-0)\times\frac{12-0.91}{100}$$

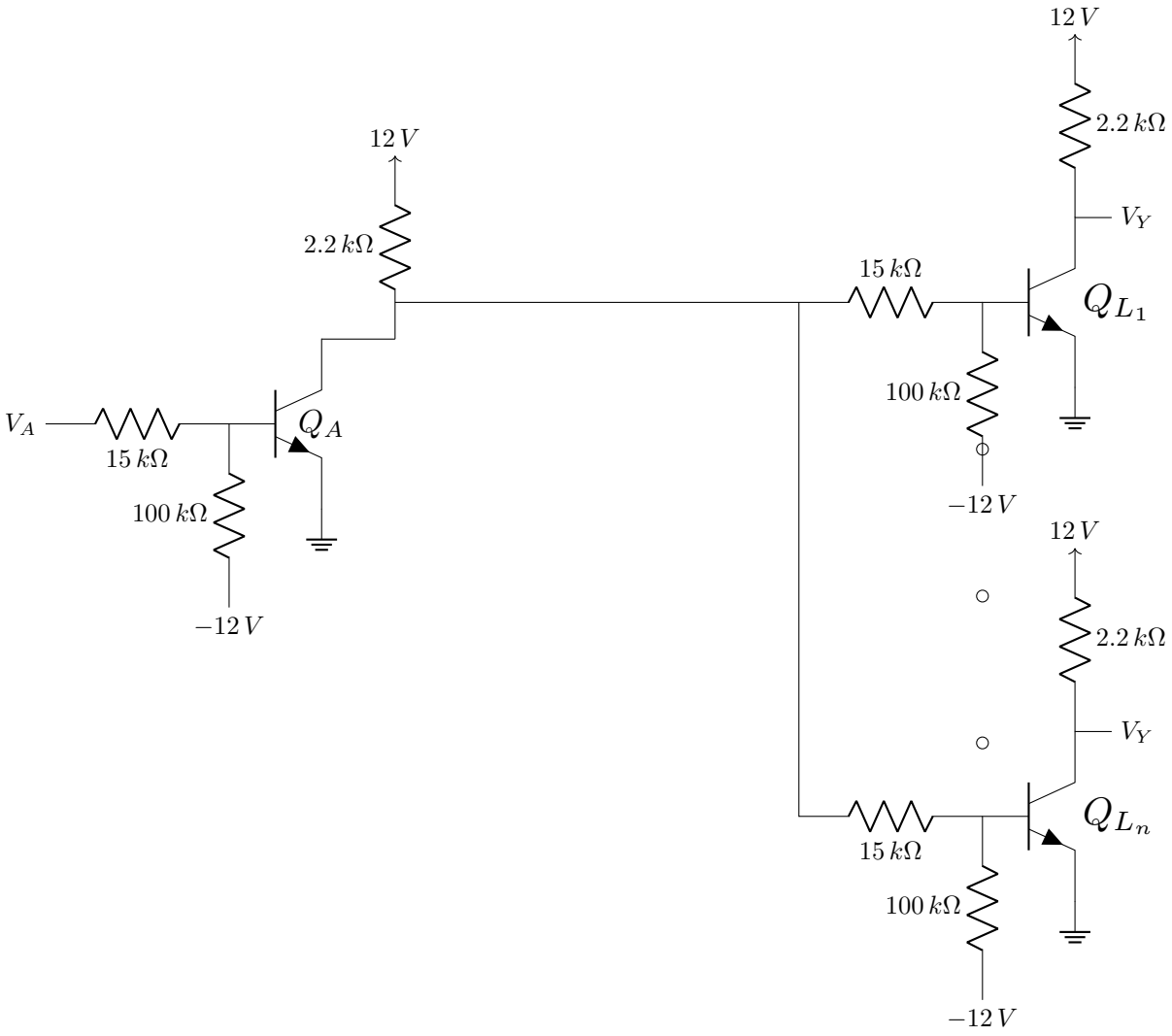
$$= 66.79\,mW$$

$$P_{avg} = \frac{0.695\times10^{-3}\times2+65.58\times2+65.62\times2+66.75+66.79}{8} = 49.49\,mW$$

(c)



Problem 15:



For the circuit given, $V_{OH} = 10.5\,V$, $V_{OL} = 0.1\,V$, $\beta_F = 27.5$.

(a)	Find the noise margin.
(b)	For the maximum fanout case, find the maximum power dissipation of the **full circuit**.

Solution:

(a) Determination of V_{IH}:

$$\beta_{forced} = \beta_F$$

$$\Rightarrow \frac{\frac{12-0.1}{2.2}}{\frac{V_{IH}-0.8}{15}-\frac{0.8-(-12)}{100}} = 27.5$$
$$\Rightarrow V_{IH} = 5.67\,V$$

Determination of V_{IL}:

$$\frac{V_{IL}-0.5}{15} = \frac{0.5-(-12)}{100} + 0$$
$$\Rightarrow V_{IL} = 2.375\,V$$

$$\therefore V_{NH} = V_{OH} - V_{IH} = 10 + \frac{5}{10} - 5.67 = 4.83\,V$$

$$\therefore V_{NL} = V_{IL} - V_{OL} = 2.375 - 0.1 = 2.275\,V$$

$$\therefore V_N = min(2.275, 4.83) = 2.275\,V$$

(b) Determination of maximum fanout:
When driver's output is high:

$$N = floor\left(\frac{\frac{12-10.5}{2.2}}{\frac{10.5-0.8}{15}}\right) = 1$$

When driver's output is low:

$$N = floor\left(\frac{\frac{12-0.2}{2.2}}{\frac{0.2-(-12)}{15+100}}\right) = 50$$

$\therefore$ Overall maximum fanout = min (1, 50) = 1.

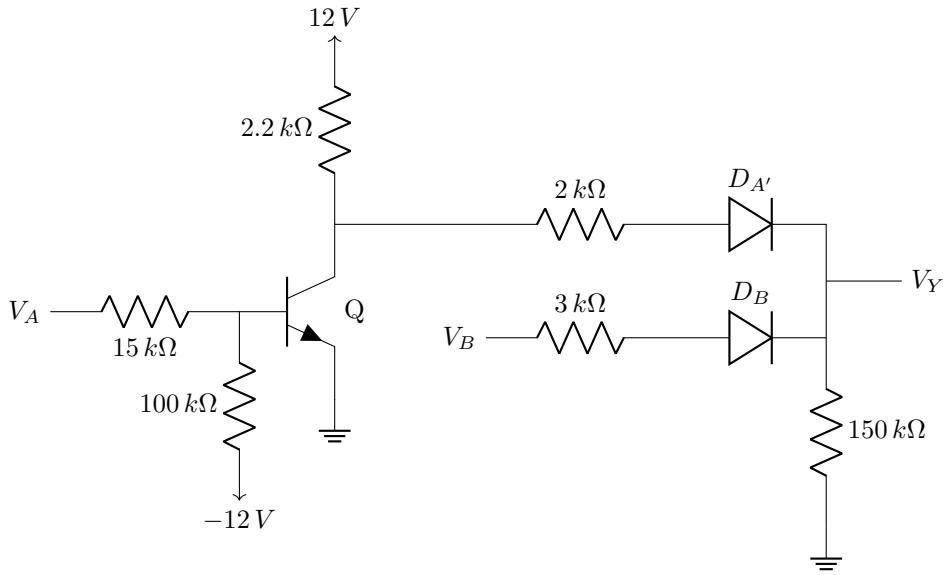
$$P_1 = (12-0.8)\times\frac{12-0.8}{15} + \frac{0.8-(-12)}{100} + (0.8-0)\times[\frac{12-0.8}{15} - \frac{0.8-(-12)}{100}] +$$
$$(12-0.2)\times\frac{12-0.2}{2.2} + (0.2-0)\times[\frac{12-0.2}{2.2} - \frac{0.2-(-12)}{15+100}] + (0.2-(-12))\times\frac{0.2-(-12)}{15+100} = 74.62\,mW$$

$$P_0 = (0.2-(-12))\times\frac{0.2-(-12)}{15+100} + (12-0.8)\times\frac{12-0.8}{2.2+15} + (0.8-(-12))\times\frac{0.8-(-12)}{100}$$

$$+(0.8-0)\times[\frac{12-0.8}{2.2+15}-\frac{0.8-(-12)}{100}]+(12-0)\times\frac{12-0.2}{2.2}=75\,mW$$

$\therefore P_{max}=P_0=75\,mW$

Problem 16:



For the given circuit, $V_{OH}=10.5\,V$, $V_{OL}=0.2\,V$, $\beta_F=27.5$.

(a)	Find the maximum fanout.
(b)	Find the output voltage of the driver when **n** number of loads are connected. Then find the average power dissipation of the **driver** for this condition.
(c)	Use additional required logic circuits to the above figure and implement the function $Y=A\overline{B}$.

Solution:

(a) When driver's output is high: Worst case is when V_B = low. So,

$$\frac{12-V_{OH}}{2.2}=N\times\frac{V_{OH}-0.7-0}{2+150}$$

$$\Rightarrow\frac{12-10.5}{2.2}=N\times\frac{10.5-0.7}{152}$$

$$\Rightarrow N=floor\left(\frac{0.682}{0.074}\right)=10$$

When driver's output is low: $D_{A'}$ is off, so no connection between driver & load. So, maximum fanout for this case will be ∞.

$\therefore$ Overall maximum fanout = min (∞, 10) = 10

(b) Case (A=1): Driver BJT in saturation. So, output of driver is 0.2 V. Now, the power dissipation in the driver for the cases when V_B = low & high are—

$$P_{(1,0)} = P_{(1,1)} = (12-0.8)\times\frac{12-0.8}{15}+(0.8-(-12))\times\frac{0.8-(-12)}{100}+(0.8-0)\times[\frac{12-0.8}{15}-\frac{0.8-(-12)}{100}]$$

$$+(12-0)\times\frac{12-0.2}{2.2} = 74.86\,mW$$

Case (A=0): Driver BJT is in cut-off. The output voltage of the driver, V_o and V_Y depends on V_B. For V_B = high, KCL at driver and load's output gives,

$$\frac{12-V_o}{2.2} = 5\times\frac{V_o-0.7-V_Y}{2}$$

$$\frac{V_o-0.7-V_Y}{2}+\frac{12-0.7-V_Y}{3} = \frac{V_Y-0}{150}$$

Solving, $V_o = 11.86\,V$, $V_Y = 11.14\,V$

For V_B = low, KCL at the driver's output,

$$\frac{12-V_o}{2.2} = 5\times\frac{V_o-0.7-0}{2+150} \Rightarrow V_o = 11.24\,V$$

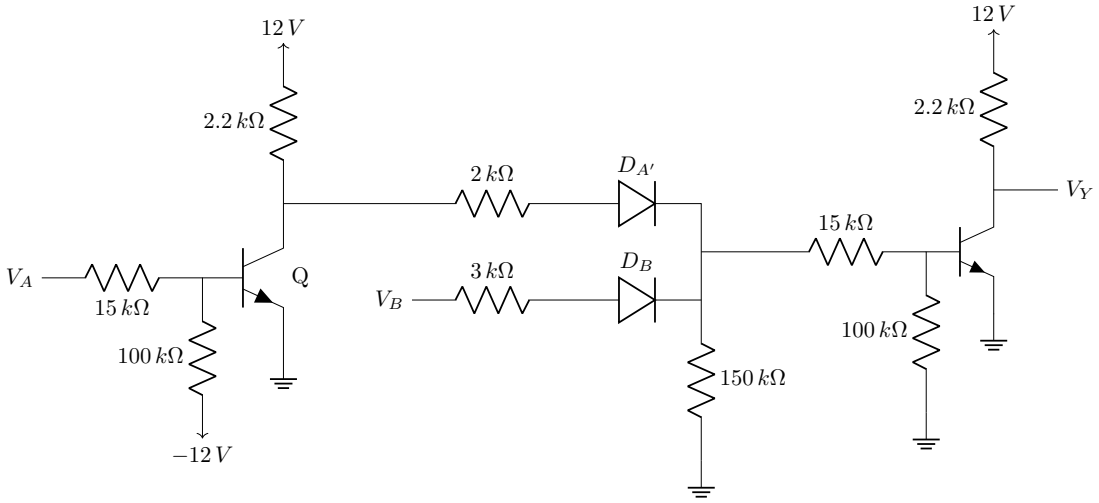
So, the power dissipation in the driver for these two cases are—

$$P_{(0,1)} = (0.2-(-12))\times\frac{0.2-(-12)}{15+100}+(12-11.86)\times\frac{12-11.86}{2.2} = 1.303\,mW$$

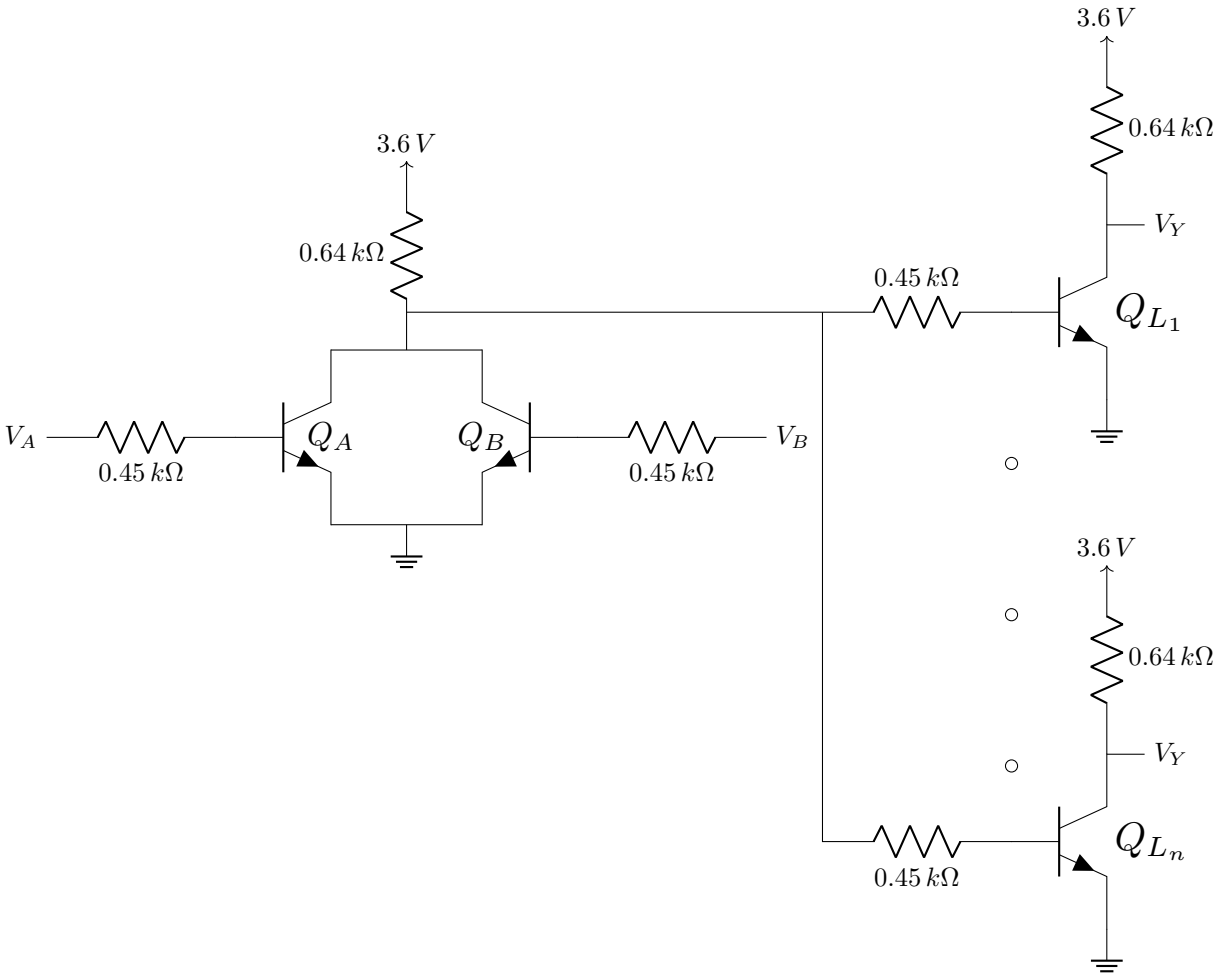
$$P_{(0,0)} = (0.2-(-12))\times\frac{0.2-(-12)}{15+100}+(12-11.24)\times\frac{12-11.24}{2.2} = 1.556\,mW$$

$$\therefore P_{avg} = \frac{1.556+1.303+74.86\times 2}{4} = 38.145\,mW$$

(c)


12 V
2.2 kΩ
2 kΩ
$D_{A'}$
V_A
15 kΩ
Q
3 kΩ
D_B
V_B
100 kΩ
−12 V
150 kΩ
12 V
2.2 kΩ
V_Y
15 kΩ
100 kΩ

Problem 17:



For the circuit given on the next page, $V_{OH} = 3.25\,V$, $V_{OL} = 0.1\,V$, $\beta_F = 27.5$.

(a)	Find the noise margin.
(b)	For the maximum fanout case, find the maximum power dissipation of the **full circuit**.

Solution:

(a) Determination of V_{IH}:

$$\frac{\frac{3.6 - 0.1}{0.64}}{\frac{V_{IH} - 0.8}{0.45}} = 27.5$$

$$\Rightarrow V_{IH} = 0.89$$

Determination of V_{IL}:

$$\frac{V_{IL} - 0.5}{0.45} = 0 \Rightarrow V_{IL} = 0.5\,V$$

$\therefore V_{NH} = (3.25 - 0.89) = 2.36\,V$
$\therefore V_{NL} = (0.5 - 0.1) = 0.4\,V$
$\therefore V_N = min(0.4,\ 2.36) = 0.4\,V$

(b) When driver's output is low, maximum fanout is ∞ due to no connection between driver and load.

When driver's output is high,

$$\frac{3.6 - 3.25}{0.64} = N \times \frac{3.25 - 0.8}{0.45} \Rightarrow N = floor\left(\frac{0.546875}{5.44}\right) = 0$$

So, maximum fanout for this case is 0. Thus, overall maximum fanout is also 0. So, no loads can be connected.

$$P_{(0,0)} = 0$$

$$P_{(1,0)} = P_{(0,1)} = (3.6 - 0) \times \frac{3.6 - 0.8}{0.45} + (3.6 - 0) \times \frac{3.6 - 0.1}{0.64} = 41.525\,mW$$

$$P_{(1,1)} = 2 \times (3.6 - 0) \times \frac{3.6 - 0.8}{0.45} + (3.6 - 0) \times \frac{3.6 - 0.1}{0.64} = 63.925\,mW$$

$\therefore P_{max} = P_{(1,1)} = 63.925\,mW$

Chapter 7

Diode Transistor Logic (DTL)

Logic circuits which are constructed using diode, BJT and resistors are called DTL circuits. Here, we will study the DTL NAND gate.

DTL NAND Gate

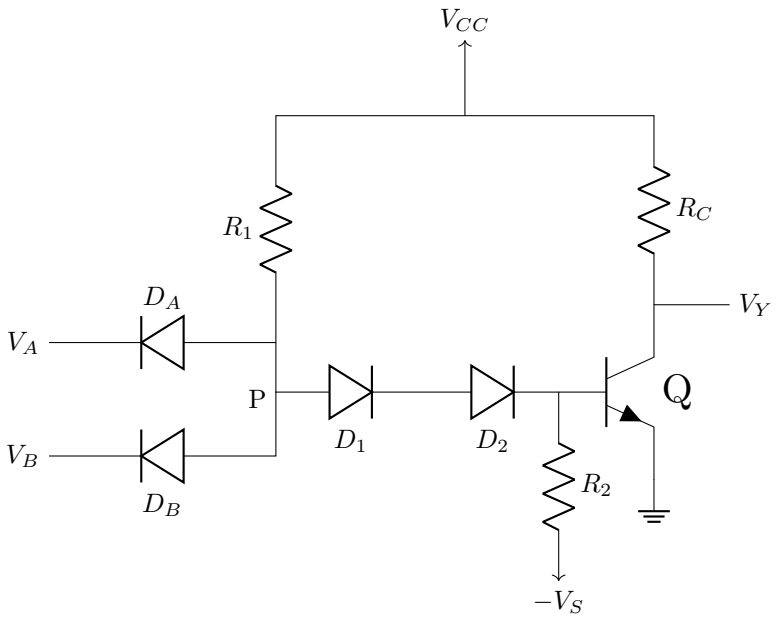


Figure 7.1: A typical DTL NAND gate

Analysis of operation:

Case (0,0), (0,1), (1,0):

When either of the inputs is low (say 0.2 V, which might be due to the input is coming from the output of some other transistor based logic circuit), the corresponding diode will turn on due to

forward biasing. While if any input is high, the diode will be off due to reverse bias. This is because, a higher voltage might appear at the anode of the diodes due to the presence of V_{CC}, compared to the low input. However, it will surely not be greater than the raw high input at the cathode end of the diode. So, for the three cases under study, there will always be at least one input diode which will be on.

The above analysis leads to the conclusion of $V_P = 0.2 + 0.7 = 0.9\,V$. Now, for the other elements of the circuit, let's see what will be there state. If the transistor 'Q' were to turn on from cut-off mode, it would need at least 0.5 V at its base (as emitter is grounded). Then again, for this to happen, D_1 and D_2 must also be on, otherwise there is no other way for the base to gain the required voltage. The diodes must have at least 0.6 V across them if they were to be on. All these if added leads to the requirement of $V_P = 0.5 + 0.6 + 0.6 = 1.7\,V$. But we have already found V_P to be $0.9\,V$. Thus, D_1, D_2 & Q cannot be on. They are all off and can be replaced by open circuits. Consequently, $I_{R_C} = 0$ and $V_Y = V_{CC}$. This is the desired high output for the mentioned three cases from a NAND gate.

Case (1,1):

As discussed in the previous cases, when an input is high, the corresponding diode will be reverse biased. Thus, in this case, both D_A & D_B will be off. So, now there is scope for V_P to be high enough as per the requirement to keep D_1, D_2 & Q on. We may assume Q to be operating in saturation mode, as we desire a low output from the circuit for this case.

Now, with these assumptions, we can actually find the value of V_P. Since, Q is assumed to be in saturation, its base voltage will be 0.8 V. The two diodes D_1 & D_2 will consume 0.7 V each. So, $V_P = 0.8 + 0.7 + 0.7 = 2.2\,V$. And of course, $V_Y = V_{CE} = 0.2\,V$.

Power Dissipation

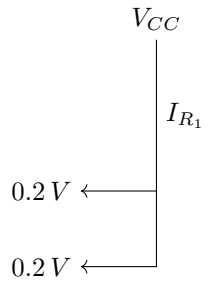


Figure 7.2: Case (0,0)

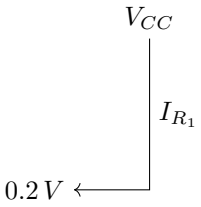


Figure 7.3: Case (0,1), (1,0)

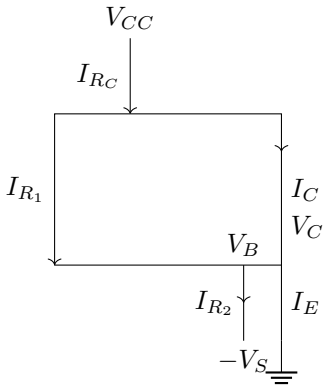


Figure 7.4: Case (1,1)

$$P_{(0,0)} = P_{(0,1)} = P_{(1,0)} = (V_{CC} - 0.2) \times I_{R_1}$$

$$P_{(1,1)} = (V_{CC} - 0) \times I_C + (V_{CC} - V_B) \times I_{R_1} + (V_B - 0) \times (I_{R_1} - I_{R_2}) + (V_B - (-V_S)) \times I_{R_2}$$

Fanout

The determination of maximum fanout of DTL NAND gate drivers is based on the similar concepts of RTL logic circuits. In case of DTL NAND gates being the load, they will deliver current to the driver. So, condition of maximum fanout when driver output is low will be $\beta_{forced} = \beta_F$ of the driver BJT. In the driver's highoutput case, the connection between the driver and load will be cut out due to the diode of the DTL load being off. The maximum fanout for these cases will then be ∞.

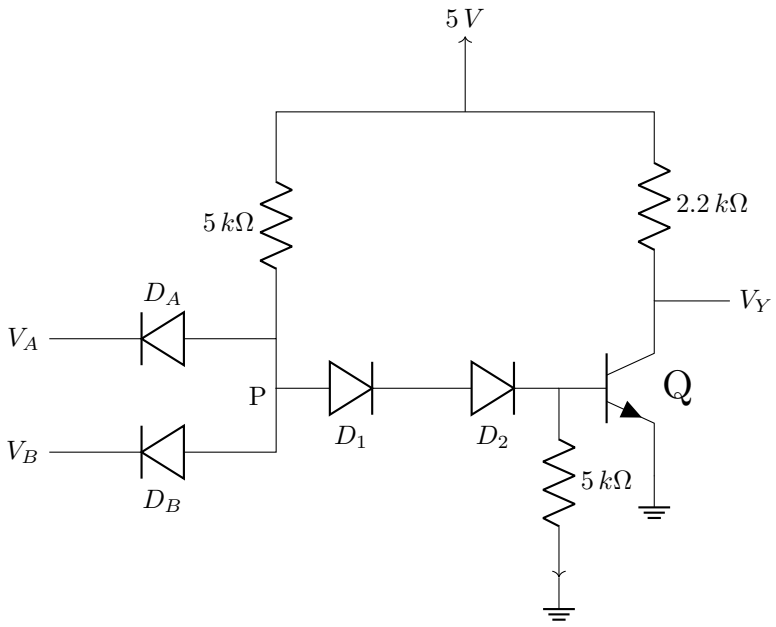
Some important facts about DTL NAND gate—

1. The two diodes connected to the base of the BJT (D_1 & D_2) are essential elements of the circuit. One might wonder, why didn't we use a resistor instead? Well, recall that for low inputs, $V_P = 0.9\,V$. So, if we had used a resistor, the voltage at the base of the transistor might as well had been greater than 0.5 V, turning on the BJT, which would have been an undesired result. D_1 & D_2 prevents this.

2. The DTL NAND gate can easily be used as a NOT gate if we always keep all but one inputs high. This is because $\overline{AB} = \overline{A.1} = \overline{A}$.

Problems Roster

Problem 1:



For the DTL NAND gate— find all voltage and currents for all logic cases with verification of assumption. Assume, high input is 5 V and low input is 0.2 V. Also, $\beta_F = 30$.

Solution:

Case (0,0): D_A & D_B will be on. D_1, D_2 & Q will be off.
$V_P = 0.2 + 0.7 = 0.9\,V$, $V_Y = 5\,V$.
$I_{2.2k} = 0$, $I_{5k} = \dfrac{5 - 0.9}{5} = 0.82\,mA$, $I_{D_A} = I_{D_B} = \dfrac{I_{5k}}{2} = 0.41\,mA$.
Verification: $V_P = 5 - I_{5k} \times 5 = 5 - 4.1 = 0.9\,V$. Required V_P to turn on D_1, D_2 & Q = 0.6+0.6+0.5 = 1.7 V. Since 0.9 ¡ 1.7, assumptions were correct. Also, $V_{D_A} = V_{D_B} = 0.9 - 0.2 = 0.7$. So, assumption of D_A & D_B being on were also right.

Case (0,1) & (1,0): Either of D_A & D_B is on, while the other is off. $V_P = 0.2 + 0.7 = 0.9\,V$ like (0,0). So, for the similar reasons, D_1, D_2 & Q will remain off and $V_Y = 5\,V$. However, I_{D_A} or I_{D_B} will be equal to I_{5k} when the corresponding diode is on. For example, for (0,1), $I_{D_A} = I_{5k} = 0.82\,mA$ and $I_{D_B} = 0$. D_B will remain off in (0,1), as there is a high voltage (5 V) applied at its cathode. Simmilar analysis can be done in case of (1,0).

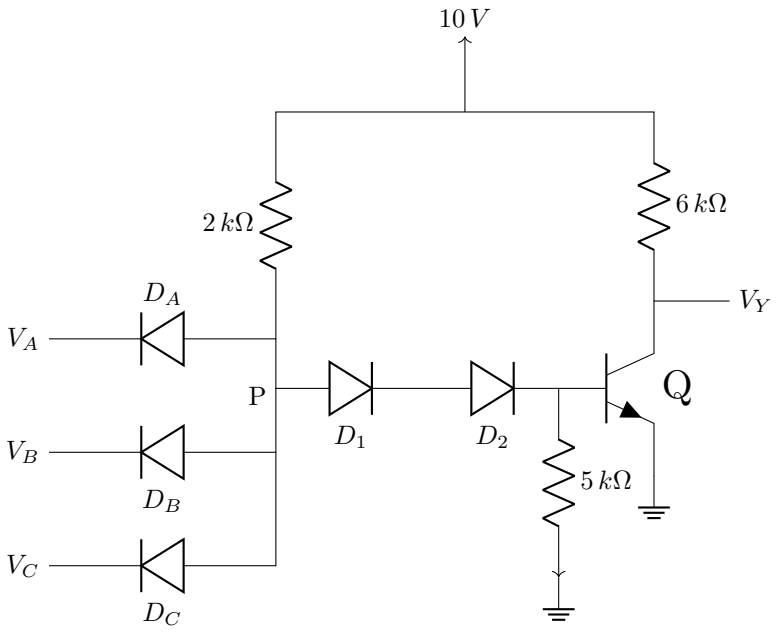
Case (1,1): D_A & D_B will both be off due to the reason already mentioned in the previous two cases. D_1, D_2 & Q can be assumed on, as there is high voltage available at 'P' now. Assuming saturation for Q, $V_P = 0.8 + 0.7 + 0.7 = 2.2\,V$ and $V_Y = V_{CE} = 0.2\,V$. Then, $I_{D_1} = I_{D_2} =$

$\frac{5-2.2}{5} = 0.56\,mA$. Also, $I_{2.2k} = \frac{5-0.2}{2.2} = 2.18\,mA = I_C$ of Q. $I_B = 0.56 - \frac{0.8-0}{5} = 0.4\,mA$.

$$\therefore \beta_{forced} = \frac{2.18}{0.4} = 5.45$$

Which is less than β_F. Thus, our assumption was valid.

Problem 2:



For the above circuit, $V_{OH} = 9.5\,V$, $V_{OL} = 0.1\,V$ & $\beta_F = 30$.

(a)	Find the value of $\beta_{F_{min}}$ when all inputs are high.
(b)	Find the average power dissipation of the circuit.
(c)	Now suppose this same circuit is used as loads and connected to this driver circuit. Find the maximum fanout.

Solution:

(a)

$$\beta_{F_{min}} = \beta_{forced} = \frac{I_C}{I_B}$$

$$= \frac{\frac{10-0.1}{6}}{\frac{10-2.2}{2} - \frac{0.8-0}{5}} = 0.441$$

(b) Case (1,1,1): D_A, D_B & D_C will be off. D_1, D_2 & Q will be on.

$$P_{(1,1,1)} = (10-0) \times \left(\frac{10-2.2}{2} + \frac{10-0.1}{6} \right) = 55.5\,mW$$

Other cases: At least one of D_A, D_B or D_C will be on. D_1, D_2 & Q will be off.

$$P_{others} = (10-0.1) \times \frac{10-(0.1+0.7)}{2} = 45.54\,mW$$

$$\therefore P_{avg} = \frac{P_{(1,1,1)} + P_{others} \times 7}{8} = 46.785\,mW$$

(a) Case (1,1,1): Output of driver NAND low. So, the connected diode of the loads will be on. Hence, $V_P = 0.1 + 0.7 = 0.8\,V$ for the loads, while $V_P = 2.2\,V$ for the driver. As, the loads will deliver current to the driver, the worst case is when the full current through $2\,k\Omega$ is delivered (i.e. (0,1,1) input case of loads). The marginal condition of maximum fanout of the driver will be $\beta_{forced} = \beta_F$.

$$\therefore I_C = 30 \times I_B$$

$$\Rightarrow \frac{10-0.1}{6} + N \times I_L = 30 \times \left(\frac{10-2.2}{2} - \frac{0.8-0}{5} \right)$$

Now, $I_L = \dfrac{10-0.8}{2} = 4.6\,mA$. So,

$$1.65 + N \times 4.6 = 30 \times 3.74 \Rightarrow N = floor(24.03) = 24$$

Thus, maximum fanout for this case is 24.

Other cases: Output from the driver is high. So, connection between driver & load will be cut out due to the corresponding diode of the loads being reverse biased. Thus, any number of loads can be connected. So, maximum fanout for these cases is ∞.

$\therefore$ Overall maximum fanout = min (∞, 24) = 24

Problem 3:

What is the current through D_B in **Problem 2**, for the logic case (1,0,0)?

Solution:

$$I_{D_B} = \frac{1}{2} \times \frac{10-0.8}{2} = 2.3\,mA$$

Problem 4:

If the number of inputs to the circuit in **Problem 2** is increased to '5', what will be the maximum and average power dissipation?

Solution:

$$P_{max} = P_{(1,1,1,1,1)} = (10 - 0) \times \left(\frac{10 - 2.2}{2} + \frac{10 - 0.1}{6} \right) = 55.5\, mW$$

$$P_{others} = (10 - 0.1) \times \frac{10 - (0.1 + 0.7)}{2} = 45.54\, mW$$

$$\therefore P_{avg} = \frac{P_{(1,1,1,1,1)} + P_{others} \times 31}{32} = 45.85125\, mW$$

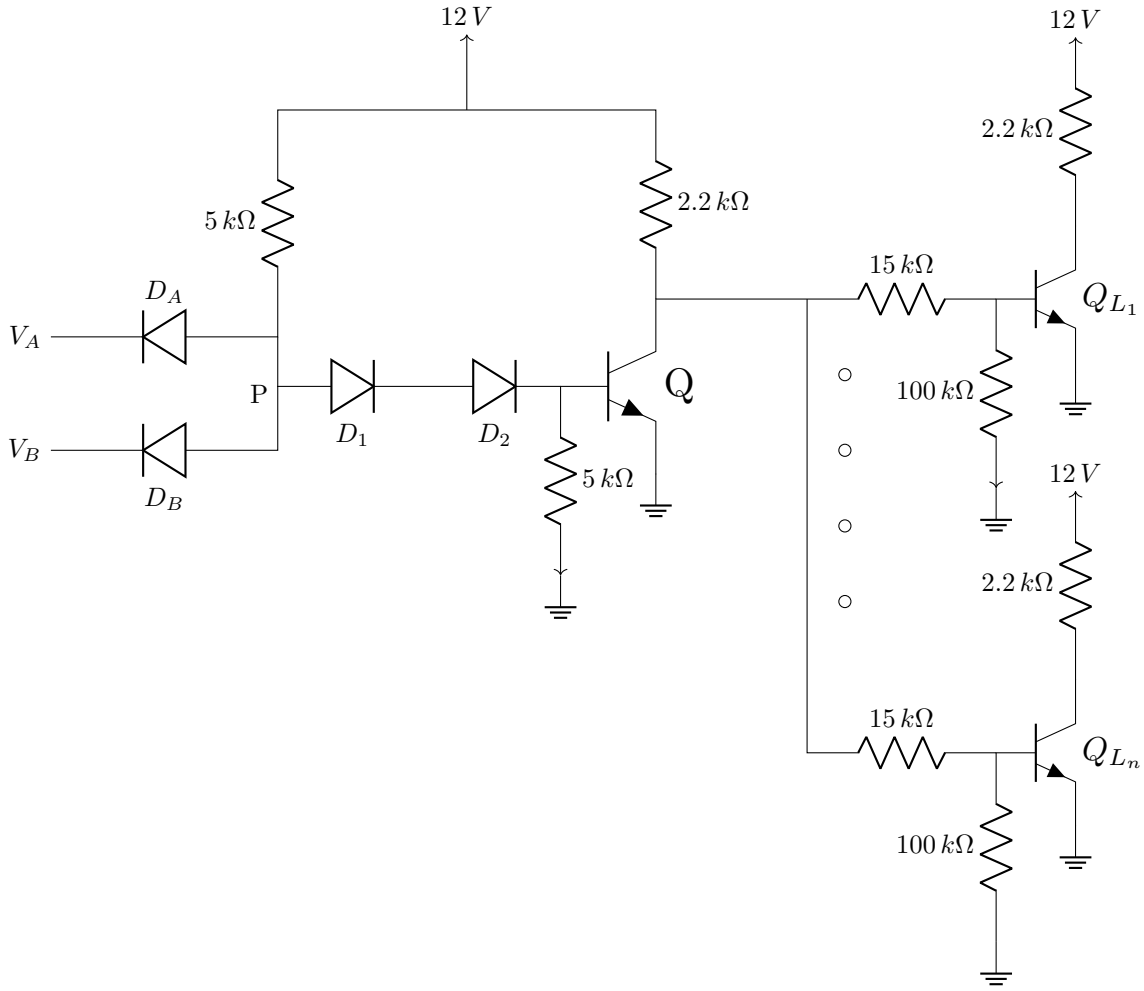
Problem 5:

Find the required collector resistance (replacing $6\, k\Omega$) in **Problem 2**, so that the maximum fanout reduces to '20'.

Solution:

$$\frac{10 - 0.1}{R'_C} + 20 \times 4.6 = 30 \times 3.74 \Rightarrow R'_C = 0.49\, k\Omega$$

Problem 6:



For the given circuit, $V_{OH} = 10\,V$, $V_{OL} = 0.2\,V$, $\beta_F = 30$

(a)	When N = 1, what logic function do we get from the output of the load?
(b)	Find the maximum fanout.
(c)	For N = maximum fanout, find the maximum power dissipation in the loads.

Solution:

(a) Y = AB

(b) Case (1,1): Output of the driver is low. So, the load BJTs will be in cut-off. However, it will still draw a current.

$$I_L = \frac{0.2 - 0}{15 + 100} = 1.74\,\mu A$$

$$I_{supply} = \frac{12 - 0.2}{2.2} = 5.363\,mA$$

So, maximum fanout for this case = floor $\left(\frac{5.363}{1.74 \times 10^{-3}}\right) = 3082$

Other cases: Output of the driver is high. Assuming it to be V_{OH},

$$I_{supply} = \frac{12 - 10}{2.2} = 0.91\,mA$$

$$I_L = \frac{10 - 0.8}{15} = 0.613\,mA$$

So, the maximum fanout for these cases = floor $\left(\frac{0.91}{0.61}\right) = 1$

Thus, the overall maximum fanout = min (3082, 1) = 1

(c) Case (1,1):

$$P_{load} = (0.2 - 0) \times \frac{0.2 - 0}{115} = 0.35\,mW$$

Other cases: KCL at the output of the driver,

$$\frac{12 - V_o}{2.2} = \frac{V_o - 0.8}{15} \Rightarrow V_o = 10.57\,V$$

$$P_{load} = (10.57 - 0) \times \frac{12 - 10.57}{2.2} + (12 - 0) \times \frac{12 - 0.2}{2.2} = 71.23\,mW$$

So, $P_{max} = 71.23\,mW$

Chapter 8

Transistor Transistor Logic (TTL)

In this logic family, we use transistors at input instead of diodes. To discuss TTL circuits, first we need to know about Multi-Emitter Transistors.

Multi Emitter BJTs

The internal structure & the symbol of a typical multi emitter BJT is shown below:

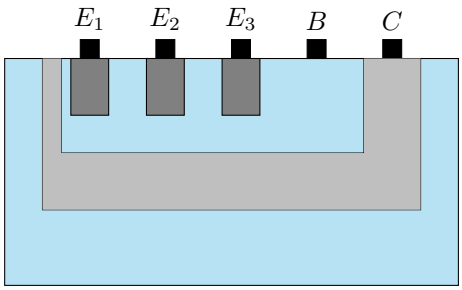


Figure 8.1: Internal structure of a typical multiemitter npn BJT

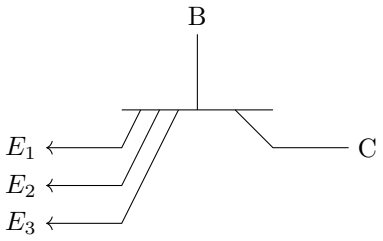


Figure 8.2: Symbol of a typical multiemitter npn BJT

One thing to note here, the emitters are not shorted. Rather, they make separate junctions with the base. So, their biasings are independent. However, the operating mode of the whole BJT depends on whether there is at least one B-E junction in forward bias. If so, the reverse biased B-E junctions (if any) will not play any role in deciding the operating mode of the BJT. This may seem weird, but think of the B-E junctions as separate diodes like the input branches of an AND gate. When any one of the input diodes is on, it doesn't matter whether the others are on or not. V_P of the AND gates gets fixed at 0.9 V. Similar thing happens here. So, effectively the multiemitter BJT's emitters behave similar to the AND gate input diodes. Well, still the whole device is a BJT. So, we must analyze TTL circuit keeping that in mind.

Now let's look at the TTL NAND gate.

TTL NAND Gate

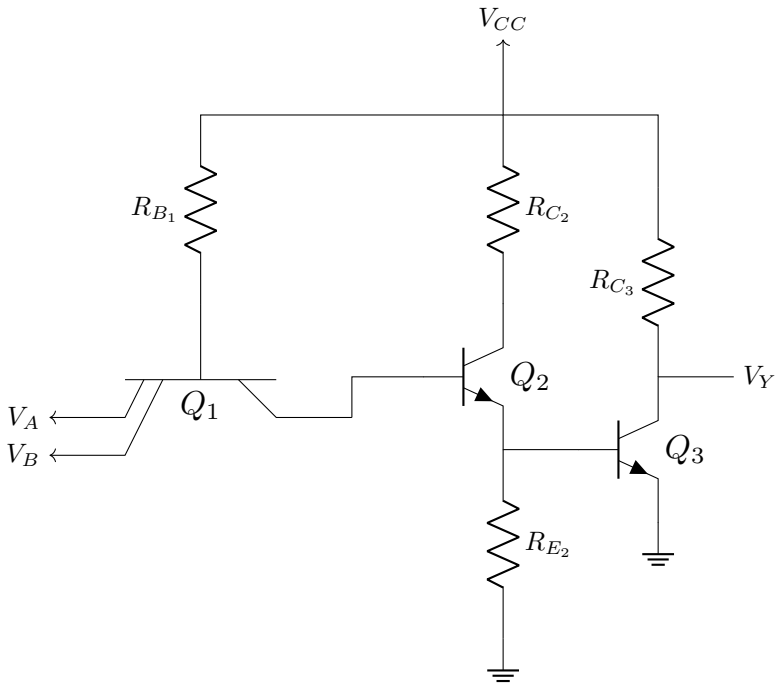


Figure 8.3: A typical two input TTL NAND Gate

Analysis of Operation:

Case (0,0): When both V_A & V_B are low (say 0.2 V), both the $B-E_A$ & $B-E_B$ junctions of Q_1 are forward biased. However, to comment on the operating mode of Q_1, we need to know the biasing of $B-C$ junction. Let's assume in accordance with our desired output for this case (1). For V_Y to be high, Q_3 needs to be in cut-off. For this to happen, Q_2 should also be in cut-off, as otherwise there will be a voltage across R_{E_2} due to the emitter current of Q_2. Now if this is the case, we can assume a low voltage at the base of Q_2 due to it being in cut-off. Since the base voltage of Q_2 is also the collector voltage of Q_1, $B-C$ junction of Q_1 can be assumed to be in forward bias due to this low voltage at the base. Thus, all junctions of Q_1 being forward bias, it can be assumed to operate in saturation mode.

Now, let's verify our assumption by reasoning from the assumed saturation mode of Q_1 and see if the other two BJTs are in accordance. As $V_{CE_{sat}} = 0.2\,V$, $V_{C_1} = 0.2 + 0.2 = 0.4\,V$. Since $V_{C_1} = V_{B_2}$, $V_{B_2} = 0.4\,V$. Also, if Q_2 was not in cut-off, the V_{E_2} of Q_2 would've been a non-zero positive value due to the voltage across R_{E_2}. This would make V_{BE_2} much lower than 0.5 V. So, Q_2 will thus indeed be in cut-off. Consequently, $V_{R_{E_2}} = 0\,V$. Hence, $V_{BE_3} = 0 - 0 = 0\,V$. Thus, Q_3 will also be in cut-off. Our assumption was thus valid. As we have already mentioned, $V_Y = V_{CC}$ for this case, which is a high voltage.

Case (0,1) or (1,0): If any one of the emitter has low input, the corresponding B-E junction will be forward biased. Thus, the emitter with high input would not have any effect on deciding

the operating mode of the BJT, as its corresponding B-E junction will be reverse biased. We can do the similar reasoning as in case (0,0), and show that Q_1 will be in saturation and Q_2, Q_3 will be in cut-off. Thus, $V_Y = V_{CC}$.

Case (1,1): When both emitters get a high input, both the B-E junctions are reverse biased. To comment on the operating mode of Q_1, we again need to know the biasing of B-C junction. The desired output for this case of the NAND gate is low. So, let's assume saturation mode for Q_3. This means $V_{B_3} = 0.8\,V$. For this to happen, the emitter current of Q_2 cannot be zero. Thus, Q_2 will also be on and can be assumed to operate in saturation too. Since, $V_{B_3} = V_{E_2}$, $V_{E_2} = 0.8\,V$. So, $V_{B_2} = 0.8 + 0.8 = 1.6\,V$. Now, the path between the base of Q_2 and the collector of Q_1 cannot have zero current, because that would mean open circuit and the '1.6 V' at the base of Q_2 will not be available as required by our assumption. So, we must assume the B-C junction of Q_1 to be in forward bias. Recall that we have already found the two B-E junctions to be in reverse bias. So, the operating mode of Q_1 will be reverse active. Thus, current from the emitter will enter the BJT, flowing towards its collector ($I_E + I_B = I_C$). Also, $V_{BC_1} = 0.7\,V$. Since, $V_{C_1} = V_{B_2} = 1.6\,V$, $V_{B_1} = 1.6 + 0.7 = 2.3\,V$. So, the output voltage for this case will be $V_Y = V_{C_3} = V_{CE_3} = 0.2\,V$, a low voltage.

Power Dissipation:

The power dissipation diagrams will be as the following:

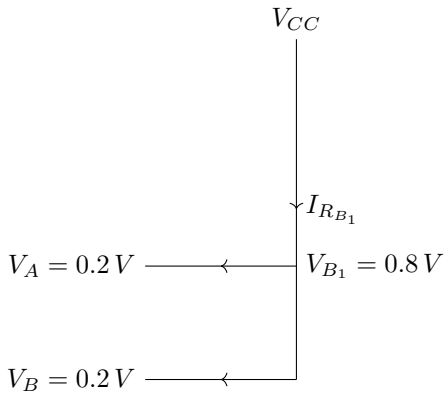


Figure 8.4: Case (0,0)

$P_{(0,0)} = (V_{CC} - 0.2) \times I_{R_{B_1}}$

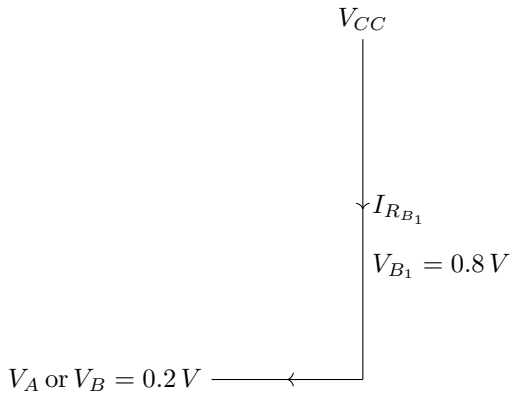


Figure 8.5: Case (0,1) or (1,0)

$P_{(0,0)} = (V_{CC} - 0.2) \times I_{R_{B_1}}$

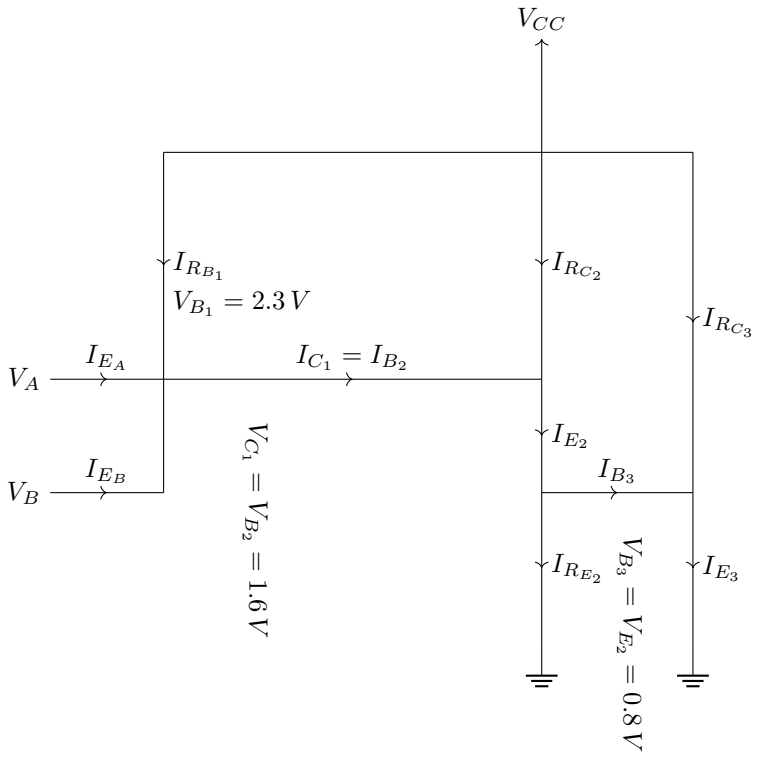


Figure 8.6: Case (1,1)

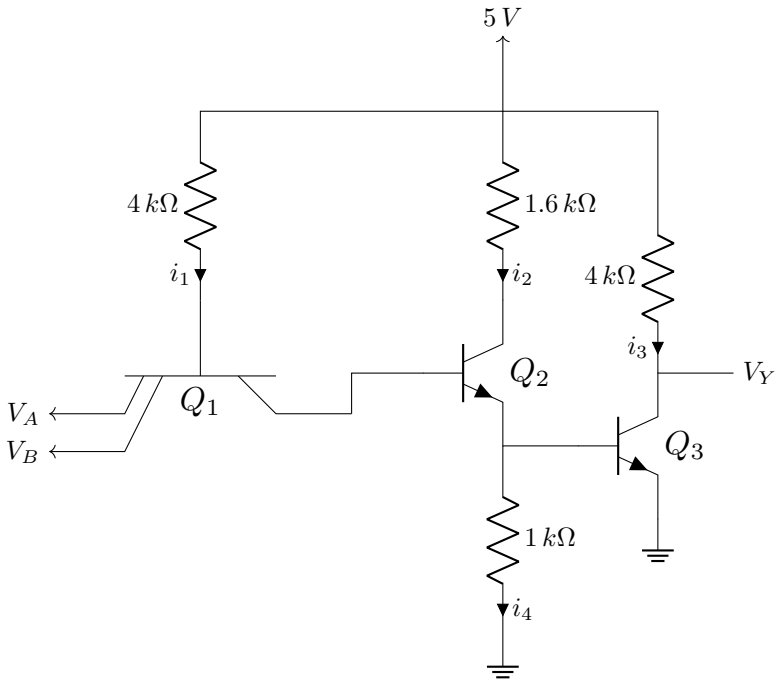
$$P_{(1,1)} = (V_A - 0) \times I_{E_A} + (V_B - 0) \times I_{E_B} + (V_{CC} - 0) \times [I_{R_{B_1}} + I_{R_{C_2}} + I_{R_{C_3}}]$$

Some points to remember:

1. Recall from BJT review in RTL, in reverse active mode, $\beta_R = \dfrac{I_E}{I_B}$. Here, in case of multiemitter BJTs, this applies to all the B-E junctions. So, $\beta_R = \dfrac{I_{E_1}}{I_B} = \dfrac{I_{E_2}}{I_B} = ...$ This is because, the emitters are identical and contribute the same amount of current.
2. Also, in reverse active mode, $I_E + I_B = I_C$. However, if there are multiple emitters, I_E will be the sum of each emitter's current. Thus, $I_{E_1} + I_{E_2} + ... + I_B = I_C$ in case of multiemitter BJTs in reverse active mode.

Problems Roster

Problem 1:



For the TTL NAND gate shown above, $\beta_F = 25$, $\beta_R = 0.1$, $V_{OH} = 3.4\,V$, $V_{OL} = 0.2\,V$. Assume high input = 5 V and low input = 0.2 V.

(a)	If at least one input is low, find i_1, i_{B_2}, i_{B_3}, i_3.
(b)	Find all the currents when both inputs are high.
(c)	Find the maximum and average power dissipation of the circuit.

Solution:

(a) Q_1 in saturation, Q_2 & Q_3 in cut-off. $V_{B_1} = 0.2 + 0.8 = 1\,V$.

$$\therefore i_1 = \frac{5-1}{4} = 1\,mA$$

$$\therefore i_{B_2} = i_{B_3} = i_3 = 0\,mA$$

(b) Q_1 in reverse active, Q_2 & Q_3 in saturation. $V_{B_1} = 0.8 + 0.8 + 0.7 = 2.3\,V$.

$$i_{B_1} = i_1 = \frac{5-2.3}{4} = 0.675\,mA$$

$$i_{E_A} = i_{E_B} = \beta_R \times i_1 = 0.1 \times 0.675 = 0.0675\,mA$$

$$i_{C_1} = i_{B_2} = i_{E_A} + i_{E_B} + i_{B_1} = 0.0675 \times 2 + 0.675 = 0.81\,mA$$

$$i_{C_2} = i_2 = \frac{5 - (0.8 + 0.2)}{1.6} = 2.5\,mA$$

$$i_{E_2} = i_{B_2} + i_{C_2} = 0.81 + 2.5 = 3.31\,mA$$

$$i_4 = \frac{0.8 - 0}{1} = 0.8\,mA$$

$$i_{B_3} = i_{E_2} - i_4 = 3.31 - 0.8 = 2.51\,mA$$

$$i_3 = i_{C_3} = \frac{5 - 0.2}{4} = 1.2\,mA$$

$$i_{E_3} = i_{B_3} + i_{C_3} = 2.51 + 1.2 = 3.71\,mA$$

(c) Case (0,0), (1,0), (0,1):

$$P = (5 - 0.2) \times \frac{5 - 1}{4} = 4.8\,mW$$

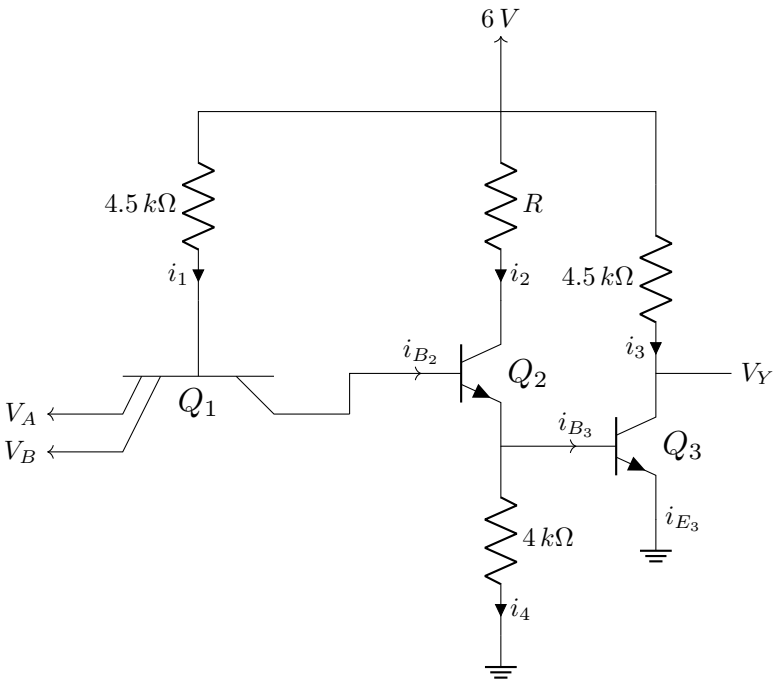
Case (1,1):

$$P = (5-0) \times [i_1 + i_2 + i_3 + i_{E_A} + i_{E_B}] = 5 \times [0.675 + 2.5 + 1.2 + 0.0675 + 0.0675] = 22.55\,mW$$

$$\therefore P_{max} = 22.55\,mW$$

$$\therefore P_{avg} = \frac{4.8 \times 3 + 22.55}{4} = 9.2375\,mW$$

Problem 2:



For the given circuit, $\beta_R = 0.2$, $V_{CE_{sat}} = 0.2\,V$. If $i_{E_3} = 4.74\,mA$ when both inputs are high, find the value of R.

Solution:

$$i_{E_3} = 4.74 = i_{B_3} + i_{C_3}$$

$$= i_{E_2} - i_4 + i_3 = i_{B_2} + i_{C_2} - i_4 + i_3$$

$$= i_{C_1} + i_2 - i_4 + i_3$$

$$= i_{B_1} + \beta_R \times i_{B_1} \times 2 + i_2 - i_4 + i_3$$

$$= i_1 + \beta_R \times i_1 \times 2 + i_2 - i_4 + i_3$$

$$= \frac{6 - 2.3}{4.5}(1 + 0.2 \times 2) + \frac{6 - 1}{R} - \frac{0.8 - 0}{4} + \frac{6 - 0.2}{4.5}$$

$$\Rightarrow R = 2\,k\Omega$$

Chapter 9

NMOS Logic

MOSFET Review

Recall from CSE251, the cross section of an n-MOSFET (NMOS) is something like the following:

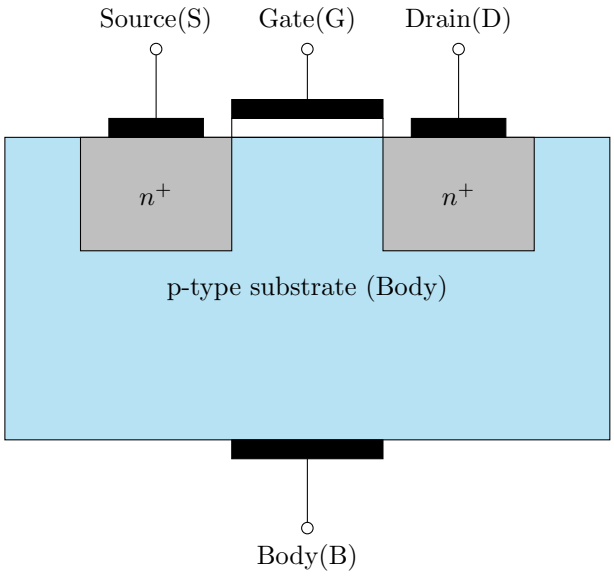


Figure 9.1: The cross section of an n-type MOSFET (NMOS)

We know that without any biasing (applied voltage at the gate), the NMOS shown in figure 9.1 will not take part in conduction. There are two p-n junctions (B-S & B-D), which have their junction barriers. To overcome these barriers and to create a conducting channel, we apply a positive voltage at the gate with respect to the source. This starts to attract the electrons from the two n^+ regions (i.e. source and drain) and starts to form an n-type channel between the two. When V_{GS} is greater than V_{TN}, the threshold voltage of the NMOS, a full channel forms between source and drain.

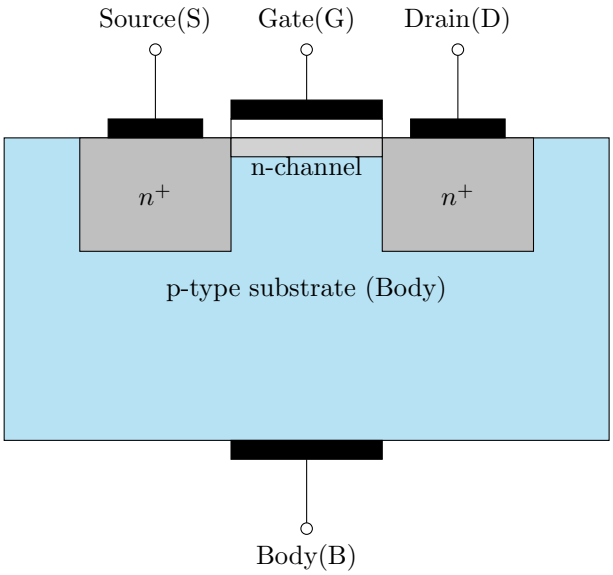


Figure 9.2: $V_{DS} = 0$, $V_{GS} > V_{TN}$

Now, if we apply a positive voltage at the drain too ($V_{DS} > 0$), then electrons will flow from the source towards the drain. So, the NMOS will conduct. However, this positive voltage at the drain attracts the electrons from the channel, which are close to the drain. Thus, the channel gets narrower with the increase of V_{DS} at the drain end. A situation comes when the channel width at the drain becomes zero due to a high enough V_{DS}. This is called the 'pinch off' of the channel. This happens when $V_{DS} = V_{GS} - V_{TN} = V_{OV}$, where V_{OV} is the overdrive voltage.

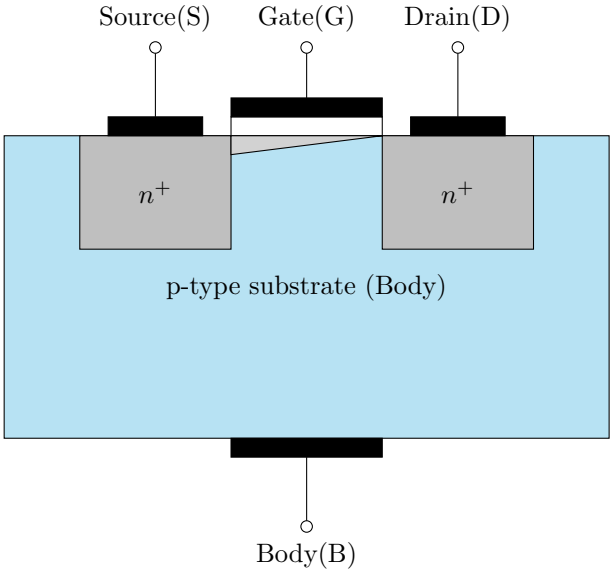


Figure 9.3: $V_{DS} = (V_{GS} - V_{TN})$, $V_{GS} > V_{TN}$

However, during this rise of V_{DS}, the current through the MOSFET rises too. After pinch off, if we increase V_{DS} further, the channel length reduces. One may think that the current flow will now stop. But this is not the case. Due to this high V_{DS}, the electrons are strongly attracted towards the drain, hence they keep moving despite the reduced channel. As electrons move from the source towards the drain, the current's direction will thus be the opposite, from the drain to the source. However, after pinch off, the current gets saturated and do not rise from the last value at pinch off.

So, we have three operating modes of the NMOS—

1. **Cut-off** $[V_{GS} < V_{TN}]$: The MOSFET does not form a complete channel. So, no current will flow, irrespective of the value of V_{DS}. The device is effectively an open circuit, like a BJT in cut-off.

2. **Triode of Linear** $[V_{GS} > V_{TN}, 0 < V_{DS} < (V_{GS} - V_{TN})]$: A complete channel forms, and its width reduce with the rise in V_{DS}. The current through the MOSFET (I_{DS}) rises with the increase in V_{DS}. This rise is approximately linear. Which is why the name 'Linear' is often used. The value of I_{DS} when derived, is expressed by, $I_{DS} = K_n[2(V_{GS} - V_{TN})V_{DS} - {V_{DS}}^2]$. Here, K_n is a parameter described by the physical structure of the NMOS. Its unit is $\frac{A}{V^2}$, in S.I. units.

3. **Saturation** $[V_{GS} > V_{TN}, V_{DS} > (V_{GS} - V_{TN})]$: The channel has already pinched off at $V_{DS} = V_{GS} - V_{TN}$. The current gets fixed to this last value and does not increase despite the rise in V_{DS}. It is expressed by, $I_{DS} = K_n(V_{GS} - V_{TN})^2$. Since V_{TN} is a constant parameter for a certain NMOS, I_{DS} in this region depends on V_{GS} only. So, different gate voltages result in different saturated currents.

The output I-V characteristics of an NMOS is found by plotting I_{DS} vs V_{DS}. If we also vary V_{GS}, we will get separate curves. The I-V curves of a typical NMOS are shown below for varying gate voltages.

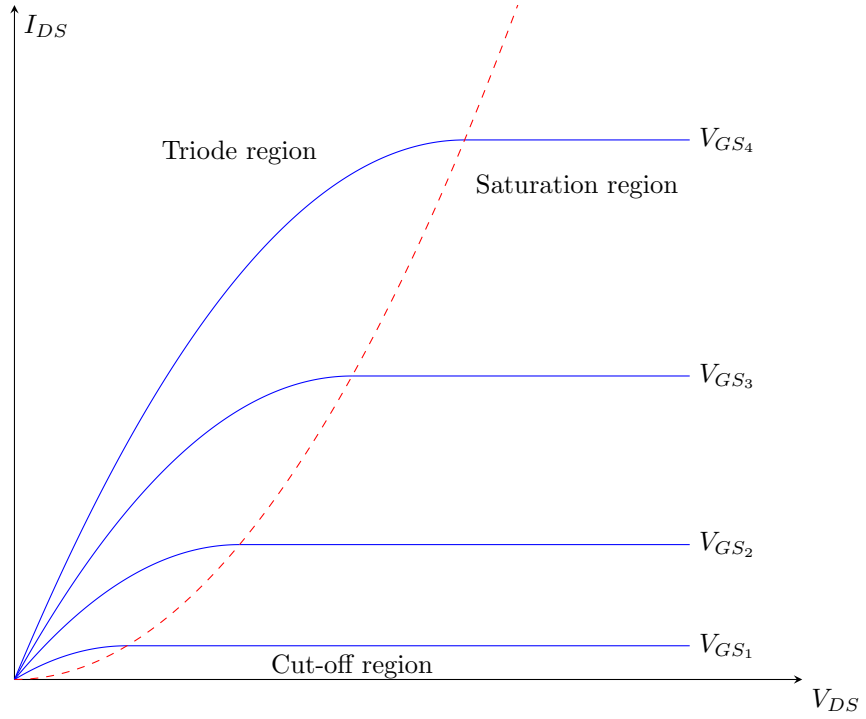
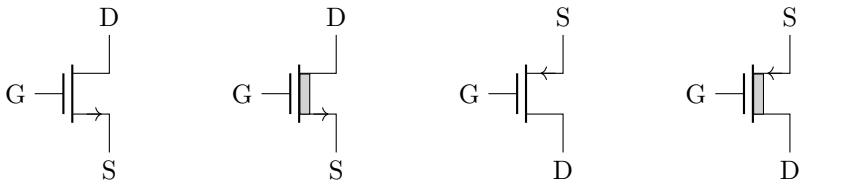


Figure 9.4: I-V characteristics of an NMOS

Till now, we have discussed the 'Enhancement type NMOS' only. There is another type, called the 'Depletion type NMOS'.

The Depletion type MOSFET: These MOSFETs have a channel already formed without any applied gate voltages. This is because their V_{TN} is negative (positive in case of PMOS). Thus, even when there is no gate voltage applied (i.e. $V_{GS} = 0$), there is a channel readily available for the NMOS.

The symbols of enhancement type and depletion type NMOS and PMOS are shown below:



Enhancement type NMOS ($V_{TN} > 0$)	Depletion type NMOS ($V_{TN} < 0$)	Enhancement type PMOS ($V_{TP} < 0$)	Depletion type PMOS ($V_{TP} > 0$)

Figure 9.5: Symbols of MOSFETs

Table 9.1: Summary of the MOSFET current–voltage relationships

NMOS	**PMOS**
Nonsaturation region ($V_{DS} < V_{OV}$)	Nonsaturation region ($V_{SD} < V_{OV}$)
$i_D = K_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$	$i_D = K_p\left[2(V_{SG} + V_{TP})V_{SD} - V_{SD}^2\right]$
Saturation region ($V_{DS} > V_{OV}$)	Saturation region ($V_{SD} > V_{OV}$)
$i_D = K_n(V_{GS} - V_{TN})^2$	$i_D = K_p(V_{SG} + V_{TP})^2$
Transition point	Transition point
$V_{OV} = V_{GS} - V_{TN}$	$V_{OV} = V_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$
Depletion mode	Depletion mode
$V_{TN} < 0$	$V_{TP} > 0$

Enough with the reviews, let's go into logic circuits using NMOS.

The NMOS Inverter

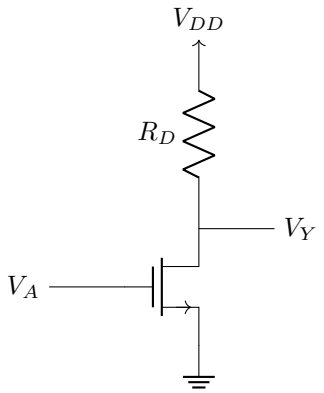


Figure 9.6: A typical NMOS Inverter

Analysis of Operation:

Case (0): When the input gate voltage V_A = low (say 0 V), in case of an enhancement type NMOS, this indicates cut-off mode operation (since for enhancement type NMOS, $V_{TN} > 0$). As in cut-off, the NMOS is effectively an open circuit, $I_{R_D} = 0$. Thus, $V_Y = V_{DD}$.

Case (1): When V_A = high (say 5 V), the NMOS will either be in triode mode or in Saturation, depending on the value of V_{DS}. The value of R_D is chosen such that it operates in triode mode for this input case. Now, in triode mode, we know that $V_{DS} < V_{OV}$. Where $V_{OV} = V_{GS} - V_{TN}$.

The exact value of V_{DS} can be found through analysis. We will soon see in mathematical problems, that this value is very small for a properly designed NOT gate. So, we get a low output for a high input.

Power Dissipation:

Since, gate current of MOSFETs are always zero, the power dissipation of case (0) is 0 as the NMOS is in cut-off. The power dissipation diagram for case (1) is given below:

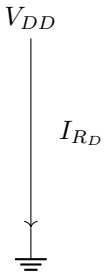


Figure 9.7: Case (1)

$P_1 = (V_{DD} - 0) \times I_{R_D}$

The NMOS NOR Gate

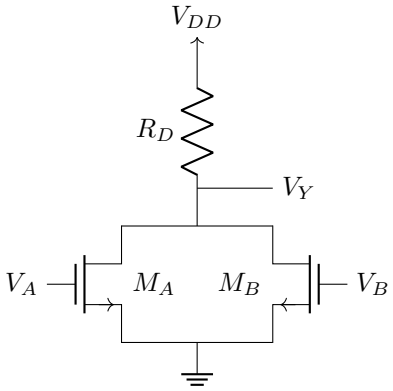


Figure 9.8: A typical NMOS NOR Gate

Analysis of Operation:

Case (0,0): For the similar reasons as in the case of NOT gate, both M_A & M_B will be off due to low voltages at their gates. This again leads to open circuits and thus, $V_Y = V_{DD}$, a high voltage.

Case (0,1) or (1,0): If the MOSFET parameters (V_{TN}, K_n) are the same for both M_A & M_B, then cases (0,1) and (1,0) will give the same result. Here, one NMOS will be in cut-off due to

low gate voltage. The other one will operate in triode mode if the circuit is properly designed. Then we will get a low output at V_Y for similar reasons as in the NOT gate.

Case (1,1): This case will also give a low output as both the NMOS will operate in triode mode in a properly designed circuit. If they have identical parameters, then I_{R_D} will be split equally between M_A & M_B as their I_{DS}.

Power Dissipation:

Case (0,0) will have zero power dissipation due to the whole circuit being open. The other three cases will have the following power dissipation diagrams:

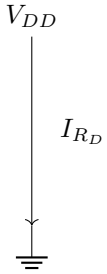


Figure 9.9: Case (0,1) or (1,0)

$$P_{(0,1)} = P_{(1,0)} = (V_{DD} - 0) \times I_{R_D}$$

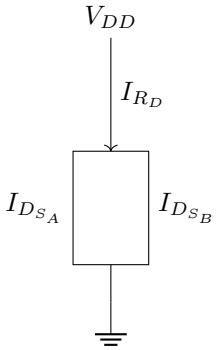


Figure 9.10: Case (1,1)

$$P_{(1,1)} = (V_{DD} - 0) \times I_{R_D}$$

Enhancement & Depletion Type Loads:

To reduce the size of NMOS logic circuits, often we use an enhancement or depletion type NMOS load instead of the resistor R_D, as resistors have a larger size.

In case of enhancement type loads, the drain and gate of the NMOS are shorted. Thus, $V_G = V_D$ for these load NMOS. So, $V_{DS} = V_{GS} > V_{OV}$, since $V_{OV} = V_{GS} - V_{TN}$. Thus, these load NMOS are always in saturation mode, as their drain is connected to the source voltage V_{DD}.

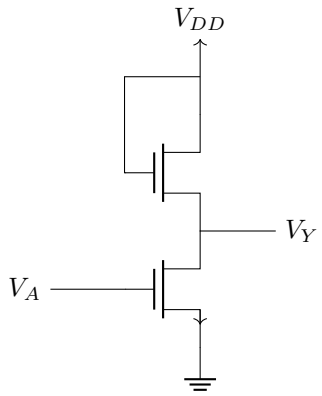


Figure 9.11: A typical NMOS Inverter with enhancement type load

The depletion type loads are just another NMOS connected in replacement of R_D. Just the fact that they are of depletion type means their $V_{TN} < 0$. Since they do not need any gate voltage to turn on, V_{GS} can be made 0, by shorting their gate with their source.

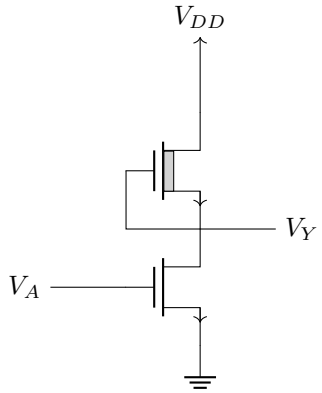
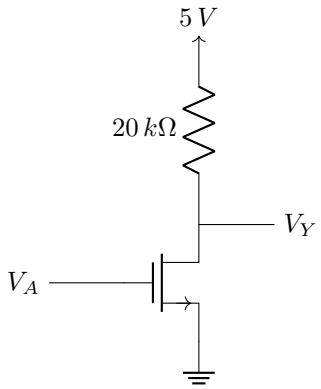


Figure 9.12: A typical NMOS Inverter with depletion type load

Problems Roster

Problem 1:



For the given NMOS inverter, $V_{TN} = 0.5\,V$, $K_n = 0.5\,\frac{mA}{V^2}$. Find the output voltage V_Y for $V_A = 1.5,\ \&\ 5\,V$.

Solution:

$V_A = 5\,V$: Assuming triode mode,

$$I_{DS} = I_{R_D} = \frac{5 - V_Y}{20}$$

$$\Rightarrow K_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2] = \frac{5 - V_Y}{20}$$

$$\Rightarrow 0.5[2(5 - 0.5)V_Y - V_Y^2] = \frac{5 - V_Y}{20}$$

$$\Rightarrow V_Y = 9.07\,V,\ 0.092\,V$$

Now, V_Y cannot be 9.07 V, as that would mean I_{R_D} is negative and flows in the opposite of assumed direction (i.e. from source to drain). So, $V_Y = 0.092\,V$.

Verification: As $V_Y = V_{DS} = 0.092 < 4.5$, which is the overdrive voltage ($V_{GS} - V_{TN} = 5 - 0.5 = 4.5\,V$), our assumption of triode mode was correct.

$V_A = 1.5\,V$: Assuming saturation mode,

$$I_{DS} = I_{R_D}$$

$$\Rightarrow K_n(V_{GS} - V_{TN})^2 = \frac{5 - V_Y}{20}$$

$$\Rightarrow 0.5 \times (1.5 - 0.5)^2 = \frac{5 - V_Y}{20}$$

$$\Rightarrow V_Y = -1\,V$$

Verification: As $V_Y = V_{DS} = -1 < V_{OV}$, our assumption of saturation mode was wrong. Let's again assume triode mode and repeat the analysis.

$$I_{DS} = I_{R_D}$$

$$\Rightarrow K_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2] = \frac{5 - V_Y}{20}$$

$$\Rightarrow 0.5[2(1.5 - 0.5)V_Y - V_Y^2] = \frac{5 - V_Y}{20}$$

$$\Rightarrow V_Y = 1.67\,V,\ 0.5\,V$$

As 1.67 V is greater than the overdrive voltage, we discard it and take 0.5 V, as it aligns with our assumption of triode mode.
Verification: As, $V_Y = 0.5 < V_{OV}$ $(V_{OV} = 1.5 - 0.5 = 1\,V)$, our assumption of triode mode was correct. So, $V_Y = 0.5\,V$.

Problem 2:

For the circuit in **Problem 1**, find the maximum drain current, transition point from triode to saturation and the maximum power dissipation.

Solution:

Maximum drain current:

$I_{DS} = I_{R_D} = \frac{5 - V_Y}{20}$. So, I_{DS} will rise if the output drops. Since it is an inverter, output will drop when input rises. The highest possible input to the NOT gate is $V_{DD} = 5\,V$. So, assuming $V_A = 5\,V$, we have already found $V_Y = 0.092\,V$.

$$\therefore I_{DS_{max}} = \frac{5 - 0.092}{20} = 0.2454\,mA$$

Maximum power dissipation, $P_{max} = P_1 = (5 - 0) \times I_{R_D} = 5 \times \frac{5 - 0.092}{20} = 1.227\,mW$
Transition point:

At transition point, $V_{DS} = V_Y = V_{GS} - V_{TN}$. Also, $I_{DS} = K_n(V_{GS} - V_{TN})^2$. So,

$$I_{DS} = I_{R_D}$$

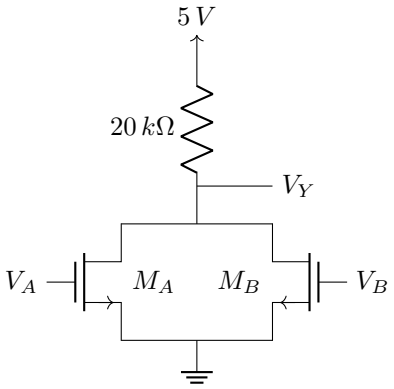
$$\Rightarrow K_n {V_Y}^2 = \frac{5 - V_Y}{20}$$

$$\Rightarrow V_Y = 0.66\,V,\ -0.76\,V$$

-0.76 V is not acceptable, since it would mean I_{DS} flows from source towards the drain. So, $V_Y = 0.66\,V$.

Now, $V_A = V_{GS} = V_{DS} + V_{TN} = V_Y + V_{TN} = 0.66 + 0.5 = 1.16\,V$. So, the transition point input is 1.16 V. At this input, the operating mode of the NMOS shifts from triode to saturation.

Problem 3:



For both M_A & M_B, $V_{TN} = 0.8\,V$, $K_n = 0.1\,\frac{mA}{V^2}$. Find the currents and output voltage for all input cases to the NOR gate.

Solution:

Case (0,0): M_A & M_B both in cut-off. So,$I_{D_A} = I_{D_B} = 0$. Thus, $I_{20} = I_{D_A} + I_{D_B} = 0$. Also, $V_Y = 5\,V$.

Case (0,1) or (1,0): Let's analyze (0,1). M_A will be in cut-off. Assuming triode mode for M_B,

$$I_{D_B} = I_{20}$$

$$\Rightarrow K_n[2(V_B - V_{TN})V_Y - V_Y^2] = \frac{5 - V_Y}{20}$$

$$\Rightarrow 0.1[2(5 - 0.8)V_Y - V_Y^2] = \frac{5 - V_Y}{20}$$

$$\Rightarrow V_Y = 8.6\,V,\ 0.29\,V$$

8.6 is unacceptable as it means I_{D_B} is negative. Thus, $V_Y = 0.29\,V$. This aligns with our assumption of triode mode (As, $V_{OV} = 5 - 0.8 = 4.2\,V$).

Now, $I_{D_B} = I_{20} = \frac{5 - 0.29}{20} = 0.235\,mA$

Case (1,1):$V_A = V_B = 5\,V$. M_A & M_B both can be assumed to operate in triode mode. Thus,

$$I_{D_A} + I_{D_B} = I_{20}$$

$$K_n[2(V_A - V_{TN})V_Y - V_Y^2] + K_n[2(V_B - V_{TN})V_Y - V_Y^2] = \frac{5 - V_Y}{20}$$

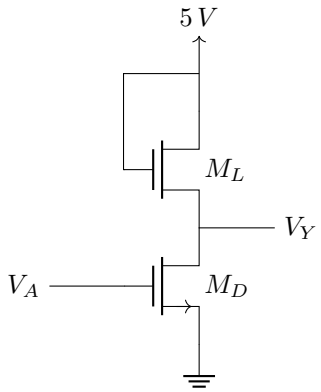
$$\Rightarrow V_Y = 4.17\,V,\ 0.149\,V$$

Now, 4.17 V is much closer to 4.2 V, that would drive the NMOS to saturation. So, the correct value of output voltage is 0.149V, which also aligns with the assumption of triode region operation. So, $V_Y = 0.149\,V$.

$$\therefore I_{20} = \frac{5 - 0.149}{20} = 0.243\,mA$$

$$\therefore I_{D_A} = I_{D_B} = \frac{0.243}{2} = 0.121\,mA$$

Problem 4:



Parameters for the driver M_D, $V_{TN_D} = 1\,V$, $K_{n_D} = 50\,\frac{\mu A}{V^2}$. Parameters for the load, M_L, $V_{TN_L} = 1\,V$, $K_{n_L} = 10\,\frac{\mu A}{V^2}$. Determine the output voltage and the current for both high and low input cases.

Solution:

Case (0): $V_A = 0\,V$: M_D will be in cut-off. Thus, $I_{D_D} = I_{D_L} = 0$. Now, the load M_L is an enhancement type NMOS. So, it will always stay in saturation. So, $I_{D_L} = K_{n_L}(V_{GS_L} - V_{TN_L})^2$. Since, $V_{G_L} = V_{D_L} = 5\,V$, $V_{GS_L} = V_{G_L} - V_{S_L} = 5 - V_Y$. So,

$$I_{D_L} = 10 \times 10^{-6}(5 - V_Y - 1)^2$$

$$\Rightarrow 0 = 10 \times 10^{-6}(5 - V_Y - 1)^2$$

$$\Rightarrow V_Y = 4\,V$$

Case (1): $V_A = 5\,V$: M_D can be assumed to be in triode. As always M_L is in saturation. So,

$$I_{D_D} = I_{D_L}$$

$$\Rightarrow K_{n_D}[2(5 - V_{TN_D})V_Y - V_Y^2] = K_{n_L}(5 - V_Y - V_{TN_L})^2$$

$$\Rightarrow 50[2(5-1)V_Y - V_Y^2] = 10(5 - V_Y - 1)^2$$

$$\Rightarrow V_Y = 7.65\,V,\ 0.34\,V$$

Since 7.65 V ¿ 5 V, the current would be negative. Thus, V_Y is 0.34 V, which is also lower than the overdrive voltage (5-1 = 4V). Thus, our assumption is valid.

$$\therefore I_{D_D} = I_{D_L} = K_{n_L}(5 - 0.34 - 1)^2 = 0.134\,mA$$

Problem 5:

Find the average power dissipation of the circuit in **Problem 4**.

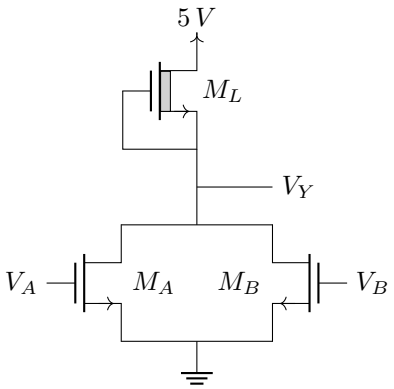
Solution:

Case (0): $P_0 = (5-0) \times I_{D_L} = 5 \times 0 = 0\,mW$

Case (1): $P_1 = (5-0) \times I_{D_L} = 5 \times 0.134 = 0.67\,mW$

$$P_{avg} = \frac{0 + 0.67}{2} = 0.335\,mW$$

Problem 6:



It is given that $K_n' = 100\,\frac{\mu A}{V^2}$, $V_{TN_A} = V_{TN_B} = 0.4\,V$, $V_{TN_L} = -0.6\,V$, $\left(\frac{W}{L}\right)_L = 4, \left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_B = 1$. **Note:** $K_n = K_n'\left(\frac{W}{L}\right)$. Find all the currents and the output voltage for all cases.

Solution:

Case (0,0): M_A & M_B are both off. Thus, $I_{DS_L} = I_{DS_A} = I_{DS_B} = 0$. Assuming triode mode for M_L,

$$I_{DS_L} = 0 = K_{n_L}[2(V_{GS_L} - V_{TN_L})V_{DS_L} - V_{DS_L}^2]$$

$$\Rightarrow K_n'\left(\frac{W}{L}\right)_L [2(0-(-0.6))(5-V_Y) - (5-V_Y)^2] = 0$$

$$\Rightarrow 100 \times 10^{-6} \times 4[2(0-(-0.6))(5-V_Y) - (5-V_Y)^2] = 0$$

$$\Rightarrow V_Y = 5\,V,\ 3.8\,V$$

Since no current flows, there will be no drops across M_L. So, $V_Y = 5\,V$ is the more acceptable answer.

Case (0,1) and (1,0): Both cases will give the same result as M_A & M_B have identical parameters. Let's analyze case (0,1). M_A will thus be off. Since, $V_{OV_L} = V_{GS_L} - V_{TN_L} = 0-(-0.6) = 0.6 < 5$, M_L might be in saturation mode. Also, as V_Y is expected to be low in this case, we can assume saturation mode for M_B. So, assuming saturation mode for M_L and triode mode for M_B,

$$100 \times 10^{-6} \times 4(0-(-0.6))^2 = 100 \times 10^{-6} \times 1[2(5-0.4)V_Y - V_Y^2]$$

$$V_Y = 9.04\,V\ 0.156\,V$$

9.04 V is unacceptable, as it indicates a negative drain current. So, $V_Y = 0.156$. This aligns with our assumption too.

$$\therefore I_{DS_L} = I_{DS_B} = 100 \times 10^{-6} \times 4(0-(-0.6))^2 = 0.144\,mA$$

Case (1,1): In this case, both M_A & M_B can be assumed to be in triode mode, and M_L can be assumed to be in saturation. So,

$$100 \times 10^{-6} \times 4(0-(-0.6))^2 = 2 \times 100 \times 10^{-6} \times 1[2(5-0.4)V_Y - V_Y^2]$$

$$\Rightarrow V_Y = 9.12\,V,\ 0.078\,V$$

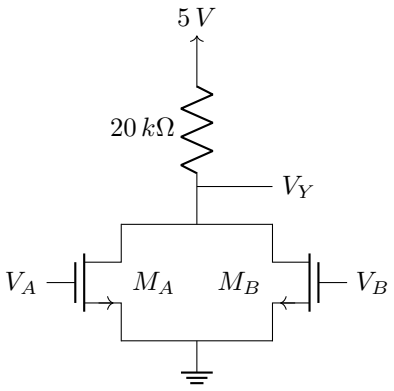
9.12 V is unacceptable due to the same reason. So, $V_Y = 0.078\,V$. This also aligns with our assumption.

$$\therefore I_{DS_L} = 100 \times 10^{-6} \times 4(0-(-0.6))^2 = 0.144\,mA$$

$$\therefore I_{DS_A} = I_{DS_B} = \frac{I_{DS_L}}{2} = 0.072\,mA$$

Tips: Usually saturation mode results in a greater voltage drop across the NMOS (as $V_{DS} > V_{OV}$). So, when the expected output (V_Y) is low, we may assume saturation mode for the depletion type load. Also, a low voltage at the drain of the NMOS means it is more likely to be in triode mode (as $V_{DS} < V_{OV}$). So, in the cases where V_Y is expected to be low, the driver MOSFET(s) can be assumed to be in triode mode. Although these assumptions are not 100% guaranteed to be correct, these are the most likely scenarios. So, starting the analysis with these assumptions will hopefully reduce the number of trials.

Problem 7:



For the NOR gate shown, $V_{TN_A} = 0.25\,V$, $V_{TN_B} = 0.3\,V$, $K_{n_A} = 0.4\,\frac{A}{V^2}$, $K_{n_B} = 0.5\,\frac{A}{V^2}$.

(a)	Find the lower threshold of output voltage.
(b)	Find the average power dissipation.
(c)	If a new NMOS M_C is used instead of M_B such that the drain currents of M_A & M_C are equal when both inputs are high, find the value of K_{n_C}. It is given that $V_{TN_C} = V_{TN_B} = 0.3\,V$.

Solution:

(a) Case (0,1): M_A in cut-off, M_B can be assumed to be in triode.So,

$$I_{20} = I_{DS_B}$$

$$\Rightarrow \frac{5 - V_Y}{20} = K_{n_B}[2(5 - V_{TN_B})V_Y - V_Y^2]$$

$$\Rightarrow \frac{5 - V_Y}{20} = 0.5[2(5 - 0.3)V_Y - V_Y^2]$$

$$\Rightarrow V_Y = 9.45\,V,\ 0.052\,V$$

9.45 V is greater than 5 V, so unacceptable. Thus, $V_Y = 0.052\,V$. This aligns with our assumption of triode mode as $V_{OV} = 5 - 0.3 = 4.7\,V$.

Case (1,0): M_A can be assumed to be in triode, M_B will be off. So,

$$I_{20} = I_{DS_A}$$

$$\Rightarrow \frac{5 - V_Y}{20} = K_{n_A}[2(5 - V_{TN_A})V_Y - V_Y^2]$$

$$\Rightarrow \frac{5 - V_Y}{20} = 0.4[2(5 - 0.25)V_Y - V_Y^2]$$

$$\Rightarrow V_Y = 9.56\,V,\ 0.064\,V$$

For the same reasons, 9.56 is unacceptable. So, $V_Y = 0.064\,V$.

Case (1,1): Both M_A & M_B can be assumed to be in triode mode. So,

$$I_{20} = I_{DS_A} + I_{DS_B}$$

$$\Rightarrow \frac{5 - V_Y}{20} = K_{n_A}[2(5 - V_{TN_A})V_Y - V_Y^2] + K_{n_B}[2(5 - V_{TN_B})V_Y - V_Y^2]$$

$$\Rightarrow \frac{5 - V_Y}{20} = 0.4[2(5 - 0.25)V_Y - V_Y^2] + 0.5[2(5 - 0.3)V_Y - V_Y^2]$$

$$\Rightarrow V_Y = 9.47\,V,\ 0.029\,V$$

For the same reasons, 9.47 V is unacceptable. So, $V_Y = 0.029\,V$.

$\therefore V_{OL} = max(0.052,\ 0.064,\ 0.029) = 0.064\,V$

(b) For case (0,0), $I_{20} = I_{DS_A} = I_{DS_B} = 0$. So,

$$P_{(0,1)} = (5 - 0) \times \frac{5 - 0.052}{20} = 1.237\,mW$$

$$P_{(1,0)} = (5 - 0) \times \frac{5 - 0.064}{20} = 1.234\,mW$$

$$P_{(1,1)} = (5 - 0) \times \frac{5 - 0.029}{20} = 1.24275\,mW$$

$$P_{(0,0)} = (5 - 0) \times 0 = 0\,mW$$

$$\therefore P_{avg} = \frac{1.237 + 1.234 + 1.24275 + 0}{4} = 0.93\,mW$$

(c) It is given that,

$$I_{DS_A} = I_{DS_C}$$

$$\Rightarrow K_{n_A}[2(5 - V_{TN_A})V_Y - V_Y^2] = K_{n_C}[2(5 - V_{TN_C})V_Y - V_Y^2]$$

$$\Rightarrow 0.4[2(5-0.25)V_Y - V_Y^2] = K_{n_C}[2(5-0.3)V_Y - V_Y^2]$$

Now,

$$I_{20} = I_{DS_A} + I_{DS_C} = I_{DS_A} + I_{DS_A} = 2I_{DS_A}$$

$$\frac{5 - V_Y}{20} = 2 \times 0.4[2(5-0.25)V_Y - V_Y^2]$$

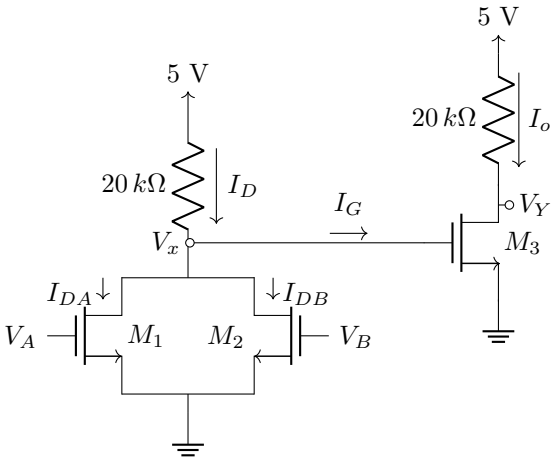
$$\Rightarrow V_Y = 9.53\,V,\ 0.0325\,V$$

For the same reasons, $V_Y = 0.0325\,V$. Using this value we get,

$$\Rightarrow 0.4[2(5-0.25)0.0325 - 0.0325^2] = K_{n_C}[2(5-0.3)0.0325 - 0.0325^2]$$

$$\Rightarrow K_{n_C} = 0.404\,\frac{A}{V^2}$$

Problem 8:



Parameter	M_1	M_2	M_3
K_n	0.3 $\frac{mA}{V^2}$	0.4 $\frac{mA}{V^2}$	0.3 $\frac{mA}{V^2}$
V_{TN}	0.6 V	0.7 V	0.6 V

From the above figure, determine the currents I_D, I_{DA}, I_{DB}, I_o, V_x and V_Y for the cases- (i) both inputs are high (ii) both inputs are low. Also find the power dissipation of M_3 only for both cases.

Solution:

(i) Both inputs are high, so assume M_1 and M_2 are in triode mode.

$$I_D = I_{D_A} + I_{D_B}$$

$$\Rightarrow \frac{5 - V_x}{20} = 0.3[2(5 - 0.6)V_x - V_x^2] + 0.4[2(5 - 0.7)V_x - V_x^2]$$

$$\Rightarrow V_x = 8.72\,V,\ 0.041\,V$$

As 8.72 V is greater than 5 V, $V_x = 0.041$.

$$I_D = \frac{5 - 0.041}{20} = 0.248\,mA$$

$$I_{D_A} = 0.3[(5 - 0.6)0.041 - 0.041^2] = 0.1077\,mA$$

$$I_{D_B} = 0.4[(5 - 0.7)0.041 - 0.041^2] = 0.1404\,mA$$

Since $V_x = V_{GM_3}$ ¡ 0.6 V, thus M_3 is in cut-off.

$$I_o = 0\,mA$$

$$I_G = 0\,mA$$

$$V_Y = 5\,V$$

(ii) Both inputs are low. So, M_1 and M_2 are in cut-off mode. Since $V_G < V_{TN}$ for both.

$$I_D = I_{D_A} = I_{D_B} = 0\,mA$$

$$V_x = 5\,V$$

$$I_G = 0\,mA$$

Since $V_x = V_{GM_3} = 5\,V$, M_3 is assumed to be in triode mode.

$$I_o = \frac{5 - V_Y}{20} = 0.3[2(5 - 0.6)V_Y - V_Y^2]$$

$$\therefore V_Y = 8.87\,V,\ 0.094\,V$$

For the same reasons, $V_Y = 0.094\,V$.

$$I_o = \frac{5 - 0.094}{20} = 0.2453\,mA$$

$$P_{(1,1)} = (5 - 0) \times 0 = 0\,mW$$

$$P_{(0,0)} = (5 - 0) \times 0.2453 = 1.2265\,mW$$

Chapter 10

CMOS Logic

CMOS circuits are the combination of an NMOS & PMOS circuits. When a certain NMOS network and its equivalent PMOS network are connected together, we get the corresponding CMOS circuit. This is a cheaper alternative of NMOS logic circuits. Let's start with the inverter.

The CMOS Inverter

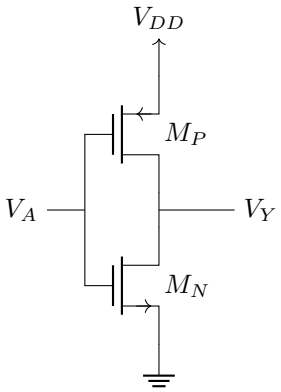


Figure 10.1: A typical CMOS Inverter

Analysis of Operation:

Case (0): When V_A is low (say 0 V), M_N will be in cut-off due to low voltage at its gate. For the same reason M_P will be in triode mode. Thus, V_{SD_P} will be very low. As, $V_{SD_P} = V_{DD} - V_Y$, $V_Y = V_{DD} - V_{SD_P}$ will be a high voltage. Thus, we get a high output for a low input. Basically, the PMOS is driving the output V_Y high by forming an approximate short circuit by operating in triode mode (the small V_{SD_P}, if ignored, can be considered a short circuit). This is called the 'Pull-up' network of the CMOS circuit.

Case (1): When V_A is high (say 5 V), M_P will be in cut-off due to a high input at its gate. This leaves M_N with no sources at its drain. So, it can be assumed to operate in triode mode. Thus, V_{DS_N} will be a very low voltage. Now, $V_{DS_N} = V_Y - V_{S_N}$. As, $V_{S_N} = 0\,V$, $V_Y = V_{DS_N}$. Using

the similar reasoing as in case (0), V_{DS_N} can be ignored and compared to a short circuit due to its small value. Thus, $V_Y \approx 0$. So, we get a low output from a high input. The NMOS is driving V_Y low by forming an effective short circuit path to the ground. For this reason, it is called the 'Pull-down' network of the CMOS circuit.

Logic Implementation using CMOS:

Some important points to remember while implementing logic using CMOS:

1. High input turns on/off the NMOS/PMOS, while the low voltage does the opposite.
2. Off MOSFET will result in open circuit, and on ones in short circuit between Drain & Source.
3. **Conduction complement:** If the intended logic function implementation by only NMOS requires series/parallel connection of multiple NMOS, then in design with CMOS, there will be the exact same number of PMOS in parallel/series connection accordingly. This is called conduction complement.
4. The network made up of PMOSFETs within the CMOS is called 'Pull up Network'. While the one made of NMOSFETs is called 'Pull down Network'.
5. Pull up network raises the output voltage to a high value, while the pull down network does the opposite.
6. If the intended Boolean function (f) does not have a 'bar' over it, we start by designing the CMOS network for the bar of that function(i.e. $\overline{f}$) first. Then, we feed the output of this designed network to a CMOS inverter. So, the final output will be the output from the inverter.
7. If we were to implement the boolean function using NMOS only, we would've needed a resistor. Same goes for logic implementation using PMOS. However, there is no requirement of any resistors in CMOS. We simply take the non-resistive part of the NMOS circuit of that function and also from the PMOS circuit, and combine them into a CMOS network.

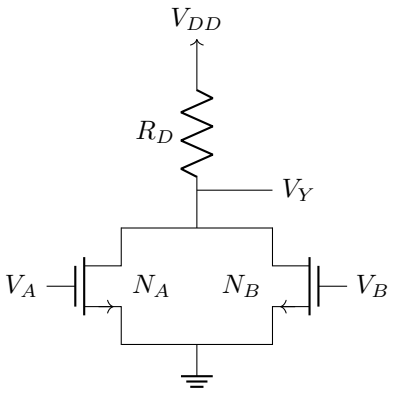
Problems Roster

Problem 1:

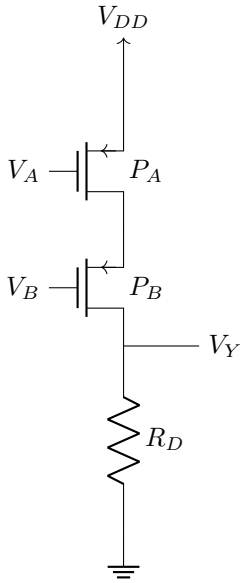
Implement a two-input NOR gate using CMOS logic.

Solution:

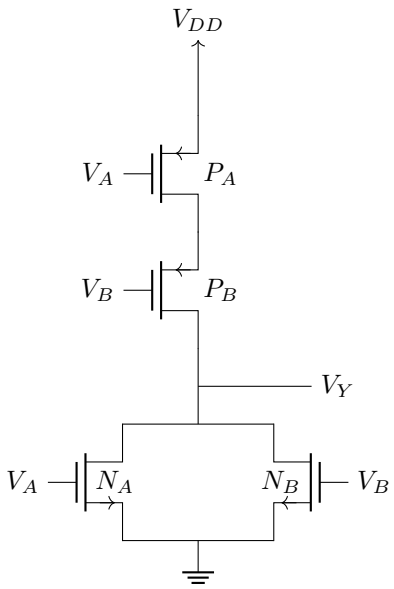
NOR gate using NMOS—



So, the NMOS network has two NMOS in parallel. Thus, according to conduction complement, the equivalent PMOS network will have two PMOS in series. If we had intended to implement the NOR gate using PMOS only, the circuit would be,



To get the CMOS network, we discard the resistances of both the NMOS & the PMOS networks, and connect their respective output nodes together. Thus, the CMOS circuit would be,

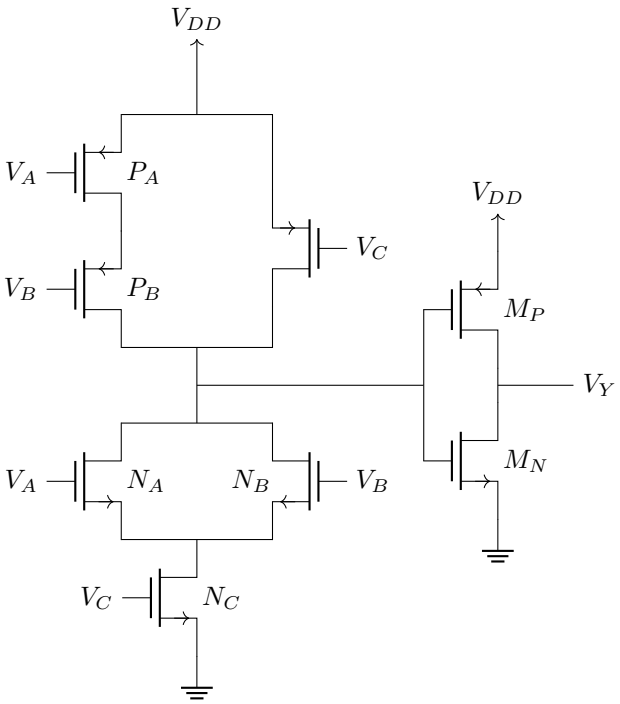


Problem 2:

Implement the logic function Y = (A+B)C using CMOS logic.

Solution:

Since the function has no bar over it, we start with designing $Y' = \overline{(A+B)C}$. Then we will use a CMOS inverter to get the actual 'Y'. So, $Y = \overline{Y'}$.


V_{DD}
V_A
P_A
V_B
P_B
V_C
V_{DD}
M_P
V_Y
V_A
N_A
N_B
V_B
M_N
V_C
N_C