

CS341 Cache HW Part A

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1. **Problem 6.26** The following table gives the parameters for a number of different caches. Your task is to fill in the missing fields in the table. Recall that m is the number of physical address bits, C is the cache size (number of data bytes), B is the block size in bytes, E is the associativity, S is the number of cache sets, t is the number of tag bits, s is the number of set index bits, and b is the number of block offset bits.

Cache	m	C	B	E	S	t	s	b
1.	32	2048	8	1	256	21	8	3
2.	32	2048	4	4	128	23	7	2
3.	32	1024	2	8	64	25	6	1
4.	32	1024	32	2	16	23	4	5

$$S_1 = 2^S$$

$$= 2^8 = 256$$

$$C_1 = S * E * B$$

$$= 256 * 1 * 8 = 2048$$

$$B_2 = 2^b$$

$$= 2^2 = 4$$

$$E_2 = \frac{C}{S * B}$$

$$= \frac{2048}{128 * 4} = 4$$

$$s_3 = \log_2(S)$$

$$= \log_2(64) = 6$$

$$t_3 = m - (s + b)$$

$$= 32 - (6 + 1) = 25$$

$$B_4 = \frac{C}{S * E}$$

$$= \frac{1024}{16 * 2} = 32$$

$$b_4 = \log_2(B)$$

$$= \log_2(32) = 5$$

2. **Problem 6.27** This problem concerns the cache in Practice Problem 6.12

(a) **List all of the hex memory addresses that will hit in set 1**

Set 1 is defined by $CI = 001$. There are two tags that are covered by this set, 45, and 23. For each tag we can have an offset of

00
01
10
11

The possible hex addresses will then be

12/24 (wrong addresses)

45 1 00 = $0x450$
 $0x451$
 $0x452$
 $0x453$
 23 1 00 = $0x230$
 $0x231$
 $0x232$
 $0x233$

(b) **List all of the hex memory addresses that will hit in set 6**

Set 6 is defined by $CI = 110$. There are two tags that are covered by this set, 91, and $F0$. For each tag we can have an offset of

00
01
10
11

The possible hex addresses will then be

12/25 (wrong addresses, the second tag) is invalid

91 6 00 = $0x910$
 $0x911$
 $0x912$
 $0x913$
 $F0$ 6 00 = $0xF00$
 $0xF01$
 $0xF02$
 $0xF03$

3. **Problem 6.29** (Notice that the addresses are 12 bits wide, but the format illustrated in part A. Show 13 bits, that is a mistake in the book)

Suppose we have a system with the following properties;

- The memory is byte addressable
- Memory addresses are to 1-byte words (not to 4-byte words)
- Addresses are 12 bits wide
- The cache is two-way set associative ($E = 2$), with a 4-byte block size ($B = 4$) and four sets ($S = 4$).

The contents of the cache are as follows, with all addresses, tags, and values given in hexadecimal notation:

Set Index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	00	1	40	41	42	43
	83	1	FE	97	CC	D0
1	00	1	44	45	46	47
	83	0				
2	00	1	48	49	4A	4B
	40	0				
3	FF	1	9A	C0	03	FF
	00	0				

- (a) The following diagram shows the format of an address (1 big per box). Indicate (by labeling the diagram) the fields that would be used to determine the following:
CO. The cache block offset
CI. The cache set index
CT. The cache tag

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CT	CT	CT	CT	CT	CT	CT	CT	CT	CI	CI	CO	CO
12	11	10	9	8	7	6	5	4	3	2	1	0

$$\text{num CO's} = \log_2(4) = 2$$

$$\text{num CI's} = \log_2(4) = 2$$

$$\text{num CT's} = 12 - (2 + 2) = 8$$

- (b) For each of the following memory accesses, indicate if it will be a cache hit or miss when carried out in sequence as listed. Also give the value of a read if it can be inferred from the information in the cache.

Operation	Address	Hit?	Read Value (or unknown)
Read	0x834	miss	Unknown
Write	0x836	miss	
Read	0xFFD	hit	C0

15/18 (the write should be a hit)

- i. **Read 0x834**

$$0x834 = 1000\ 0011\ 0100$$

$$CO = 00$$

$$CI = 11$$

$$CT = 1000\ 0011 = 83$$

We have the tag FF which is valid, but our valid bit section is set as 00, so this will still be a miss.

Since the value is not in the cache, it will stay as unknown.

- ii. **Write 0x836**

$$0x836 = 1000\ 0011\ 0110$$

$$CO = 10$$

$$CI = 11$$

$$CT = 1000\ 0011 = 83$$

Since tag 83 is not found as a valid entry in set 3 we mark this call as a miss.

- iii. **Read 0xFFD**

$$0xFFD = 1111\ 1111\ 1101$$

$$CO = 01$$

$$CI = 11$$

$$CT = 1111\ 1111 = FF$$

Our tag of FF is present, and our valid bit is set which tells us we do have this value in the cache. We then can see our read value in set 3 will be $CO = 01$.