

Real Time Image Process

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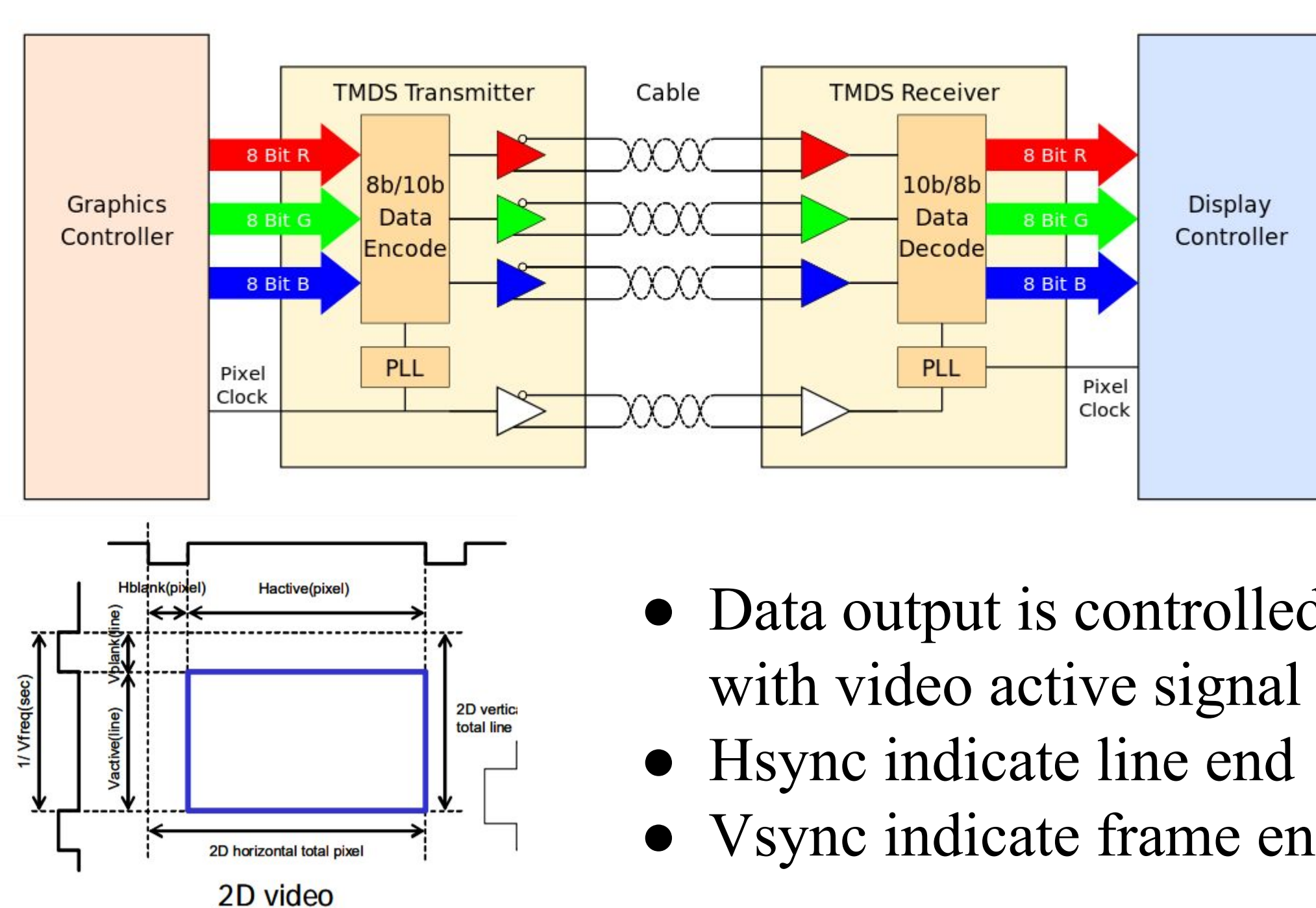
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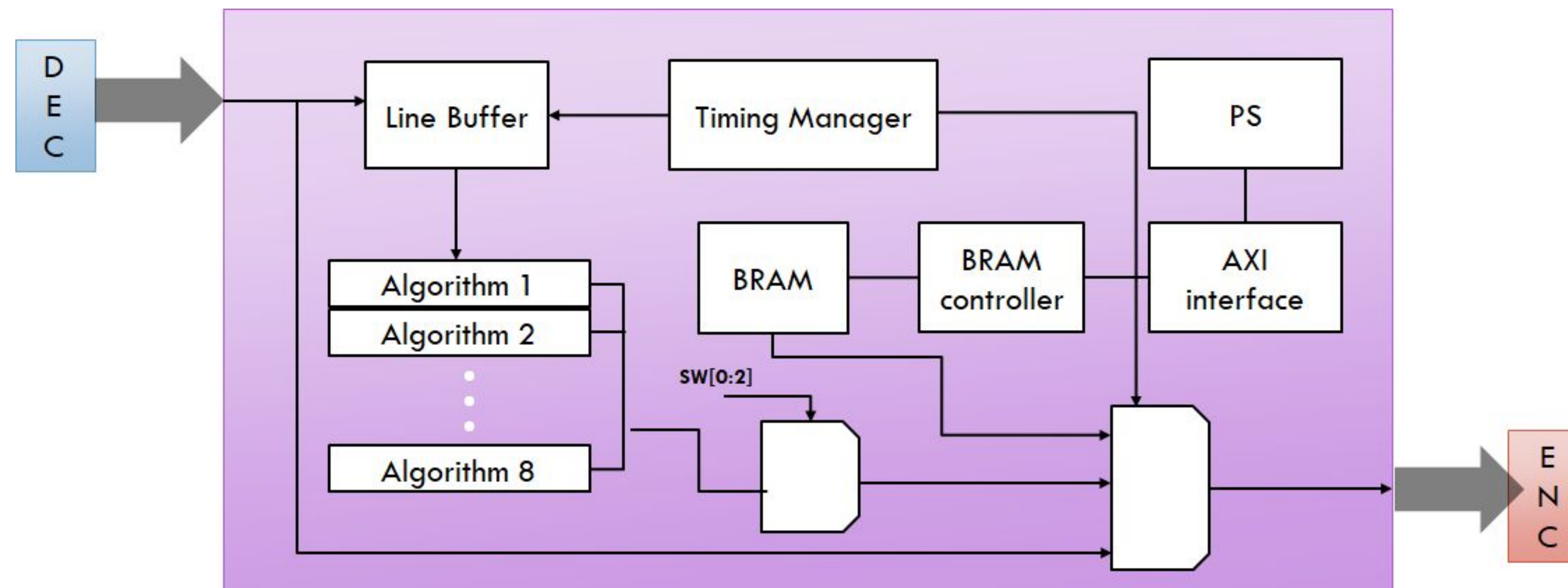
ECE530

**Software and Hardware
Co-Design with Zybo
Instructor: Jianjian Song**

TMDS Video Format



Overview of System

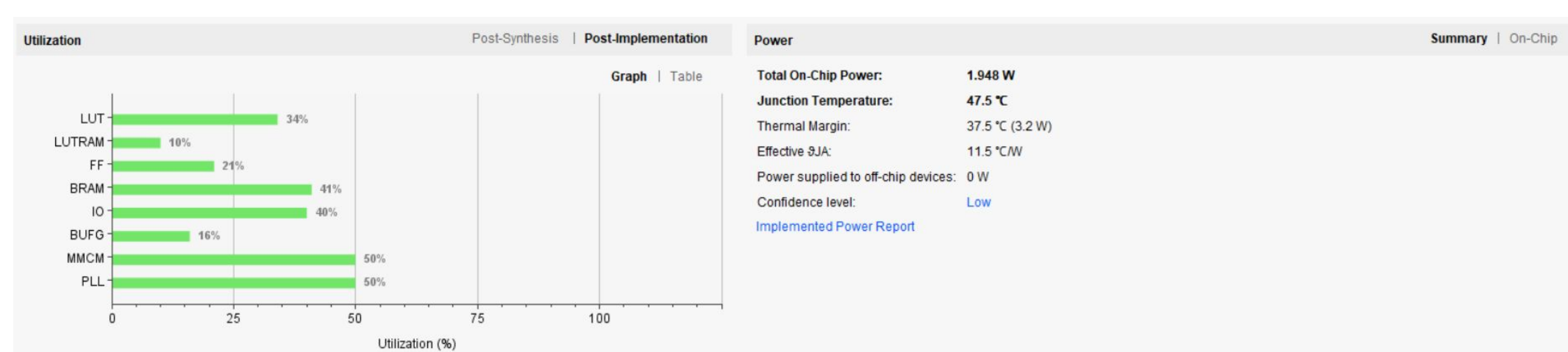


Line Buffer

- Store pixel data into memory cell
 - memory cell size 1280
- 4 lines of memory module is used
 - 3 lines for img process algorithm
 - 1 line for storing ongoing pixel
- Each line buffer rotates when its memory cell is full stored.

PL Design

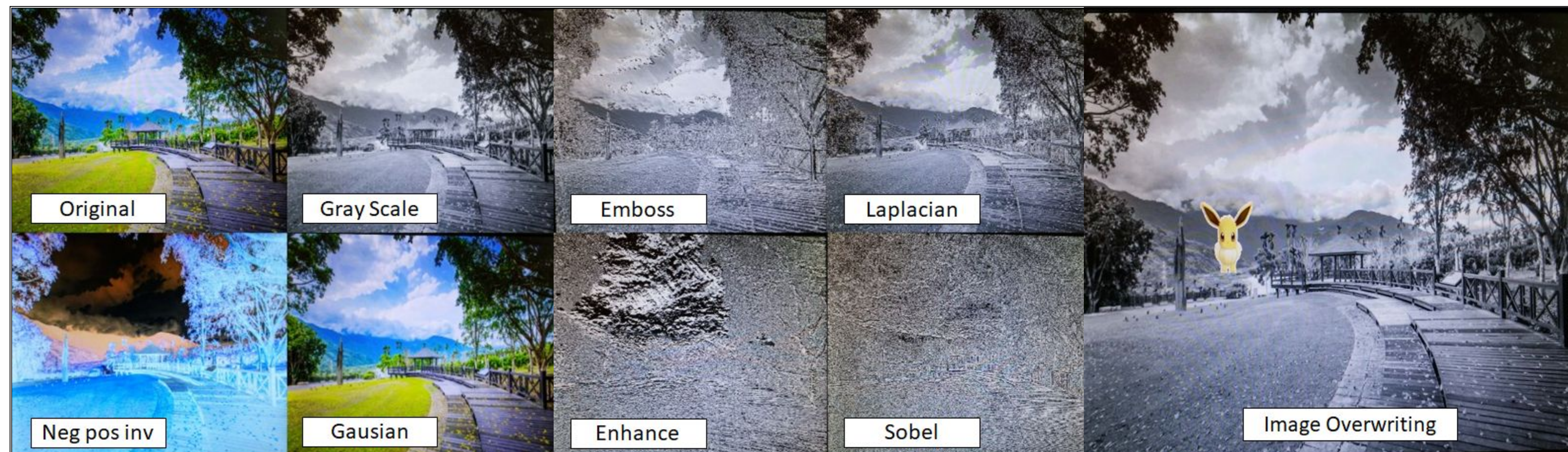
- TMDS image processing system was designed with verilog HDL with
 - 4 line line Buffer
 - Image Processing algorithm
 - TMDS Timing Manager



PS Function

- Image overwrite function was implemented, which display image data stored in BRAM
- Zynq PS write image data into BRAM via SDK
- AXI 4 interface is used to connect Zynq PS and BRAM via BRAM controller module

Image Process Algorithms



- Pixel wise and Window wise algorithms were implemented
 - 3x3 filter (Convolution operation) was applied
- Applied Algorithms
- Gray Scale:
 - Color to black and white
 - Neg Pos Inv:
 - Invert luminance
 - Gaussian filter:
 - smoothing effect ($\sigma=1.3$)
 - Emboss filter:
 - emphasize emboss outline
 - Laplacian filter:
 - Edge detection
 - Sobel filter:
 - Edge detection + emboss
- 3x3 window size Laplacian filter operation
- $$\begin{bmatrix} 4 & 9 & 2 & 5 \\ 8 & 6 & 2 & 4 \\ 3 & 4 & 5 & 4 \end{bmatrix} * \begin{bmatrix} 1 & 1 & 1 \\ 1 & -8 & 1 \\ 1 & 1 & 1 \end{bmatrix} = 23$$
- $$9*1 + 2*1 + 5*1 + 6*1 - 2*8 + 4*1 + 4*1 + 5*1 + 4*1 = 23$$

TMDS Timing Manager

- Manage current position of output
 - count Horizontal address with pixel clock from TMDs
 - count Vertical address with active of Horizontal Synchronization pulse
 - Current position will be reset with Vertical Synchronization pulse

BRAM

- Image data is stored from SDK
 - can change contents without synthesizing
- Connected with both PS and PL module
 - PS connection: via AXI interface
 - PL connection: Image Process