Implementation and Evaluation of Soft-Error Resilient Method for *OASIS* Network-on-Chip

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Abstract

Recently, demand for Many-core based system is increasing in System-on-Chip (SoC). Networ-on-Chip paradigm offers more promising scalability than conventional shared-bus architecture. As device scale shrinks and power optimized, on-chip interconnects became unreliable. Transient fault is caused by several noise problems such as cross-talk, coupling noise. These transient error leads to performance degradation or system crash. In this research, providing on-chip interconnects resilience from transient error is focused.

1 Introduction

1.1 Background

Recently demand for Many-core based system is increasing. In Many/Multi-core System-on-Chips (MSoCs) architecture, global interconnects is the major performance bottleneck. Major and modern backbone architecture is shared-bus. Although shared-bus architecture has simple structure, high extensibility and low area cost, it suffers from some limitations. Low scalability - practical number of cores is only up to tens of cores. No parallelism - shared bus allows only one communication at a time. Long wire Problem - the longer wires become when many cores are attached, and the more delay increases due to long path and capacitance. Therefore, efficient global interconnect is necessary for future Many-core based system architecture.

1.2 Network-on-Chip

Network-on-Chip (NoC) interconnects has been proposed for future MSoCs. Compared with shared-bus based architecture, NoC is better regarding scalability and parallelism. NoC paradigm allows more processing elements to be efficiently integrated into a SoC. Processing elements are connected via a packet-switched communication network NoC paradigm is suitable for connections between heterogeneous processing elements. In our laboratory, optimized NoC named as OASIS was designed, that is intended for massively parallel applications and safety-critical applications.

1.3 Motivation

In deep submicron technology (DSM), device shrinks towards nanometer scale and on-chip interconnects turn out to be a critical bottleneck in performance and power consumption. Shrinking future size of the device should make the power supply voltage and device voltage decrease, and the wires become unreliable. Several problems occur in on-chip interconnects, decreasing supply voltage, and increasing wire density and faster clock rates. These problem cause data corruption, timing fault and IR drop. Hence, these transient error leads to performance degradation or system crash. We must provide resilience for on-chip interconnects from such transient delay and logic error. Otherwise proper system operation cannot be assured.

1.4 Research goal

In this research, there are two types of approach to solve the soft error problems in NoC system. Single-erorr-correction, double-error-detection (SECDED) is an error protection method widely used to increase computer memory reliability. This method can detect or correct errors, that occur from data signals. Error correction ability of SECDED is not so high, but it can process quickly. This method is intended for time critical safety applications.

In this paper, Soft-error-resilient (SER) 2D-NoC router architecture is proposed. The proposed architecture can recover from transient errors.

2 *OASIS* Network-on-Chip

The *OASIS*-NoC system is targeted for safety critical embedded applications. This system architecture and the router block diagram with its three main pipeline stages: (Buffer Writing, Routing calculation/Switch Arbitration and the Crossbar Traversal), are shown in Fig. 1. OASIS-NoC adopts Mesh topology, *Stall-go* flow control and *Wormhole*-like switching as parameters.

In *OASIS* NoC system, router's utilization of buffer is efficient because of switching the forwarding method by depending on the buffer size [3]. The forwarding method is determined by its level of packet

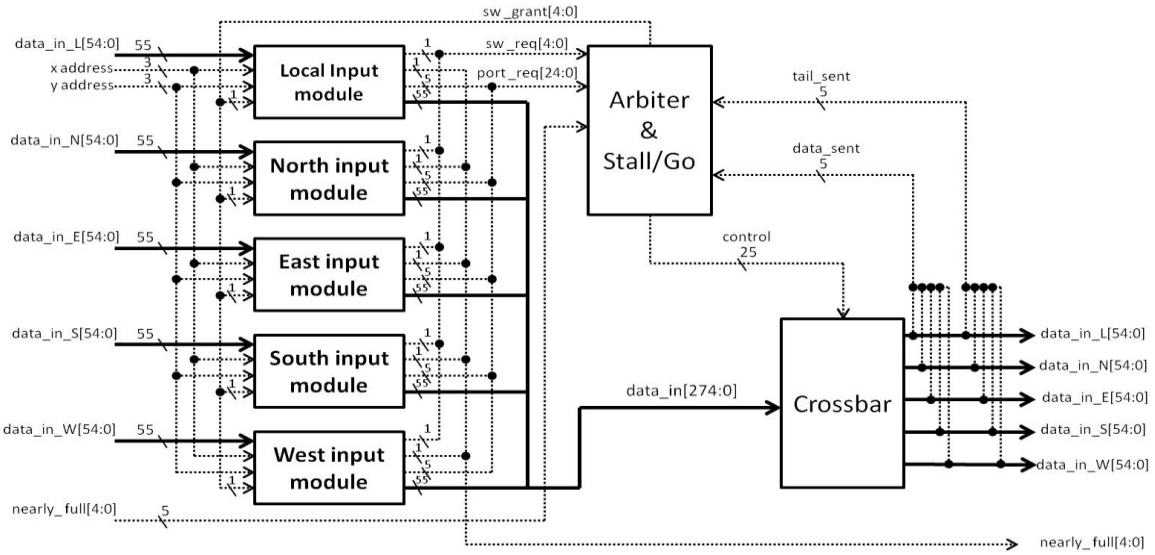

Figure 1. OASIS NoC router architecture

fragmentation. There are two types of forwarding method - *Virtual Cut Through* and *Wormhole switching*. When the buffer size is greater than the number of flits, *Virtual-Cut-Through* is used. However, when the buffer size is less than or equal to the number of flits, *Wormhole switching* is used. Therefore, we can forward data efficiently with a small buffer size. Fig. xx shows the flit format of OASIS NoC and its size is 28 bit. The first bit indicates the tail bit informing the end of the packet. The next 5-bit are dedicated for the Next Port that

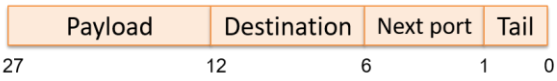

Figure 2. Flit format

will be used by the Look-Ahead routing algorithm to define the direction of the next downstream neighboring node where the flit will **be sent to**. Then, 3-bit are used to store destination information of each x-destination(xdest) and y-destination(ydest). Finally, the remaining 16 bits are dedicated to store the payload.

The OASIS NoC router contains three main module as Input-port(IP), Switch-Allocator(SA) and Crossbar-Traversal(CT). Those handle the transfer of the data from next adjacent router. The Input-port module contains input-buffer(FIFO structure) and next-port router calculation module. First the flit from the connecting router or tile is sent to Input-port module and stored in Input-buffer. This is conducted at first pipeline stage-Buffer Writing(BW). After that, the flit is read from the buffer and calculated for next port direction at 2nd pipeline stage-Next-port-computing/Switch Allocation(NPC/SA). NPC is done by computing the next router's output port by using source and destination address. In LAFT system, the next port direction is already calculated in the previous upstream node. At the same time, SA is done for flow-control of router's communication. This module check the next router's buffer, if the buffer is nearly full(stall signal is active). Otherwise,

Go signal is active and can send the data to the next router.

3 Soft error resilient method

In this research, the single error correction and double error detection(SECDED) was adopted as an Error correcting code(ECC) to provide reliability from soft errors. ECC module was based on "a class of optimal minimum odd-weight-column SECDED" [4]. This is an error protection method widely used to increase computer memory reliability. This method can detect or correct error occurred on data signals. In the case of 1 bit error, this method can correct the error by inverting the corresponding bit. In the case of 2 bit errors, this method just detects the error. Error correction ability of SECDED is not so high, but it can process quickly. This method is intended for time critical safety applications. This chapter explained about encoder module and decoder module.

3.1 A class of optimal minimum odd-weight-column SECDED

This method is basically based on Hamming-based

Byte	Bit	sb0	sb1	sb2	sb3	sb4	sb5	sb6
0	0	1				1		1
	1	1			1		1	
	2	1		1		1		
	3	1	1		1			
	4	1					1	1
	5	1	1				1	
	6	1				1	1	
	7	1			1			1
1	8		1	1				1
	9		1				1	1
	10		1			1	1	
	11		1		1	1		
	12		1	1	1			
	13	1	1					1
	14		1	1		1		
	15		1			1		1
2	16	1	1	1				
	17	1		1			1	
	18			1			1	1
	19			1	1		1	
	20			1	1	1		
	21			1		1	1	
	22			1		1		1
	23			1	1			1
3	24	1			1	1		
	25		1		1			1
	26				1	1	1	
	27				1		1	1
check	28	1						
	29		1					
	30			1				
	31				1			
	32					1		
	33						1	
	34							1

Table 1 (35,28) H-matrix for SECDED

SECDED, but its generating process of H-matrix(parity check bit matrix) is optimized in terms of composing minimum 1's bit. Minimum number of 1's bit in H-matrix means that it needs minimum number of logic gates in its module because of 1's bit reduction. H-matrix generates parity check bits covering different subsets of bits, comprising of a data word, and then gets coded data by just attaching the code to the data. Decoding process is done by recalculating parity over the encoded data word with parity check bits. The parity check bits encoded at the encoder are defined as syndrome bit. In this research case, (35, 28)-H-matrix in Table 1 was used for encoding flit(28bit) to encoded data(35bit).

3.2 Encoder process and module

As mentioned before, encoder process is done by using H-matrix. The minimum number of check bits needed for single error correction is calculated in following relationship:

$$D + P + 1 \leq 2^p$$

In here, D means the number of data bits and P denotes the number of parity check bits. Hence, 6 bits is needed for single error case in 28-bit data word case. Double error detection is done by an additional check bit across all the data and other parity bits. Therefore, total 7 bits are needed for correcting and detecting error. Parity check bits are generated by XORing and the corresponding data bits specified in Table 1. Figure 3 shows modified flit format for code word.

For instance:
Check_bit[0] = data_in[0] ^ data_in[1] ^ data_in[2] ^ data_in[3] ^ data_in[4] ^ data_in[5] ^ data_in[6] ^ data_in[7] ^ data_in[13]^ data_in[16]^ data_in[17]^ data_in[24];

Figure 3. Modified flit format

3.4 Decoder process and module

In decoder process, syndrome bits are calculated over the corresponding data and parity check bit. In no error case, calculated syndrome bits contain all-0's bit. Hence, if there's any 1's bit in syndrome bits, it means error has occurred.

i.e. error = | syndrome_bit;
{syndrome_bit is 7 bit signal, [6:0]}

In single error case, error mask bits are generated by syndrome relationship. A bit corresponding the error location will be set. Corresponding process is done by XORing and the data word and error mask. In this case,

syndrome bits compose an odd number of 1's bit.
i.e. single_error = error & (^ syndrome_bit);
In double error case, no bits will be set in the error mask and its syndrome bits compose an even number of 1's bit.
i.e. double_error = error & !(^ syndrome_bit);

4 Implementation

In this research, 2x2 and 3x3 network size OASIS Network-on-Chip was designed in *VerilogHDL*, and synthesized with *Altera Quartus II* ver 13.0 sp1. 2x2 OASIS with error injection module was shown in Figure 4.

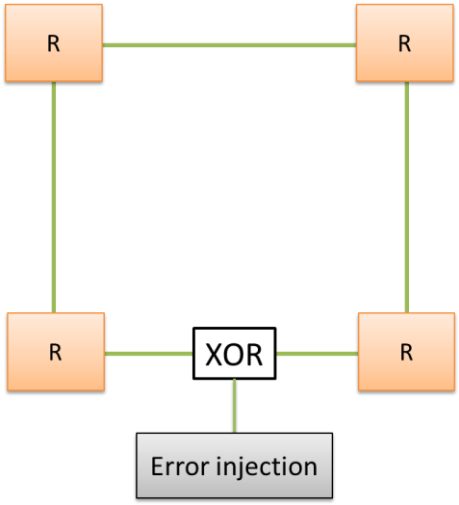

Figure 4. 2x2 network OASIS

SECDED encoder and decoder modules were also implemented. Figure 5 shows router architecture with integration encoder and decoder modules. Encoder and decoder modules were implemented in input-port and crossbar-traversal modules respectively. Simulation was conducted by *ModelSim*.

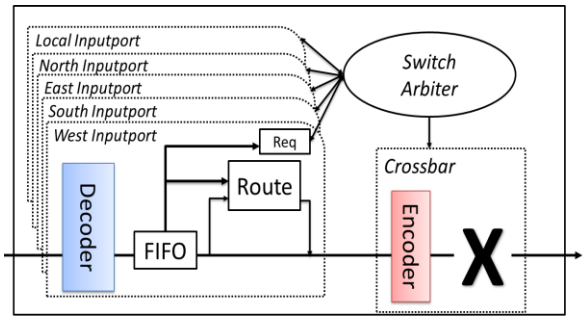

Figure 5. Router with SECDED modules

5 Evaluation

In this research, 2D layer (2x2 network size) OASIS NoC was designed in Verilog HDL. Synthesize and simulation was conducted by Quartus II(ver 13.0 sp1). Evaluation methods for timing and power consumption were conducted by *Time Quest* and *PowerPlay* tools. Target devices is *Stratix IV: EP4SGX530NF45C3*.

5.1 Hardware complexity

Figure 6 shows the hardware complexity evaluation result, 2x2 and 3x3 network with Original and Soft-error-resilient OASIS respectively. Original OASIS means conventional OASIS that is no-fault-tolerant. SER-OASIS means original OASIS with ECC-module for error protection. Area utilization and power consumption results were conducted with 160MHz operating frequency rate. In area utilization evaluation result, SER OASIS increased dedicated logic registers 2,060 to 2,074 with 2x2 network size and 0.06% increased with 3x3 network size. Power consumption was calculated by PowerPlay Power Analyzer.

	2x2		3x3	
	Original	SER	Original	SER
Area - ALUTs (usage /424,960)	1,748 (1%)	2,881 (1%)	5,790 (1%)	8,913 (2%)
- Registers (usage /424,960)	2,060 (1%)	2,074 (1%)	5,702 (1%)	5,709 (1%)

Figure 6. Hardware complexity results

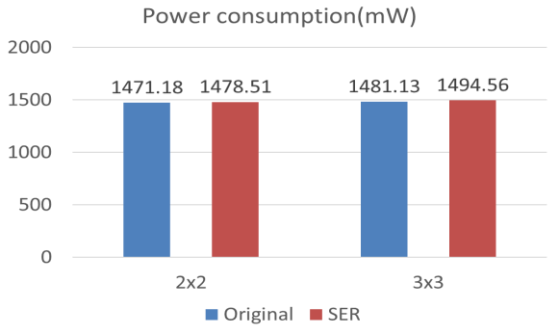

Figure 7. Power consumption

Quartus II compiler results show the result of hardware complexity. In result of area utilization, although usage of ALUTs increased 1,748/424,960(1%) to 2,881/424,960(1%) in 2x2 network size. In 3x3 network size, increased 5,790/424,960(1%) to 8,913/424,960(2%). Usage of

registers were nearly the same results in 2x2 and 3x3 respectively. We achieved reasonable results in area utilization. Figure 7 shows power consumption evaluation in 160MHz operating frequency. As you can see, SER-OASIS increased 0.005% and 0.009% in 2x2 and 3x3 network respectively. These overhead were also small.

6 Conclusion

In this paper soft error resilient method was proposed for critical error problem on OASIS NoC. 2x2 and 3x3 network size OASIS NoC was implemented with only router. SECDED encoder and decoder were implemented as ECC module. ECC module was integrated into OASIS NoC in router, called SER OASIS. Hardware complexity evaluation was conducted. Although ECC-module was integrated into routers, overhead, area utilization and power consumption, was very small. Soft error approach on switch-to-switch reliability was improved with small overhead.

6.1 Future work

For higher error protection mechanism, there are two approaches as future work. This OASIS NoC does not support retransmission mechanism for error detection case. Also additional pipeline stage for redundant calculation is necessary for further reliability. To achieve this, *auto-repeat-request(ARQ)* mechanism and additional hardware, compare and rollback modules are necessary.

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