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P1 MIDTERM PROJECT

In Partial Fulfillment for the Subject

CPE C401–301G: Computer Architecture and Organization

Submitted to the Computer Engineering Department

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June 2025

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Google Drive Link for Video Presentation:

https://drive.google.com/drive/folders/1RMc4Qei7JrQ7bIN52P4YAGsYqWnEMIDE?usp=sharing

Introduction

This project implements a 4-bit binary adder and subtractor circuit using discrete logic on ICs on a breadboard. The circuit can perform both addition and subtraction operations on two 4-bit binary numbers (A and B) and displays the results in both binary form (using LEDs) and decimal form (using 7-segment display).

The circuit uses the two's complement method for subtraction, where subtraction A - B is performed as $A + (\bar{B} + 1)$, where $\bar{B}$ represents the bitwise complement of B.

Objectives:

1. Add 2 4-bit inputs and display on the sum of outputs on the 7-segment display
2. Subtract 2 4-bit inputs and display the difference between the inputs on the 7-segment display, it should also display negative values.
3. Use a switch to change modes between addition and subtraction
4. Use LEDs to determine if an input is switched on. Display the sum or difference of the inputs through LEDs (in binary).
5. Use a 7-segment display to display the output of the sum and difference, and convert the binary output into decimal output for the 7-segment.

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Materials:

Materials	Quantity
5-9V Power Source	1
Breadboard	4
Jumper Wires	several
7-Segment Display	1
LED	several
Switch	1
Resistor (220Ω)	several
4-Dip Switch SPDT	2
74LS83- 4-bit adder IC	1
74LS86 - XOR IC	1
CD4511 - BCD to 7-Segment IC	1

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Truth Tables:

Addition Truth Table				
A3 A2 A1 A0	**B3 B2 B1 B0**	**Sum**	**S3 S2 S1 S0**	**Carry**
0000 (0)	0000 (0)	0	0000	0
0001 (1)	0001 (1)	2	0010	0
0101 (5)	0011 (3)	8	1000	0
1000 (8)	0111(7)	15	1111	0
1001 (9)	1000 (8)	17	0001	1
1111 (15)	1111 (15)	30	1110	1

Subtraction Truth Table						
A3 A2 A1 A0	**B3 B2 B1 B0**	**Difference**	**S3 S2 S1 S0**	**Sign**	**Display**	**2's Complement Display**
1000 (8)	0011 (3)	+5	0101	0	05	1
1000 (8)	1111 (15)	-7	1001	1	-07	9
0101 (5)	1010 (10)	-5	1011	1	-05	11
1111 (15)	0001 (1)	+14	1110	0	14	14
0000 (0)	1111 (15)	-15	0001	1	-15	-15

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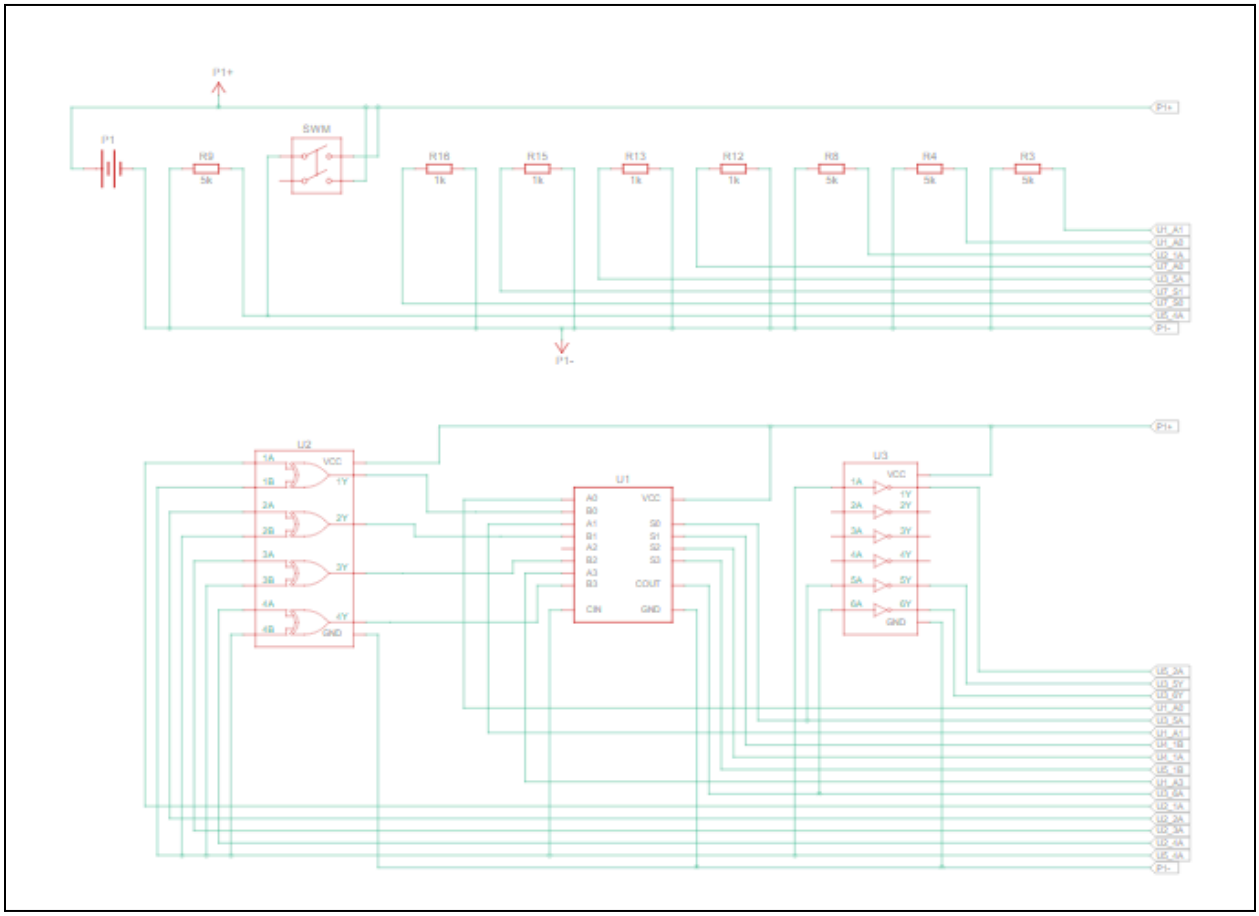
XOR Gate Truth Table		
B	**SUB**	**B SUB**
0	0	0
0	1	1
1	0	1
1	1	0

Schematic Diagram:



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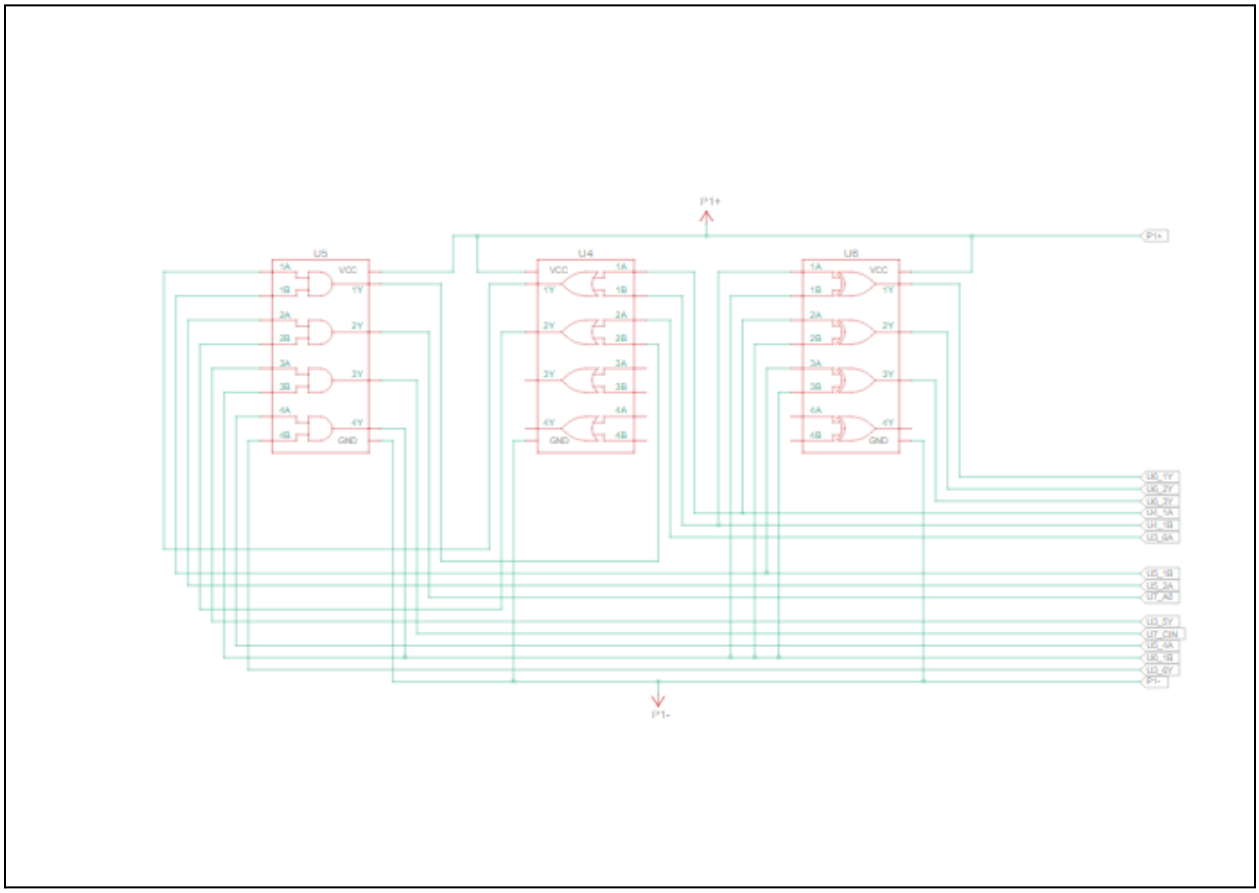

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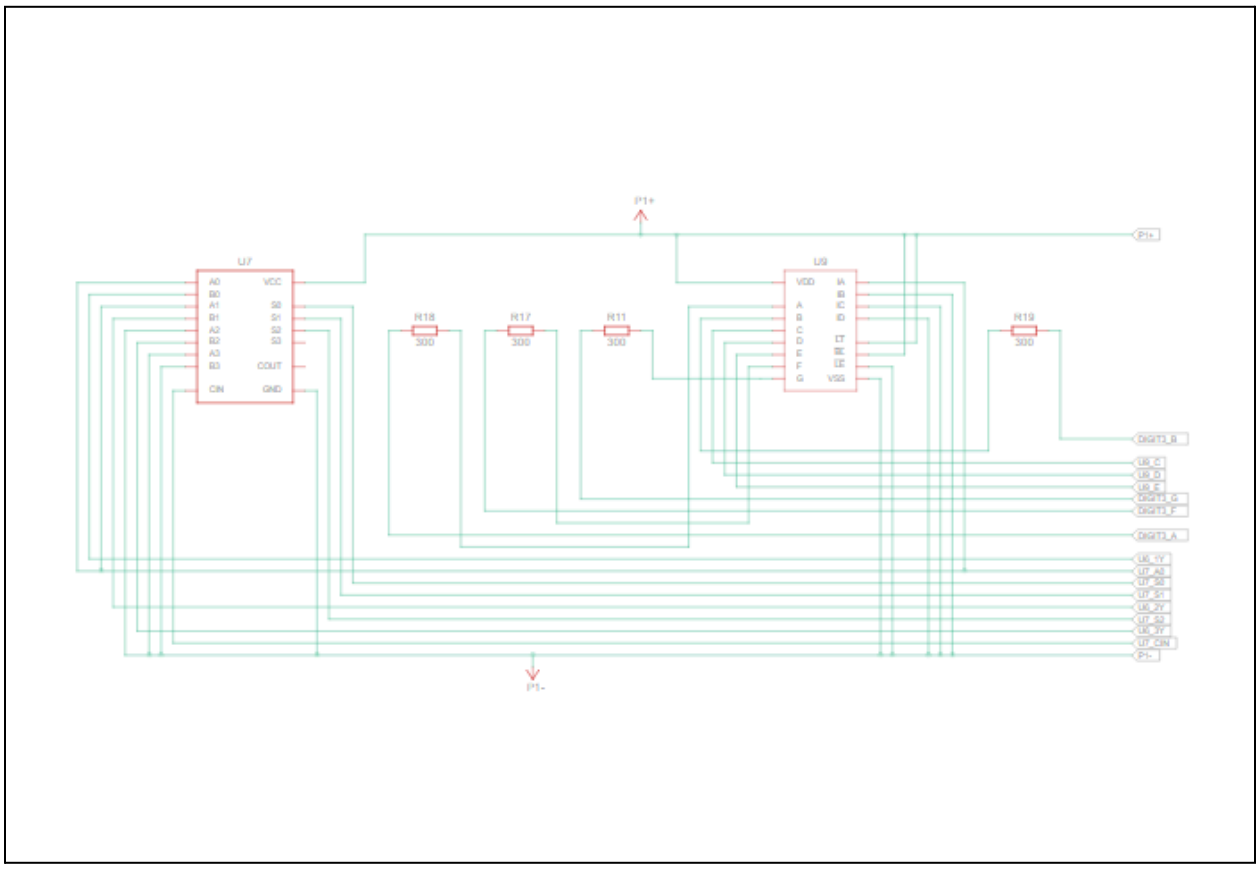

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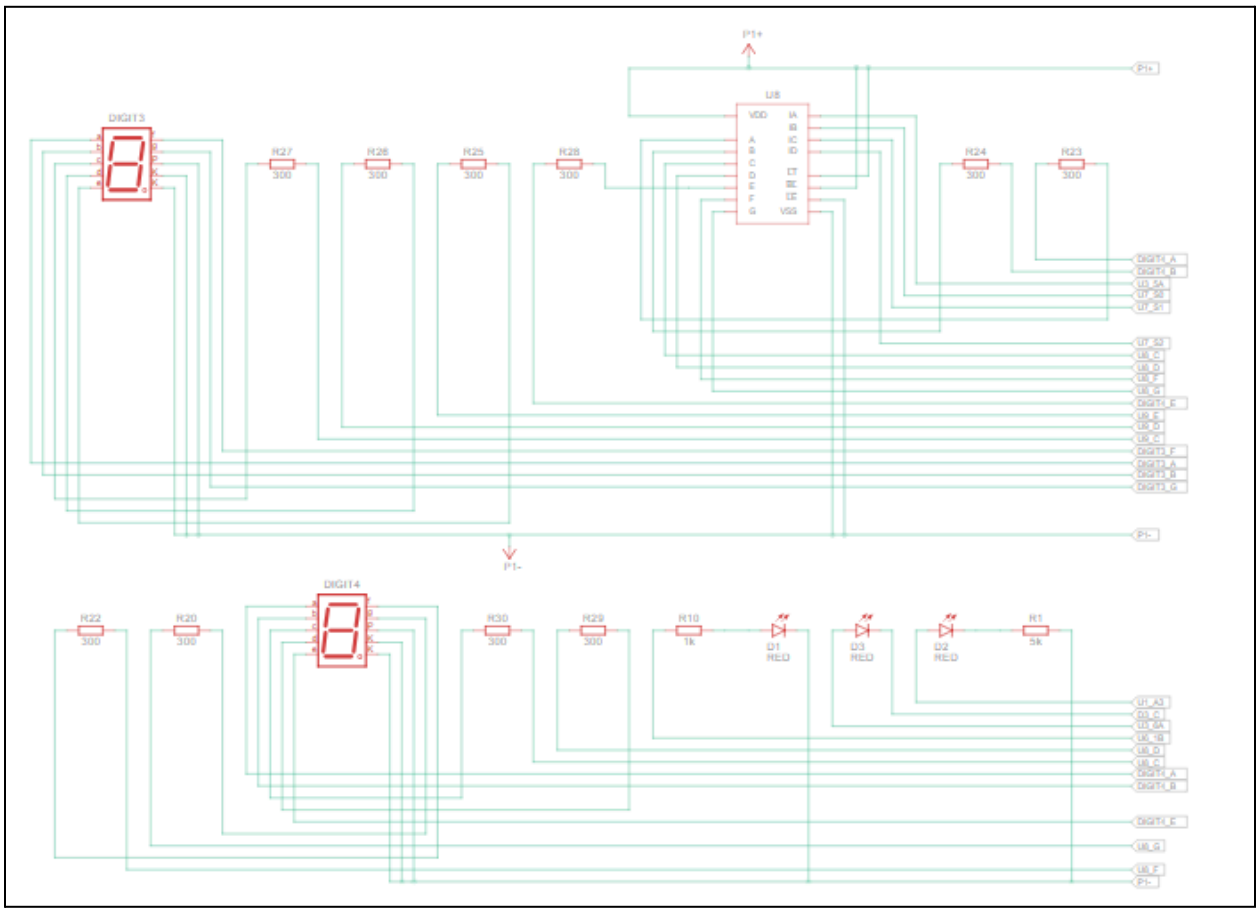

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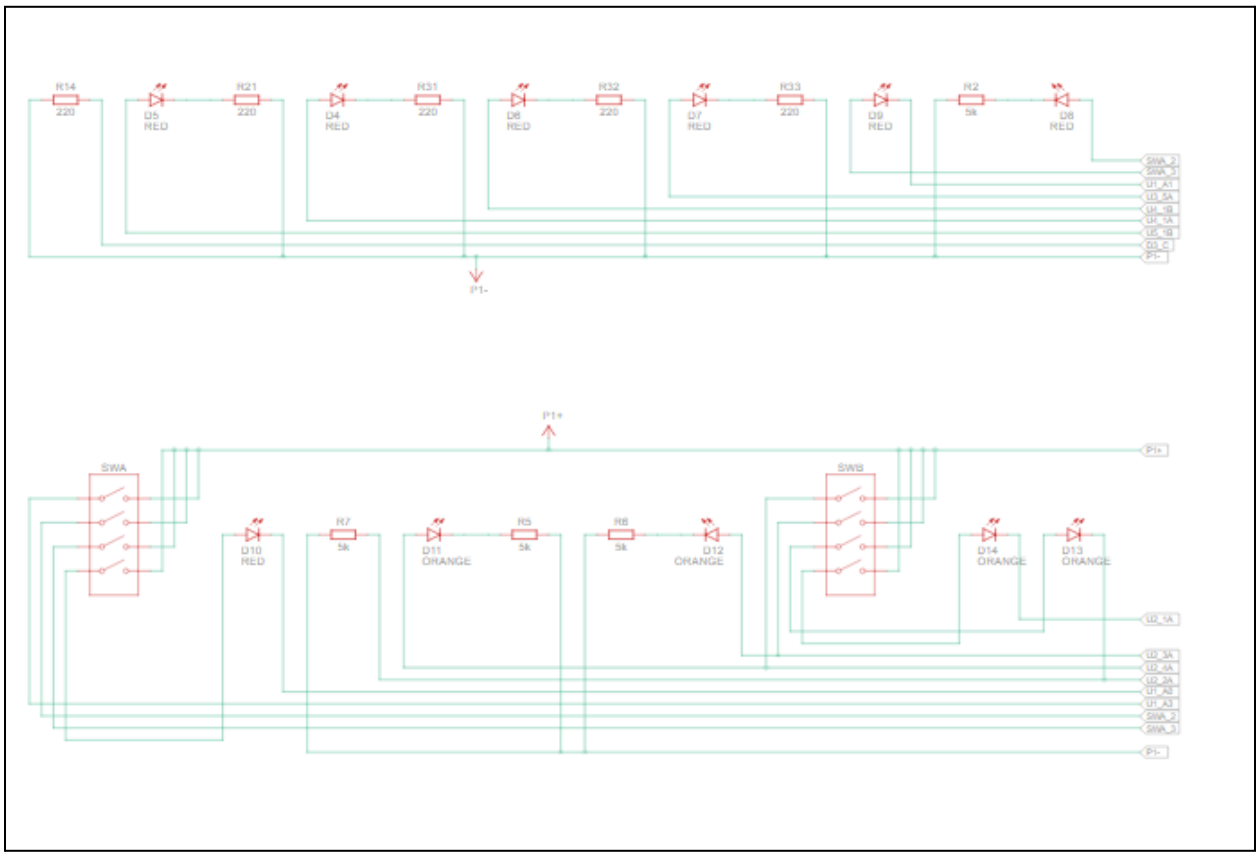

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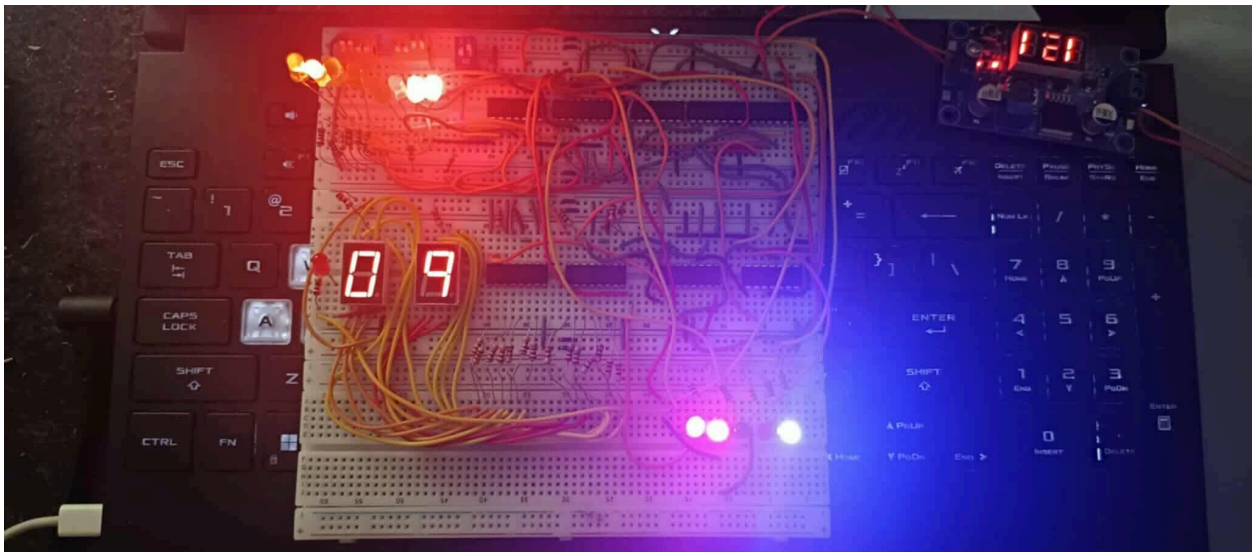
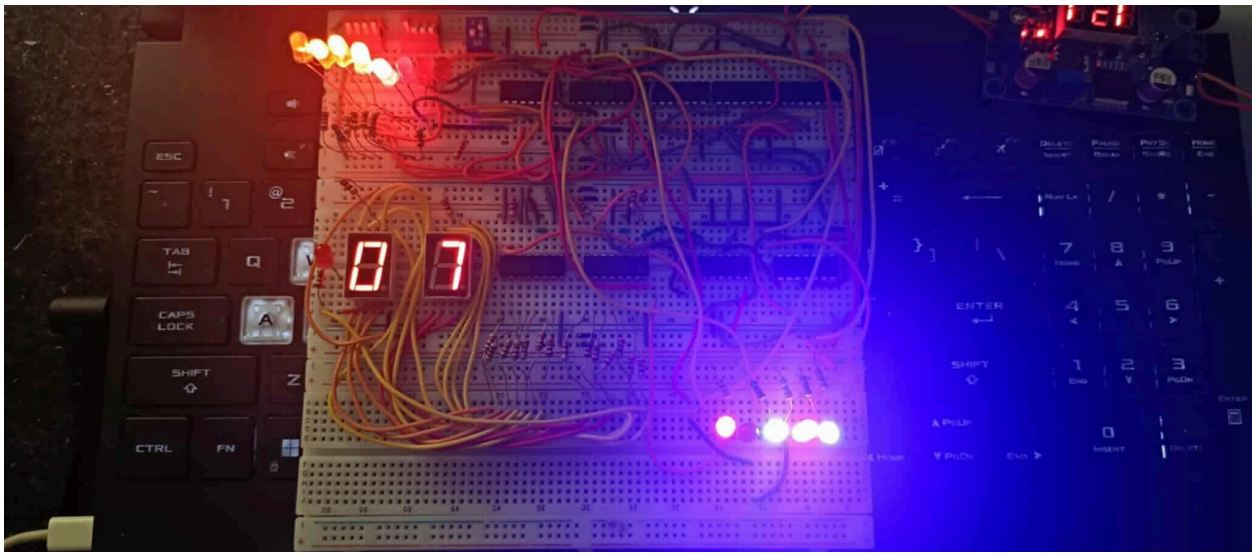
Pictures:

Final Output

12 - 3



15 - 8



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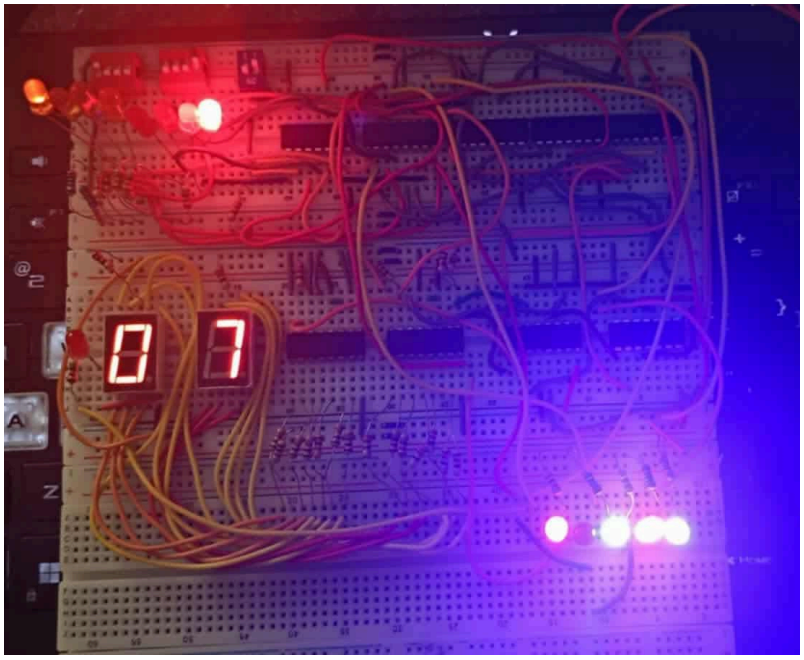
8-1



8 + 8

M.

3 + 9

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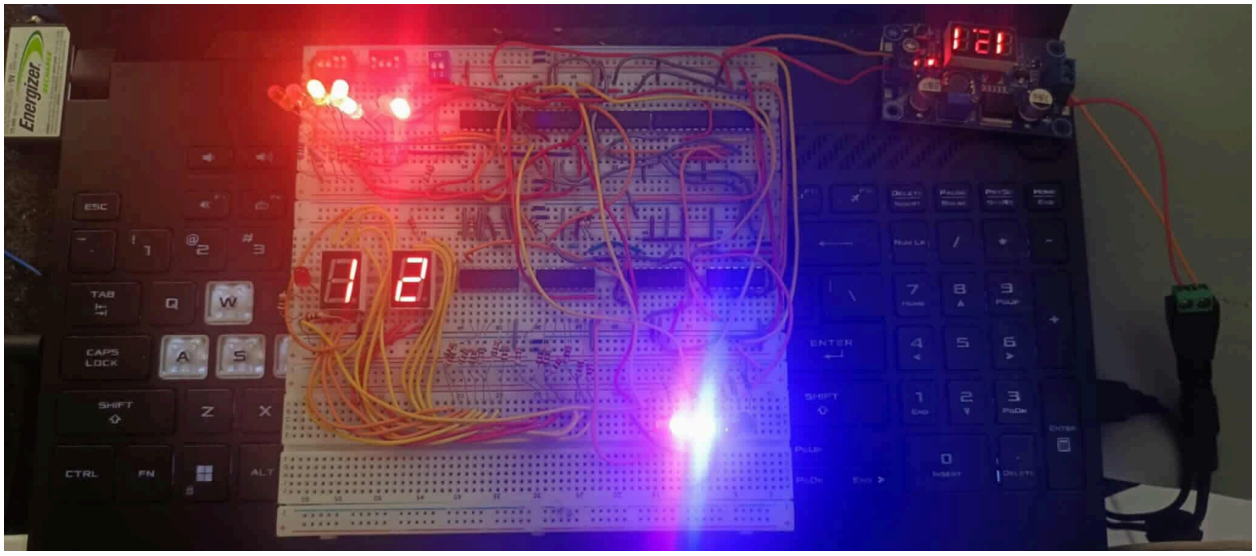
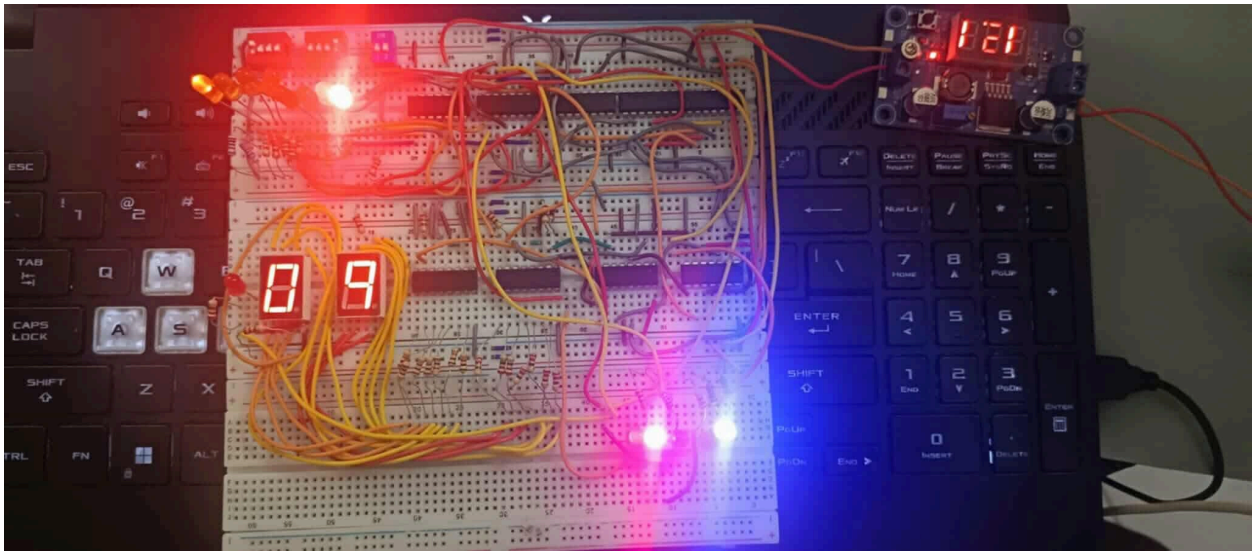


8 + 1



Trial and Error:

Initial design with 1 7-Segment Display:

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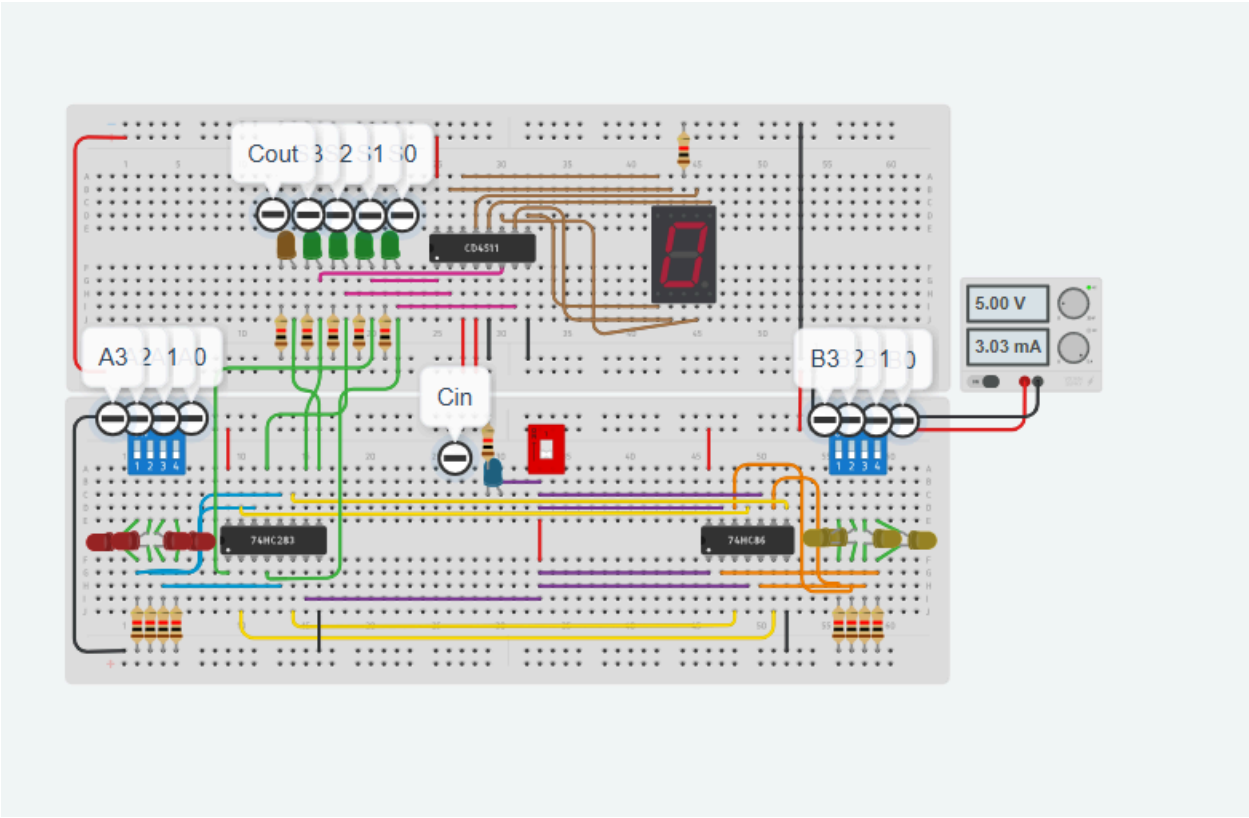

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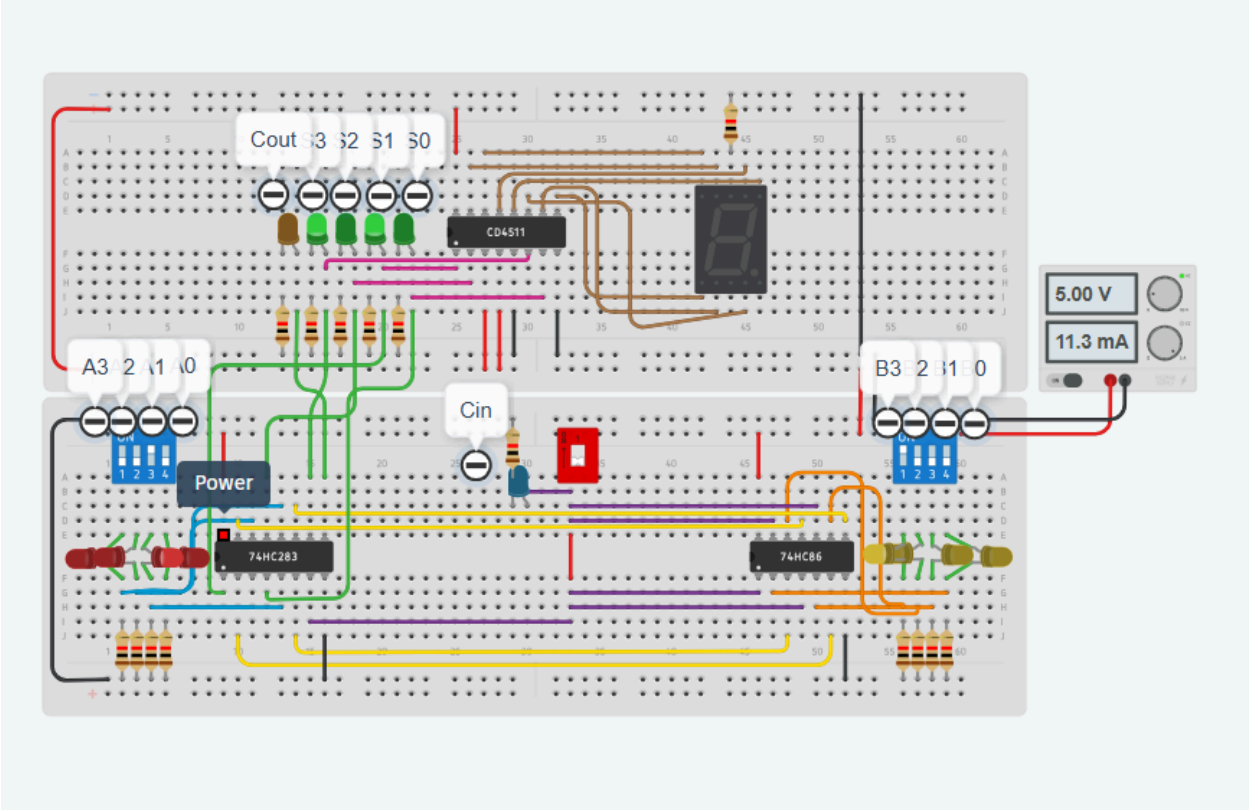

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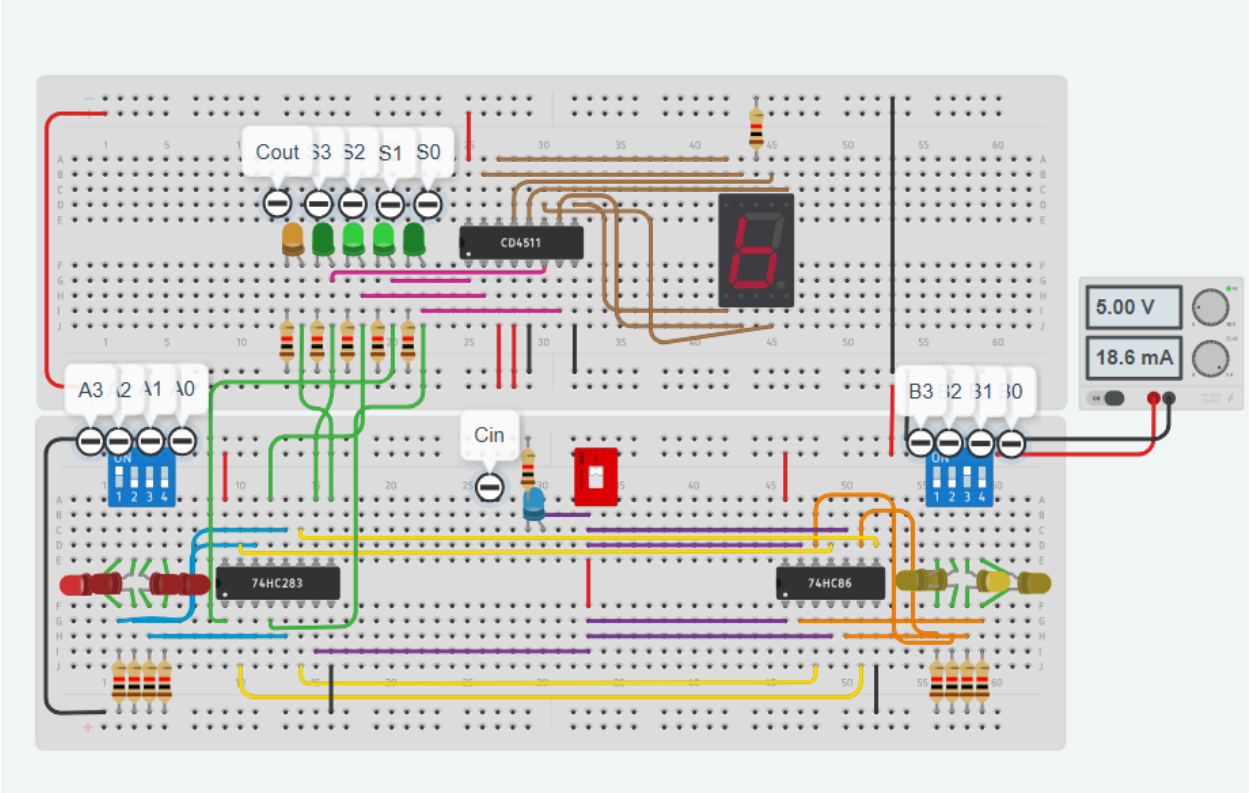

Reflection:

We discovered that the output for subtraction uses two's complements to display negative values hence why equations that lead to negative values such as 8 minus 15 display an output of 1001 which is the two's complement of -7. In order to improve the display of 7-segment from 1 digit to 2 digits, a process/algorithm called double dabble is needed, but it would require a lot of logic gates to implement just to display 2-digit numbers through the 7-segment displays.