

# SHAYAUN BASHAR

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## EDUCATION

### University of California, San Diego

Sep 2019 – June 2024

*Undergraduate, Bachelor of Science Electrical Engineering, Provost Honors 22'*

### Publications/Awards

- “**ForceSticker: Wireless, Batteryless, Thin & Flexible Force Sensors**” (Co-Author) [Demo Video](#), [ACM IMWUT '23](#)
- “Design and Evaluation of a miniaturized Force Sensor Based on Wave Backscattering” (Co-Author) [IEEE RA-L, IROS '22](#)
- “PaciForce” (Co-Presenter) (Won Best Poster Award in ECE at UC San Diego’s Research Expo 2025)

## Work Experience

### R&D Engineer, WCSNG Lab (@UC San Diego)

Aug 2024 – Ongoing

#### Wireless Force Sensing Baby Pacifier

- Project Overview:
  - Embedded a **battery-less pressure/vacuum sensor** into pacifiers to replace the subjective "gloved finger" test, providing clinicians with quantitative data for diagnosing newborn feeding issues during a critical window
  - Developed a custom sensor that translates applied force into phase changes in backscattered RF signals, enabling low power operation
  - Provides a cost-effective solution for pediatric healthcare with potential for FDA medical device certification
- Responsibilities:
  - Improved fabrication of sensor
    - Increased sensor batch **yield** 80% by improving polymer adhesion techniques & eliminating air bubbles
    - Improved sensor **consistency, reducing operating frequency standard deviation** by 80% through optimizing polymer-based sensor geometry
    - Reduced **fabrication time** by 25% by streamlining processes and removing redundant steps
    - Increased **sensor sensitivity** by 167% by optimizing polymer material selection
  - Conducted vacuum pressure performance testing to benchmark the sensor against industry-standard pacifier sensors, validating its dual-functionality for both force and vacuum pressure sensing
  - Sensor testing and data analysis
    - Conducted extensive sensor testing across multiple batches to identify fabrication improvements that enhanced yield, consistency, and sensitivity
    - Developed **Python** script to communicate with **VNA/Arduino**/actuator to apply step forces to collect S11 data, generating phase vs force graphs for analysis
    - Created a simple algorithm in **python** to identify the optimal frequency that maximize phase change while ensuring linearity error control and maintaining > -5db differential magnitude

## Undergraduate Research / Course Projects

### ForceSticker: Wireless, Battery-less, Thin & Flexible Force Sensors

April 2021 – March 2023

*Undergraduate Researcher, WCSNG Lab UC San Diego, Under Prof. Dinesh Bharadia and Tania Morimoto*

- Developed a thin sticker-like wireless and battery-less force sensor at 900MHz, designed for industrial and medical applications
- Engineered a novel capacitive sensor design that translates applied force into analog phase changes in backscattered RF signals, enabling low power operation
- Led technical efforts in designing flex PCB in **Altium/HFSS**, simulating performance in **HFSS**, performing sensor fabrication, PCB soldering, and **VNA** testing for antenna and circuit verification
- Commercialization efforts by completing NSF I-Corps regionals and IGE MedTech Accelerator Programs

### SHA256/Bitcoin Hashing Algorithm RTL Model in System Verilog

September 2023 – December 2023

*ECE 111 (System Verilog Design course) Final Project*

- Designed and implemented a SHA-256 cryptographic hashing algorithm in **System Verilog** using **Quartus Prime**
- Implemented SHA-256 algorithm to design a Bitcoin parallel processing hash function in System-Verilog

### Custom 8-bit Adder

April 2023 – June 2023

*ECE 165 (VLSI course) Final Project*

- Created a custom PG 8-bit adder in **45nm CMOS** design using **Cadence Virtuoso**, presented in ISSCC format
- Developed a Kogge-Stone Adder from transistor level to logic and block-level architecture (PG, FCO, PPC blocks)
- Achieved a maximum clock frequency of 3GHz with a power consumption of 78.6uW/per cycle (For VDD=1.1V)

## Skills

**Software/Coding Languages:** Altium, Cadence Virtuoso, Intel Quartus Prime, HFSS, System Verilog, LT Spice, C/C++, MATLAB, Python

**Technical:** VNA testing, EE lab tools, Soldering, 3D printing

**Relevant Courses:** Digital Integrated Circuit Design, Introduction to active Circuit Design, Advanced Digital Design Project, Software foundation I & II, Programming for Data Analysis