Module MA-INF 4307	**Lab Field Programmable Gate Arrays**		
Workload 270 h	**Credit points** 9 CP	**Duration** 1 semester	**Frequency** at least every 2 years
Module coordinator	Prof. Dr. Joachim K. Anlauf		
Lecturer(s)	Prof. Dr. Joachim K. Anlauf		
Classification	**Programme** M. Sc. Computer Science	**Mode** Optional	**Semester** 2. or 3.
Technical skills	Development and simulation of digital circuits in VHDL and SystemC, experience with synthesizable subsets, knowledge of the design path from the idea to a realized circuit implemented in an FPGA (field programmable gate array)		
Soft skills	Communicative skills (oral and written presentation of results), social skills (ability to cooperate in small teams, discussions of solution concepts) self competences (ability to accept and formulate criticism, ability to analyze and find practical solutions to problems)		
Contents	VHDL for Hardware Description, Simulation, and Synthesis, SystemC for Hardware Description, Simulation, and Synthesis, Synthesizable Subsets, Test of Implementations on FPGA Evaluation Boards		
Prerequisites	**Recommended:** MA-INF 4207 – Dynamically Reconfigurable Systems		
Format	**Teaching format** / **Group size** / **h/week** / **Workload[h]** / **CP** Lab / 8 / 4 / 60 T / 210 S / 9 T = face-to-face teaching; S = independent study		
Exam achievements	Oral presentation, written report (graded)		
Study achievements	none (not graded)		
Forms of media			
Literature	Technical documentation		