JOHANNES KEPLER
UNIVERSITY LINZ

Hardware Design Course

WS24/25 382.048, 382.049

Michael Lunglmayr, Michael Köfinger
Institute of Signal Processing, Institute for Integrated Circuits

2025-01-20

JOHANNES KEPLER
UNIVERSITY LINZ
Altenberger Straße 69
4040 Linz, Austria
jku.at

Quartus Clock Frequency

- Run synthesis once with default clock settings
- *Compilation Report* → *Timing Analyzer* → *Clocks* → Right click on clock signal → *Edit Clock Constraint*

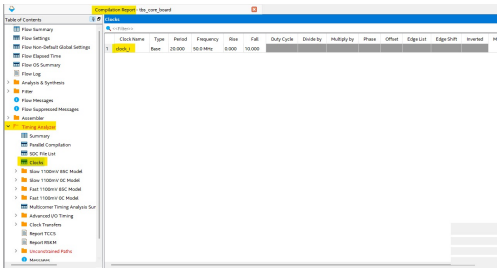

Figure 1: Compilation Report.

Quartus Clock Frequency cont’

- Adjust *Period*, *Rising* and *Falling* accordingly, press *Run*

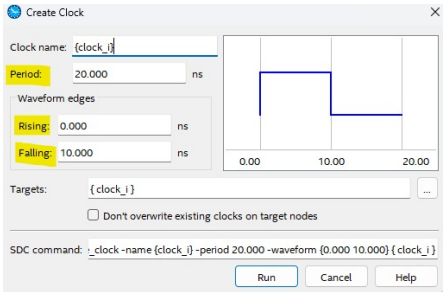

Figure 2: Edit Clock.

Quartus Clock Frequency cont’

- Close *Timing Analyzer UI*
- Save new timing constraint, remove “.out” from name
- Run synthesis again

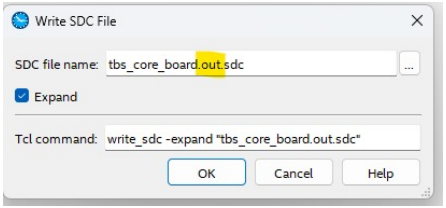

Figure 3: Save SDC.