Progress Report

We finished a draft of our Out-of-Order design. Each of us made our own design and then combined them together. We are not sure if this design works, and we are hoping to get feedback on our design from our mentor.

Roadmap

For checkpoint 1, we hope to make any design changes that our mentor provides during our initial meeting and create several modules to lessen the workload later on. We hope to, at minimum, finish designing and verifying the instruction queue. In addition, we would like to design and verify the regfile, ALU, and comparator modules - these will likely be very similar if not identical to the modules provided in MP2. If there is additional time, we would like to finish the other queues/buffers (ROB, load/store queue, etc).