

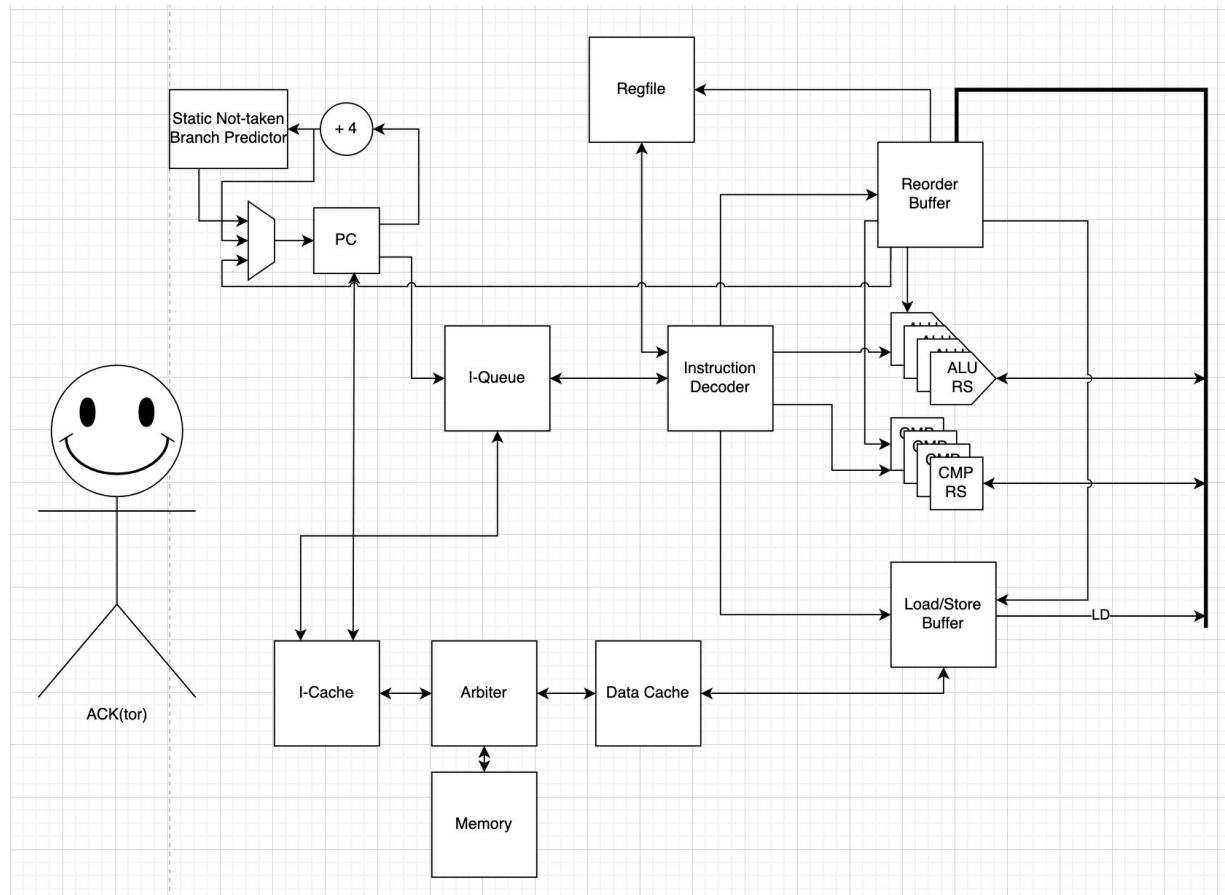
# spenserCPU

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ECE 411 SP22

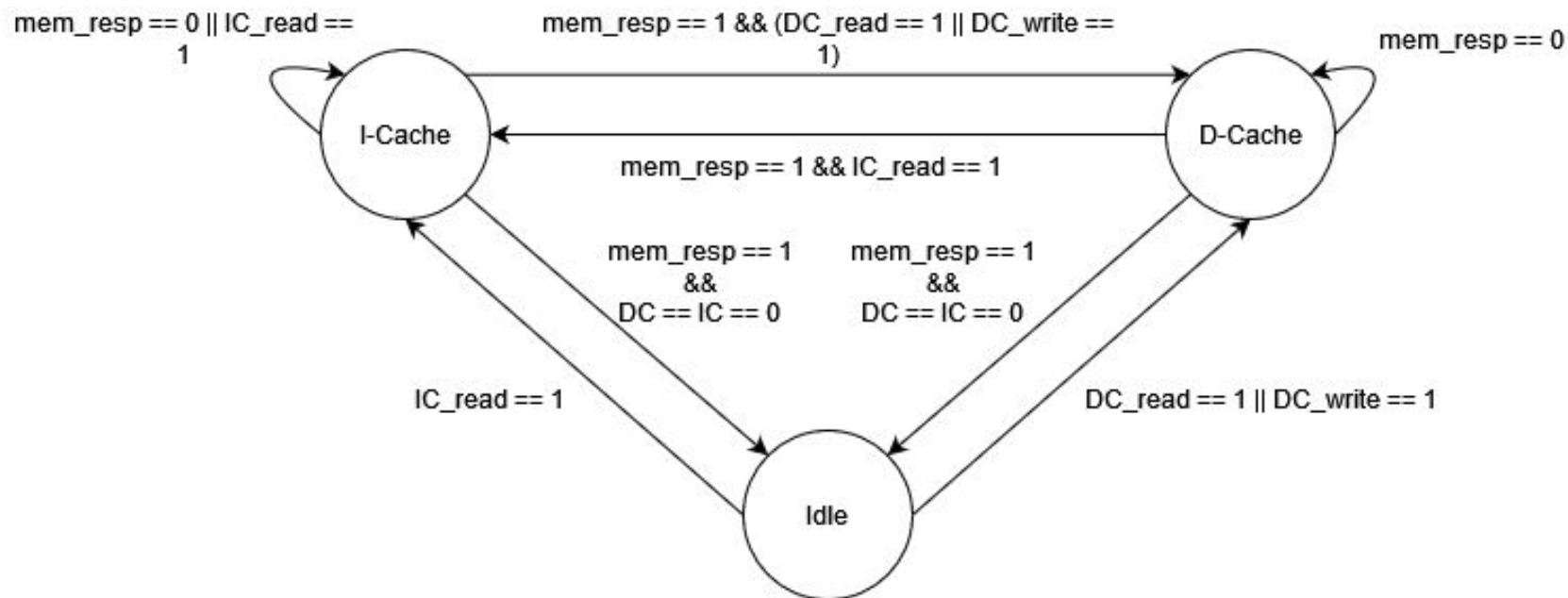
# Overview

- Speculative Tomasulo
- Static-not-taken branch predictor
- Direct-mapped Split Caches
- 8-Entry Reorder Buffer
- 6 ALUs + 6 Single-Entry ALU Reservation Stations
- 6 Compare LUs + 6 Single-Entry Compare LU Reservation Stations

# Datapath



# Arbiter



# Implementation

## Design Choices:

- Instead of mapping a multi-entry reservation station to a single ALU, we decided to map a single reservation station entry to a single ALU. This meant that we did not need to worry about combinational execution time

# Challenges

1. We had a hard time going from theory to implementation. Spent a lot of time trying to figure out how the textbook design correlated to actual code.
2. Not stalling instruction fetching properly.
3. Tag array updated one clock cycle late.
4. Lots of edgecases - needed tag broadcasted at the same time instruction was added to RS

# Performance – Checkpoint Code

	<b>MP2</b>	<b>MP4</b>	<b>Speedup</b>
<b>CP1</b>	33.505 $\mu$ s	7.345 $\mu$ s	356.16%
<b>CP2</b>	15.955 $\mu$ s	6.405 $\mu$ s	149.10%

# Performance – Fmax

	<b>MP2</b>	<b>MP4</b>
<b>Slow 900mV 100C</b>	105.15MHz	104.8MHz
<b>Slow 900mV -40C</b>	112.08MHz	111.54MHz



# Performance – Power

MP2		MP4	
Total Thermal Power Dissipation	392.53 mW	Total Thermal Power Dissipation	699.94 mW
Core Dynamic Thermal Power Dissipation	33.18 mW	Core Dynamic Thermal Power Dissipation	327.22 mW
Core Static Thermal Power Dissipation	318.97 mW	Core Static Thermal Power Dissipation	322.39 mW
I/O Thermal Power Dissipation	40.39 mW	I/O Thermal Power Dissipation	50.32 mW

# What We Wish We Did Differently

1. Simpler structs and less signals going between modules
2. Smaller Decode
3. Simpler ROB
4. Used modports
5. Create a robust datapath diagram before starting to code

Questions?