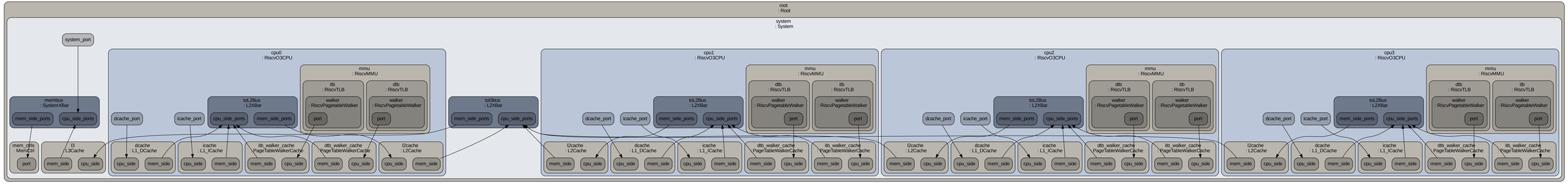
root
: Root
system
: System
system_port
membus
: SystemXBar
mem_side_ports
cpu_side_ports
mem_ctrls
: MemCtrl
port
l3
: L3Cache
mem_side
cpu_side
cpu0
: RiscvO3CPU
dcache_port
icache_port
toL2Bus
: L2XBar
cpu_side_ports
mem_side_ports
mmu
: RiscvMMU
itb
: RiscvTLB
dtb
: RiscvTLB
walker
: RiscvPagetableWalker
port
dcache
: L1_DCache
icache
: L1_ICache
itb_walker_cache
: PageTableWalkerCache
dtb_walker_cache
: PageTableWalkerCache
l2cache
: L2Cache
toL3bus
: L2XBar
cpu1
: RiscvO3CPU
cpu2
: RiscvO3CPU
cpu3
: RiscvO3CPU