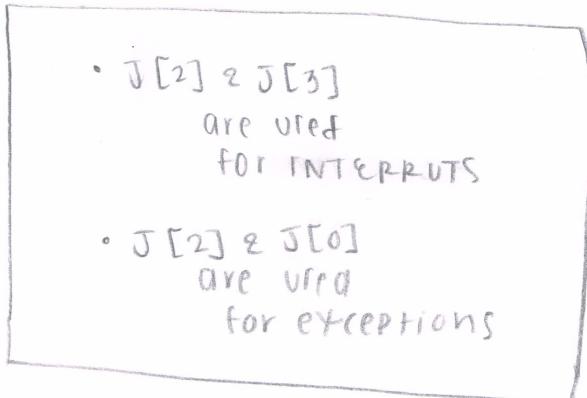
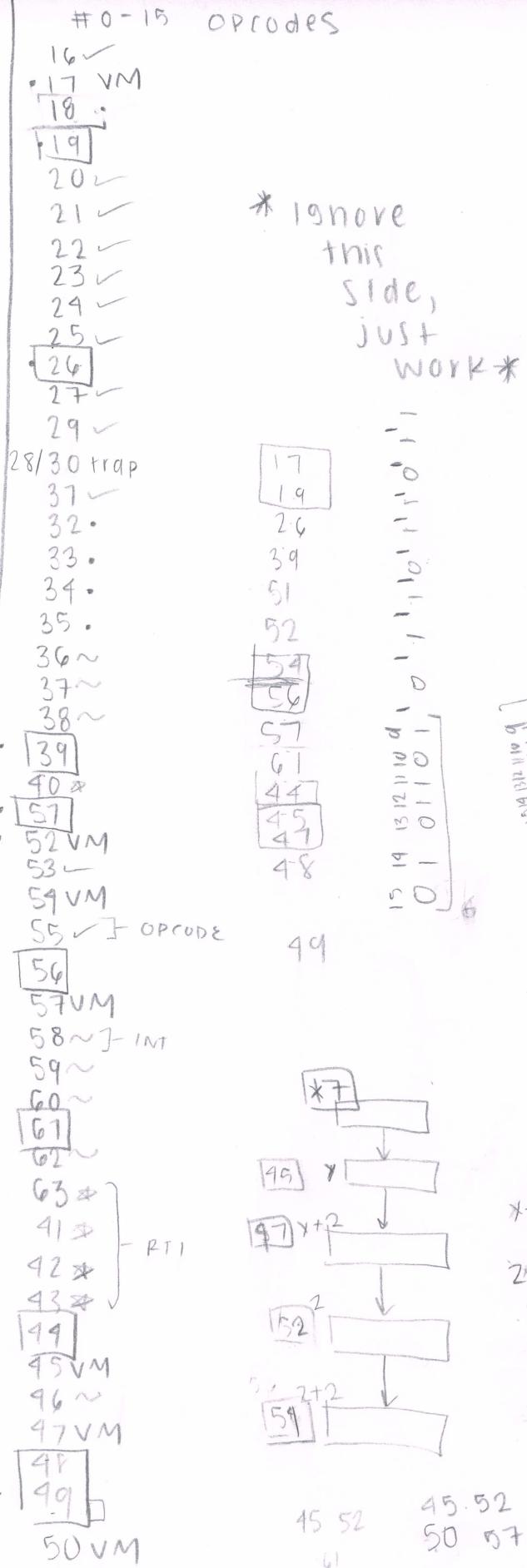


→ all new states
8 state transitions



ADDITIONS
TO FSM
(pg 3)



Datapath, already existing from Lab9 MUXES

RegMUX
0 - BUS
1 - USP

PSRMUX

0 - 0
1 - 1

Vec MUX

0 - x9
1 - INTV
2 - EXCV

DR MUX]
SR1 MUX] 2 - RG

NEW MUXES

RET MUX

0 - 40 }
1 - 41 } RTI
2 - 38 }
3 - 37 } INT
4 - 60 }
5 - 33 } Fetch
6 - 28 } TRAP
7 - 25
8 - 23
9 - 29
10 - 29

MDRMUX

0 - FROM MID.EN
1 - MDR[15:2] 'R.W'
2 - FROM SAVEMDR

NEW SIGNALS / REGS

→ PTBR

GATEPTBR - 1 bit

→ VA

GATEVA - 1 bit
LD.VA - 1 bit

- RET

LD.RET - 1 bit

- RET MUX - 4 bits

- SAVE MDR

LD.SAVEMDR - 1 bit

- VAMUX 1 bit

- VARETURNMUX - 1 bit

- MDRMUX [1:0] - 2 bit

→ R.W register *

LD.RW

MVY RW

VAMUX

0 - BUS
1 - MDR[13:9]
VA[9:0]

VARETMUX

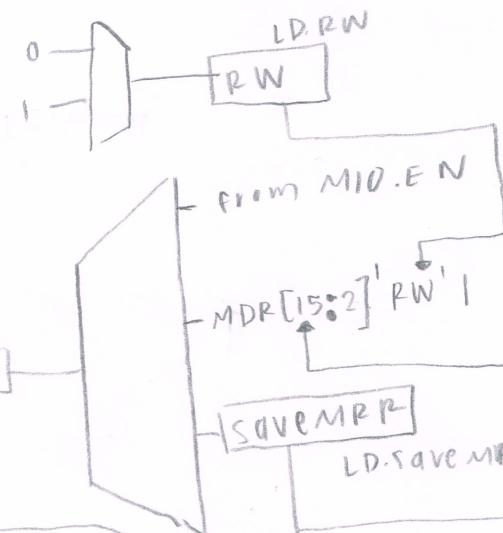
1 - RET

0 - VALUE FROM IRD MUX

MVY RW *

0 - read

1 - write

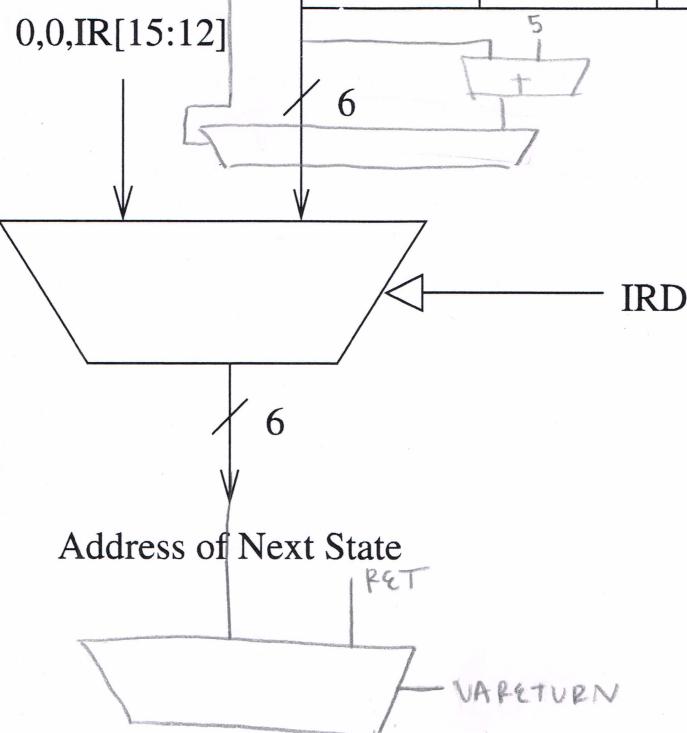
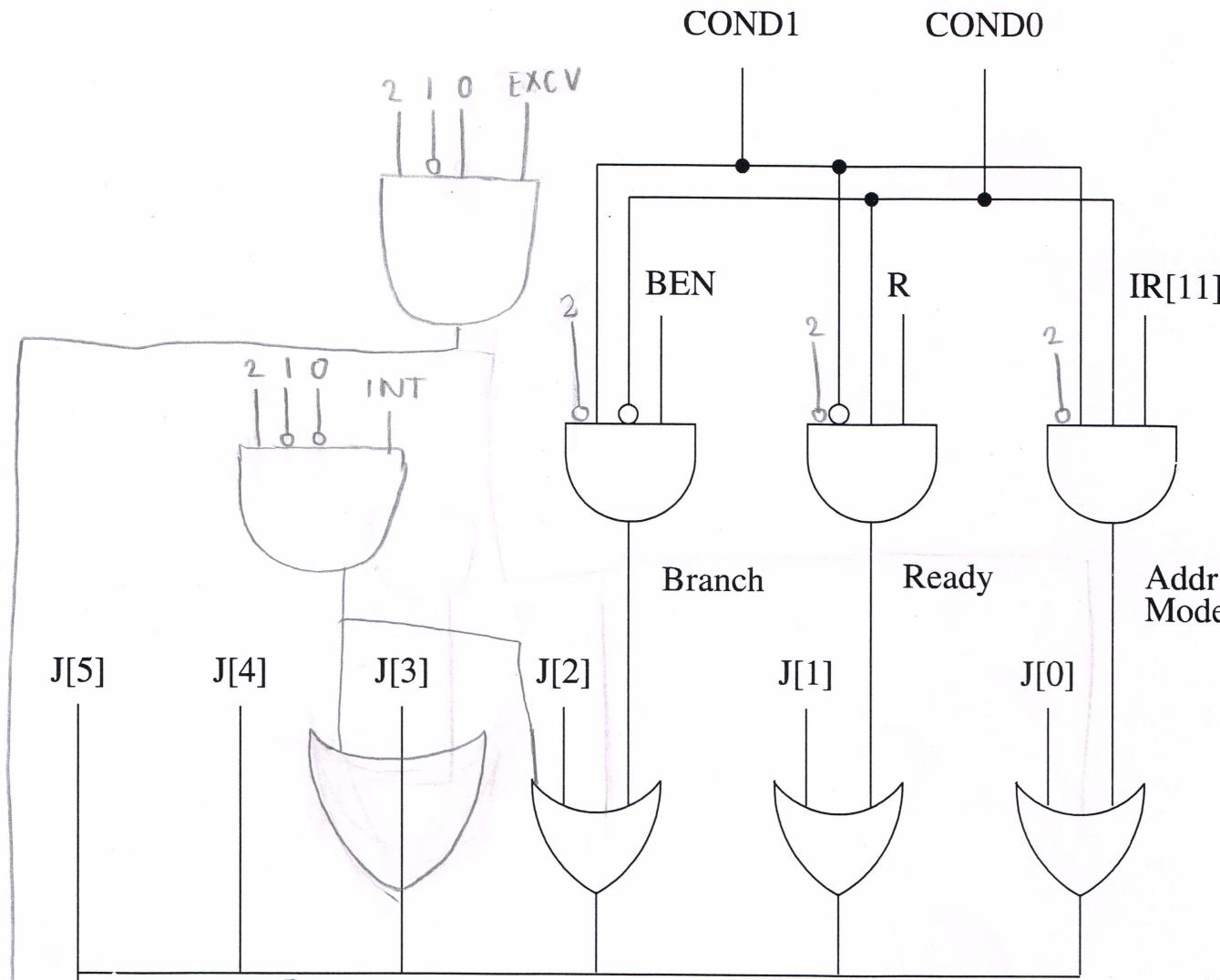


EXCMUX

0 - checkunaligned

1 - PGFAULT/protected





COND

- 0 → Normal
- 1 → JSR/R
- 2 → R/R
- 3 → BR
- 4 → INT
- 5 → EXC (add 5)

