

DATAPATH, already existing from Lab9 MUXES

REGMUX

0 - BUS

1 - USP

PSRMUX

0 - 0

1 - 1

VEC MUX

0 - x4

1 - INTV

2 - EXCV

DR MUX]
SR MUX] 2 - RG

NEW SIGNALS / REGS

→ PTBR

GATEPTBR - 1 bit

→ VA

GATEVA - 1 bit

LD.VA - 1 bit

- RET

LD.RET - 1 bit

- RET MUX - 4 bits

- SAVE MDR

LD.SAVEMDR - 1 bit

- VAMUX 1 bit

- VARETURNMUX - 1 bit

- MDRMUX [1:0] - 2 bit

NEW MUXES

RET MUX

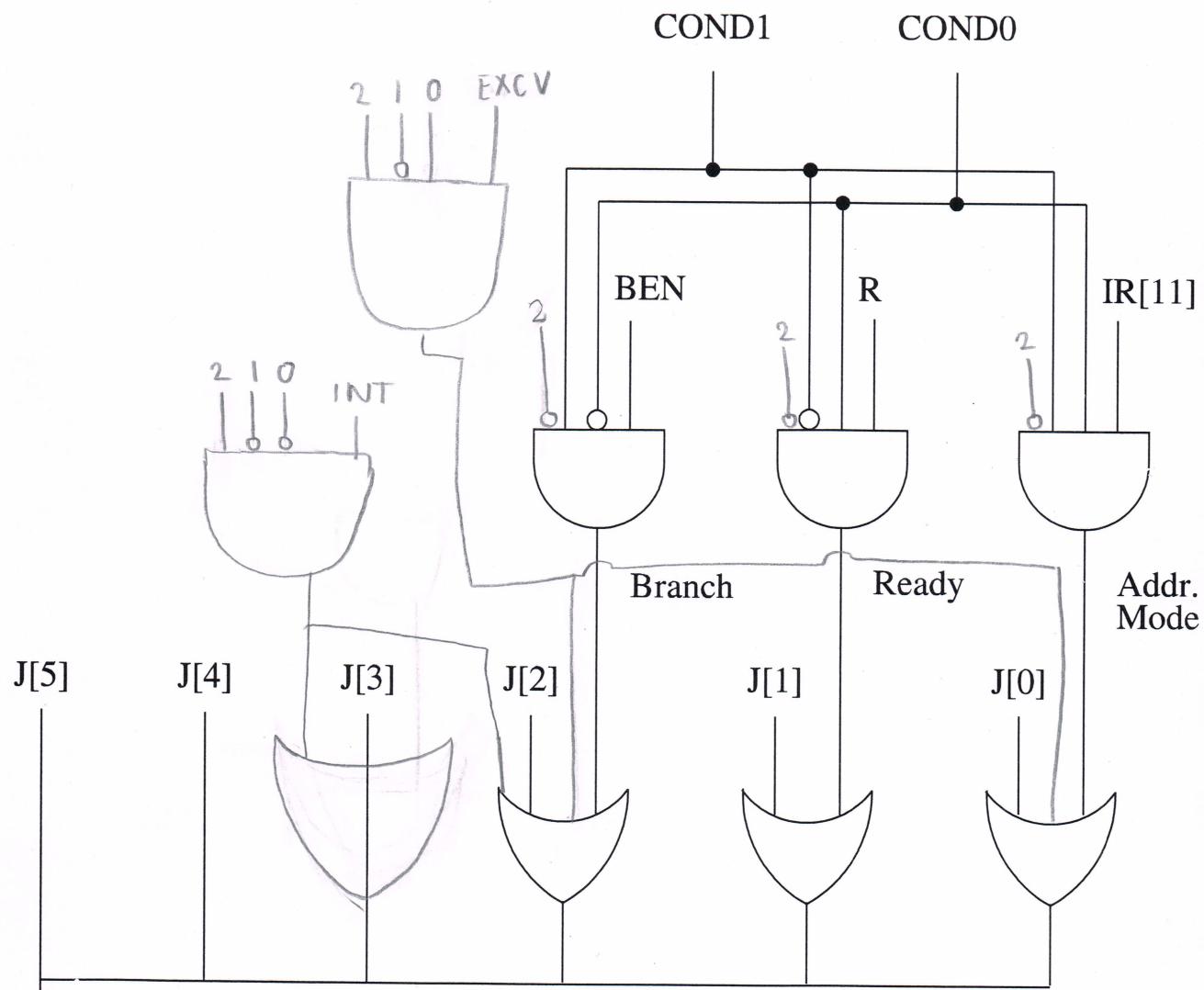
0 - 40 } RTI
1 - 41 }
2 - 36 } INT
3 - 37 }
4 - 60 }
5 - 33 } Fetch
6 - 28 TRAP
7 - 25
8 - 23
9 - 24
10 - 29

VAMUX

0 - BUS
1 - MDRE[13:9]
VA[9:0]

MDRMUX

0 - MDR[1:0]
1 - 01
2 - 11



0,0,IR[15:12]

6

IRD

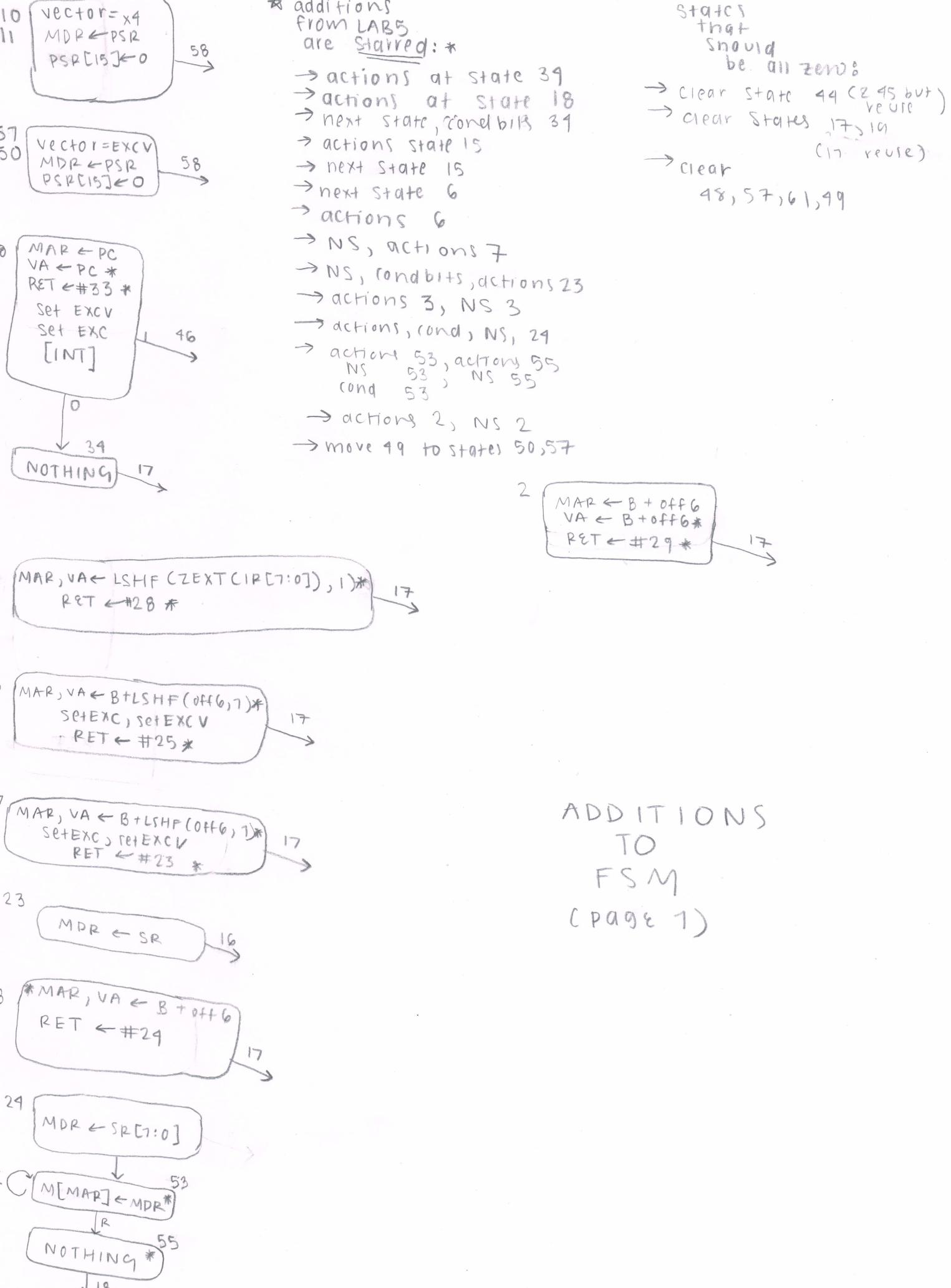
6

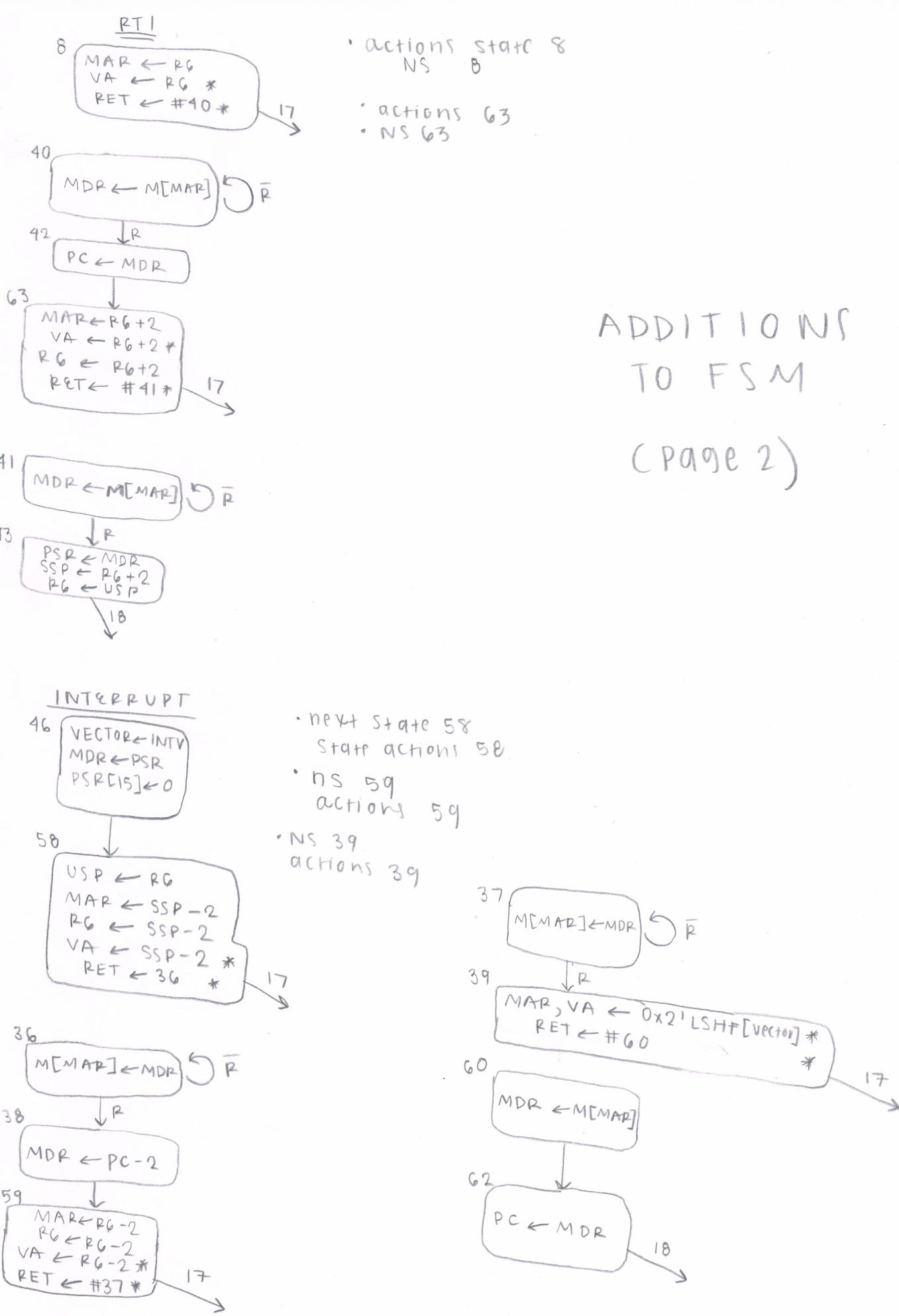
Address of Next State

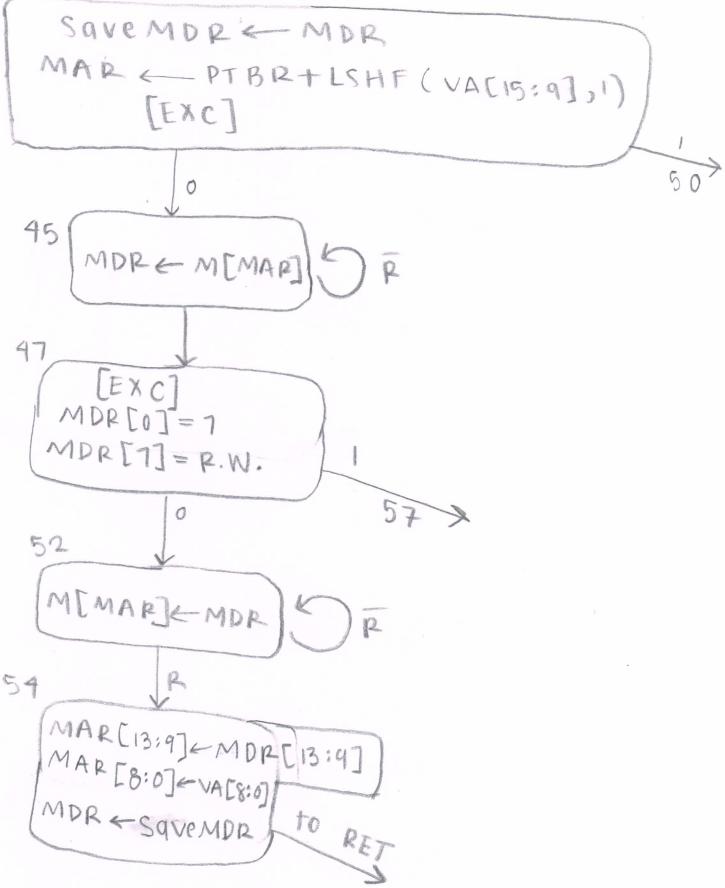
RET

VARETURN

COND 0 → Normal
 1 → JSR/R
 2 → R/R
 3 → BR
 4 → INT
 5 → EXC



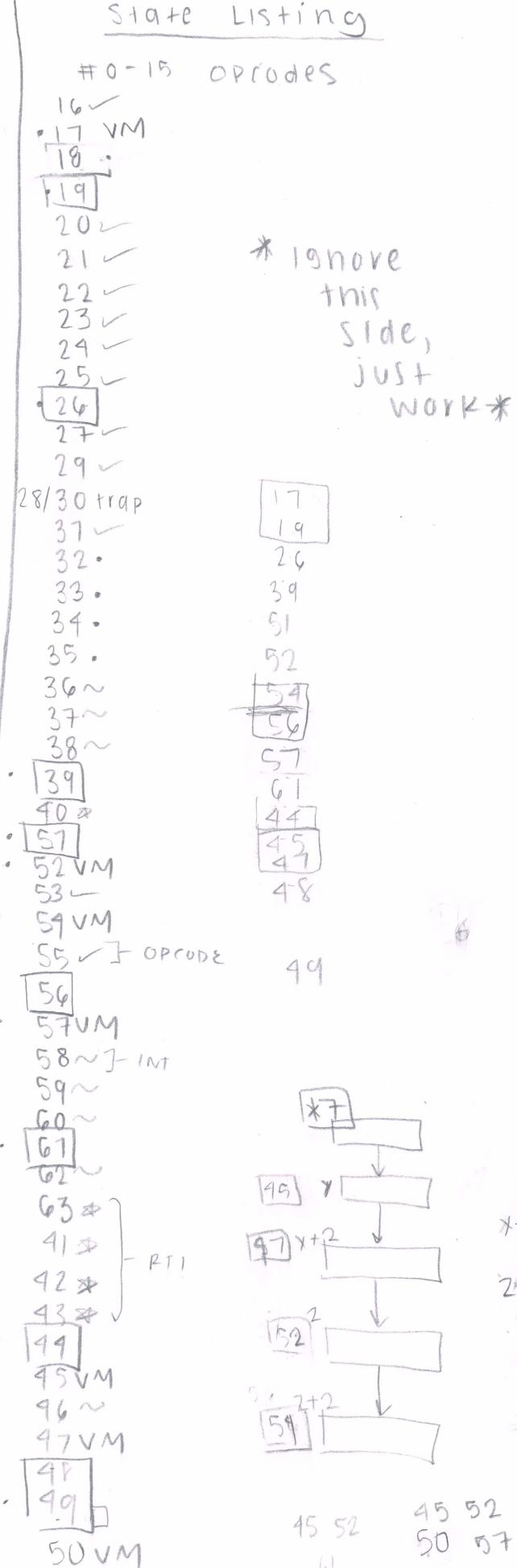




• $J[2] \& J[3]$
are used
for interrupts

• $J[2] \& J[0]$
are used
for exceptions

ADDITIONS
TO FSM
(Pg 3)



45 52
50 57
61