Lathif Sharieff

AI ASIC enthusiast seeking dynamic opportunities to excel and innovate

Germany +49-15758185645 sharieff.lathif@gmail.com linkedin.com/lathifs lathifs.tech

Summary

Motivated and accomplished graduate student specializing in Hardware-Software co-design of AI ASIC architecture, equipped with practical experience gained from diverse internships and projects. With a strong foundation in AI hardware and in-depth knowledge of Domain-Specific Accelerator principles.

Experience

Gemesys **June 2023 – Present**

AI Engineer - Working Student *Germany*

- Developing and deploying customized AI solutions on a proprietary in-house AI ASIC and pioneering the exploration of cutting-edge Tensorflow-based AI models and algorithms exclusively crafted for low-power and edge devices.
- Spearheading cross-functional collaboration with software and hardware engineers to implement and optimize AI models on an in-house AI ASIC for training.

University of Tübingen **May 2023 – Present**

Master Thesis - DSP Engine for ML Accelerator *Stuttgart, Germany*

- Architecting and implementing a high-performance DSP engine with MFCC extraction for a custom ML accelerator, specifically designed for efficient audio processing in ML applications and developing a robust streaming interface utilizing the ARM-AMBA protocol, facilitating seamless integration of the accelerator templates into the **UltraTrail**.

Bosch Centre for Artificial Intelligence **Oct 2022 – Mar 2023**

Deep Learning Hardware Engineer Intern *Stuttgart, Germany*

- Assisted in developing and implementing the RTL design for an in-house AI IP (Neural Computing Engine), driving significant performance enhancement of AI IP.
- Mapped neural networks on silicon (FPGA) and implemented state-of-the-art on-chip interconnection bus interfaces.
- Expertly executed RTL simulation of the previously developed AI IP, *CESARIA*, utilizing advanced EDA and tool-chain software within Linux and Git-based environments.
- Contributed to the micro-architecture design of AI IP while conducting extensive research and analysis

Projects

Audio Processing using FPGA | *Verilog, Lattice ice40, iCEcube, I2S, I2C, SPI*

- Developed and executed an innovative Master's project in collaboration with Telocate GmbH, designing an Audio processing system using a Lattice FPGA, Audio Codec, and MEMS microphone.

HoloCube puzzle using esp32 | *C, Arduino IDE, NFC, MQTT, Altium, FreeCAD*

- Led a multinational team in the development of a puzzle for Ubiquitous Lab. Conceptualized a challenging ESP32-based puzzle. It was implemented using an IMU and NFC card with a human-machine interface (HMI).

Design and analysis of 10 port router for NoC | *Verilog, NoC, Xilinx Spartan-6, ISE design*

- Spearheaded a team to design and implement a router for NoC on a FPGA. The project was awarded by IISc, India.

Technical Skills

Languages: SystemVerilog, Verilog, Python (TensorFlow & PyTorch), C, TCL
Developer Tools and IDEs: Cadence Xcelium, Xilinx Vivado & Vitis, ModelSim, Lattice iCEcube, Azure, Git
Technologies: RTL design (ASIC & FPGA flow), AI Accelerators, Neuromorphic computing

Education

University of Freiburg **Apr 2021 – Present**

Master of Science in Embedded Systems Engineering *Freiburg, Germany*

Visvesvaraya Technological University **Aug 2016 – July 2020**

Bachelor of Engineering in Electronics and Telecommunication *Bangalore, India*

Achievements

- **Certifications**: 1. Accelerators for Deep Learning - IIT Roorke 2. Xcelium & Verilog - Cadence 3. Innovation Management - IBMI, Berlin 4. AI Product Management
- **Awards**: *STIBET-I* by DAAD, *VELA Stipendiat* by Eccelisia group and *Maria-Ladenburger-Stipendium*.
- **Volunteering**: Provided counseling and support to incoming master's students as an *intercultural mentor*.