Design the single-stage CMOS amplifier shown in Fig. 1 with the following specifications:

- Open-loop DC gain ≥ 25 V/V
- Output voltage swing ≥ 0.5 V_{pp}
- CMRR ≥ 35 dB
- Settling time with 0.5% settling error in unity-gain sample & hold configuration ≤ 2 ns
- Load capacitance: C_L = 1 pF
- Sample & hold capacitance: C_H = 1 pF
- Input common-mode voltage: V_{cmi} = 0.3 V
- Output common-mode voltage: V_{cmo} = 0.5 V
- Ideal DC voltage: V_{dc} = 0.2 V
- Power supply voltage: V_{DD} = 1.0 V
- Power dissipation: as low as possible
- Technology: 90 nm CMOS

Figure 2 shows a switched-capacitor sample & hold circuit which is used to evaluate the transient performance of the amplifier. You are to design the amplifier to settle within 2 ns with a 0.5% settling accuracy for both positive and negative input steps with a height of 0.25 V while driving a 1 pF load capacitance. You can use ideal switches in switched-capacitor S/H circuit to realize the switches controlled by different clock phases, but as a ***bonus*** you may also use actual MOS devices for the switches.

Document your results in a regular report including all of the simulation results. You are to report both analytical design and simulation results in a Table and compare them together with sufficient explanations.

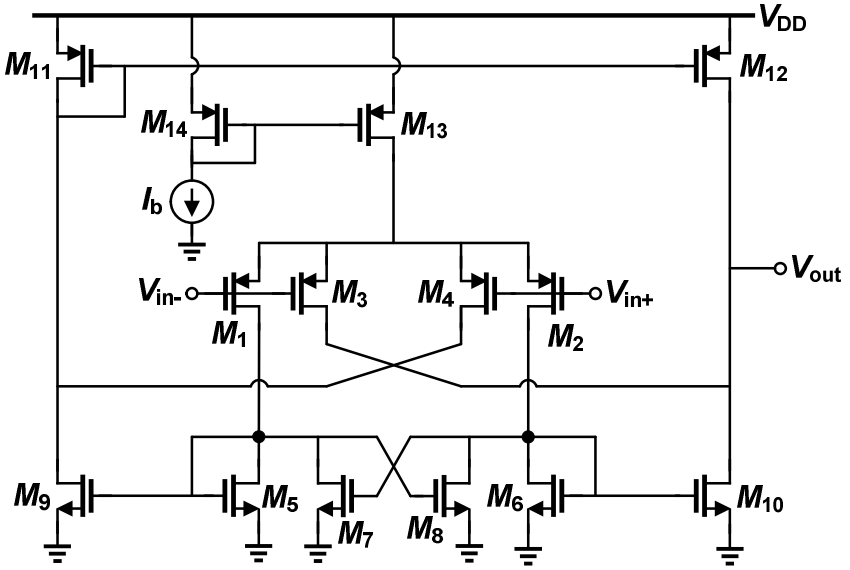

Fig. 1: A single-stage amplifier.

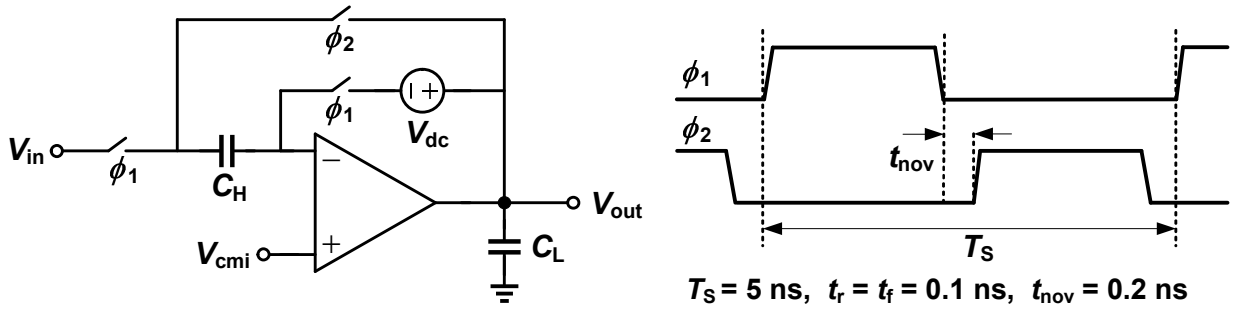

Fig. 2: Transient simulation circuit.