SEYED MOHAMMAD KASHANI 9423422

To design the circuit I start with considering the negative slew rate rather than positive slew rate because SR^- is more important. I consider SR^- takes 8.8% of 2ns.

$$SR^- = \frac{Vpulse - \sqrt{2}Veff}{0.088 \times 2ns}$$

Then from output swing I consider Veff = 0.12V and I define:

$$(\frac{w}{l})_{1,2} = k1(\frac{w}{l})_{3,4} \qquad (\frac{w}{l})_{5,7} = k2(\frac{w}{l})_{6,8}$$

$$(\frac{w}{l})_{9,10} = k3(\frac{w}{l})_{5,7} \qquad (\frac{w}{l})_{13} = 69(\frac{w}{l})_{14}$$

For simplicity and symmetry I consider k1 = 1.

To have high gain due to the gain formula k2 = 1.1 is chosen.

For power consumption and higher unity gain frequency k3 = 5.

Then summation of M1, M2, M3, and M4 I_D currents is 0.15mA which

leads I_b = 2.5µA.

Now knowing every branch currents considering L = 0.1µm to have the maximum speed I got:

M1	W=3.47u	L=0.1u	M=1
M2	W=3.47u	L=0.1u	M=1
M3	W=3.47u	L=0.1u	M=1
M4	W=3.47u	L=0.1u	M=1
M5	W=0.45u	L=0.1u	M=1
M6	W=0.45u	L=0.1u	M=1
M7	W=0.41u	L=0.1u	M=1

M8	W=0.41u	L=0.1u	M=1
M9	W=2.27u	L=0.1u	M=1
M10	W=2.27u	L=0.2u	M=2
M11	W=5.62u	L=0.1u	M=1
M12	W=5.62u	L=0.17u	M=1.7
M13	W=0.26u	L=0.13u	M=69
M14	W=0.26u	L=0.13u	M=1
I_b	dc=2.5u		

Simulating those above will give below results:

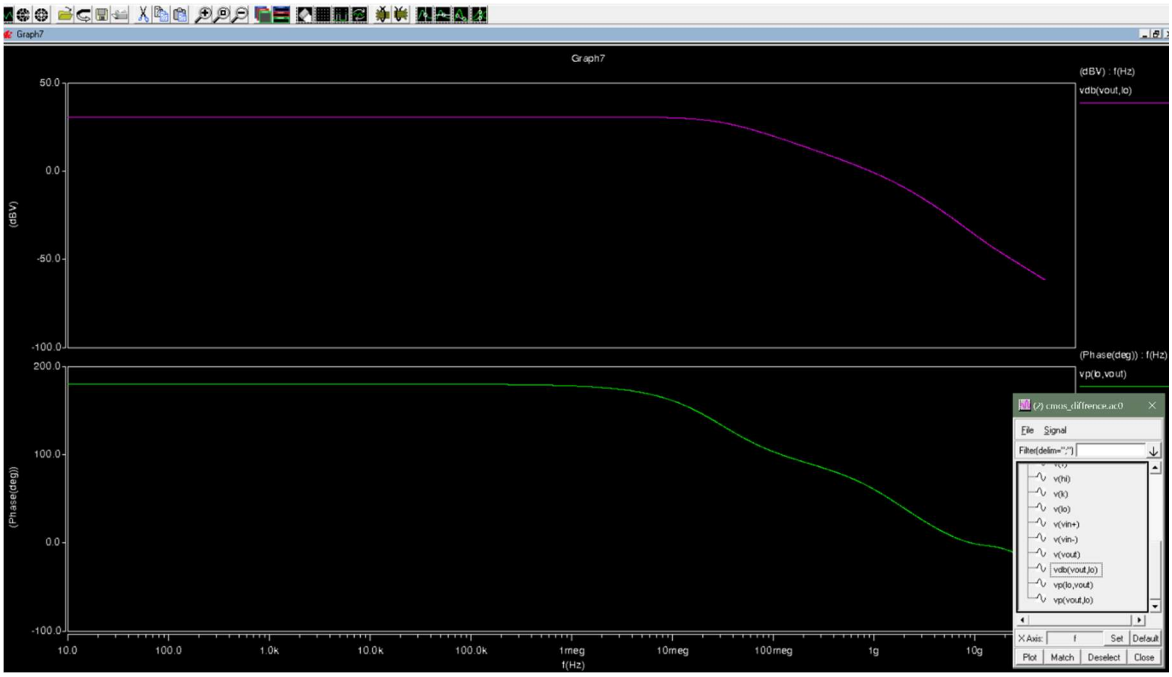
Gain = **30.7126 dB**

Unity gain frequency = **927.6271MHz**

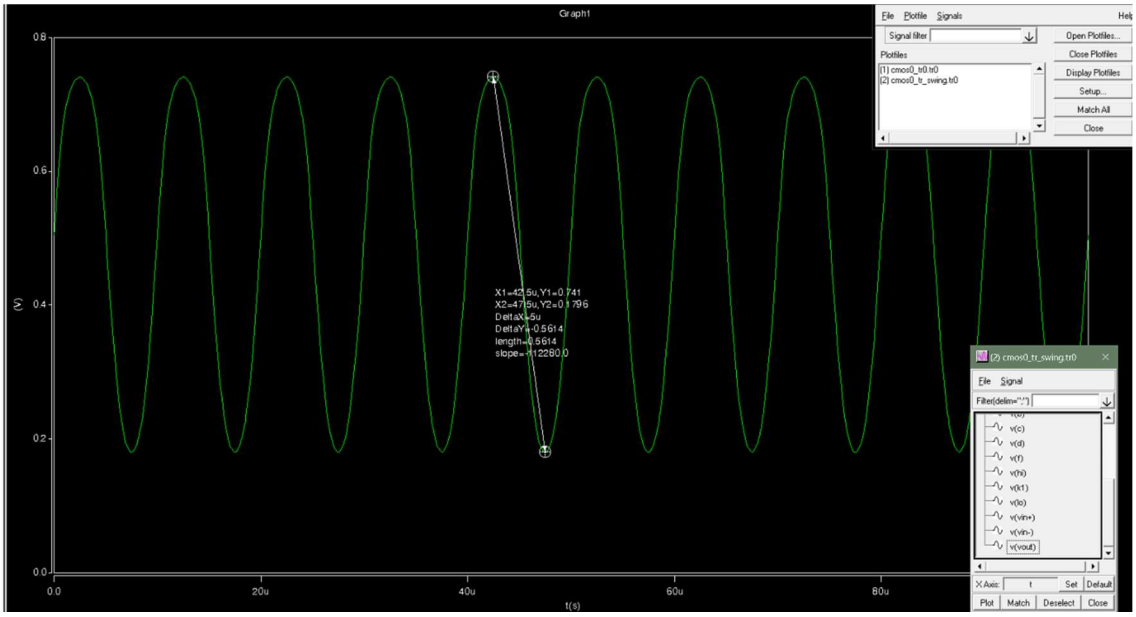
Phase margin = **62.9714 degree**

Which it satisfies the gain needed in question.

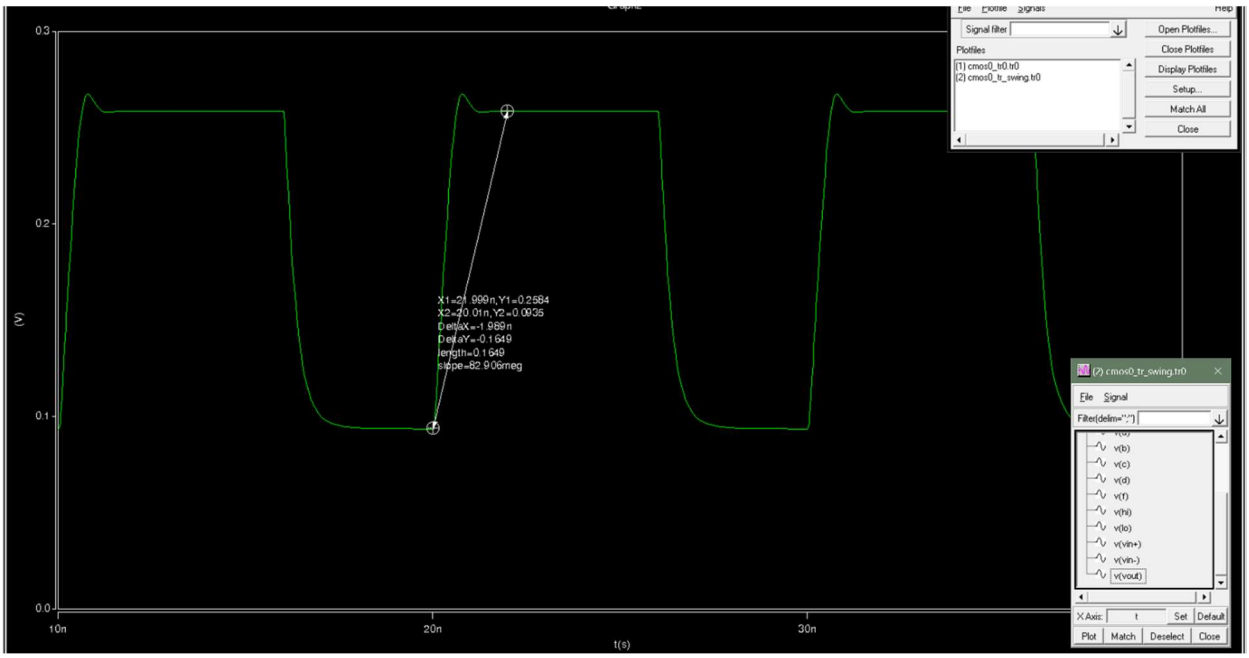
The Bode plot is shown below.



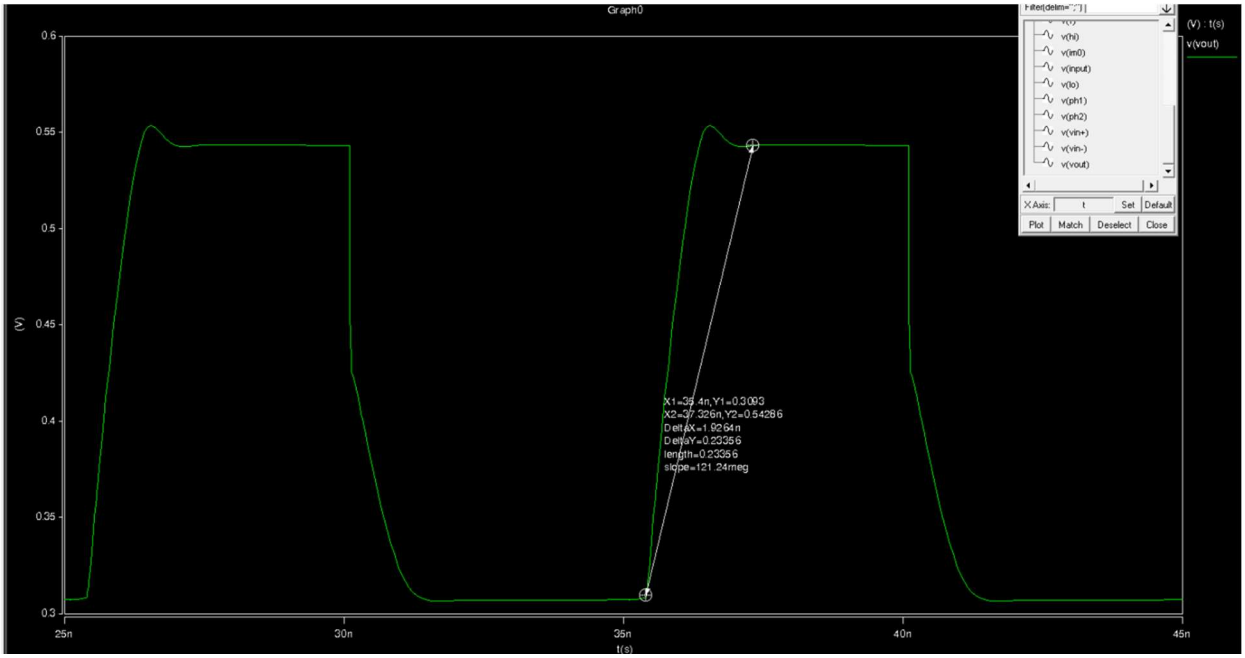
For swing the below diagram shows it can handle up to 0.56 V_{p-p} and this is satisfied too.



The diagram below shows the settelling time as it is below it settels 1.98ns which is acceptable.



The Figure below is the simulated output for switch capasitor circuites that is all OK.



parameters	Theory	simulation
ω_{ta}	2.87 GHz	927.62 MHz
t_s	2ns	1.92 ns
gain	27.95 dB	30.71 dB
V_{out}	0.5 V	0.505 V
Phase margin	-	62.97°
CMRR	>35	56.68
Power consumption	-	394.75 µW