

ENEL 353 Lab 3

Group 13:

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RTL Picture is in PDF file called RTL.PDF

Quartus Prime Lite Edition - C:/Users/steve/OneDrive/Documents/Year_3_ENEL/ENEL453/Lab_3/Lab3 - Voltmeter

File Edit View Project Assignments Processing Tools Window Help

Voltmeter

Project Navigator Hierarchy

EntityInstance

MAX 10: 10M50DAF484C7G

Voltmeter

IP upgrade recommended. Launch IP Upgrade Tool.

Tasks

Task

Assembler (Generate programming files)

Timing Analysis

Edit Settings

View Report

Timing Analyzer

EDA Netlist Writer

Edit Settings

Program Device (Open Programmer)

Compilation Report - Voltmeter

Table of Contents

Slow 1200mV 85C Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	65.14 MHz	65.14 MHz	clk	
2	147.47 MHz	147.47 MHz	ADC_Conversion_ins[u0]altpll_sys[sd1]pll7[clk[0]	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges

Testbench is on next page.

