Multilevel Active Rectifier with Independent Phase Control

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***Abstract*— This paper introduces the control algorithm designed for the three-phase voltage-source active rectifier multilevel converter. The presented control strategy allows direct current control separately for each phase, that's important during non-symmetrical converter load. The control provides voltage balancing on individual power cells directly at the control structure level. The behavior of designed control is analyzed by simulations tests. The experiment is made on low-voltage laboratory prototype of single-phase part of converter.**

Keywords—Multilevel converter; Active rectifier; three-phase; Converter control

I. INTRODUCTION

The main objective of this paper has been the analysis and design of control algorithm for three-phase multilevel voltage-source active rectifier, connected directly to AC-grid without transformer. The multilevel converter topology is based on cascaded H-bridge (CHB) cells, in this case seven levels CHB is used as a shown in Fig. 1 (three H-bridge cells per phase). This type of converter topology is well known for industrial application as a shown at [1]-[7]. This converter topology This topology is usually used for high power applications (order MW) with medium-voltage source, but this paper presents simulation and experimental results for low-voltage laboratory prototype and converters are based on standard semiconductor parts. These test are use to evaluate the behavior of designed control.

One promising application for three-phase grid connected active rectifier is described in [8], where the converter is used as the input part of ultra-fast charging station for electric vehicles. In this case is possible uneven loading of converter phase. For this reason, it is important to ensure separate control of individual phase. The proposed control of voltage-source active rectifier has these important proprieties: (i) the distribution of dc-link voltage on each H-bridge cell is identical to required value (U_{c_mXw} = 150 V) and (ii) harmonic ac currents with very low THDi. These requirements are great challenge for design of converter control, because it is necessary that the converter must be operated well even for non-symmetrical load. In this case we want to ensure a very low current ripple therefore we using PS-PWM (phase shifted pulse-width modulation) with zero vector alternating, which is well described in [6] and [7]. That is reason why is necessary to solve the voltage balancing on individual cells directly to control level.

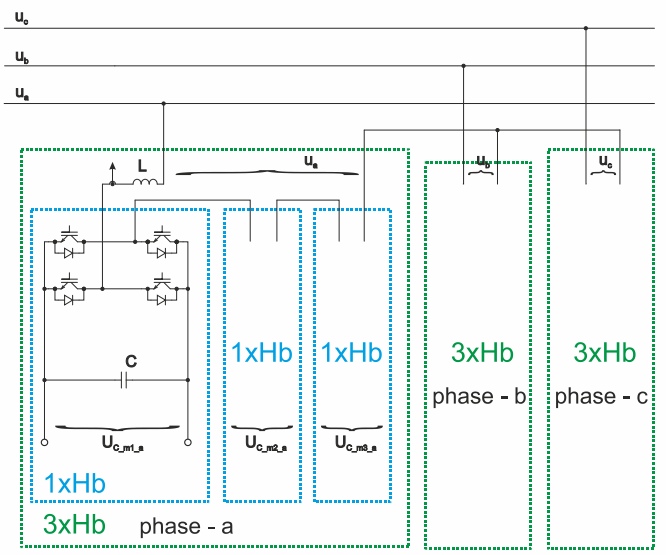

Fig. 1. Configuration of designed three-phase voltage source active rectifier composed of H- bridge cells

II. CONVERTER CONTROL

Designed control algorithm of voltage-source active rectifier uses three separate control loops (these control loops are the same and each is intended for single phase – a, b, c). Each one of these independent control loops is composed of three parts as a shown in Fig. 2: (i) feed-forward (mathematical model) branch is located in the upper section of figure, (ii) voltage and current control branch which is located in the middle section of figure and (iii) voltage balancing branch which is located in the downer section of figure. Very important part of control is synchronization with ac grid. The designed control is composed of standard parts as PI and PR controllers that greatly simplifies the complexity of control and increases resistance to external disturbances. Each phase

modulation is solved separately by PS-PWM (firing pulses phase_a, b, c) realized in FPGA.

The detail of control algorithm designed for each phase (it means single-phase control) of converter is shown in Fig. 3. These control loops (Fig. 3 intended for phase_a) are composed from synchronization block, with output signals Um (voltage magnitude), ω (voltage angular velocity), ϑ_a (position of voltage vector) these signals are important for mathematical model and also for direct current control lop. Mathematical model helps to faster transients (especially at the start sequence of the converter), this block use equation (1) for calculation signal u_{v_estim}. The values R (parasitic resistance) and L (induction) are constants representing input inductor, signal I_m magnitude of required value of ac current (output signal from voltage controller R_{Uc_a}). The PI controller (R_{Uc_a}) is used for control sum of dc-link voltage (ΣU_{c_a}) to required value U_{cw}, with output signal I_m (magnitude of requirement current) The value ΣU_{c_a} is sum of dc-links voltage of phase_a. The direct current control is provided by PR controller R_{ia} and resonant controller R_{3rd}. This resonant controller (R_{3rd}) is in this case use as third harmonic compensator, on the other hand it is possible to use filtration as described in [9] and [10]. The resulting signal $u_{v\_m1\_a}$ enters into PWM modulator and by firing pulses is switching first H-bridge of phase_a. The second and the third cells are switched according signals $u_{v\_m2\_a}$ and $u_{v\_m3\_a}$. The value of these modulation signals $u_{v\_m2\_a}$, $u_{v\_m3\_a}$ are modified to ensure balancing of DC-links of each cell in the phase_a by PI controllers $R_{\Delta Uc\_m2}$ and $R_{\Delta Uc\_m3}$. These controllers only modify the value of modulation signals size $u_{v\_m2\_a}$, $u_{v\_m3\_a}$ from the master signal $u_{v\_m1\_a}$. The signals modification depends on sign of requirement current magnitude (sign(I_m)).

$$u_{v\_estim} = (U_m - R.I_m).sin\left(\vartheta_a - atan\frac{\omega.L.I_m}{U_m - R.I_m}\right) \quad (1)$$

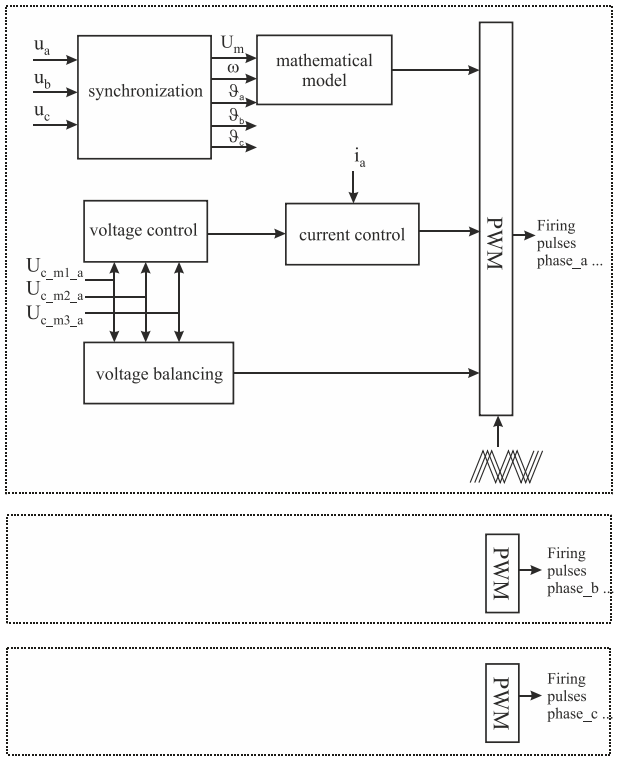

Fig. 2. Proposed control for three-phase voltage source active rectifier composed of H- bridge cells

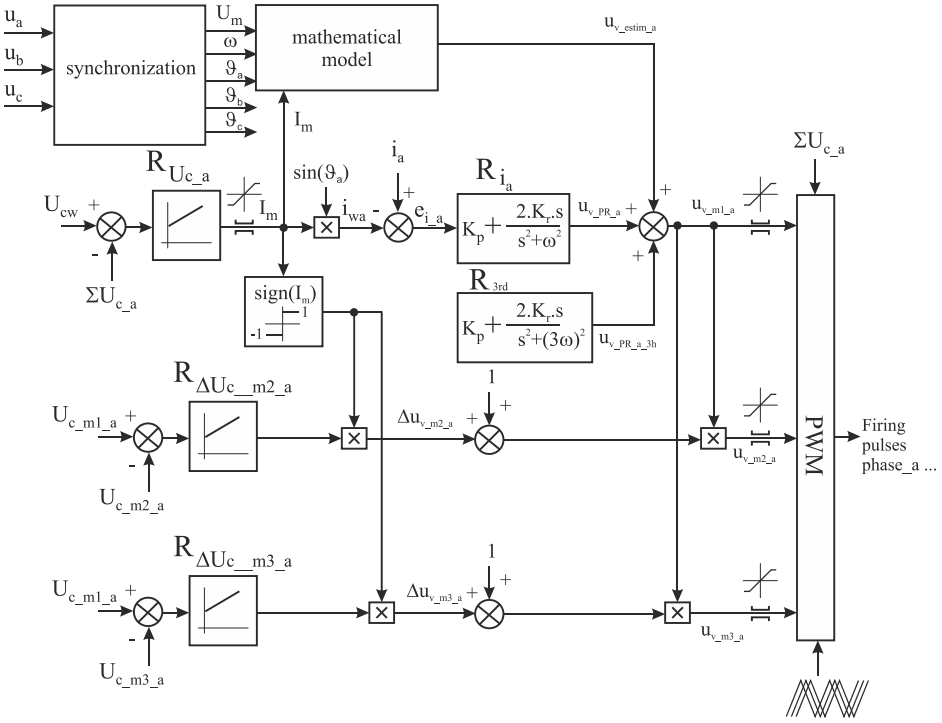

Fig. 3. Detail of single-phase part of control of voltage source active rectifier

III. Simulation Results

The converter behaviour and designed converter control was at first time tested on simulation model of active rectifier, Fig. 4. The simulation model consists of three-phase voltage source (u_a, u_b, u_c), input inductance L, three H-bridge cells for each phase are connected in series, their dc-link capacitors (C) and nine separate equivalent current sources ($i_{z\_a\_M1}$ - $i_{z\_c\_M3}$) representing the load of active converter. The switching frequency of IGBTs is fixed to 800 Hz. The PS-PWM with shifted carriers is used for the modulation of converter. The major benefit of employed shifted carriers is the significant decrease of the ac current ripple due to multilevel nature of the voltage at the converter ac terminals. In this particular case with three modules in series, the phase-voltage at the converter ac side is seven-level (described in more detail in chapter IV).

Fig. 5 illustrates modulation and saw signals of PS-PWM modulation. The Fig. 6 shows simulation result of active rectifier under steady-state condition for symmetrical load 9.45 kW. The waveforms i_a, i_b, i_c represents ac phase currents which are harmonic and in phase with ac-grid voltage u_a, u_b, u_c. The direct current control for each phase ensures the harmonic currents for non-symmetrical load as a shown in Fig. 7. In this case, it is important to ensure a balancing dc voltage on separate H-cells as a presented in Fig. 8. The Fig. 8 shows the response of CHB active rectifier to step change of non-symmetrical load ($i_{z\_a\_M1}$=7A, $i_{z\_a\_M2}$=7.3A, $i_{z\_a\_M3}$=7.6A, $i_{z\_b\_M1}$=5.6A, $i_{z\_b\_M2}$=5A, $i_{z\_b\_M3}$=5.3A, $i_{z\_c\_M1}$=5A, $i_{z\_c\_M2}$=6A, $i_{z\_c\_M3}$=7A). The simulation result shows satisfactory operation of the balancing PI controllers. In this case the non-symmetrical load is reflected in the different ac current value and by the current ripple difference as can be seen in Fig. 7.

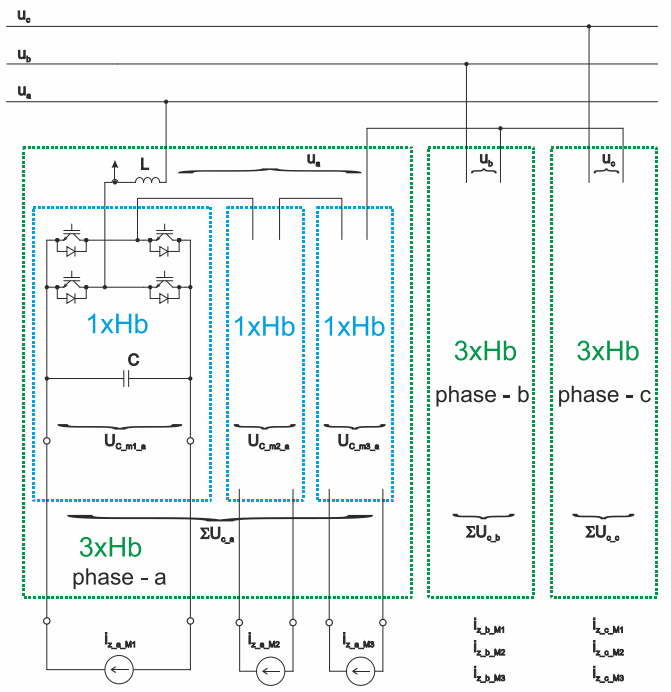

Fig. 4. Simulation model of three-phase voltage source active rectifier composed of H- bridge cells

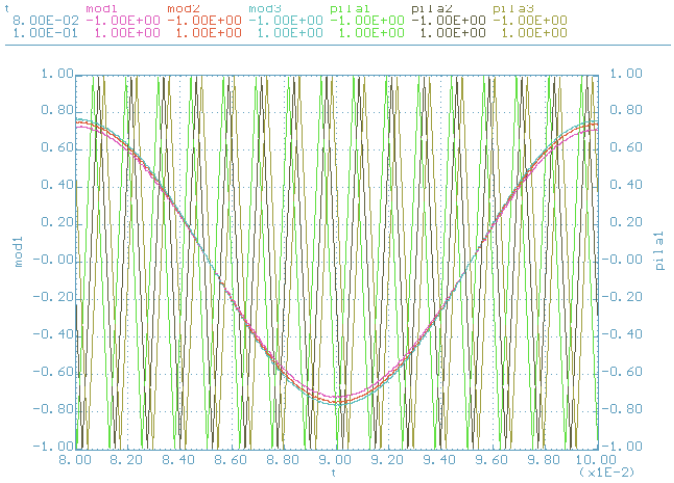

Fig. 5. Illustration of modulation and saw signals for PS-PWM phase_a of voltage source active rectifier
mod1: modulation signal for first cell,
mod2: modulation signal for second cell,
mod3: modulation signal for thirth cell,
pila1: saw signal for first cell,
pila2: saw signal for second cell,
pila3: saw signal for thirth cell

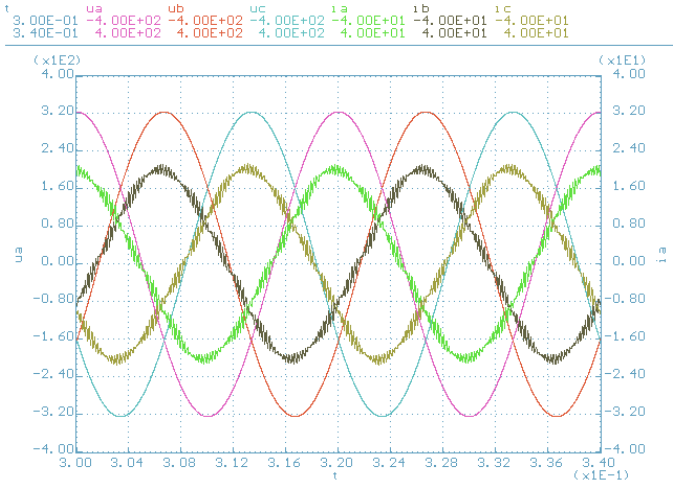

Fig. 6. Behaviour of phase-voltage and current of voltage-source active rectifier under steady-state conditions in rectifier mode (load P = 9.45 kW) for symmetrical load: $i_{z\_a\_M1}$=7 A, $i_{z\_a\_M2}$=7 A, $i_{z\_a\_M3}$=7 A, $i_{z\_b\_M1}$=7 A, $i_{z\_b\_M2}$=7 A, $i_{z\_b\_M3}$=7 A, $i_{z\_c\_M1}$=7 A, $i_{z\_c\_M2}$=7 A, $i_{z\_c\_M3}$=7 A
ua: AC source voltage phase_a [80V/div],
ub: AC source voltage phase_b [80V/div],
uc: AC source voltage phase_c [80V/div],
ia: AC converter-side current phase_a [8A/div],
ib: AC converter-side current phase_a [8A/div],
ic: AC converter-side current phase_a [8A/div]

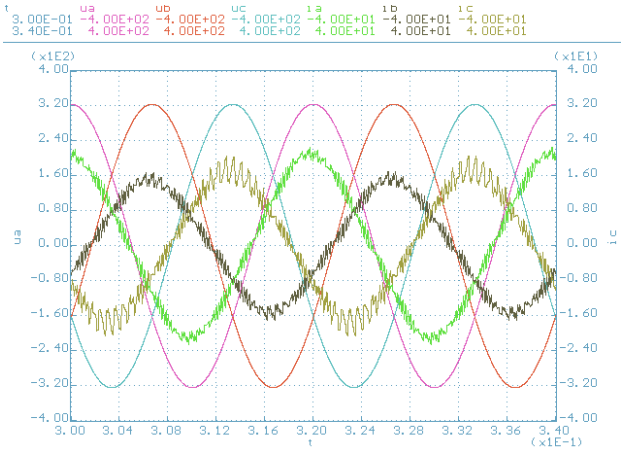

Fig. 7. Behaviour of phase-voltage and current of voltage-source active rectifier under steady-state conditions in rectifier mode for non-symmetrical load: $i_{z\_a\_M1}$=7 A, $i_{z\_a\_M2}$=7.3 A, $i_{z\_a\_M3}$=7.6 A, $i_{z\_b\_M1}$=5.6 A, $i_{z\_b\_M2}$=5 A, $i_{z\_b\_M3}$=5.3 A, $i_{z\_c\_M1}$=5 A, $i_{z\_c\_M2}$=6 A, $i_{z\_c\_M3}$=7 A
ua: AC source voltage phase_a [80V/div],
ub: AC source voltage phase_b [80V/div],
uc: AC source voltage phase_c [80V/div],
ia: AC converter-side current phase_a [8A/div],
ib: AC converter-side current phase_a [8A/div],
ic: AC converter-side current phase_a [8A/div]

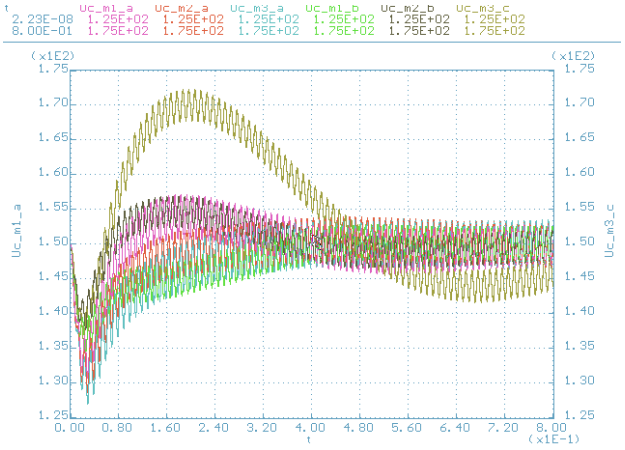

Fig. 8. Behaviour of DC-link voltage on selected modules of converter - Step change of converter load for non-symmetrical load.$i_{z\_a\_M1}$=7 A, $i_{z\_a\_M2}$=7.3 A, $i_{z\_a\_M3}$=7.6 A, $i_{z\_b\_M1}$=5.6 A, $i_{z\_b\_M2}$=5 A, $i_{z\_b\_M3}$=5.3 A, $i_{z\_c\_M1}$=5 A, $i_{z\_c\_M2}$=6 A, $i_{z\_c\_M3}$=7 A
$U_{c\_m1\_a}$: DC-link voltage of module1 phase_a [5V/div],
$U_{c\_m2\_a}$: DC-link voltage of module2 phase_a [5V/div],
$U_{c\_m3\_a}$: DC-link voltage of module3 phase_a [5V/div],
$U_{c\_m1\_b}$: DC-link voltage of module1 phase_b [5V/div],
$U_{c\_m2\_b}$: DC-link voltage of module2 phase_b [5V/div],
$U_{c\_m3\_c}$: DC-link voltage of module3 phase_c [5V/div

IV. Laboratory Prototype

Experimental tests of voltage-source active rectifier were performed for the low-voltage single-phase variant of CHB active rectifier and controlled inverters representing load. The final power circuit of laboratory prototype is shown in Fig. 9 and the converter power was reduced to 1.1 kW. The control of multilevel converter has been implemented in the floating-point digital signal microcontroller Texas Instruments TMS320F28335 and PS-PWM modulator was realized in FPGA Altera EP3C40. Both devices are located on development board specially designed to control multi-level converters, see [11]. Utilization of FPGA allows us to have perfectly synchronous PWM outputs, which are needed for proper function of PS-PWM. The FPGA design consist of basic system part as described in [11] and block of modulators itself. Each full H-bridge has its own modulator (Fig. 10). The input signals ($u_{v\_mX\_a}$, Period, Dead-time and Sawtooth phase shift) are type of int_16t and are available in memory space of microcontroller. The control signals (dashed lines) are accessible through single configuration register. It is very easy to expand design to support more H-bridges, thus creating more levels of output voltage. The complete experimental test values and parameters are given in TABLE I.

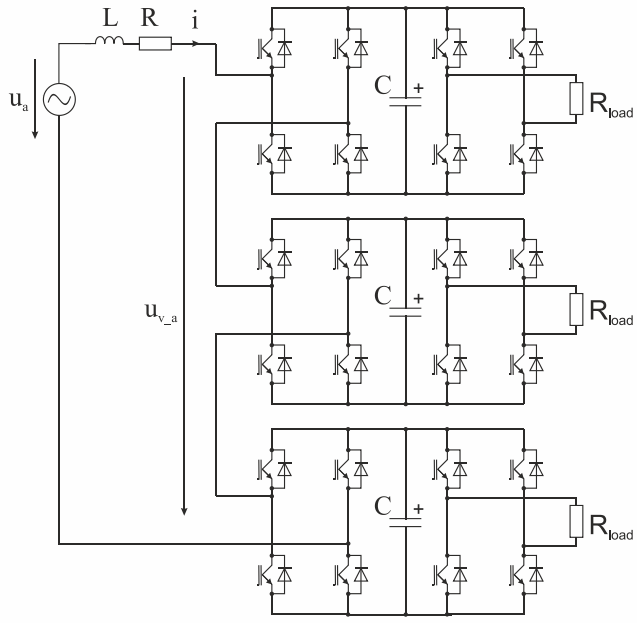

Fig. 9. Experimental low-voltage prototype of single-phase seven-level CHB active rectifier

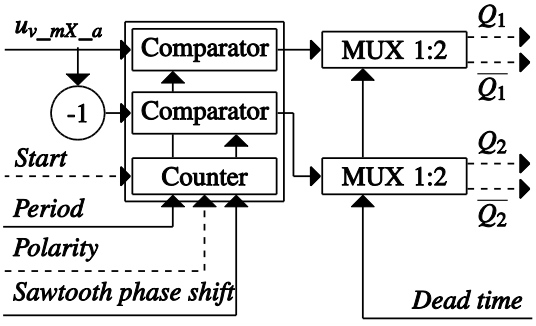

Fig. 10. Block schematics of modulator for one H-bridge cell

TABLE I. PARAMETERS OF LABORATORY PROTOTYPE

Converter power for experiments	P = 1.1 kW
AC-grid voltage	u_a = 230 V_{rms} / 50 Hz
Input inductor	L = 6 mH R = 0.2 Ω
Value of dc-link capacitors	C = 6 mF
Required dc-link voltage	U_{DCw} = 150 V
Switching frequency of IGBTs	F_{swit} = 800 Hz

The Fig. 11-Fig. 14 presents single-phase seven-level CHB active rectifier experimental results. The Fig. 11 illustrates the converter start-up under non-load conditions. It is a standard transient, where the control behaviour is reviewed. Very fast rise of the current i (violet signal) is caused by requirement to maximal current, at the first moment operates mainly model part of control. The voltage at dc-links U_{c_m1}, U_{c_m2}, U_{c_m3} (dark blue, light blue, green signals) rise from value 108 V (charged via diode rectifier) to required value 150 V during three periods. Fig. 12 shows converter behavior in rectifier mode under steady-state condition with load 1.1 kW. The green signal represents ac-grid voltage U_a that is in phase with ac current i (violet signal). The dark blue signal represents voltage on ac converter terminals (u_{v_a}), seven levels voltage in this case (it is due the correct functions of PS-PWM for three H-bridge cells). The frequency of current ripple is 4800 Hz that is result of PS-PWM and zero vectors alternating modulation technique. The Fig. 13 shows converter response to step change of load (with 10% asymmetry for second cell). The light blue signal U_{c_m2} representing the voltage on dc-link of second cell, this voltage raises faster because the load of this cell is less than other cells. The PI balancing controller has slow setting, that is reason for slow voltage stabilizing to required value 150 V as shown in Fig. 14. This type of voltage balancing is slow, but is performed directly on control level. Fig. 14 shows converter behavior in rectifier mode under steady-state condition with load 1 kW, during non-symmetrical load. In case of CHB converter is very interesting chapter the current distortion and resulting THDi, for example [12]-[14].

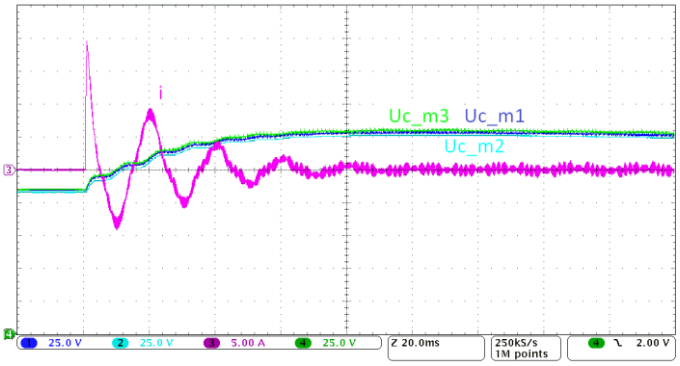

Fig. 11. Start-up sequence of laboratory prootype (converter load P = 0 kW)
U_{c_m1} – DC-link voltage on first cell [25V/div],
U_{c_m2} – DC-link voltage on second cell [25V/div],
i – AC current (5A/div),
U_{c_m3} – DC-link voltage [25V/div]

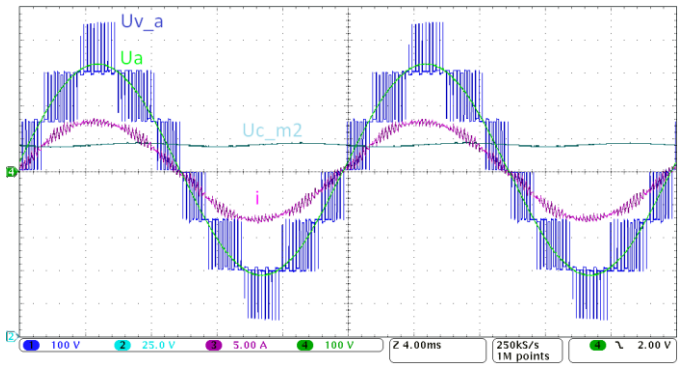

Fig. 12. Laboratory prototype under steady-state (symmetrical converter load P = 1.1 kW)
u_{v_a} – Voltage at converter ac-terminals [100V/div],
U_{c_m2} – DC-link voltage on second cell [25V/div],
i – AC current (5A/div),
u_a – Voltage of ac source [100V/div]

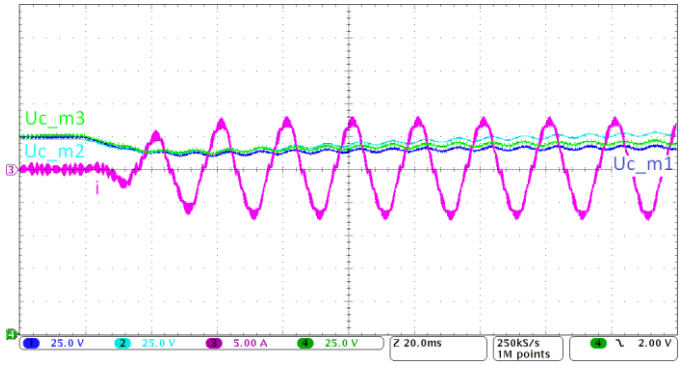

Fig. 13. Laboratory prototype under step change of non-symmetrical load (converter load 0 kW→1kW, second cell load 90%)
U_{c_m1} – DC-link voltage on first cell [25V/div],
U_{c_m2} – DC-link voltage on second cell [25V/div],
i – AC current (5A/div),
U_{c_m3} – DC-link voltage [25V/div]

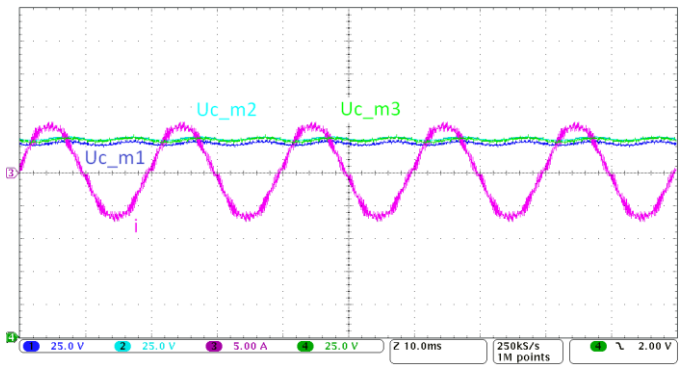

Fig. 14. Steady after transient with non-symmetrical load from Fig. 13 (converter with non-symmetrical load P=1kW, second cell load 90%)
U_{c_m1} – DC-link voltage on first cell [25V/div],
U_{c_m2} – DC-link voltage on second cell [25V/div],
i – AC current (5A/div),
U_{c_m3} – DC-link voltage [25V/div]

V. CONCLUSION

This paper presents multilevel topology of voltage-source active rectifier converter powered directly from ac-grid. From the control point of view, the main attention is paid in this contribution to the control and specifically active power cell dc-link voltage balancing strategy of input active rectifier. Designed control of multilevel voltage-source active rectifier provides sinusoidal current waveform shape (even for non-symmetrical converter load). The control provides voltage balancing on individual power cells directly at the control structure level. This is the simple and powerful approach which can be easily implemented using conventional PR and PI controllers which are industry-standard components.

ACKNOWLEDGMENT

This research has been supported by the European Regional Development Fund and Ministry of Education, Youth and Sports of the Czech Republic under project No. CZ.1.05/2.1.00/03.0094: Regional Innovation Centre for Electrical Engineering (RICE) and project No. SGS-2015-038.

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