Voltage Balancing Control of a Novel Modular Multilevel Converter

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Abstract—**The Modular Multilevel Converter (MMC) is an emerging and highly attractive multilevel converter topology for medium and high voltage applications. In this paper, the equivalent circuit and power transmission model of MMC is proposed, based on which, the idea that control the current of positive leg and negative leg independently is brought up and a new multi-hierarchy method to balance the capacitor voltages is deduced. First, the average voltage of all submodules in a phase leg is got as a feedback to regulate the dc component of current command, which controls the average voltage of capacitors in a phase leg. Second, by adding active current to the positive leg current command and reverse phase active current to the negative leg can balance the average voltage of the capacitors in positive leg between negative leg. Third, a compensate signal which is added into the PWM control signal of each submodule makes each capacitor voltage in a leg balanced. The feasibility of independent leg current control, as well as the effectiveness of voltage-balancing control is verified by simulation.**

Keywords-Modular multilevel converter, voltage-balancing control, current control, phase-shifted carrier PWM, HVDC

I. INTRODUCTION

In recent years the interest in a novel modular multilevel converter (MMC) has increased because of its modular construction without transformers, especially its suitability for medium and high voltage applications[1-5]. Due to the special structure, power transmission via MMC leads to the oscillation of capacitor voltage. Only balancing the capacitor voltages effectively, MMC can work normally and control strategy can be realized. Thus, it becomes especially important to control capacitor voltages. In order to avoid voltage unbalance, some paper published has discussed in different ways[6-9]. Reference [7] describes the mathematical model of the MMC based on differential equations, but the capacitors' voltage balancing is not deeply studied. Reference [9] proposed a balancing control method with phase-disposition carrier PWM(PD-PWM), but it is not suitable for phase-shifted carrier PWM(PS-PWM), and the leg current is not well controlled. When using PS-PWM in MMC, reference [8] presented a voltage-balancing control method using an independent controller for each submodule, but without an theoretical foundation to rely on [8].

This paper focuses on controlling the positive leg and negative leg current independently to achieve voltage balancing of a novel MMC topology. Based on the power equations derived from the equivalent circuit, control strategy are proposed. Simulation results are also presented in this paper.

II. STRUCTURE AND EQUIVALENT CIRCUIT OF THE NOVEL MODULAR MULTILEVEL CONVERTER

A. Structure of MMC

The topology of MMC discussed in this paper is shown in Fig. 1(a). A converter consists of six converter legs, and a phase leg consists of a series connection of submodules(SM) with buffer reactors. There are two legs in one phase leg which we call positive leg and negative leg. As shown in Fig. 1(b), an IGBT half bridge and a dc storage capacitor constitute a submodule.

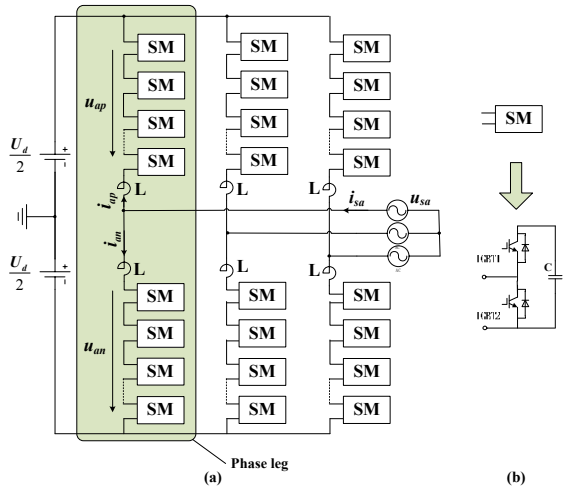

Figure 1. Circuit structure of the novel modular multilevel converter: (a) Power circuit; (b) Structure of the submodule

B. Equivalent circuit of phase-a

Fig. 2 shows the equivalent circuit of phase-a in MMC shown in Fig.1(a). The sum of capacitor voltages in positive leg and negative leg are equivalent to the controlled voltage source U_{ap} and U_{an} .The voltage of U_{ap} is defined as u_{ap} and

Project Supported by Shandong Provincial Natural Science Foundation, China (2009ZRB01402)

the voltage of U_{an} is u_{an}. i_{ap}, i_{an} are positive leg and negative leg currents.

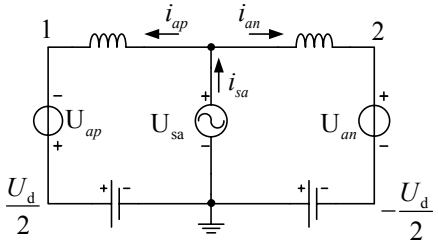

Figure 2. Equivalent circuit of phase-a in MMC

III. CURRENT CONTROL AND VOLTAGE BALANCING METHOD

The power difference between input and output of a submodule, as well as the difference of active power consumption in different submodules, causes the capacitor voltages imbalance. Through effective leg current control, power control can be realized, and so is the balance.

A. Current Analysis

The following circuit equation is obtained from Fig. 2:

$$i_{sa} = i_{ap} + i_{an}, \tag{1}$$

$$\begin{cases} L\dfrac{di_{ap}}{dt} = u_{sa} - \dfrac{U_d}{2} + u_{ap} \\ L\dfrac{di_{an}}{dt} = u_{sa} + \dfrac{U_d}{2} - u_{an} \end{cases}. \tag{2}$$

Where, i_{sa} is the ac source current, L is the buffer inductor, U_d is the dc supply voltage, u_{sa} is the ac source voltage. Considering the equivalent circuit of phase-a shown in Fig. 2, it is not difficult to make the conclusion that i_{ap} and i_{an} can be controlled by adjusting U_{ap} and U_{an}.

i_{ap} and i_{an} can be decomposed as following:

$$\begin{cases} i_{ap} = i_{apAC} + i_0 \\ i_{an} = i_{anAC} - i_0 \end{cases}. \tag{3}$$

Where, define i_{apAC}, i_{anAC} and i_0 as

$$\begin{cases} \int_0^T U_d i_{apAC} dt = 0 \\ \int_0^T U_d i_{apnAC} dt = 0 \\ \int_0^T u_{sa} i_0 dt = 0 \end{cases}. \tag{4}$$

Here, T is an ac period.

The following equation is derived from the law of conservation of energy:

$$P_{DC} = P_{AC} + P_{ap} + P_{an} \tag{5}$$

Where, P_{AC} is the absorbed power by ac source, P_{DC} is the power issued from dc supply, P_{ap} and P_{an} are the power absorbed by controlled voltage source U_{ap} and U_{an}. They are defined by following equations:

$$\begin{cases} P_{AC} = -\dfrac{1}{T}\int_0^T u_{sa} i_{sa} dt = -\dfrac{1}{T}\int_0^T u_{sa}(i_{apAC} + i_{anAC}) dt \\ P_{DC} = -\dfrac{1}{T}\int_0^T \dfrac{U_d}{2} i_{ap} dt + \dfrac{1}{T}\int_0^T \dfrac{U_d}{2} i_{an} dt = -\dfrac{1}{T}\int_0^T U_d i_0 dt \end{cases}, \tag{6}$$

$$\begin{cases} P_{ap} = -\dfrac{1}{T}\int_0^T u_{ap} i_{ap} dt = -\dfrac{1}{T}\int_0^T \dfrac{U_d}{2} i_0 dt + \dfrac{1}{T}\int_0^T u_{sa} i_{apAC} dt \\ P_{an} = \dfrac{1}{T}\int_0^T u_{an} i_{an} dt = -\dfrac{1}{T}\int_0^T \dfrac{U_d}{2} i_0 dt + \dfrac{1}{T}\int_0^T u_{sa} i_{anAC} dt \end{cases}. \tag{7}$$

Obviously in (6), by adjusting the dc component of i_0, active power issued from dc supply is adjusted. Thus, active power absorbed by all submodules in a phase leg and average voltage of all submodules in a phase leg are adjusted at the same time.

In (7), by adjusting the ac current component in i_{apAC} and i_{anAC} which has the same frequency and the same phase angle or same shape with u_{sa}, the active power that distributes between all submodules in positive leg and negative leg is reassigned. So the average voltage of positive leg and negative leg can be adjusted meanwhile.

Δi_{AC} is a current which also has the same frequency and the same phase angle with u_{sa}. It is also defined by

$$\Delta i_{AC} = i_{apAC} - i_{anAC}. \tag{8}$$

From (1) and (3), obviously

$$\begin{cases} i_{apAC} = \dfrac{1}{2}(i_{sa} + \Delta i_{AC}) \\ i_{anAC} = \dfrac{1}{2}(i_{sa} - \Delta i_{AC}) \end{cases}. \tag{9}$$

Define i_0^* as the dc component of i_0, and define i_{aL}^* as the non-dc component（e.g. i_{aL}^* can be zero or 2-th harmonic current）. The following circuit equation exists:

$$i_0 = i_0^* + i_{aL}^* \tag{10}$$

We call i_{aL}^* circulating current in this paper. i_{aL}^* is current that we add manually to i_0 for balancing capacitor voltages and improving other MMC performance. Although we know i_{aL}^* can be controlled expediently, how i_{aL}^* works and its influence requires more research. Following equation is also worked to make sure neither ac source nor dc supply be affected by i_{aL}^*.

$$\begin{cases} \int_0^T U_d i_{aL}^* dt = 0 \\ \int_0^T u_{sa} i_{aL}^* dt = 0 \end{cases} \tag{11}$$

In a word, the positive leg current command i_{ap}^* and the negative leg current command i_{an}^* are obtained as:

$$\begin{cases} i_{ap}^* = \frac{1}{2}(i_{sa}^* + \Delta i_{AC}) + i_0^* + i_{aL}^* \\ i_{an}^* = \frac{1}{2}(i_{sa}^* - \Delta i_{AC}) - i_0^* - i_{aL}^* \end{cases} \tag{12}$$

Where, i_{sa}^* is the current command of i_{sa}.

B. Control Strategy

1) Current Control

The voltage-balancing control method proposed in this paper bases on effective current controlling. The best way to achieve this aim is controlling the i_{ap} and i_{an} separately via controlling U_{ap} and U_{an} as mentioned before. As shown in Fig. 5(a), the feedback controller $W_{iR}(s)$ in current loop force i_{ap} to follow its command i_{ap}^* and i_{an} follow i_{an}^*. d_{ap} is common duty cycle command of positive leg and d_{an} is common duty cycle command of negative leg.

2) Average voltage control

As discussed above, the average voltage of all submodules in a phase can be controlled by adjusting i_0^*. Define u_{dc}^* as the average voltage command of dc-capacitor voltage. u_{apj} is the measured capacitor voltage value of the *j*-th submodule in positive leg and the u_{anj} is the *j*-th capacitor voltage in negative leg. u_{dc} is the average voltage of capacitors in a phase leg. Fig. 3 shows a block diagram of the the average voltage control. i_0^* which is the output of controller $W_{uR}(s)$ makes sure u_{dc} follow its command u_{dc}^* rapidly.

3) Balance control between positive and negative leg

As discussed, balance control between positive and negative leg can be realized by power distribution via adjusting Δi_{AC}. In Fig. 4, u_{sau} has unit amplitude which has the same frequency and the same phase angle with u_{sa}. u_{dcp} and u_{dcn} are average voltage of positive leg and negative leg. Using the difference between u_{dcp} and u_{dcn} as controller $W_{uAC}(s)$'s input, the adjusting current $\frac{1}{2}\Delta i_{AC}$ is obtained by multipling the output of $W_{uAC}(s)$ with constant $\frac{1}{2}$ and u_{sau} as shown in Fig. 4.

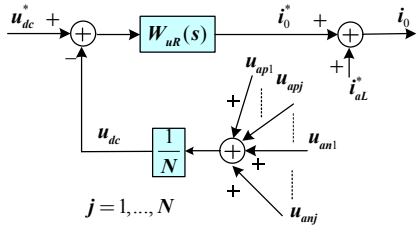

Figure 3. Block diagram of average voltage control

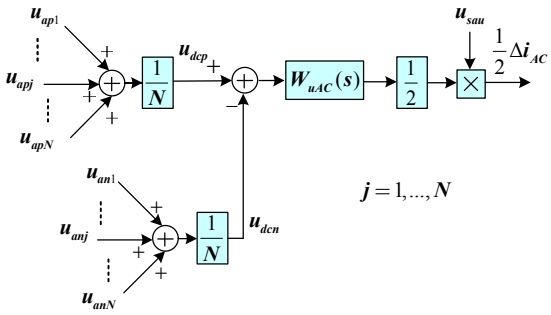

Figure 4. Block diagram of the voltage balancing between positive leg and negative leg

4) Balance control in a leg

As stated before, under the average voltage control of a phase leg and balance control between positive and negative leg, u_{dcp} and u_{dcn} control have been realized as shown in Fig. 3 and Fig. 4. Unfortunately, each submodule has parameters difference from others which cause voltage imbalance among them. To counteract the power loss difference among the submodules connected in a leg, this paper presents a strategy by re-distributing the active power among them as shown in Fig. 5(b) by adding Δd_{apj} or Δd_{anj} to d_{ap} or d_{an} $(j = 1,2,...,N)$ [10]. In Fig. 5(b), i_{sau} is the current which has the same frequency and the same phase angle with i_{ap} or i_{ap}^* and with unit amplitude, and d_{apj} is duty cycle command for *j*-th submodule in positive leg.

When i_{ap} or i_{an} is too little, even though Δd_{apj} or Δd_{anj} is large, the re-distributing power is not enough for balancing control. At present, proper i_{aL}^* is useful to make power re-distributing effectively by increasing i_{ap} or i_{an}. On the other hand, proper i_{aL}^* can reduce rippling voltage of capacitors, but no deeply study presented in this paper.

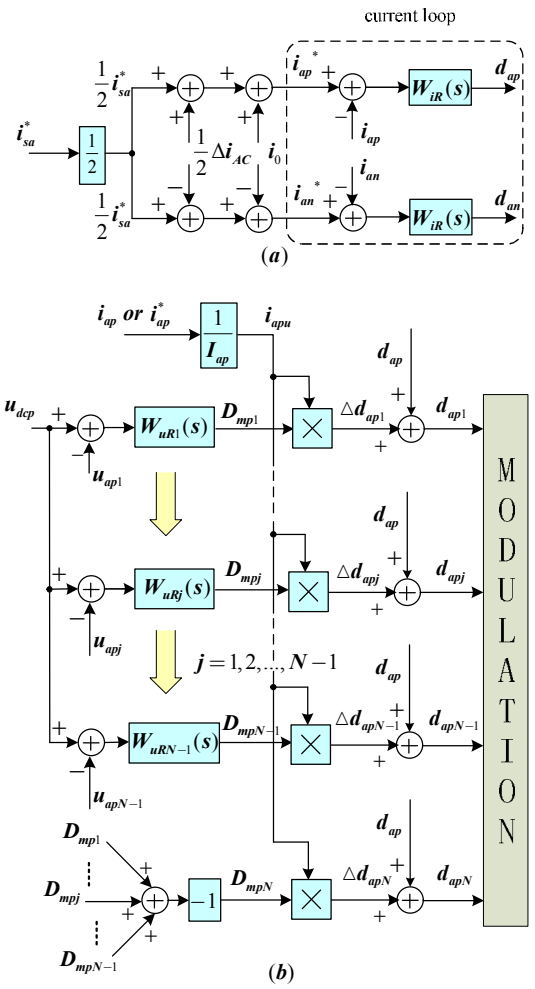

Figure 5. Whole voltage balancing strategy block diagram

Because u_{dcp} and u_{dcn} control have achieved by superior controllers, to avoid affecting u_{dcp} and u_{dcn} control, the voltage command for positive and negative leg is u_{dcp} and u_{dcn}, and the total variation of the duty cycle output must be zero. So for the *N*-th submodule in positive leg, following equation exists:

$$D_{mpN} = -\sum_{j=1}^{N-1} D_{mpj} \tag{13}$$

Where, D_{mpj} is the output of $W_{uRj}(s)(j = 1,2,...,N)$.

Fig. 5(b) only shows control strategy block diagram for positive leg, and for the negative leg, it is the same.

5) Summary

Balancing strategy presented in this paper includes three hierarchies as shown in Fig. 5.

a) By adjusting dc component i_0^*, the average voltage control of a phase leg can be realized.

b) By adding ac component $\frac{1}{2}\Delta i_{AC}$ to current commands, the balance between u_{dcp} and u_{dcn} in a phase leg can be realized.

c) Balance control in a leg makes sure every capacitor voltage is equal to others.

About how three controlling hierarchies works is shown in Fig. 5. The active power command i_{sa}^* can be obtained from the dc bus voltage control loops or power transmission command.

IV. Simulated Results

In order to verify the performance of the proposed control method, several simulations have been carried out using PSIM software package. The modulation method used in simulation is PS-PWM which is commonly adopted by MMC topology. The eight submodules have eight triangular waveforms with the same frequency but a phase difference of 45° (360° / 8) to each other [8]. Every capacitor in phase legs is shunt with a resistor to simulate its active power consumption difference to other submodules. In following simulations, the equivalent resistors in positive leg are 300Ω、400Ω、500Ω、600Ω and in negative leg are 400Ω、500Ω、600Ω、700Ω,and $i_{aL}^* = 0$. TABLE I shows other parameters used for simulations.

TABLE I. Circuit Parameters Used for Simulation

Rated rms current	I_{sa}	80A
Dc supply voltage	U_d	800V
Dc capacitor voltage	U_{dc}	200V
Number of submodule in a leg	N	4
Submodule capacitor	C	5000uF
Rated frequency	f	50Hz
Carrier frequency	f_C	1kHz
Equivalent switching frequency	f_s	8kHz
Buffer inductance	L	1mH
Rated ac voltage	U_{sa}	220V

Fig. 6(a) shows the simulation results including capacitors voltages, average voltage of capacitors in positive leg and negative leg, average voltage of capacitors in a phase leg when the initial voltage of all submodule capacitors is 200V. Fig. 6(b) shows ac supply current, positive leg current, negative leg current and adjusting current $\frac{1}{2}\Delta i_{AC}$ and i_0 at the same simulation condition. In Fig. 6(a) and Fig. 6(b), it is obviously that voltage balancing control and current control works well and all capacitor voltages are balanced around 200V.

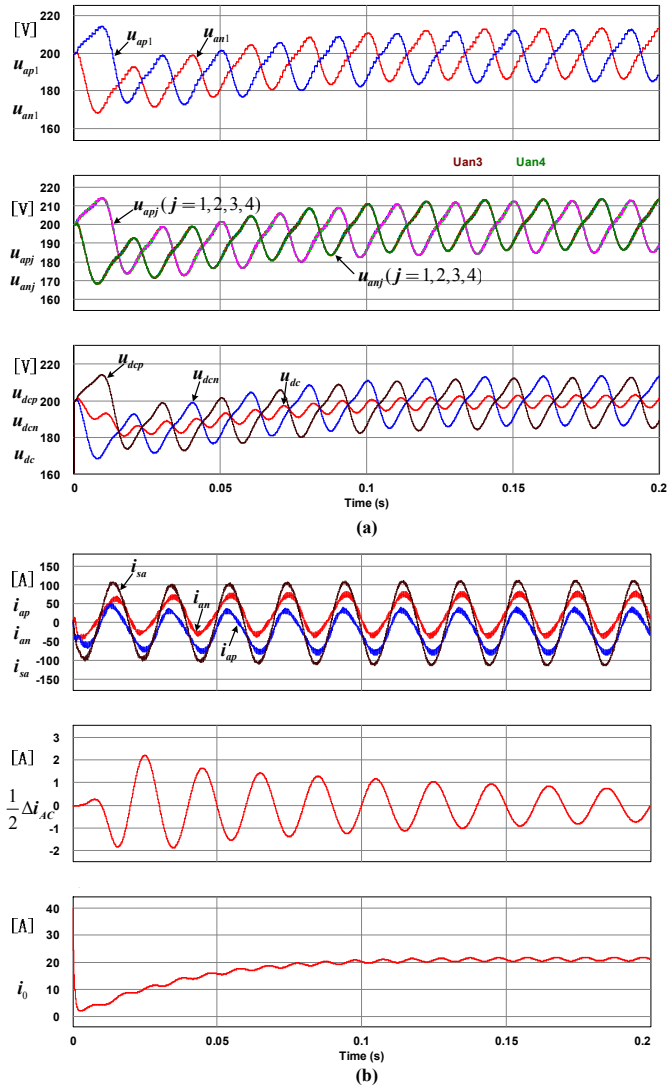

Figure 6. (a) Capacitor voltages and average voltages, (b) ac supply current, leg currents and adjusting current when initial voltage of all submodule capacitors is 200V

Fig. 7(a) shows the simulation results of the initial condition that every submodule capacitor voltage is different, and the average voltage of them is equal to U_{dc}. Fig. 7(b) shows the simulation results when every submodule initial voltage is 160V. As for the simulation results shown in Fig. 7(c), all submodule initial capacitor voltages are different and the average voltage of them is 160V. Obviously, under every condition mentioned above, the control strategy presented in this paper can control leg currents and ac source current effectively, and all the capacitor voltages can keep balanced.

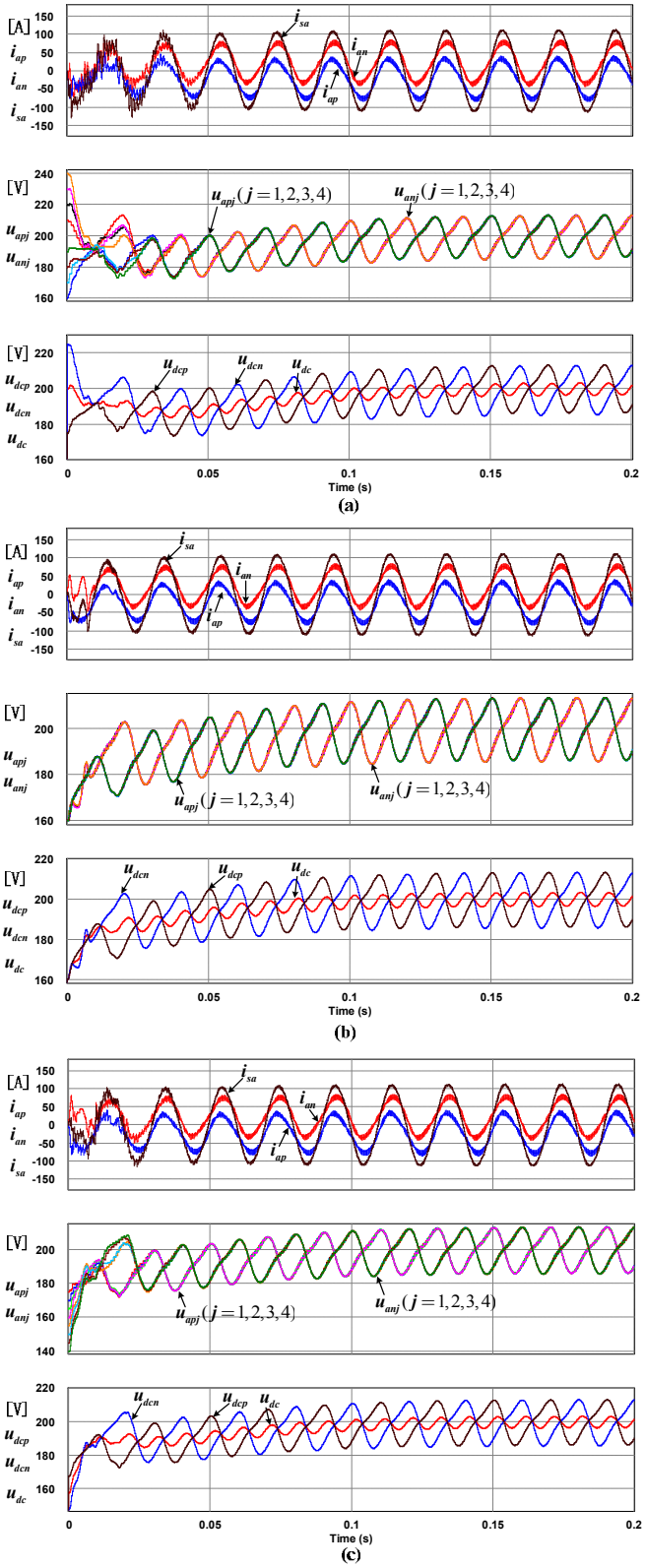

Figure 7. Leg currents and ac supply current, capacitor voltages, average voltages on different initial conditions

V. CONCLUSIONS

In this paper, we have presented and discussed a balancing control method about MMC topology. About how to control the positive leg current and negative leg current independently and how to control circulating current is also proposed. Simulation based on "PSIM" soft package has confirmed both of them, verifying the good performance in different simulation conditions. Benefits from its modular construction without transformer, the MMC topology shows amazing promise for medium-voltage and high-voltage systems, e.g. motor-drives, HVDC, STATCOMs.

REFERENCES

[1] J. DORN, H. HUANG, and D. RETZMANN, "Novel Voltage-Sourced Converters for HVDC and FACTS Applications," presented at the OSAKA 2007, Japan, 2007.

[2] R. Marquardt, "Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications," in Power Electronics Conference (IPEC), 2010 International, 2010, pp. 502-507.

[3] E. Solas, G. Abad, J. A. Barrena, Ca, x, et al., "Modulation of Modular Multilevel Converter for HVDC application," in Power Electronics and Motion Control Conference (EPE/PEMC), 2010 14th International, 2010, pp. T2-84-T2-89.

[4] Z. Yan, H. Xue-hao, T. Guang-fu, and H. Zhi-yuan, "A study on MMC model and its current control strategies," in Power Electronics for Distributed Generation Systems (PEDG), 2010 2nd IEEE International Symposium on, 2010, pp. 259-264.

[5] G. Minyuan, X. Zheng, and L. Huijie, "Analysis of DC voltage ripples in modular multilevel converters," in Power System Technology (POWERCON), 2010 International Conference on, 2010, pp. 1-6.

[6] A. Antonopoulos, L. Angquist, and H. P. Nee, "On dynamics and voltage control of the Modular Multilevel Converter," in Power Electronics and Applications, 2009. EPE '09. 13th European Conference on, 2009, pp. 1-10.

[7] E. Solas, G. Abad, J. A. Barrena, Ca, x, et al., "Modelling, simulation and control of Modular Multilevel Converter," in Power Electronics and Motion Control Conference (EPE/PEMC), 2010 14th International, 2010, pp. T2-90-T2-96.

[8] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," Power Electronics, IEEE Transactions on, vol. 24, pp. 1737-1746, 2009.

[9] W. Kui, L. Yongdong, and Z. Zedong, "Voltage balancing control and experiments of a novel modular multilevel converter," in Energy Conversion Congress and Exposition (ECCE), 2010 IEEE, 2010, pp. 3691-3696.

[10] J. A. Barrena, L. Marroyo, M. A. Rodriguez, O. Alonso, and J. R. Torrealday, "DC Voltage Balancing for PWM Cascaded H-Bridge Converter Based STATCOM," in IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on, 2006, pp. 1840-1845.