CM5 socket

File: cm5_socket_mcu.kicad_sch

STM32H7 MCU

File: STM32H7_MCU.kicad_sch

Ethernet PHY, PSRAM, eMMC

File: eth_psram_emmc.kicad_sch

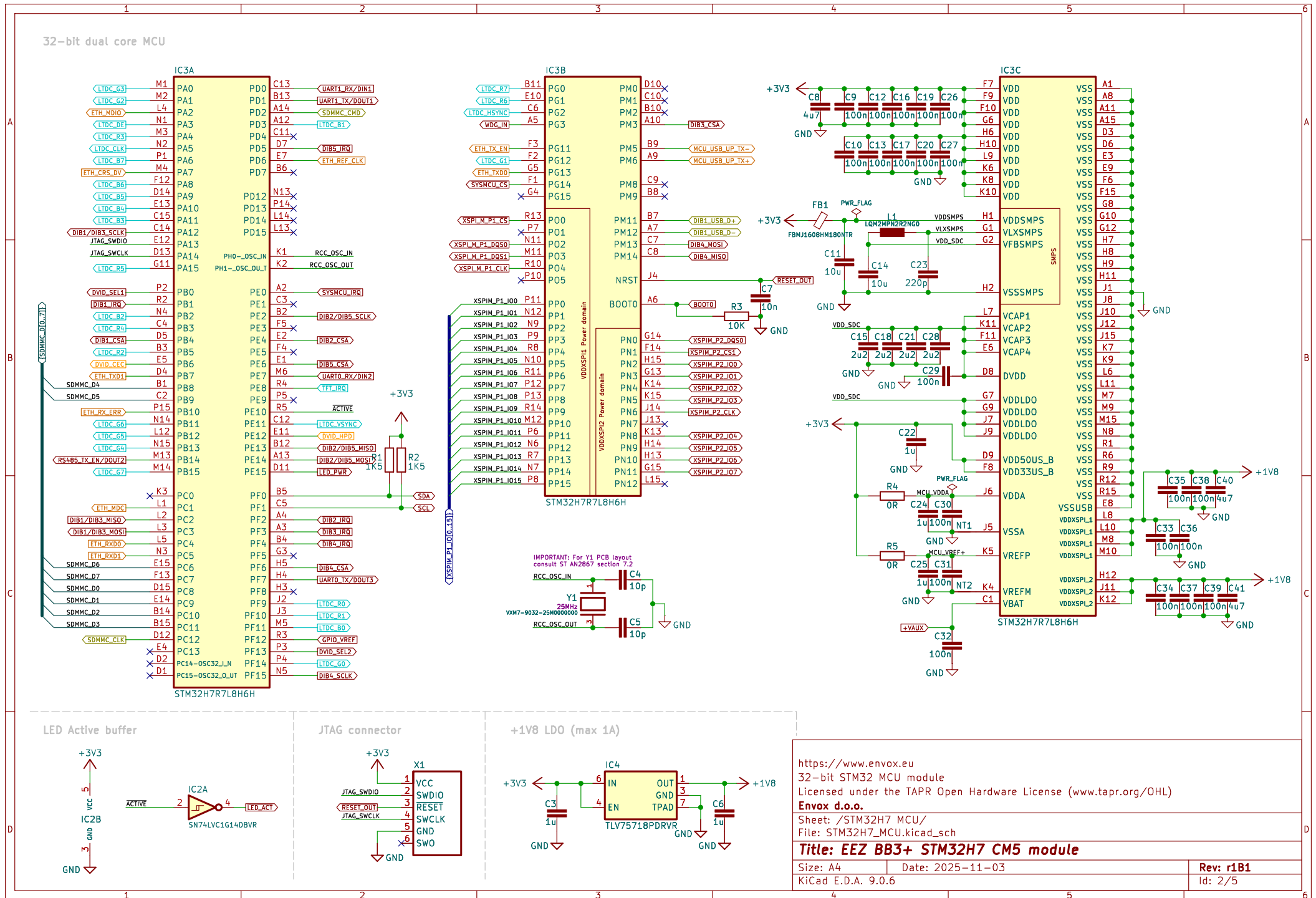DVID converter, NOR Flash

File: Ethernet_flash.kicad_sch

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File: BB3plus CM5 STM32H7 module.kicad_sch

Title: EEZ BB3+ STM32H7 CM5 module

| Size: A4 | Date: 2025-11-03 | Rev: r1B1 |
| KiCad E.D.A. 9.0.6 | | Id: 1/5 |

SoM1A
2x DF40HC(3.0)-100DS-0.4V(51

Pin	Signal		Signal	Pin
2	GND		GND	1
4	Ethernet_Pair1_P		Ethernet_Pair3_P	3
6	Ethernet_Pair1_N		Ethernet_Pair3_N	5
8	GND		GND	7
10	Ethernet_Pair0_N		Ethernet_Pair2_N	9
12	Ethernet_Pair0_P		Ethernet_Pair2_P	11
14	GND		GND	13
16	Fan_Tacho		Ethernet_nLED3(3.3v)	15
18	Ethernet_SYNC_OUT(1.8v)		Ethernet_nLED2(3.3v)	17
20	EEPROM_nWP		Fan_PWM	19
22	GND		LED_nACT	21
24	GPIO26		GPIO21	23
26	GPIO19		GPIO20	25
28	GPIO13		GPIO16	27
30	GPIO6		GPIO12	29
32	GND		GND	31
34	GPIO5		ID_SC/GPIO1	33
36	ID_SD/GPIO0		GPIO8	35
38	GPIO11		GPIO8	37
40	GPIO9		GPIO25	39
42	GND		GPIO25	41
44	GPIO10		GND	43
46	GPIO22		GPIO24	45
48	GPIO27		GPIO23	47
50	GPIO17		GPIO18	49
52	GND		GPIO15	51
54	GPIO4		GND	53
56	GPIO3		GPIO14	55
58	GPIO2		SD_CLK	57
60	GND		GND	59
62	SD_CMD		SD_DAT3	61
64	SD_DAT5		SD_DAT0	63
66	GND		GND	65
68	SD_DAT4		SD_DAT1	67
70	SD_DAT7		SD_DAT2	69
72	SD_DAT6		GND	71
74	GND		SD_VDD_Override	73
76	VBAT		SD_PWR_ON	75
78	GPIO_VREF(1.8v/3.3v_Input)		+5v(Input)	77
80	SCL0		+5v(Input)	79
82	SDA0		+5v(Input)	81
84	CM5_3.3v		+5v(Input)	83
86	CM5_3.3v		+5v(Input)	85
88	CM5_1.8v		+5v(Input)	87
90	CM5_1.8v		WiFi_nDisable	89
92	PWR_Button		BT_nDisable	91
94	CC1		nRPIBOOT	93
96	CC2		LED_nPWR	95
98	GND		CAM_GPIO0	97
100	CAM_GPIO1		PMIC_EN	99

Net labels (SoM1A left): ETH_TXRX_B+, ETH_TXRX_B-, ETH_TXRX_A-, ETH_TXRX_A+, SYSMCU_CS, DIB1_IRQ, DIB1/DIB3_MISO, DIB4_MOSI, DIB4_MISO, DIB2/DIB5_SCLK, DIB2/DIB5_MISO, DIB2/DIB5_MOSI, DIB4_IRQ, WDG_IN, DIB3_CSA, DIB4_CSA, UART0_TX/DOUT3, UART0_RX/DIN2, +VAUX, GPIO_VREF, SCL, SDA, +3V3, +1V8, RESET_OUT, UART1_RX/DIN1

Net labels (SoM1A right): ETH_LINK_ACT, ETH_LINK100, LED_ACT, DIB3_IRQ, DIB2_IRQ, RS485_TX_EN/DOUT2, DIB1_CSA, DIB4_SCLK, DIB2_CSA, TFT_IRQ, SYSMCU_IRQ, DIB5_IRQ, DIB5_CSA, DIB1/DIB3_SCLK, DIB1/DIB3_MOSI, BOOT0, LED_PWR, UART1_TX/DOUT1, +5V_IN

PWR_FLAG, PWR_FLAG, PWR_FLAG

SoM1B
2x DF40HC(3.0)-100DS-0.4V(51

Pin	Signal		Signal	Pin
102	PCIe_CLK_nREQ		USB_OTG_ID	101
104	PCIE_nWAKE		USB_N	103
106	PCIE_PWR_EN		USB_P	105
108	GND		GND	107
110	PCIe_CLK_P		PCIe_nRST	109
112	PCIe_CLK_N		VBUS_EN_(3.3v)	111
114	GND		GND	113
116	PCIe_RX_P		MIPI0_D0_N	115
118	PCIe_RX_N		MIPI0_D0_P	117
120	GND		GND	119
122	PCIe_TX_P		MIPI0_D1_N	121
124	PCIe_TX_N		MIPI0_D1_P	123
126	GND		GND	125
128	USB3-0-RX_N		MIPI0_C_N	127
130	USB3-0-RX_P		MIPI0_C_P	129
132	GND		GND	131
134	USB3-0-DP		MIPI0_D2_N	133
136	USB3-0-DM		MIPI0_D2_P	135
138	GND		GND	137
140	USB3-0-TX_N		MIPI0_D3_N	139
142	USB3-0-TX_P		MIPI0_D3_P	141
144	GND		HDMI1_HOTPLUG	143
146	HDMI1_TX2_P		HDMI1_SDA	145
148	HDMI1_TX2_N		HDMI1_SCL	147
150	GND		HDMI1_CEC	149
152	HDMI1_TX1_P		HDMI0_CEC	151
154	HDMI1_TX1_N		HDMI0_HOTPLUG	153
156	GND		GND	155
158	HDMI1_TX0_P		USB3-1-RX_N	157
160	HDMI1_TX0_N		USB3-1-RX_P	159
162	GND		GND	161
164	HDMI1_CLK_P		USB3-1-DP	163
166	HDMI1_CLK_N		USB3-1-DM	165
168	GND		GND	167
170	HDMI0_TX2_P		USB3-1-TX_N	169
172	HDMI0_TX2_N		USB3-1-TX_P	171
174	GND		GND	173
176	HDMI0_TX1_P		MIPI1_D0_N	175
178	HDMI0_TX1_N		MIPI1_D0_P	177
180	GND		GND	179
182	HDMI0_TX0_P		MIPI1_D1_N	181
184	HDMI0_TX0_N		MIPI1_D1_P	183
186	GND		GND	185
188	HDMI0_CLK_P		MIPI1_C_N	187
190	HDMI0_CLK_N		MIPI1_C_P	189
192	GND		GND	191
194	MIPI1_D3_N		MIPI1_D2_N	193
196	MIPI1_D3_P		MIPI1_D2_P	195
198	GND		GND	197
200	HDMI0_SCL		HDMI0_SDA	199

Net labels (SoM1B left): DIB1_USB_D+, DIB1_USB_D-, TFT_DVID_TX2_P, TFT_DVID_TX2_N, TFT_DVID_TX1_P, TFT_DVID_TX1_N, TFT_DVID_TX0_P, TFT_DVID_TX0_N, TFT_DVID_CLK_P, TFT_DVID_CLK_N, REAR_DVID_TX2_P, REAR_DVID_TX2_N, REAR_DVID_TX1_P, REAR_DVID_TX1_N, REAR_DVID_TX0_P, REAR_DVID_TX0_N, REAR_DVID_CLK_P, REAR_DVID_CLK_N, REAR_DVID_SCL

Net labels (SoM1B right): TFT_DVID_HPD, TFT_DVID_SDA, TFT_DVID_SCL, TFT_DVID_CEC, REAR_DVID_CEC, REAR_DVID_HPD, MCU_USB_UP_TX-, MCU_USB_UP_TX+, REAR_DVID_SDA

+3V3 LDO (max 1A)

IC1 — AZ1117CH2-3.3TRG1

INPUT / OUTPUT / ADJ/GND / ADJ/GND

Pins: 1 INPUT, 3 OUTPUT, 2 ADJ/GND, 4 ADJ/GND

+5V_IN → INPUT
OUTPUT → +3V3

C1 10u — GND
C2 10u — GND

Title: EEZ BB3+ STM32H7 CM5 module

Size: A4	Date: 2025-11-03	Rev: r1B1
KiCad E.D.A. 9.0.6		Id: 1/5

32-bit dual core MCU

IC3A — STM32H7R7L8H6H

Pin	Signal
M1	PA0 / LTDC_G3
M2	PA1 / LTDC_G2
L4	PA2 / ETH_MDIO
N1	PA3 / LTDC_DE
M3	PA4 / LTDC_R3
N2	PA5 / LTDC_CLK
P1	PA6 / LTDC_B7
M4	PA7 / ETH_CRS_DV
F12	PA8 / LTDC_B6
D14	PA9 / LTDC_B5
E13	PA10 / LTDC_B4
C15	PA11 / LTDC_B3
C14	PA12 / DIB1/DIB3_SCLK
E12	PA13 / JTAG_SWDIO
D13	PA14 / JTAG_SWCLK
G11	PA15 / LTDC_R5

Pin	Signal
P2	PB0 / DVID_SEL1
R2	PB1 / DIB1_IRQ
N4	PB2 / LTDC_B2
C4	PB3 / LTDC_R4
D5	PB4 / DIB1_CSA
B3	PB5 / LTDC_R2
E5	PB6 / DVID_CEC
D4	PB7 / ETH_TXD1
B1	PB8 / SDMMC_D4
C2	PB9 / SDMMC_D5
P15	PB10 / ETH_RX_ERR
N14	PB11 / LTDC_G6
L12	PB12 / LTDC_G5
N15	PB13 / LTDC_G4
M13	PB14 / RS485_TX_EN/DOUT2
M14	PB15 / LTDC_G7

Pin	Signal
K3	PC0
L1	PC1 / ETH_MDC
L2	PC2 / DIB1/DIB3_MISO
L3	PC3 / DIB1/DIB3_MOSI
L5	PC4 / ETH_RXD0
N3	PC5 / ETH_RXD1
E15	PC6 / SDMMC_D6
F13	PC7 / SDMMC_D7
D15	PC8 / SDMMC_D0
E14	PC9 / SDMMC_D1
B14	PC10 / SDMMC_D2
B15	PC11 / SDMMC_D3
D12	PC12 / SDMMC_CLK
E4	PC13
D2	PC14-OSC32_I_N
D1	PC15-OSC32_O_UT

Pin	Signal
C13	PD0 / UART1_RX/DIN1
B13	PD1 / UART1_TX/DOUT1
A14	PD2 / SDMMC_CMD
C11	PD3 / LTDC_B1
D7	PD4
E7	PD5 / DIB5_IRQ / ETH_REF_CLK
B6	PD6
	PD7
N13	PD12
P14	PD13
L14	PD14
L13	PD15

Pin	Signal
A2	PE0
C3	PE1 / SYSMCU_IRQ
B2	PE2
F5	PE3 / DIB2/DIB5_SCLK
E2	PE4
F4	PE5 / DIB2_CSA
E1	PE6 / DIB5_CSA
M6	PE7 / UART0_RX/DIN2
R5	PE8 / TFT_IRQ
P5	PE9 / ACTIVE
R5	PE10
C12	PE11 / LTDC_VSYNC
E11	PE12 / DVID_HPD
B12	PE13 / DIB2/DIB5_MISO
A13	PE14 / DIB2/DIB5_MOSI
D11	PE15 / LED_PWR

Pin	Signal
B5	PF0 / SDA
C5	PF1 / SCL
A4	PF2 / DIB2_IRQ
A3	PF3 / DIB3_IRQ
B4	PF4 / DIB4_IRQ
G3	PF5
H5	PF6 / DIB4_CSA
H4	PF7 / UART0_TX/DOUT3
H3	PF8
J2	PF9 / LTDC_R0
J3	PF10 / LTDC_R1
M5	PF11 / LTDC_B0
R3	PF12 / GPIO_VREF
P3	PF13 / DVID_SEL2
P4	PF14 / LTDC_G0
N5	PF15 / DIB4_SCLK

RCC_OSC_IN — K1 — PH0-_OSC_IN
RCC_OSC_OUT — K2 — PH1-_OSC_OU_T

SDMMC_D[0..7]
XSPIM_P1_IO[0..15]

IC3B — STM32H7R7L8H6H

Pin	Signal
B11	PG0 / LTDC_R7
E10	PG1 / LTDC_R6
C6	PG2 / LTDC_HSYNC
A5	PG3 / WDG_IN
F3	PG11 / ETH_TX_EN
F2	PG12 / LTDC_G1
G5	PG13 / ETH_TXD0
F1	PG14 / SYSMCU_CS
G4	PG15

Pin	Signal
R13	PO0 / XSPI_M_P1_CS
P7	PO1
N11	PO2 / XSPI_M_P1_DQS0
M11	PO3 / XSPI_M_P1_DQS1
R10	PO4 / XSPI_M_P1_CLK
P10	PO5

VDDXSPI1 Power domain
Pin	Signal
P11	PP0 / XSPIM_P1_IO0
N12	PP1 / XSPIM_P1_IO1
P9	PP2 / XSPIM_P1_IO2
R8	PP3 / XSPIM_P1_IO3
N10	PP4 / XSPIM_P1_IO4
R11	PP5 / XSPIM_P1_IO5
P12	PP6 / XSPIM_P1_IO6
P13	PP7 / XSPIM_P1_IO7
R14	PP8 / XSPIM_P1_IO8
M12	PP9 / XSPIM_P1_IO9
P6	PP10 / XSPIM_P1_IO10
N6	PP11 / XSPIM_P1_IO11
R7	PP12 / XSPIM_P1_IO12
N7	PP13 / XSPIM_P1_IO13
P8	PP14 / XSPIM_P1_IO14
	PP15 / XSPIM_P1_IO15

VDDXSPI2 Power domain

Pin	Signal
D10	PM0
C10	PM1
B10	PM2
A10	PM3 / DIB3_CSA
B9	PM5 / MCU_USB_UP_TX-
A9	PM6 / MCU_USB_UP_TX+
C9	PM8
B8	PM9
B7	PM11 / DIB1_USB_D+
A7	PM12 / DIB1_USB_D-
C7	PM13 / DIB4_MOSI
C8	PM14 / DIB4_MISO

Pin	Signal
G14	PN0 / XSPIM_P2_DQS0
F14	PN1 / XSPIM_P2_CS1
H15	PN2 / XSPIM_P2_IO0
G13	PN3 / XSPIM_P2_IO1
K14	PN4 / XSPIM_P2_IO2
K15	PN5 / XSPIM_P2_IO3
J14	PN6 / XSPIM_P2_CLK
J13	PN7
K13	PN8
H14	PN9 / XSPIM_P2_IO4
H13	PN10 / XSPIM_P2_IO5
G15	PN11 / XSPIM_P2_IO6
L15	PN12 / XSPIM_P2_IO7

J4 — NRST — RESET_OUT
A6 — BOOT0 — BOOT0
R3 10K
C7 10n — GND

IC3C — STM32H7R7L8H6H (SMPS / power)

+3V3
C8 4u7 / C9 100n / C12 100n / C16 100n / C19 100n / C26 100n — GND
C10 100n / C13 100n / C17 100n / C20 100n / C27 100n — GND

VDD pins: F7, F9, F10, G6, H6, H10, L9, K6, K8, K10
VSS pins: A1, A8, A11, A15, D3, D6, E3, E6, F6, F15, G8, G10, G12, H7, H8, H9, H11, J1, J8, J10, J12, J15, K7, K9, L6, L11, M7, M9, M15, N8, R1, R6, R9, R12, R15, E8, L8, L10, M8, M10, H12, J11, K12

FB1 — PWR_FLAG — L1 LQM2MPN2R2NG0
FBMJ1608HM180NTR
+3V3 — VDDSMPS H1 / VLXSMPS G1 / VFBSMPS G2
VDD_SDC G2
C11 10u — C14 10u — C23 220p — GND
VSSSMPS H2

VDD_SDC
C15 2u2 / C18 2u2 / C21 2u2 / C28 2u2 — GND
C29 100n — GND
VCAP1 L7 / VCAP2 K11 / VCAP3 F11 / VCAP4 E6
DVDD D8

+3V3
C22 1u — GND
VDDLDO G7, G9, J7, J9
PWR_FLAG
R4 0R — MCU_VDDA — VDDA J6
C24 1u / C30 100n NT1 — GND
VSSA J5
R5 0R — MCU_VREF+ — VREFP K5
C25 1u / C31 100n NT2 — GND
VREFM K4
VBAT C1 — +VAUX — C32 100n — GND

VDD50US_B D9
VDD33US_B D9
VSSUSB E8
VDDXSPI1 L8, L10, M8, M10 — C33 100n / C36 100n — GND
VDDXSPI2 H12, J11, K12 — C34 100n / C37 100n / C39 100n / C41 4u7 — GND
+1V8 — C35 100n / C38 100n / C40 4u7 — GND
+1V8

IMPORTANT: For Y1 PCB layout consult ST AN2867 section 7.2

RCC_OSC_IN — C4 10p
Y1 25MHz VXM7-9032-25M0000000
RCC_OSC_OUT — C5 10p — GND

LED Active buffer
+3V3
IC2A / IC2B — SN74LVC1G14DBVR
ACTIVE 2 — 4 LED_ACT
VCC 5, GND 3
GND

JTAG connector
+3V3
X1
1 VCC
JTAG_SWDIO — 2 SWDIO
RESET_OUT — 3 RESET
JTAG_SWCLK — 4 SWCLK
5 GND
6 SWO
GND

+1V8 LDO (max 1A)
IC4 TLV75718PDRVR
+3V3 — 6 IN — OUT 1 — +1V8
4 EN — GND 3 / TPAD 7
C3 1u — GND
C6 1u — GND

R1 1K5 / R2 1K5 / +3V3
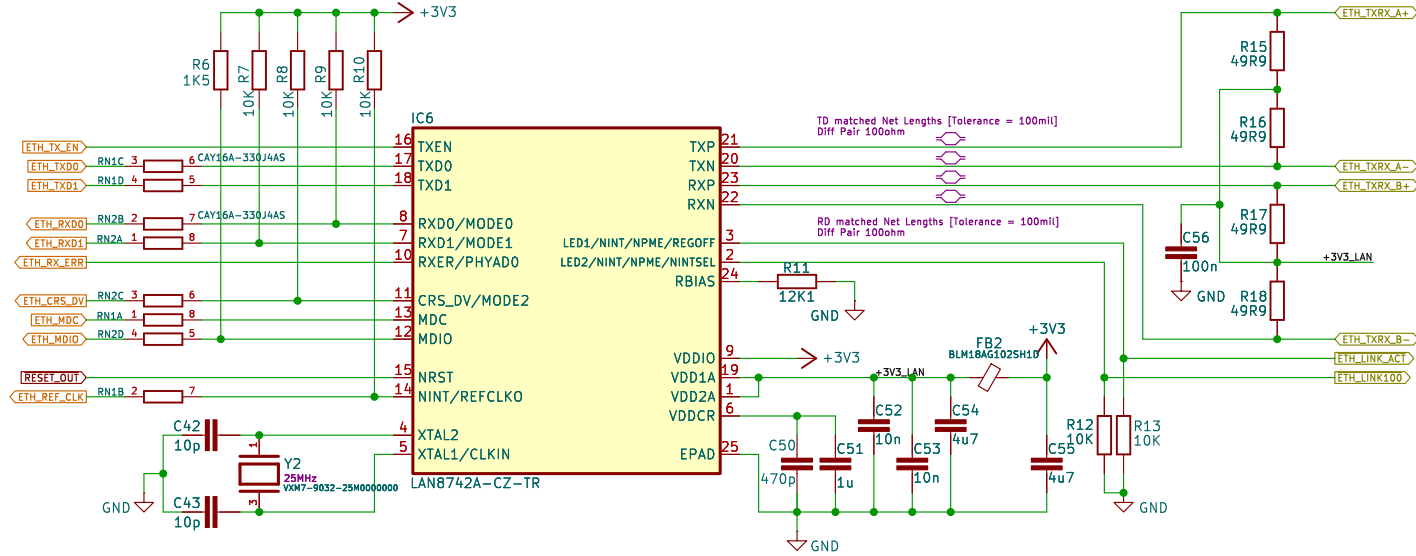
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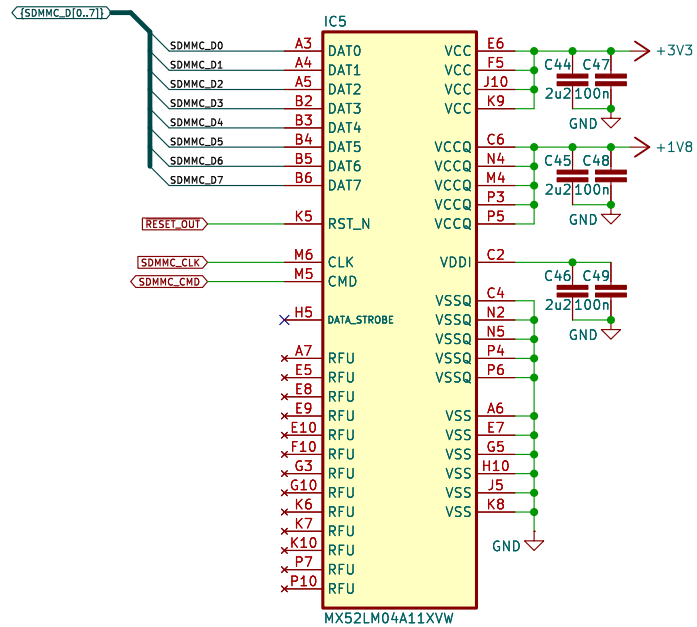Envox d.o.o.
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Title: EEZ BB3+ STM32H7 CM5 module
Size: A4   Date: 2025-11-03   Rev: r1B1
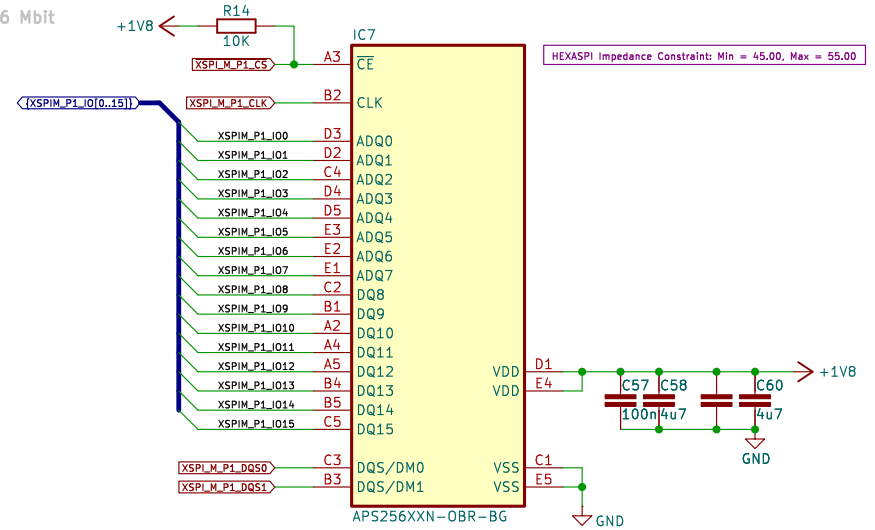KiCad E.D.A. 9.0.6   Id: 2/5

Ethernet RMII PHY

IC6 — LAN8742A-CZ-TR

R6 1K5, R7 10K, R8 10K, R9 10K, R10 10K → +3V3

Net	Pin	Signal
ETH_TX_EN	16	TXEN
ETH_TXD0 (RN1C 3 / CAY16A-330J4AS 6)	17	TXD0
ETH_TXD1 (RN1D 2 / 5)	18	TXD1
ETH_RXD0 (RN2B 2 / CAY16A-330J4AS 7)	8	RXD0/MODE0
ETH_RXD1 (RN2A 1 / 8)	7	RXD1/MODE1
ETH_RX_ERR	10	RXER/PHYAD0
ETH_CRS_DV (RN2C 3 / 6)	11	CRS_DV/MODE2
ETH_MDC (RN1A 1 / 8)	13	MDC
ETH_MDIO (RN2D 4 / 5)	12	MDIO
RESET_OUT (RN1B 2 / 7)	15	NRST
ETH_REF_CLK	14	NINT/REFCLKO

Right side pins:
- TXP 21
- TXN 20
- RXP 23
- RXN 22
- LED1/NINT/NPME/REGOFF 3
- LED2/NINT/NPME/NINTSEL 2
- RBIAS 24
- VDDIO 9 → +3V3
- VDD1A 19 → +3V3_LAN
- VDD2A 1
- VDDCR 6
- EPAD 25

R11 12K1 → GND

TD matched Net Lengths [Tolerance = 100mil] Diff Pair 100ohm
RD matched Net Lengths [Tolerance = 100mil] Diff Pair 100ohm

R15 49R9 → ETH_TXRX_A+
R16 49R9 → ETH_TXRX_A−
R17 49R9 → ETH_TXRX_B+
R18 49R9 → ETH_TXRX_B−
C56 100n → +3V3_LAN / GND

FB2 BLM18AG102SH1D → +3V3
ETH_LINK_ACT
ETH_LINK100
R12 10K, R13 10K

C50 470p, C51 1u, C52 10n, C53 10n, C54 4u7, C55 4u7 → GND

Y2 25MHz VXM7-9032-25M0000000
C42 10p, C43 10p → GND
XTAL2 4, XTAL1/CLKIN 5

eMMC 4 GB

IC5 — MX52LM04A11XVW

Net	Pin	Signal
SDMMC_D0	A3	DAT0
SDMMC_D1	A4	DAT1
SDMMC_D2	A5	DAT2
SDMMC_D3	B2	DAT3
SDMMC_D4	B3	DAT4
SDMMC_D5	B4	DAT5
SDMMC_D6	B5	DAT6
SDMMC_D7	B6	DAT7
RESET_OUT	K5	RST_N
SDMMC_CLK	M6	CLK
SDMMC_CMD	M5	CMD
	H5	DATA_STROBE

{SDMMC_D[0..7]}

VCC: E6, F5, J10, K9 → +3V3
VCCQ: C6, N4, M4, P3, P5 → +1V8
VDDI: C2
VSSQ: C4, N2, N5, P4, P6 → GND
VSS: A6, E7, G5, H10, J5, K8 → GND

RFU: A7, E5, E8, E9, E10, F10, G3, G10, K6, K7, K10, P7, P10

C44 2u2, C47 100n → GND
C45 2u2, C48 100n → GND
C46 2u2, C49 100n → GND

PSRAM 256 Mbit

IC7 — APS256XXN-OBR-BG

HEXASPI Impedance Constraint: Min = 45.00, Max = 55.00

+1V8 ← R14 10K
XSPI_M_P1_CS → A3 CE
XSPI_M_P1_CLK → B2 CLK

Net	Pin	Signal
XSPIM_P1_IO0	D3	ADQ0
XSPIM_P1_IO1	D2	ADQ1
XSPIM_P1_IO2	C4	ADQ2
XSPIM_P1_IO3	D4	ADQ3
XSPIM_P1_IO4	D5	ADQ4
XSPIM_P1_IO5	E3	ADQ5
XSPIM_P1_IO6	E2	ADQ6
XSPIM_P1_IO7	E1	ADQ7
XSPIM_P1_IO8	C2	DQ8
XSPIM_P1_IO9	B1	DQ9
XSPIM_P1_IO10	A2	DQ10
XSPIM_P1_IO11	A4	DQ11
XSPIM_P1_IO12	A5	DQ12
XSPIM_P1_IO13	B4	DQ13
XSPIM_P1_IO14	B5	DQ14
XSPIM_P1_IO15	C5	DQ15

{XSPIM_P1_IO[0..15]}

XSPI_M_P1_DQS0 → C3 DQS/DM0
XSPI_M_P1_DQS1 → B3 DQS/DM1

VDD: D1, E4 → +1V8
VSS: C1, E5 → GND

C57 100n, C58 4u7, C60 4u7 → +1V8 / GND

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File: eth_psram_emmc.kicad_sch

Title: EEZ BB3+ STM32H7 CM5 module

Size: A4 | Date: 2025-11-03 | Rev: r1B1
KiCad E.D.A. 9.0.6 | Id: 3/5

RGB-to-DVID converter

IC8 — TFP410PAP

Pin	Signal		Pin	Signal
57	IDCK+		21	TXC−
56	IDCK−		22	TXC+
2	DE		24	TX0−
4	HSYNC		25	TX0+
5	VSYNC		27	TX1−
3	VREF		28	TX1+
63	DATA0		30	TX2−
62	DATA1		31	TX2+

LTDC_CLK → IDCK+ 57
IDCK− 56
GND

LTDC_DE → DE 2
LTDC_HSYNC → HSYNC 4
LTDC_VSYNC → VSYNC 5
+3V3 — R20 10K — VREF 3

TXC− 21 → TXC−
TXC+ 22 → TXC+
TX0− 24 → TX0−
TX0+ 25 → TX0+
TX1− 27 → TX1−
TX1+ 28 → TX1+
TX2− 30 → TX2−
TX2+ 31 → TX2+

BLUE:
LTDC_B0 → DATA0 63
LTDC_B1 → DATA1 62
LTDC_B2 → DATA2 61
LTDC_B3 → DATA3 60
LTDC_B4 → DATA4 59
LTDC_B5 → DATA5 58
LTDC_B6 → DATA6 55
LTDC_B7 → DATA7 54

TFADJ 19 — R21 510R — GND

GREEN:
LTDC_G0 → DATA8 53
LTDC_G1 → DATA9 52
LTDC_G2 → DATA10 51
LTDC_G3 → DATA11 50
LTDC_R4 → DATA12 47
LTDC_R5 → DATA13 46
LTDC_R6 → DATA14 45
LTDC_R7 → DATA15 44

EDGE/HTPLG 9 — R22 1K — +3V3
PWR_FLAG

RED:
LTDC_R0 → DATA16 43
LTDC_R1 → DATA17 42
LTDC_R2 → DATA18 41
LTDC_R3 → DATA19 40
LTDC_G4 → DATA20 39
LTDC_G5 → DATA21 38
LTDC_G6 → DATA22 37
LTDC_G7 → DATA23 36

RESERVED 34
DVDD 1
DVDD 12
DVDD 33
PVDD 18
TVDD 29
TVDD 23

DVDD — C61 100n, C64 100n, C66 100n, C67 10u — FB3 60R@100MHz → +3V3
PVDD — C62 100n, C68 10u — FB4 60R@100MHz
TVDD — C63 100n, C65 100n, C69 10u — FB5 60R@100MHz
GND

+3V3 — R19 4K7 — MSEN/PO1 11
RESET_OUT — ISEL/RST 13
SCL → BSEL/SCL 15
SDA → DSEL/SDA 14
PD 10

+3V3 — JP1 — DKEN 35
GND
CTL1/A1/DK1 8
CTL2/A2/DK2 7
CTL3/A3/DK3 6

DGND 16
DGND 48
DGND 64
TGND 20
TGND 26
TGND 32
PGND 17
EPAD 65
GND

Video MUX 1:2

IC9 — TS3DV642A0RUAR

Pin	Signal		Pin	Signal
6	D0−		38	D0+A
5	D0+		37	D0−A
8	D1−		36	D1+A
7	D1+		35	D1−A

TX2− → D0− 6
TX2+ → D0+ 5
TX1− → D1− 8
TX1+ → D1+ 7
TX0− → D2− 11
TX0+ → D2+ 10
TXC− → D3− 13
TXC+ → D3+ 12

D0+A 38 → TFT_DVID_TX2_P
D0−A 37 → TFT_DVID_TX2_N
D1+A 36 → TFT_DVID_TX1_P
D1−A 35 → TFT_DVID_TX1_N
D2+A 34 → TFT_DVID_TX0_P
D2−A 33 → TFT_DVID_TX0_N
D3+A 32 → TFT_DVID_CLK_P
D3−A 31 → TFT_DVID_CLK_N

D0+B 29 → REAR_DVID_TX2_P
D0−B 28 → REAR_DVID_TX2_N
D1+B 27 → REAR_DVID_TX1_P
D1−B 26 → REAR_DVID_TX1_N
D2+B 25 → REAR_DVID_TX0_P
D2−B 24 → REAR_DVID_TX0_N
D3+B 23 → REAR_DVID_CLK_P
D3−B 22 → REAR_DVID_CLK_N

SCL → SCL 3
SDA → SDA 4
DVID_CEC → CEC 15
DVID_HPD → HPD 14

SCL_A 42 → TFT_DVID_SCL
SDA_A 41 → TFT_DVID_SDA
HPD_A 19 → TFT_DVID_HPD
CEC_A 18 → TFT_DVID_CEC

SCL_B 40 → REAR_DVID_SCL
SDA_B 39 → REAR_DVID_SDA
HPD_B 21 → REAR_DVID_HPD
CEC_B 20 → REAR_DVID_CEC

RESET_OUT → EN 2
DVID_SEL1 → SEL1 16
DVID_SEL2 → SEL2 17

VCC 1 → +3V3 — C70 10n — GND
EPAD 43 — GND

NOR flash memory 256 Mbit (32 MB x 8, 200 MHz)

IC10 — MX25UM25645GXDI00−T

+1V8 — R23 10K

XSPIM_P2_CS1 → CS C2
XSPIM_P2_CLK → SCLK B2
XSPIM_P2_DQS0 → DQS C3
XSPIM_P2_IO0 → SIO0 D3
XSPIM_P2_IO1 → SIO1 D2
XSPIM_P2_IO2 → SIO2 C4
XSPIM_P2_IO3 → SIO3 D4
XSPIM_P2_IO4 → SIO4 D5
XSPIM_P2_IO5 → SIO5 E3
XSPIM_P2_IO6 → SIO6 E2
XSPIM_P2_IO7 → SIO7 E1

RESET_OUT → RESET A4

VCC B4
VCCQ D1
VCCQ E4
GND B3
VSSQ C1
VSSQ E5
ECS A5

DNU B1
DNU B5
NC A2
NC A3
NC C5

+1V8 — C72 100n, C73 4u7, C74 100n, C75 4u7, C76 100n, C77 4u7 — GND
+1V8 — R24 10K — GND

OCTOSPI Impedance Constraint: Min = 45.00, Max = 55.00

DQS0 with IO0..7 (Byte0), and CLK, all in 50 mils
NCS length can be in the range of up to CLK length +/− 750 mils

Title: EEZ BB3+ STM32H7 CM5 module

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