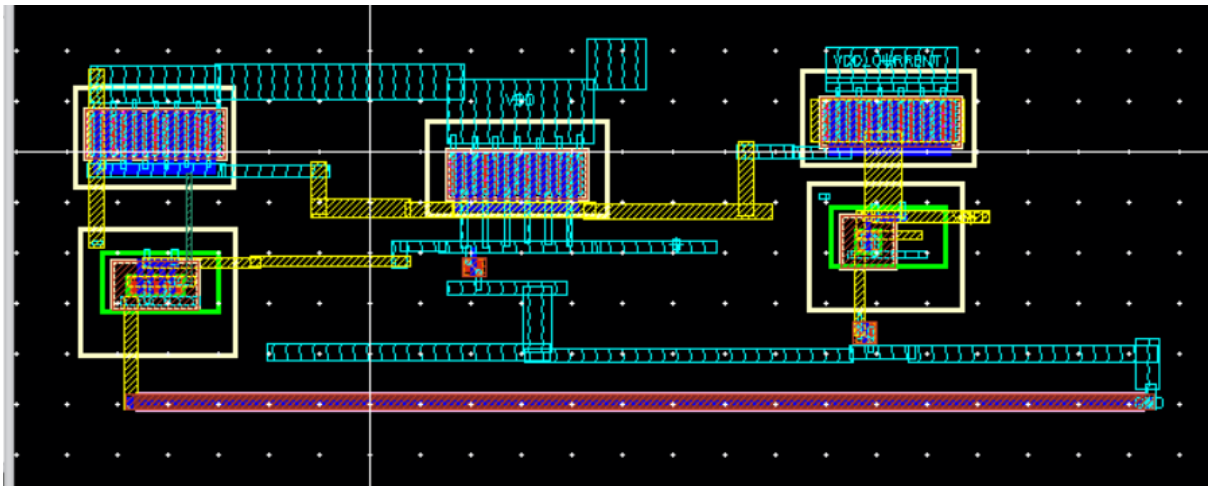
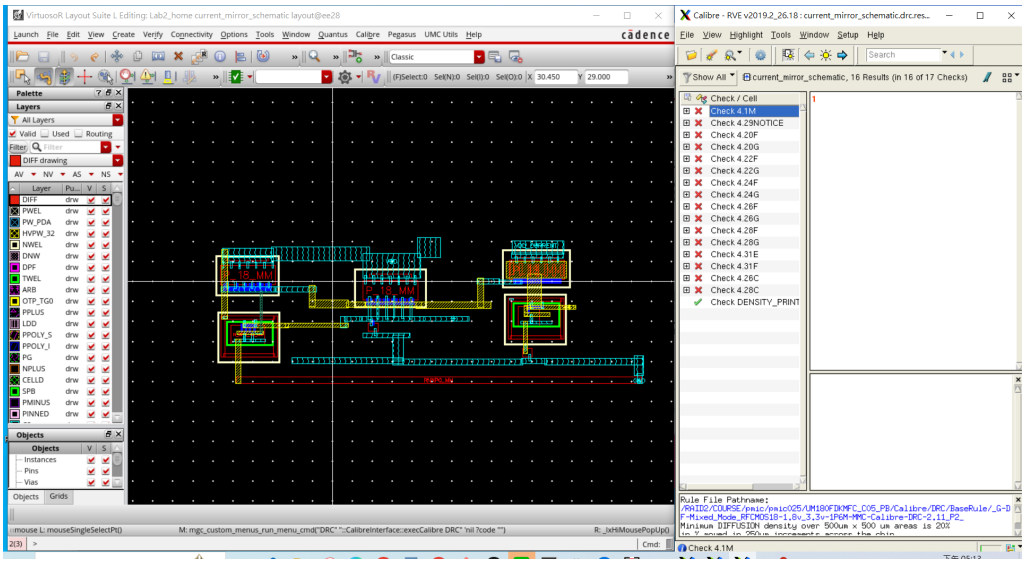
parameters	Target spec		Pre-sim	Post-sim
VREF	1.2V (+/- 1%) @ VDD=1.8V	Value (V)	1.1952	1.1951
		Error (%)	-0.4%	-0.41%
VREF	1.2V (+/- 1%) @ VDD=1.7V-1.9V	Value (V)	1.188~1.202	1.188~1.202
		Error (%)	-1%~0.2%	-1%~0.2%
IREF	10μA (+/- 1%) @ VDD=1.8V	Value (V)	9.996	9.98
		Error (%)	–0.04%	-0.4%
IREF	10μA (+/- 5%) @ VDD=1.7V-1.9V	Value (V)	9.6~10.36	9.58~10.4
		Error (%)	-4%~3.6%	-4.2%~4%
PVDD	<150uW @ VDD=1.8V	Power (uW)	53.97uW	53.89uW

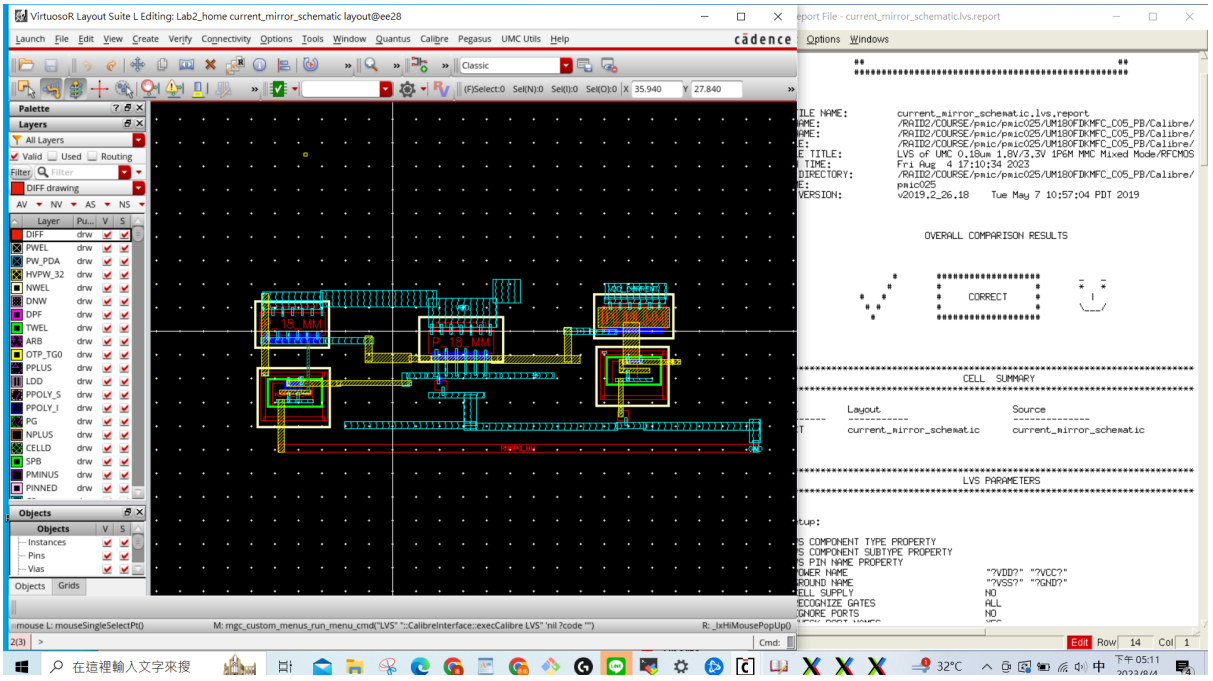
Layout圖:



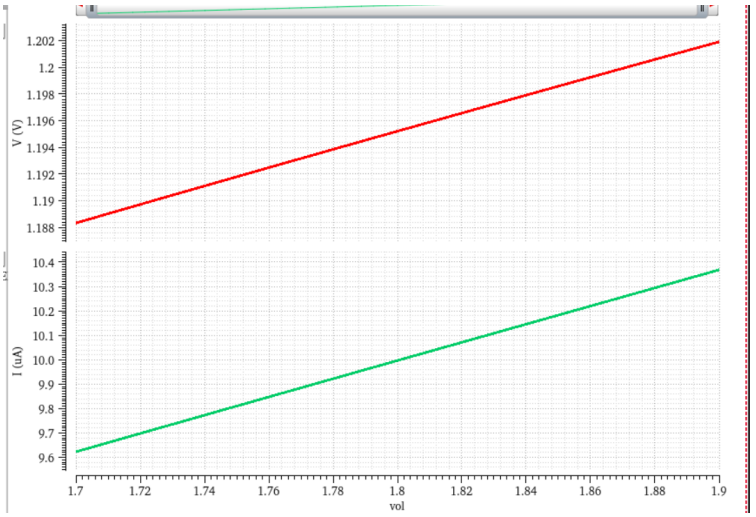
DRC圖:



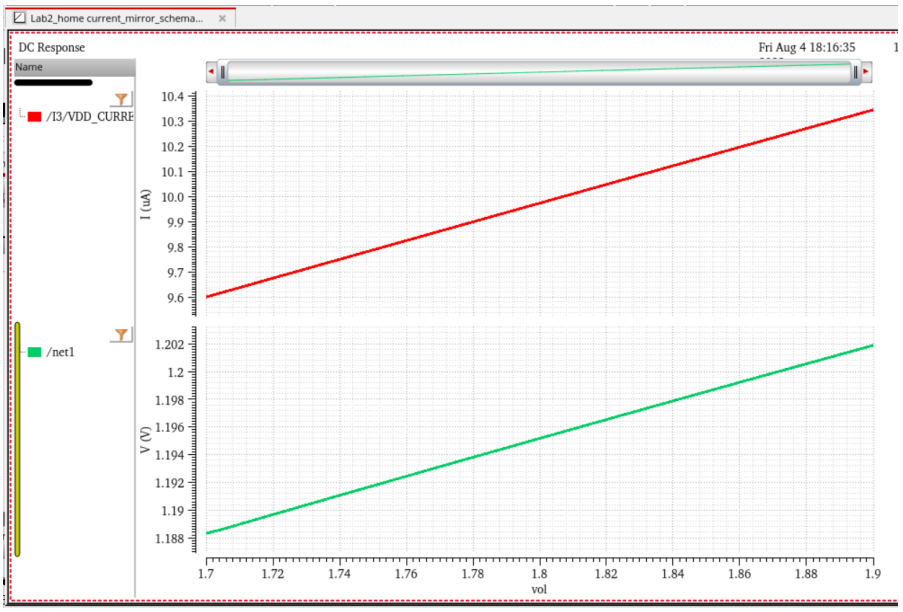
LVS圖:



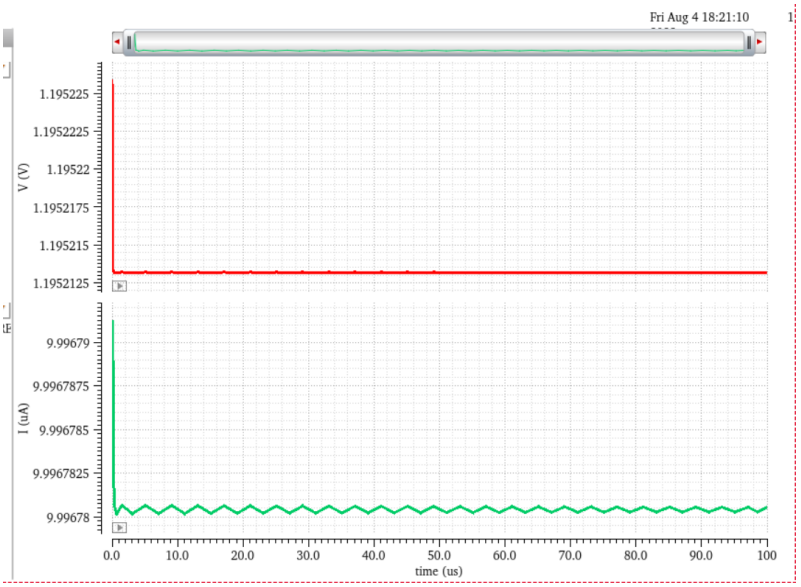
pre_sim1.7-1.9:



post_sim1.7-1.9:



pre_sim1.8:



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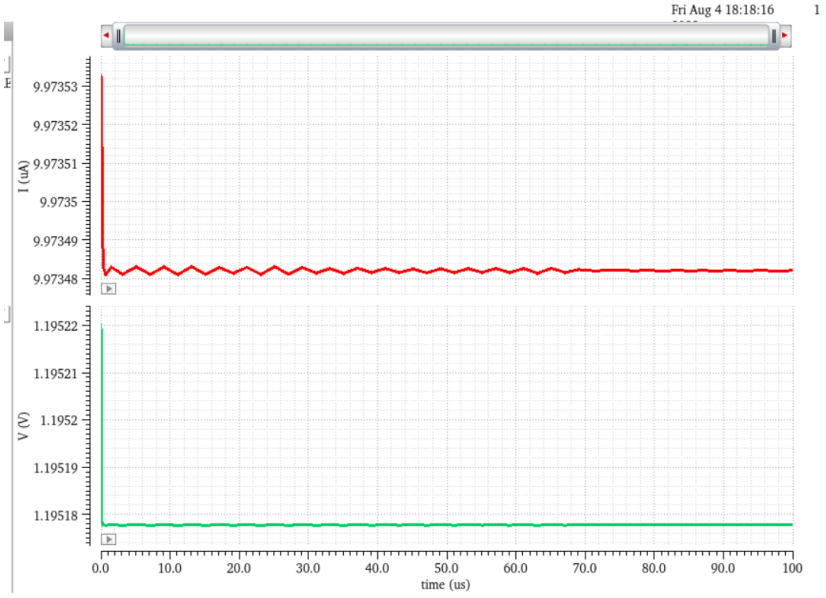
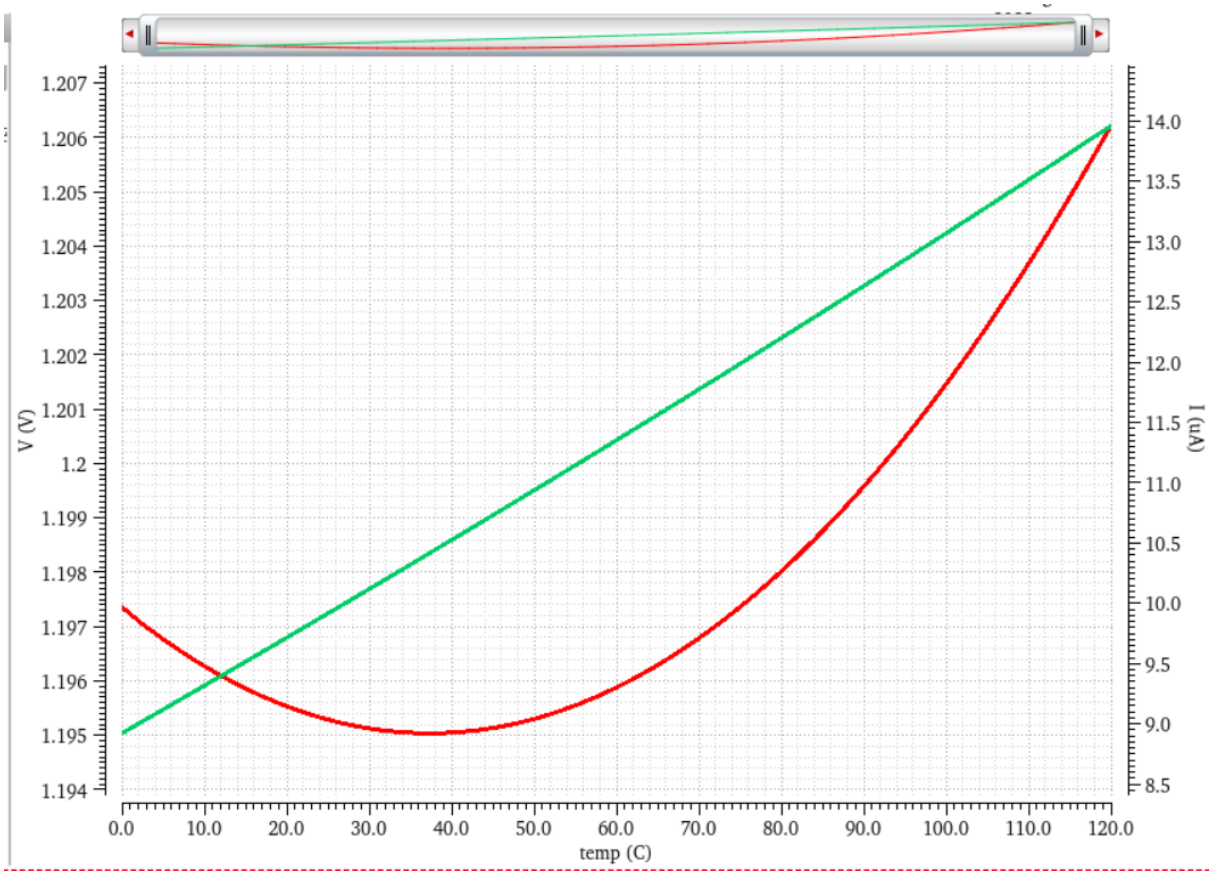
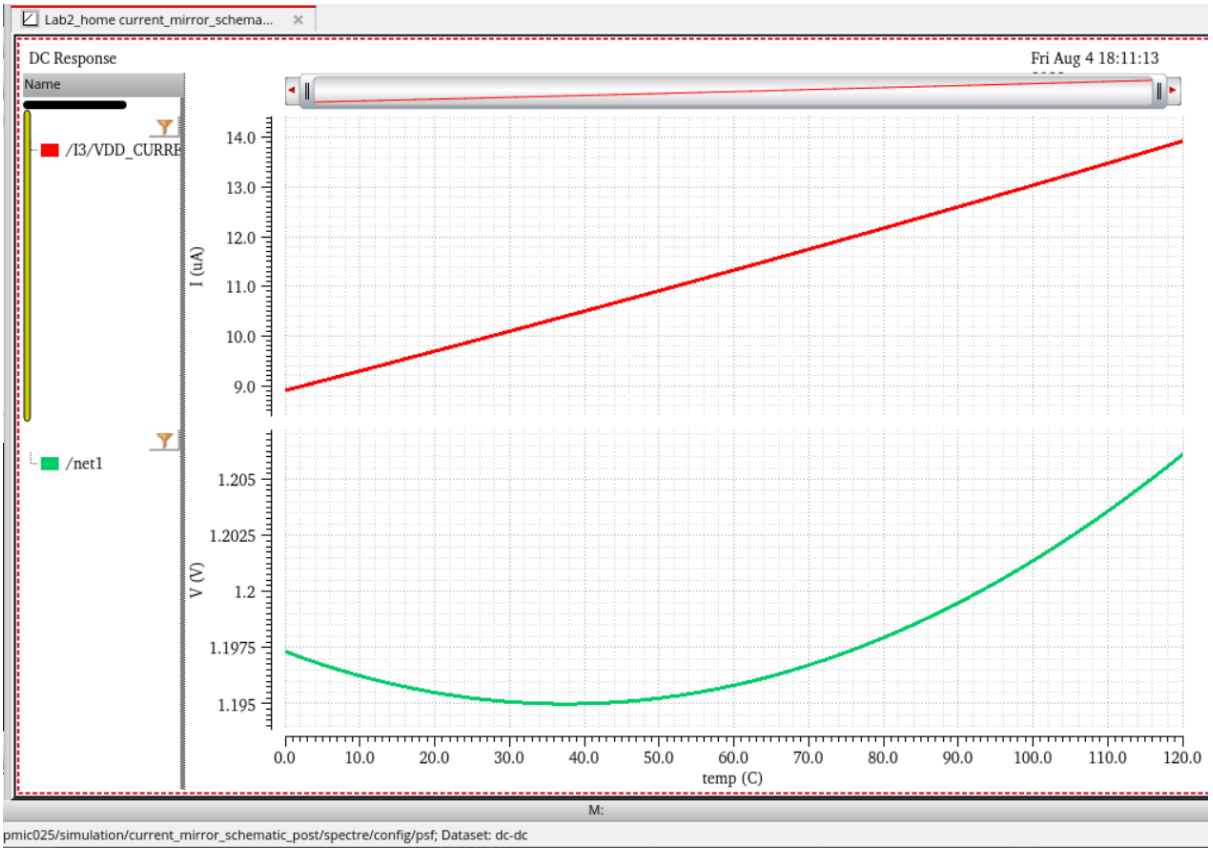


pre_sim_temp:



post_sim_temp:



問題與討論:

$$I_{REF} = \frac{2}{\mu_n C_{OX}\left(\frac{W}{L}\right)_{N2}} \frac{1}{R^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

透過右邊公式可推得電阻約為10k歐姆，但實際電路會與理論有一點誤差，所以經過微調電阻約為12.5k歐姆，可得電流10uA，M4的drain電壓約為630mv，假如M6與M7與M4一樣size，Vref大約為1.26V大於1.2V，所以M6與M7的W/L要大一點，讓電流變大Vref變小，所以經過微調M6與M7的W選1.3u剛好可以讓Vref變1.2V。