

Influence of the output filter parasitic elements on the control loop in a switch-mode audio amplifier

Jeppe Hinrichs

Project Report



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January, 2021

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Cover photo: Pok Rie, 2018, with permission

Published by: Technical University of Denmark, Department of Electrical Engineering, Elektrovej, Building 325, 2800 Kgs. Lyngby Denmark
www.ele.elektro.dtu.dk

Project Period: Thursday 3rd September, 2020–Friday 22nd January, 2021

ECTS: 20

Education: Bachelor of Engineering

Field: Electrical Engineering

Approval

This report has been prepared over one semester at the Department of Electrical Engineering in the Technical University of Denmark, DTU, in partial fulfilment for the degree Bachelor of Engineering in Electrical Engineering, BEng (E.E.)

It is assumed that the reader has a basic knowledge in the areas of electrical engineering and circuit analysis.

Jeppe Hinrichs - s163555

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Signature

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Date

Abstract

Class-D amplifiers are commonly used in audio amplifications to achieve a highly efficient power amplification stage. The topic of this project is to investigate the parasitic elements of the output filter and its effects on the system. In transient states of a switch-mode audio amplifier and the complementary filtering stage, aliasing can be introduced. When this aliasing is fed back through the regulator loop it becomes part of the input signal. The consequence of this can be that the amplified output signal has a significant component of the introduced aliasing signal, which can lead to distortion in the signal that is put to the loudspeaker. In order to gain a sufficient understanding of the design of a class-D audio amplifier, one will be designed and built. Afterwards, some analysis revealed a significant change in the control loop in a specific frequency band from the introduction of parasitic elements in the inductor of the output filter. Through a second synthesis calculation it was proposed to make the integrator element in the control loop more aggressive to compensate for influence of parasitic elements in a higher frequency band.

Acknowledgements

The project would not be possible without the help and resources from every project participant. I would like to thank Arnold Knott for helping me start the project, arranging the collaboration with PURIFI Audio and taking the time to help me when needed. I would also like to thank Søren Poulsen for helping me throughout the project.

Abbreviations

AC	Alternating current
AIM	Astable integration modulator
BPF	Band-pass filter
BTL	Bridge-tied load
DC	Direct current
DR	Dynamic Range
EMI	Electro-magnetic interference
ESR	Equivalent series resistance
HIGH	Logic level high
HPF	High-pass filter
IC	Integrated Circuit
KCL	Kirchoff's current law
KVL	Kirchoff's voltage law
LOW	Logic level low
LPF	Low-pass filter
LQR	Linear-quadratic regulator
MOSFET	Metal-oxide-semiconductor field-effect transistor
OP-AMP	Operational amplifier
PI	Proportional-integral regulator
PID	Proportional-integral-derivative regulator
PWM	Pulse Width Modulation
PCM	Pulse Code Modulation
RLC	Resistor-inductor-capacitor
RMS	Root-mean-square
RVS	Reduced voltage switching
SMPS	Switched-mode power supply
SNR	Signal-to-noise ratio
SPICE	Electronic circuit simulator

THD	Total harmonic distortion
THD+N	Total harmonic distortion plus noise
VCVS	Voltage Controlled Voltage Source
ZVS	Zero voltage switching

Denotation

Category	Name	Unit	Description
Preamplifier	V_{ref}	V	Reference voltage
	C_{hp}	F	High pass filter capacitor
	R_{hp}	Ω	High pass filter resistor
	f_{hp}	Hz	High pass cut-off frequency
	C_{lp}	F	Low pass filter capacitor
	R_{lp}	Ω	Low pass filter resistor
	f_{lp}	Hz	Low pass cut-off frequency
	A_v	1	Amplification factor
Modulator	R_1	Ω	AIM voltage divider resistor
	R_2	Ω	AIM voltage divider resistor
	R_{in}	Ω	AIM input resistor
	R_{fb}	Ω	AIM feedback resistor
	C_1	F	AIM capacitor
	V_{in}	V	Input signal voltage
	V_{span}	V	Voltage range of input signal
	V_{pwm}	V	PWM signal
	V_H	V	V_{pwm} high level voltage
	V_L	V	V_{pwm} low level voltage
	V_{out}	V	V_{pwm} voltage range ($V_H - V_L$)
	V_{hys}	V	Hysteresis voltage
	V_{hw}	V	Hysteresis width
	V_{th_H}	V	Hysteresis threshold upper voltage
	V_{th_L}	V	Hysteresis threshold lower voltage
	V_c	V	PWM carrier voltage
	V_{c_H}	V	PWM carrier upper voltage
	V_{c_L}	V	PWM carrier lower voltage
	f_{sw}	Hz	PWM signal frequency
Gate driver	D	1	PWM signal duty cycle
	t_H	s	PWM carrier charge time
	t_L	s	PWM carrier discharge time
	τ	1	PWM carrier charge constant
	R_{th}	Ω	PWM carrier thevenin resistance
	f_{idle}	Hz	PWM signal idle switching frequency
	k_2	1	$R_{\text{fb}}, R_{\text{in}}$ voltage divider
	D_{dt}	1	Dead-time circuit diode
	R_{dt}	Ω	Dead-time circuit resistor
	C_{dt}	F	Dead-time circuit capacitor
	V_C	V	Dead-time circuit supply voltage
	V_s	V	IC supply voltage
	t_c	s	Charging circuit time

Category	Name	Unit	Description
Power stage	V_{DD}	V	Power supply voltage
	Q_1, Q_2, Q_3, Q_4	1	Power stage switches
	V_g	V	Gate driver signal
	V_o	V	Output voltage
	I_o	A	Output current
Output filter	R_{BTL}	Ω	Speaker equivalent load resistance
	R_f	Ω	Output filter single-ended load
	C_{BTL}	F	Output filter differential capacitance
	C_f	F	Output filter single-ended capacitance
	L_f	H	Output filter inductance
	ΔI_L	A	Output filter ripple current
	Q	1	Output filter quality factor
	f_c	Hz	Output filter cut-off frequency
	ω_n	rad s^{-1}	Output filter natural frequency
Shunt regulator	ζ	1	Output filter damping ratio
	R_{sh}	Ω	Shunt current limiting resistor
	I_K	A	Shunt cathode current
	$I_{K_{\max}}$	A	Shunt maximum cathode current
	$I_{K_{\min}}$	A	Shunt minimum cathode current
	I_{su}	A	Shunt supply current
	R_{A1}	Ω	Shunt adjust resistor 1
	R_{A2}	Ω	Shunt adjust resistor 2
	C_L	F	Shunt load capacitance
	$V_{\text{ref}_{\text{IC}}}$	V	Shunt internal reference voltage

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Chapter 1: Introduction

This section of the report will explain to the reader how to reference this document and explain the fundamental structure of the project as well as the report.

1.1 Reading comprehension

Throughout the report, the reader will be assumed to be knowledgeable of basic circuit analysis and familiar with standard abbreviations typically used in electrical engineering. If not, readers can refer to the denotation section at the beginning of the report.

Please refer to Abbreviation page and Denotation page for abbreviations and variable names found within the report.

Furthermore, as a notation convention, large-signal DC quantities are denoted by uppercase letters with uppercase subscripts. Small-signal quantities are denoted using lowercase letters with lowercase subscripts. Quantities composed of both large-signal and small-signal elements are denoted using lowercase letters and uppercase subscripts.

1.1.1 Sources

Calculus expressions present in the report will typically have a reference explaining their origin. All references are prominently displayed with square brackets and a number, directing to the appendix in the last section of the report.

1.1.2 Report structure

The report is divided into five chapters, where the first part is an introduction to the project. The second chapter will focus on explaining the theory of a class-D amplifier with its modulation schemes and output filter. The third chapter focuses on the synthesis of a PCB to test. The fourth chapter explains the production of the hardware. The fifth chapter will explain the testing methodology performed on the hardware. Finally, the documentation of testing and diagrams of laboratory setups can be found in the appendix.

1.2 Project description

In the following report, an analysis of a class-D amplifier module is documented. The work is conducted in the Department of Electrical Engineering at the Technical University of Denmark.

An audio amplifier is a device that amplifies low-power audio signals within the audio spectrum perceptible to the human hearing to a level suitable for loudspeakers. It is typically the second last stage in an audio playback chain. While the input signal to an audio amplifier measures a low power, the output of the amplifier typically measures a high power delivery to the load, in this case, a loudspeaker. The output power of the amplifier depends on several key factors, characteristics of the output stage, heat dissipation, and parasitic elements among others.

A class-D audio amplifier is a typology of audio amplifiers that utilizes transistors as switches instead of gain devices as in other amplifier systems. As the transistors are operating non-linearly, the input signal is converted into a stream of pulses that resemble the input signal through a pulse-width modulation scheme. The time-averaged power of the modulated pulses is directly proportional to the input signal, so after amplification, the signal can be converted back into an analog signal through a passive low-pass filter. The purpose of this filter is to reduce high-frequency components in the amplified signal and thereby restore the audible spectrum frequency signal.

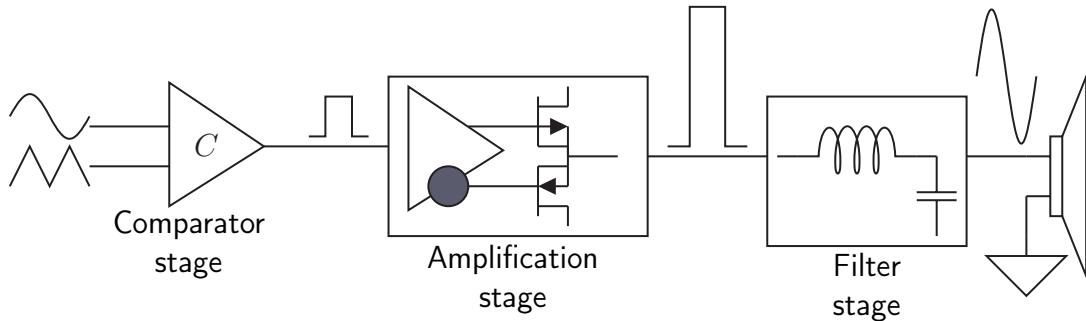


Figure 1.1: Block diagram of basic class-D amplifier topology.

See Figure 1.1 for a block diagram overview of a class-D amplifier system with waveform illustrations. The primary benefit of the class-D topology is an increased power efficiency as the maximum theoretical power efficiency for class-D amplifiers are near 100%, whereas Class-A- and Class-B amplifiers maximum theoretical power efficiency is 25% and 78.5%, respectively.

The design process in this project will be based on previous work by [14], [21]. These two works explored using LQR in a control loop and minimizing the generated noise within the circuit from that implementation. The result was a circuit design that was implemented in-house within the DTU laboratory that is documented through an iterative design process.

1.3 Project scope

As this project deals with a synthesis of a peculiar design and an analytical examination of a class-D system, this initial design will determine the specific direction of the qualitative analysis. The project is focused on the output stage of the system. Therefore analysis will comprise of distinctive variations of parasitic element combinations in the chosen output filter topology.

1.3.1 Learning objectives

See below for an outline of the project activities

Project specification

- Learn a class-D amplifier topology, calculate component values
 - Understand and design a self-oscillating modulator amplifier
 - Investigate and test open loop output filter
 - Investigate and test closed loop output filter
 - Investigate output filter parasitic elements affects control loop
 - Make quantifiable performance measurements on system
 - Write a technical report documenting the project work
-

Table 1.1: Project specification table

Chapter 2: Theory

2.1 Amplifier model

Before the optimisation phase of the project can begin, we must synthesise a reasonable model of the class-D amplifier topology. As mentioned in the previous chapter, this project is dealing with a switched-mode audio amplifier and therefore it differs from controlled conduction angle amplifiers by operating power stage devices as switches. In the aforementioned amplifiers, the power stage is designed to operate somewhere between the ON and OFF state and defined by the length of their conductive regions to control the output. As the devices are operated with voltage drops and current throughput there are significant losses limiting the efficiency of the output stage. Generally, these amplifiers, for a similar audio application as this project, are implemented with as class-AB stages, which are a blend of class-A and class-B operation.

In a class-A power stage, both transistors are always conducting quiescent current, even under no input amplitude, with low efficiency. With a class-B power stage, there is an alternating complimentary current conducted with zero quiescent currents, resulting in a higher efficiency but with audible cross-over distortion due to dead-band present in the transistors non-linear regions. With the class-AB power stage, a bias voltage is placed on the class-B amplifier power stage input thereby linearising the devices and eliminating cross-over distortion, however, a quiescent current will be conducted, resulting in a lower efficiency than a pure class-B stage. However, a class-D topology is used in this project. Further documentation of the model will explain the functions of each stage in the amplifier.

A simplified block diagram of the system is seen the diagram below.

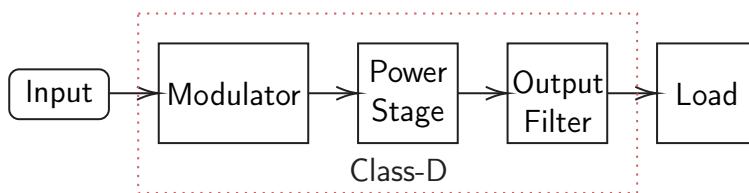


Figure 2.1: Most basic block diagram of a class-D system

The most basic block diagram of a class-D system can be seen in Figure 2.1. This is not in practical use, as the system lacks a feedback loop. The power stage is directly proportional to the supply level to feed a low impedance directly to the load. Therefore, any disturbances in the supply will directly degrade the output. This is why a control loop is typically connected from the output of the amplifier going to the input of the amplifier [3].

In this project, a system will be implemented corresponding to the block diagram below. As seen in Figure 2.2 the input signal will go directly into an input filter and preamp. This block consists of a subcircuit with a filter combined with a pre-amp and level-shifting

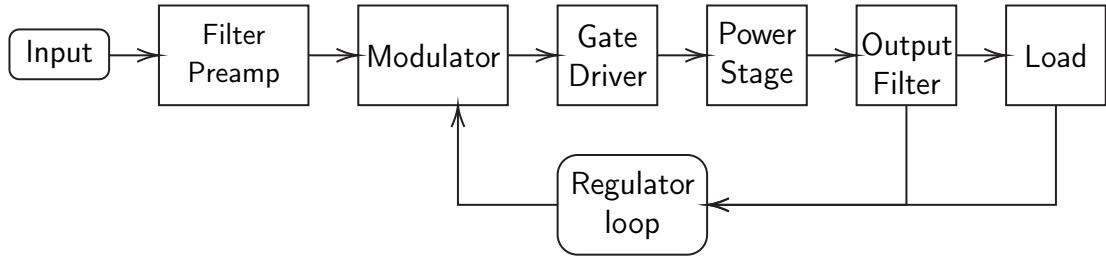


Figure 2.2: Overview block diagram of class-D circuit

circuit combined in one. This block takes an unbalanced line-level signal from an audio source and filters undesirable frequencies out of the input signal and level-level shifts it to a desired operating point in the centre of the supply voltage DR.

In the second stage, the filtered and shifted signal enters the modulator, where it will be converted to a logic-level pulse-train modulated in a PWM scheme (a binary representation of the audio). This logic-level signal is sent to the gate driver circuit that controls the power stage. At the power stage, the logic-level signal is amplified to a high-amplitude signal through the switching operation.

After the power stage, the high-amplitude binary signal is sent through the output filter, which converts the modulated pulse-train back to its original form. In practice, this is done by a low-pass filter which removes the high-frequency components of the PWM signal and leaves an amplified version of the original input signal to pass to the load (in this application, a speaker).

In this design, a control loop (or regulator loop) is connected from the output stage and load and back to the modulator stage to control the amplification of the system using feedback.

2.2 Preamplifier and Input Filter

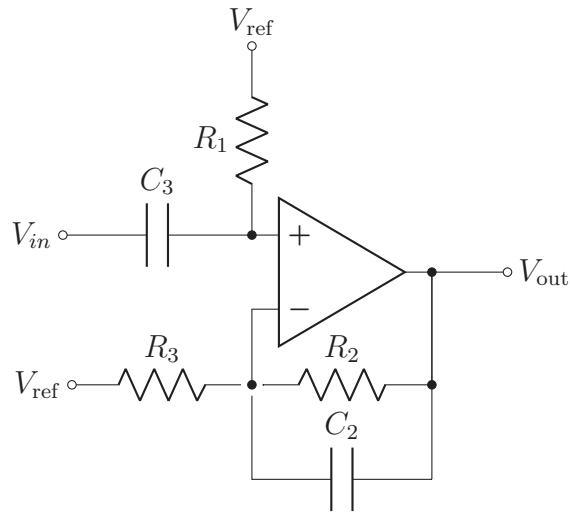


Figure 2.3: Part-schematic of Filter and input preamp

The part-schematic for the input filter can be seen in Figure 2.3 and is used to attenuate undesired frequencies outside the audio frequency range. Fundamentally, it is a non-inverting amplifier coupling with some added filters. There is also a DC bias point V_{ref}

which will operate the audio output of the preamplifier to a bias point of V_{ref} . The input capacitor C_1 is intentionally used for blocking any DC component on the input prior to the level-shift. In a practical sense, this sub-circuit works as a band-pass filter with a high-pass filter (C_1, R_1) on the positive input and a low-pass filter (C_2, R_2) on the negative input of the operational amplifier. The fundamental equations for each cut-off in the part-filter can be seen in Equation 2.1.

$$f_{hp} = \frac{1}{2\pi \cdot R_1 C_1} \quad (2.1a)$$

$$f_{lp} = \frac{1}{2\pi \cdot R_2 C_2} \quad (2.1b)$$

With the amplification factor given by the voltage divider in the feedback network as Equation 2.2.

$$A_v = 1 + \frac{R_2}{R_3} \quad (2.2)$$

2.3 Modulator

The modulator in a class-D amplifier is the module that converts the continuous audio signal to a rail level discrete pulse coded signal. Generally, using pulse coded signals a PWM method is utilised. The audio input is coded into a PWM signal by comparison of a triangle-shaped carrier waveform. A comparator will set the output to HIGH when the audio signal has a higher potential than the carrier waveform and a LOW will be set on the output when the audio signal is lower than the carrier waveform. The portion of time where the modulator has a high output to a single period is called the DUTY cycle. Referring to Figure 2.4, the modulator comparator is connected to its input signal

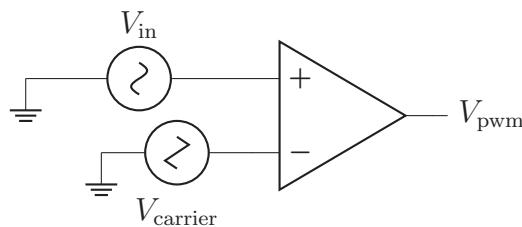


Figure 2.4: Simple comparator modulator

sinusoidal signal on its positive terminal and the carrier signal on the negative terminal, providing a PWM signal on the output with a fixed PWM frequency. This standard configuration entails an open-loop system and no error-correction. Furthermore, the fixed frequency can increase EMI in the circuit [9].

Seen in Figure 2.5 is a typical PWM operation. The input and carrier waveform is compared to give a PWM output as described in Figure 2.4 according to Listing E.1 and fig. E.1.

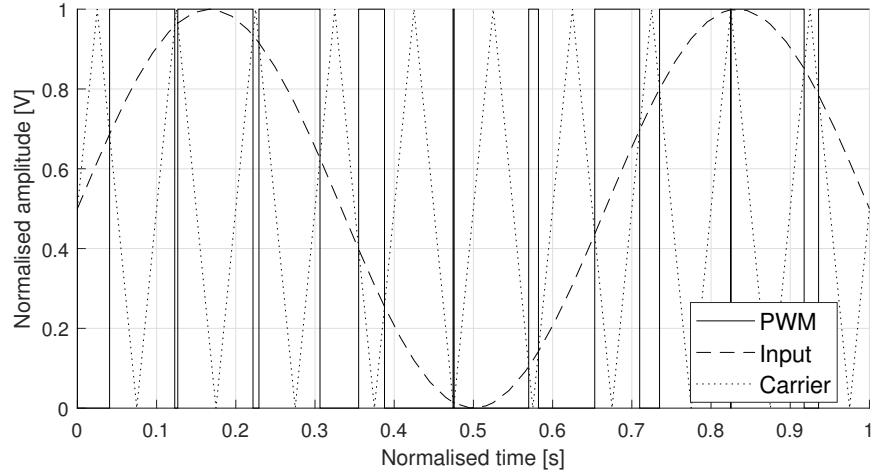


Figure 2.5: Typical PWM modulation scheme example

It is chosen to utilise a self-oscillating modulation scheme for this project. This modulation scheme is different as it does not require an externally clocked carrier waveform to modulate the digital pulses on the comparator sub-circuit. Instead, the reference signal is added together with the feedback signal and fed into a hysteretic comparator. For this system, the AIM design is based on the article [12].

2.3.1 Astable Integrating Modulator

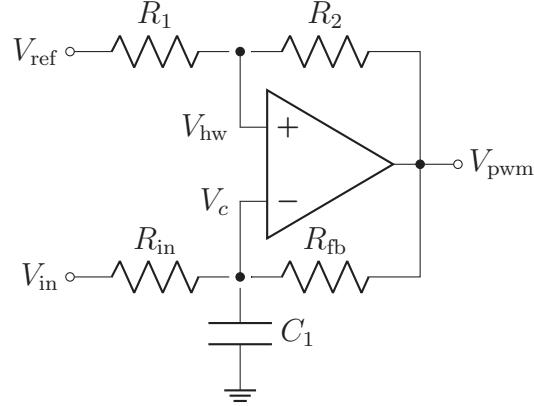


Figure 2.6: Part-schematic of modulator

The part-schematic for the AIM sub-circuit can be seen in Figure 2.6. Other than the OP-AMP, the sub-circuit consists of a voltage divider (R_1 and R_2) and a charging circuit with R_{in} , R_{fb} and C_1 . V_{in} represents the continuous audio signal from the pre-amplifier and filter. V_{ref} is a reference voltage. V_{pwm} represents the modulated output signal. This system fundamentally works by employing a filter on the output to generate the carrier waveform in a feedback configuration [12]. The system is operated in a perpetual self-oscillating state by intentionally introducing a hysteresis window or a 180° phase shift in the feedback network [4], [5]. Since the feedback network results in a variable switching frequency, which infers a reduction in EMI [9]. In this project derived equations from [12], [14], [23] will be used.

The PWM signal V_{pwm} has the two states HIGH (V_H) and LOW (V_L), both of which are

defined in the expressions below.

$$V_H = V_{\text{ref}} + \frac{V_{\text{out}}}{2} \quad (2.3a)$$

$$V_L = V_{\text{ref}} - \frac{V_{\text{out}}}{2} \quad (2.3b)$$

Where V_{ref} is the reference voltage and $V_{\text{out}} = (V_H - V_L)$ is the output voltage span of V_{pwm} .

Additionally, the hysteresis window has threshold voltages V_{th_H} (upper) and V_{th_L} (lower) described as:

$$V_{\text{th}_H} = V_{\text{hw}} \cdot \frac{V_H - V_{\text{ref}}}{V_H - V_L} + V_{\text{ref}} \quad (2.4a)$$

$$V_{\text{th}_L} = V_{\text{hw}} \cdot \frac{V_L - V_{\text{ref}}}{V_H - V_L} + V_{\text{ref}} \quad (2.4b)$$

Where V_{hw} is the hysteresis window width.

The switching frequency f_{sw} of output signal V_{pwm} is expressed by:

$$f_{\text{sw}} = \frac{1}{t_{\text{high}} + t_{\text{low}}} = \frac{1}{-C \cdot R_t \cdot \ln \left(\frac{(V_{\text{hw}} - 2V_{\text{th}_H})(2V_{\text{th}_L} + V_{\text{hw}})}{(V_{\text{hw}} - 2V_{\text{th}_L})(2V_{\text{th}_H} + V_{\text{hw}})} \right)} \quad (2.5)$$

And DUTY cycle given by:

$$D = \frac{t_{\text{high}}}{t_{\text{high}} + t_{\text{low}}} = \frac{\ln \left(\frac{2V_{\text{th}_H} - V_{\text{hw}}}{2V_{\text{th}_H} - V_{\text{hw}}} \right)}{\ln \left(\frac{(V_{\text{hw}} - 2V_{\text{th}_H})(2V_{\text{th}_L} + V_{\text{hw}})}{(V_{\text{hw}} - 2V_{\text{th}_L})(2V_{\text{th}_H} + V_{\text{hw}})} \right)} \quad (2.6)$$

The timing variables t_{high} and t_{low} are expressed by the following:

$$t_{\text{high}} = \tau \cdot \ln \left(\frac{V_{c_H} - V_{\text{th}_L}}{V_{c_H} - V_{\text{th}_H}} \right) \quad (2.7a)$$

$$t_{\text{low}} = -\tau \cdot \ln \left(\frac{V_{c_L} - V_{\text{th}_L}}{V_{c_L} - V_{\text{th}_H}} \right) \quad (2.7b)$$

Where carrier waveform limits V_{c_H} and V_{c_L} are given by:

$$V_{c_H} = V_{\text{in}} + \frac{V_{\text{span}} \cdot (V_H - V_{\text{in}}) + V_{\text{hw}} \cdot (V_H - V_{\text{in}})}{V_H - V_L + V_{\text{span}}} \quad (2.8a)$$

$$V_{c_L} = V_{\text{in}} + \frac{V_{\text{span}} \cdot (V_L - V_{\text{in}}) + V_{\text{hw}} \cdot (V_L - V_{\text{in}})}{V_H - V_L + V_{\text{span}}} \quad (2.8b)$$

Where V_{span} is the input voltage range of V_{in}

The time constant τ is defined by the feedback network containing R_{in} , R_{fb} and C_1 and is given by:

$$\tau = R_t \cdot C_1 \quad (2.9)$$

Where R_t is the Thevenin resistance of the feedback network.

To determine the Thevenin resistance the circuit is evaluated with no input, at $V_{\text{in}} = V_{\text{ref}}$. That means the self-oscillating switching frequency becomes the idle frequency f_{idle} . Then the expression for the Thevenin resistance becomes:

$$R_t = \frac{1}{f_{\text{idle}} C_1 \ln \left(\frac{(V_{c_H} - V_{\text{th},L})(V_{c_L} - V_{\text{th},H})}{(V_{c_H} - V_{\text{th},H})(V_{c_L} - V_{\text{th},L})} \right)} \quad (2.10)$$

Where V_{c_H} and V_{c_L} are carrier waveform limits found in Equation 2.8. The expressions for R_{in} and R_{fb} are desired. The Thevenin resistance is expressed by a parallel connection of the following:

$$R_t = R_{\text{in}} \parallel R_{\text{fb}} = \frac{R_{\text{in}} \cdot R_{\text{fb}}}{R_{\text{in}} + R_{\text{fb}}} \quad (2.11)$$

The k_2 of R_{in} and R_{fb} voltage divider can be described as:

$$k_2 = \frac{V_{c_H} - V_{c_L}}{V_H - V_L} = \frac{V_{c_H} - V_{c_L}}{V_{\text{out}}} \quad (2.12)$$

By inserting from Equation 2.8 into Equation 2.12 and simplifying the expression becomes Equation 2.13, the derived expression becomes Equations (2.14a) and (2.14b).

$$k_2 = \frac{V_{\text{span}} + V_{\text{hw}}}{V_{\text{span}} + V_{\text{out}}} = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{fb}}} \implies \quad (2.13)$$

$$R_{\text{fb}} = R_t \cdot \frac{V_{\text{span}} + V_{\text{out}}}{V_{\text{span}} + V_{\text{hw}}} \quad (2.14a)$$

$$R_{\text{in}} = \frac{R_{\text{fb}} \cdot R_t}{R_{\text{fb}} - R_t} \quad (2.14b)$$

Where the hysteresis V_{hw} is expressed by the voltage divider in R_1 and R_2 :

$$V_{\text{hw}} = \frac{R_1}{R_1 + R_2} \cdot V_{\text{out}} \quad (2.15)$$

Finally, the two expression to determine the the two resistor values R_1 and R_2 are obtained:

$$R_1 = \frac{V_{\text{hw}}}{V_{\text{out}} - V_{\text{hw}}} \cdot R_2 \quad (2.16a)$$

$$R_2 = \left(\frac{V_{\text{out}}}{V_{\text{hw}}} - 1 \right) \cdot R_1 \quad (2.16b)$$

It is noted that in Equation 2.16 that if a resistor value is chosen, the other can be calculated.

2.4 Gate Driver

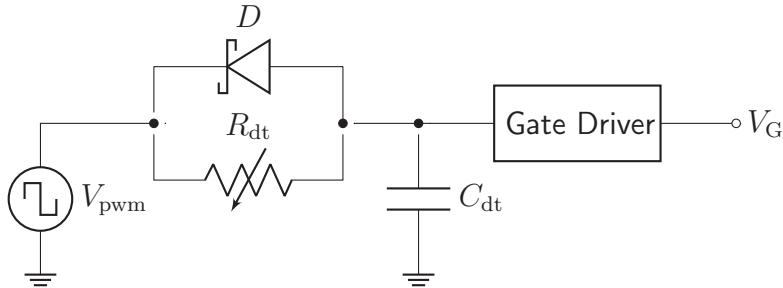


Figure 2.7: Part-schematic of the dead-time and gate driver

The gate driver subcircuit is based on a design from [21]. It is comprised of an integrated circuit from Texas Instruments, LM5113 [10] and a dead-time circuit. This subcircuit is responsible for the timing of the gate drive and ripple present in the drive signal before it reaches the power stage. The LM5113 IC has built-in bootstrap port to drive the MOSFETs HIGH [16] and two output ports, one for each gate on the half-bridge. The IC does not include a built-in dead-time circuit, which is why an external one is present. Using a variable resistor, the timing of the PWM signal can be adjusted and tuned to the desired dead-time in the HIGH and LOW side on the power stage. It consists of a simple RC-network and a Schottky diode.

The external dead-time circuit seen in Figure 2.7 on the left side leading into the gate driver. The output of the gate driver V_G is connected to the gate of the power stage switch. The voltage across the capacitor C_{dt} is equal to the input voltage of the gate drive IC and is described by:

$$V_C = V_{\text{pwm}} \cdot e^{-\frac{t}{R_{dt}C_{dt}}} \quad (2.17)$$

When V_C in Equation 2.17 reaches the threshold voltage of the gate driver input, the output V_G will switch to a HIGH state. Effectively, controlling the charge time of the capacitor means adjusting the time it takes for the gate driver to flip state.

2.5 Power Stage

In the power stage, the PWM signal needs to be amplified to deliver significantly more power to the load. This is achieved by feeding the PWM signal to drive complementary transistor pairs. The power stage can be configured either as a half-bridge or full-bridge. The choice on design here is application dependent. The load, a loudspeaker in this application, requires a voltage signal symmetric around the reference voltage.

Referring to Figure 2.8(a), it is noted that applying a half-bridge power stage would require a dual-supply configuration with both positive and negative voltage rails. The half-bridge needs only two switching devices compared to a full-bridge seen in Figure 2.8(b), which needs four. Inherently, the switching losses in a full-bridge configuration are more significant due to there being more switching devices [14], although it has better common-mode rejection [6]. Furthermore, delivering two supply rails to a half-bridge

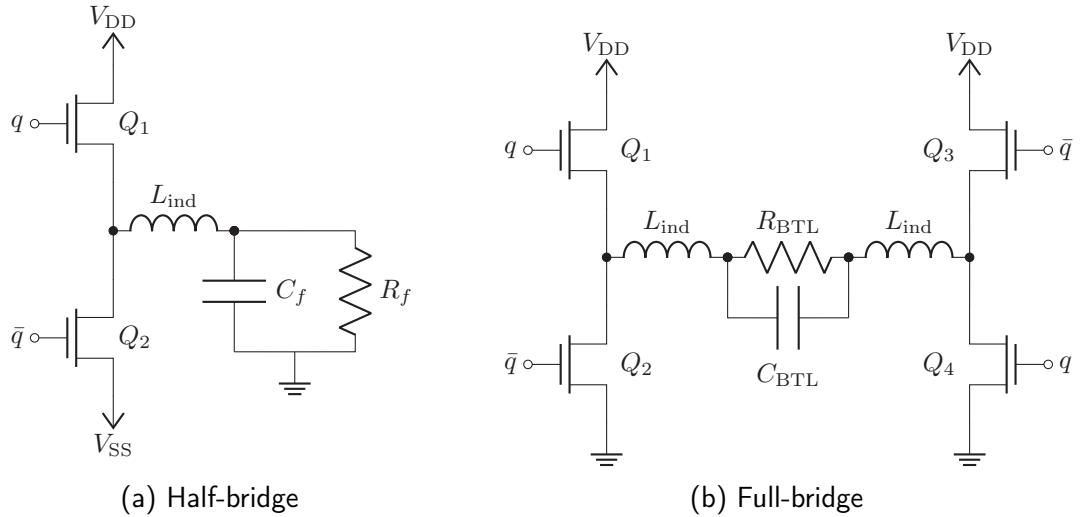


Figure 2.8: Bridge configurations for power stage and output filter

configuration can be more impractical than one supply voltage. Especially in a battery powered application. Therefore, a full-bridge is used in this system. In the full-bridge power stage, the four switches are controlled by the gate signal q and its complimentary signal \bar{q} . The system contains states depending on the value of q . In the first state, the switch pair Q_1 and Q_4 conducts a current from the left side supply V_{DD} to the right side ground terminal. In the other state, the switch pair Q_2 and Q_3 conducts a current from the right side supply V_{DD} to the left side ground terminal.

The current flow is marked on the dashed line in Figure 2.9 by the two red dashed arrows.

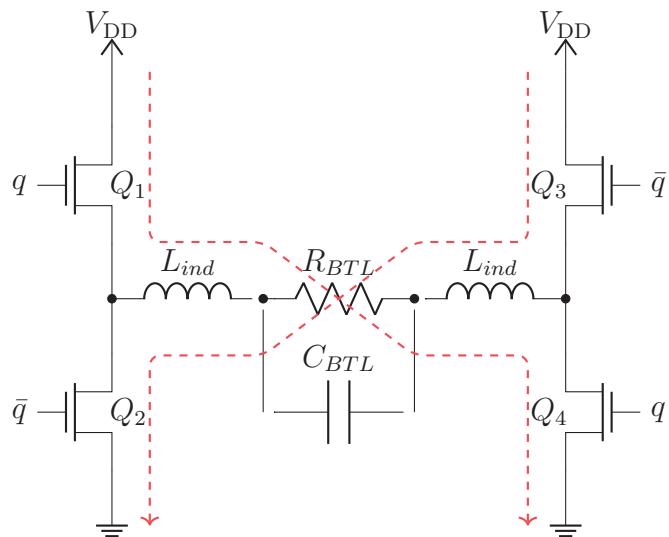


Figure 2.9: Full-bridge power stage with current flow

Across the load R_{BTL} , the output voltage V_{out} is found by Equation 2.18.

$$V_{\text{out}} = (2D - 1) \cdot V_{\text{DD}} \quad (2.18)$$

And output current determined by Ohms law. Rewriting by inserting Equation 2.18 in Equation 2.19.

$$I_{\text{out}} = \frac{V_{\text{out}}}{R_{\text{BTL}}} = \frac{(2D - 1) \cdot V_{\text{DD}}}{R_{\text{BTL}}} \quad (2.19)$$

2.6 Output Filter

The purpose of the output filter is to dampen the high-frequency components of the square-wave shaped signal from the power stage to convert the output signal back to its original sinusoidal shape. Most commonly the output filter on class-D audio amplifiers are implemented as a second order low-pass filter as an RLC configuration. The output filter topology depends on the preceding output stage design. If the power stage is a half-bridge, the output filter becomes single-ended. If the power stage is a full-bridge, it will be a differential filter. Typically, the filter is designed as a single-ended filter and then converted using transformation equations [14].

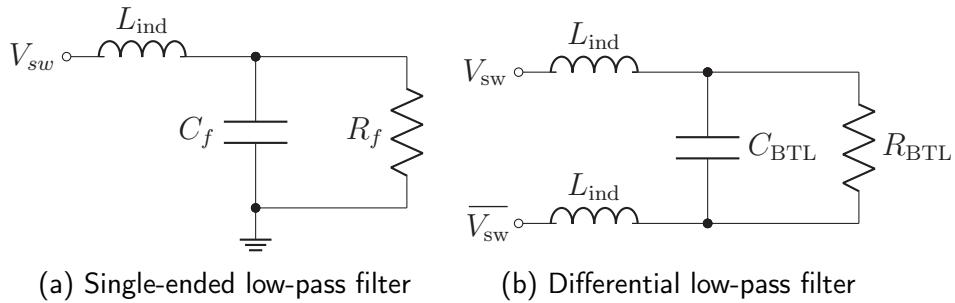


Figure 2.10: Comparison of single-ended and differential type low-pass filter

The single-ended filter can be seen in Figure 2.10(a) and the differential filter can be seen in Figure 2.10(b). V_{sw} is the input of the filter. Using [6] we find the transformations in Equations (2.20a) to (2.20c).

$$L_{\text{ind}} = L_{\text{ind}} \quad (2.20a)$$

$$C_{\text{BTL}} = \frac{C_f}{2} \quad (2.20b)$$

$$R_{\text{BTL}} = 2R_f \quad (2.20c)$$

Where L_{ind} and C_f/C_{BTL} are filter components. R_f and R_{BTL} are crude resistive representations of the load (i.e. loudspeaker). The transfer function can be found by Equation 2.21 [14].

$$H_{\text{LPF}} = \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{\frac{1}{C_f L_{\text{ind}}}}{s^2 + \frac{1}{C_f R_f} s + \frac{1}{C_f R_f}} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.21)$$

Where ω_n is the natural frequency in rad s^{-1} , ζ is the damping ratio and s is the complex frequency variable. In the filter design, selecting a high natural frequency is desirable for a high bandwidth. On the other hand, too high bandwidth leads to insufficient

attenuation of the PWM pulse. Thus, a middle ground must be selected with reasonable bandwidth and satisfactory high-frequency attenuation. The damping ratio is typically chosen somewhere in the region of $\zeta = 0.707$ due to its similarity of a Butterworth filter. A Butterworth characteristic is a maximally flat gain in the pass-band which means low amplitude distortion in the frequency spectrum.

The quality factor Q of the system and its relation to the damping ratio are as described as:

$$Q = \frac{1}{2\zeta} \quad (2.22)$$

When a value for Q is attained, the output filter values can be calculated. This is achieved by first converting the full-bridge load R_{BTL} to a single-ended load R_f from Equation (2.20c) rewriting it to:

$$R_f = \frac{R_{BTL}}{2} \quad (2.23)$$

Next the reactive single-ended filter elements can be calculated by:

$$L_{ind} = \frac{R_f}{2\pi Q f_c} \quad (2.24a)$$

$$C_f = \frac{Q}{2\pi f_c R_f} \quad (2.24b)$$

Finally, the single-ended capacitor C_f must then be transformed back into the differential capacitor C_{BTL} using a rewritten Equation (2.20b) that naturally becomes Equation 2.25.

$$C_{BTL} = \frac{C_f}{2} \quad (2.25)$$

2.7 Reduced Voltage Switching

To decrease switching losses in the power stage, it is beneficial to achieve reduced voltage switching and zero voltage switching by ensuring the inductance of the output filter can charge and discharge the power stage during the dead-time period. Functionally, this decreases the required voltage across the MOSFETs before they are turned on and thereby decreasing switching losses in the power stage.

As seen in Figure 2.11 there are various parasitic components embedded within the construction of a MOSFET device. As the parasitic components contribute to various types of losses within each switching cycle, we categorise them into four: switching loss, conduction loss, diode loss, and gate losses. The switching losses occurs every time a transient state is initiated (every turn-off and turn-on cycle) and is described by Equation 2.26 [18].

$$P_{sw} = \frac{C_{ds} v_{ds}^2 f_{sw}}{2} \quad (2.26)$$

Where C_{ds} represents the parasitic capacitance between drain and source of the MOSFET and v_{ds} is the voltage across C_{ds} . Reviewing the expression in Equation 2.26 it is identical

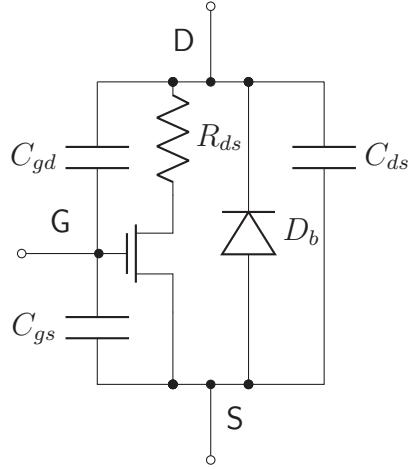


Figure 2.11: Model of MOSFET with parasitic components

to the fundamental formula for stored energy in a capacitor (although with a multiplied switching frequency variable). It is apparent the switching losses are due to the charge and discharge of the capacitive element.

As it is attempted to decrease the switching loss, the ripple current in the output filter inductor must be higher than the output current [23].

$$\Delta I_L = \frac{V_{DD}(D - D^2)}{2L_f f_{sw}} \quad (2.27)$$

Combining Equation 2.19 and Equation 2.27 the expression becomes as Equation 2.28.

$$\frac{V_{DD}(D - D^2)}{2L_f f_{sw}} > \frac{(2D - 1) \cdot V_{DD}}{R_{BTL}} \quad (2.28)$$

Rewriting the expression as the following:

$$\begin{aligned} \frac{V_{DD}(D - D^2)}{2L_f f_{sw}} &> \frac{(2D - 1) \cdot V_{DD}}{R_{BTL}} \\ \frac{\frac{V_{DD}(D - D^2)}{2L_f f_{sw}}}{\frac{(2D - 1) \cdot V_{DD}}{R_{BTL}}} &> 1 \\ \frac{V_{DD}(D - D^2)R_{BTL}}{V_{DD}(2D - 1)2L_f f_{sw}} &> 1 \quad (2.29) \\ \frac{(D - D^2)R_{BTL}}{(2D - 1)2L_f f_{sw}} &> 1 \\ \frac{R_{BTL}}{2L_f} \cdot \frac{D - D^2}{(2D - 1)f_{sw}} &> 1 \end{aligned}$$

The quality factor Q can be expressed as Equation 2.30.

$$Q = \frac{R_{BTL}}{2\pi L_f f_c} \quad (2.30)$$

Where f_c is the cut-off frequency of the output filter. Looking back to Equation 2.28 and combining with Equation 2.30 we get Equation 2.31.

$$\frac{\pi(D - D^2)Qf_c}{(2D - 1)f_{sw}} > 1 \quad (2.31)$$

Which includes the quality factor Q and therefore is dependent on this variable for determining the switching losses.

2.8 Reference Voltage

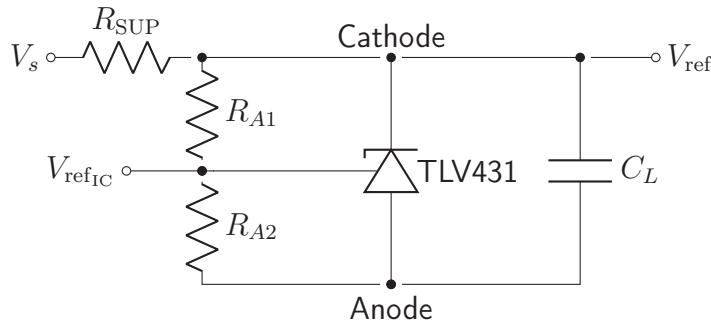


Figure 2.12: Part-schematic of the reference voltage

Since the system is operated by a single voltage rail, a reference level in the centre of the DR is required known as V_{ref} . In this system, a precision shunt regulator TLV431A [1] is used. The subcircuit can be seen in Figure 2.12. According to the datasheet of the TLV431, the maximum current on the cathode node must be between 0.1 mA to 15 mA. Therefore the R_{SUP} resistor must be scaled thereafter. V_s is the 5 V supply voltage. The output voltage V_{ref} is given by the equation in the datasheet as:

$$V_{ref} = \left(1 + \frac{R_{A1}}{R_{A2}}\right) \cdot V_{ref_{IC}} \quad (2.32)$$

2.9 Regulation and Control

The regulation of this system is based on control theory. In an amplifier system, the desired output is equal to the input multiplied by a gain factor. Any disturbance or variations should be compensated. Ordinarily, this is accomplished in systems control by adding a feedback loop between the output and the input of the system with some regulator module in between. The implementation in this project uses a PID controller loop and an LQR loop in conjunction. This was implemented in the reference design and will be preserved for this implementation.

2.9.1 Proportional-Integral-Derivative Control

This controller is a dynamic controller and is expressed in its transfer function as:

$$K_{PID} = K_p + K_i \frac{1}{s} + K_d s \quad (2.33)$$

Where K_p is the proportional gain, K_i is the integrator gain and K_d is the derivative gain coefficients. The PID controller works by error signal acquisition ($e = r - y$) where it will attempt to regulate to zero error. The error signal is occurring from a reference signal r and the output y . Each term in the transfer function Equation 2.33 produces a unique behaviour on the error signal. The K_p will consistently be an instantaneous proportional regulation to the error signal. K_i integrates a compensation over time-based on its time constant and is a slower reacting component, which eliminates steady-state errors. K_d reacts strongly on fast changes, and can also dampen overshoots based on the momentum of the slower integrator. All these components are unique in the way they affect the system in the control theory of PID controllers. In this project, only the integrator is used since it is effective at tracking the fairly low-frequent input audio waveform and reducing non-linear effects. Since this system is categorised as a switched-mode system, where there are extra noise considerations, it is preferred to abstain from applying the derivative term from the regulator. Through removing the derivative term an increase in noise performance is attained [14]. It does not eliminate high-frequent oscillations occurring through the low damping ratio (or rather a high quality factor) of the output filter imposed through a desire to decrease switching losses.

2.9.2 Linear-Quadratic Regulator

As discussed in the previous section, the high-frequent oscillation remains unaffected by the PID controller, which is why LQR loop is present in the system. The LQR is a static controller that can assign transfer function poles in an optimal manner [14]. It is based on two weight matrices. The first describes a deviation penalty in the control variables, and the second describes the acceptable control signal strength.

2.9.3 Remarks

Further exploration of LQR control theory in the family of switched-mode systems for audio applications (class-D) is outside the scope of the report. The control system will be implemented using discrete analogue components, for a most simple implementation and a fast reaction time. Since the feedback will contain a limited frequency spectrum, due to the nature of the output LPF and audible range of 20 Hz to 20 kHz, it should therefore contain a reasonable margin [15]. The synthesis chapter will explain the expressions employed to obtain the component values and were based on the reference design.

Chapter 3: Synthesis

In this chapter of the report, the theory discussed in the previous chapter will be applied to synthesise the design parameters of the class-D amplifier. The initial design parameters can be seen in Table 3.1.

Name	Value	Unit	Description
V_{sup}	5	V	Low-voltage supply
V_{DD}	30	V	Power supply
V_{ref}	2.5	V	Reference voltage
R_{BTL}	4	Ω	Bridge-tied load

Table 3.1: Initial design parameters of the amplifier

Through each section of this chapter, the methodology of calculating component values to the various sub-circuits will be explained.

3.1 Preamplifier and Input Filter

As mentioned in section 2.2 the circuit will be designed with a high-pass and a low-pass filter in mind. The result is a bandpass filter. The methodology here will be choosing a capacitor value and dimensioning the resistive component based on the expression.

Name	Value	Unit	Description
f_{hp}	10	Hz	High-pass cut-off frequency
f_{lp}	80	kHz	Low-pass cut-off frequency
C_1	1	μF	High-pass filter capacitor
C_2	1	nF	Low-pass filter capacitor
A_v	2	1	Gain

Table 3.2: Initial design parameters of the preamp and filter

As the two capacitive components are now decided, the values from Table 3.2 are now input in Equations (2.1a) and (2.1b).

$$R_1 = \frac{1}{2\pi \cdot 10 \text{ Hz} \cdot 1 \mu\text{F}} = 15.92 \text{ k}\Omega \quad (3.1a)$$

$$R_2 = \frac{1}{2\pi \cdot 80 \text{ kHz} \cdot 1 \text{ nF}} = 1.989 \text{ k}\Omega \quad (3.1b)$$

Finally, based on the decided parameter A_v , R_3 will be determined using Equation 2.2 resulting in:

$$R_3 = \frac{R_2}{A_v - 1} = \frac{1.989 \text{ k}\Omega}{2 - 1} = 1.989 \text{ k}\Omega \quad (3.2)$$

Using the synthesized values, the obtained frequency response of the preamplifier and input filter is:

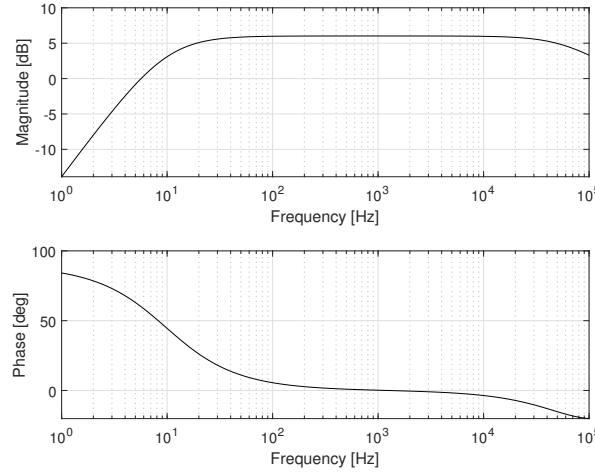


Figure 3.1: Bode plot of the designed preamplifier and input filter from a small-signal analysis

In Figure 3.1 is the bode plot with magnitude and phase. The 6 dB equal to a gain of 2 is present in the passband. The two cut-off frequencies in 10 Hz and 80 kHz respectively are also seen.

3.2 Modulator

Based on the original design of the system [14], the following parameters for the modulator are given by Table 3.3.

Name	Value	Unit	Description
V_{ref}	2.5	V	Reference voltage
V_{span}	2	V	Peak-peak maximum input voltage
V_{hw}	0.5	V	Hysteresis window
V_{out}	5	V	PWM voltage level
f_{idle}	600	kHz	Self-oscillating idle frequency
C	1.5	nF	Modulator capacitor

Table 3.3: Initial design parameters of the modulator

To determine the V_{pwm} voltage levels, Equations (2.3a) and (2.3b) are used resulting in Equations (3.3a) and (3.3b).

$$V_H = \frac{V_{\text{out}}}{2} + V_{\text{ref}} = \frac{5 \text{ V}}{2} + 2.5 \text{ V} = 5 \text{ V} \quad (3.3a)$$

$$V_L = -\frac{V_{\text{out}}}{2} + V_{\text{ref}} = -\frac{5 \text{ V}}{2} + 2.5 \text{ V} = 0 \text{ V} \quad (3.3b)$$

Then the threshold voltages V_{th_H} and V_{th_L} can be calculated from Equations (2.4a) and (2.4b) resulting in Equations (3.4a) and (3.4b).

$$V_{\text{th}_H} = V_{\text{hw}} \cdot \frac{V_H - V_{\text{ref}}}{V_H - V_L} + V_{\text{ref}} = 0.5 \text{ V} \cdot \frac{5 \text{ V} - 2.5 \text{ V}}{5 \text{ V} - 0 \text{ V}} + 2.5 \text{ V} = 2.75 \text{ V} \quad (3.4a)$$

$$V_{\text{th}_L} = V_{\text{hw}} \cdot \frac{V_L - V_{\text{ref}}}{V_H - V_L} + V_{\text{ref}} = 0.5 \text{ V} \cdot \frac{0 \text{ V} - 2.5 \text{ V}}{5 \text{ V} - 0 \text{ V}} + 2.5 \text{ V} = 2.25 \text{ V} \quad (3.4b)$$

Next the carrier waveform voltage limits are calculated from Equations (2.8a) and (2.8b) and results in Equations (3.5a) and (3.5b). Here an IDLE state is assumed, therefore $V_{\text{in}} = V_{\text{ref}}$.

$$\begin{aligned} V_{c_H} &= V_{\text{in}} + \frac{V_{\text{span}} \cdot (V_H - V_{\text{in}}) + V_{\text{hw}} \cdot (V_H - V_{\text{in}})}{V_H - V_L + V_{\text{span}}} \\ &= 2.5 \text{ V} + \frac{2 \text{ V} \cdot (5 \text{ V} - 2.5 \text{ V}) + 0.5 \text{ V} \cdot (5 \text{ V} - 2.5 \text{ V})}{5 \text{ V} - 0 \text{ V} + 2 \text{ V}} \\ &= 3.393 \text{ V} \end{aligned} \quad (3.5a)$$

$$\begin{aligned} V_{c_L} &= V_{\text{in}} + \frac{V_{\text{span}} \cdot (V_L - V_{\text{in}}) + V_{\text{hw}} \cdot (V_L - V_{\text{in}})}{V_H - V_L + V_{\text{span}}} \\ &= 2.5 \text{ V} + \frac{2 \text{ V} \cdot (0 \text{ V} - 2.5 \text{ V}) + 0.5 \text{ V} \cdot (0 \text{ V} - 2.5 \text{ V})}{5 \text{ V} - 0 \text{ V} + 2 \text{ V}} \\ &= 1.607 \text{ V} \end{aligned} \quad (3.5b)$$

The Thevenin resistance as described in Equation 2.10 results in Equation 3.6.

$$\begin{aligned} R_t &= \frac{1}{f_{\text{idle}} C_1 \ln \left(\frac{(V_{c_H} - V_{\text{th}_L})(V_{c_L} - V_{\text{th}_H})}{(V_{c_H} - V_{\text{th}_H})(V_{c_L} - V_{\text{th}_L})} \right)} \\ &= \frac{1}{600 \text{ kHz} \cdot 1.5 \text{ nF} \cdot \ln \left(\frac{(3.393 \text{ V} - 2.25 \text{ V})(1.607 \text{ V} - 2.75 \text{ V})}{(3.393 \text{ V} - 2.75 \text{ V})(1.607 \text{ V} - 2.25 \text{ V})} \right)} \\ &= 965.6 \Omega \end{aligned} \quad (3.6)$$

In Equations (2.14a) and (2.14b) the expressions for R_{in} and R_{fb} were derived. The resulting calculation becomes:

$$R_{\text{fb}} = \frac{2 \text{ V} + 5 \text{ V}}{2 \text{ V} + 0.5 \text{ V}} \cdot 965.6 \Omega = 2.704 \text{ k}\Omega \quad (3.7a)$$

$$R_{\text{in}} = \frac{2.704 \text{ k}\Omega \cdot 965.6 \Omega}{2.704 \text{ k}\Omega + 965.6 \Omega} = 1.502 \text{ k}\Omega \quad (3.7b)$$

In Equations (2.16a) and (2.16b) the expressions were obtained. It was noted that if one resistor was chosen, the other can be calculated. If value $R_2 = 20 \text{ k}\Omega$ is chosen the calculation for R_1 then becomes Equation (3.8).

$$R_1 = \frac{0.5 \text{ V}}{5 \text{ V} - 0.5 \text{ V}} \cdot 20 \text{ k}\Omega = 2.22 \text{ k}\Omega \quad (3.8)$$

The chosen $V_{hw} = 0.5$ V is a relatively minor hysteresis window in a DR of 5 V. The benefit is a more linear transfer function [14]. Implementing the calculations above, a prediction can be calculated of the behavior of the self-oscillating characteristic of the AIM modulator.

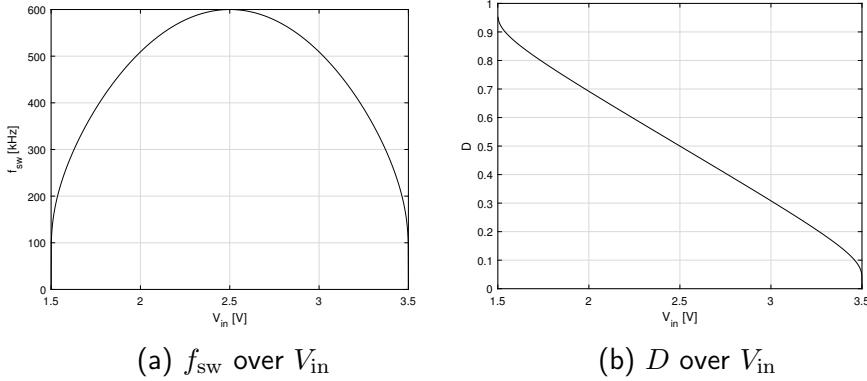


Figure 3.2: Calculated f_{sw} and D over different DC levels of V_{in}

Seen in Figure 3.2(a), the idle frequency is determined as the vertex point of the arc shape at 600 kHz. This is in agreement with the initial design specifications. There is a symmetrical roll-off when V_{in} deviates to either side within V_{span} . Looking at Figure 3.2(b), if V_{in} is outside the operating region of $V_{ref} \pm \frac{V_{span}}{2} = 2.5 \text{ V} \pm 1 \text{ V}$, the duty cycle becomes either 0 % or 100 %, resulting in modulator clipping.

3.3 Gate Driver

In the reference design, the capacitive components were specified to be 100 pF. That means the remaining unknown variable is the resistive component in the RC-network. As this is a variable resistor, it will have to be carefully tuned once the amplifier is produced.

3.4 Power Stage

In the full-bridge output configuration of the class-D amplifier, there will be a 30 V DC supply. The N-channel BSZ097N10NS5 [11] MOSFET is used as a switching device for Q_1 , Q_2 , Q_3 and Q_4 . The component is from the original design [21], and is a good fit in cost-effectiveness, and has robust specifications for this application.

3.5 Output Filter

For the output filter, the design method is also based on the previous design [21]. The output LPF cut-off frequency is designated as

$$f_n = f_c = \frac{1}{10} \cdot f_{idle} = \frac{1}{10} \cdot 600 \text{ kHz} = 60 \text{ kHz} \quad (3.9)$$

That puts its -3 dB cut-off point a decade below the modulation frequency in the spectrum and follows the convention of the previous design [14]. The initial design parameters can be seen in Table 3.4.

Name	Value	Unit	Description
f_n	60	kHz	Low-pass filter natural frequency
Q	3	1	Quality factor
R_{BTL}	4	Ω	Bridge-tied load
V_{DD}	30	V	Power supply voltage

Table 3.4: Initial design parameters of the power stage

The Q value is a chosen and somewhat arbitrary value that is required before the component selection can be initiated. Although based on previous stipulations of desired resonance, a rather high value is chosen. According to Equation 2.22, with the chosen Q factor of the filter, the damping ratio would thus become:

$$\zeta = \frac{1}{2Q} = 0.167 \quad (3.10)$$

To design the output filter and obtain its component values, the single-ended load must be determined. According to Equation (2.23), the transformation expression is:

$$R_f = \frac{4\Omega}{2} = 2\Omega \quad (3.11)$$

Now that the equivalent single-ended load is determined, the two output filter reactive elements for the single-ended configuration can be calculated. From Equations (2.24a) and (2.24b) the calculation becomes:

$$L_{ind} = \frac{2\Omega}{2\pi \cdot 3 \cdot 60 \text{ kHz}} = 1.768 \mu\text{H} \quad (3.12a)$$

$$C_f = \frac{3}{2\pi \cdot 60 \text{ kHz} \cdot 2\Omega} = 3.96 \mu\text{F} \quad (3.12b)$$

Now the single-ended capacitor C_f is transformed back into the differential capacitor C_{BTL} according to Equation 2.25 and the straightforward calculation becomes:

$$C_{BTL} = \frac{3.96 \mu\text{F}}{2} = 1.98 \mu\text{F} \quad (3.13)$$

Now the single-ended output filter components have been calculated and transformed into differential output filter components that can be applied in the circuit.

3.6 Reference Voltage

In the section explaining the theory of this subcircuit, it was specified that the cathode node current should be between 0.1 mA to 15 mA. An insufficient or excessive node current is outside the operating ranges of the shunt regulator. Therefore, a 2 mA node current is chosen. Using Ohm's law, we have:

$$R_{sup} = \frac{V_s}{I_{sup}} = \frac{5 \text{ V}}{2 \text{ mA}} = 2.5 \text{ k}\Omega \quad (3.14)$$

The reference voltage is then determined by its two resistors R_{A1} and R_{A2} in a voltage divider configuration. Referring to the theory section on this subcircuit, where $V_{\text{ref}_{\text{IC}}} = 1.24 \text{ V}$ according to the datasheet, and $R_{A1} = 4.75 \text{ k}\Omega$ is chosen, we calculate by rewriting Equation 2.32 and the calculation becomes:

$$R_{A2} = \frac{V_{\text{ref}_{\text{IC}}} \cdot R_{A1}}{V_{\text{ref}} - V_{\text{ref}_{\text{IC}}}} = \frac{1.24 \text{ V} \cdot 5 \text{ k}\Omega}{2.5 \text{ V} - 1.24 \text{ V}} = 4.92 \text{ k}\Omega \quad (3.15)$$

Now the numeric values of both resistors have been determined as $R_{A1} = 5 \text{ k}\Omega$ and $R_{A2} = 4.68 \text{ k}\Omega$. This appears logical, as the resistors are placed in a voltage divider configuration. The two resistances are practically equivalent, and as half of the supply voltage is desired it conforms well with the fundamental principles of electric circuits. In practice, they will possess an equal value. In the PCB reference notation, the components are $R_{A1} = R_4$ and $R_{A2} = R_7$.

3.7 Regulation and Control

As mentioned in the theory section of the regulation and control there are a PI controller and an LQR present in the system. The synthesis process will be explained in this section and the initial design parameters described in the table below:

Name	Value	Unit	Description
C_{BTL}	1.98	μF	Output filter capacitance
L_{ind}	1.768	μH	Output filter inductance
R_{ind}	15	$\text{m}\Omega$	Output filter shunt
R_{BTL}	4	Ω	Bridge-tied load
R_{in}	1.5	$\text{k}\Omega$	Modulator input resistance
Gain	25	1	Amplifier gain

Table 3.5: Initial design parameters of the regulator

The PI regulator is synthesised based on an initial chosen variable and hand-tuning it based on the result of the expressions. First the filter component values are transformed to single-ended, based on Equations (3.11) and (3.12b), yields:

$$R_f = 2 \Omega$$

$$C_f = 3.96 \mu\text{F}$$

Through some hand-tuning, the following coefficients were chosen for the regulator synthesis:

$$K_i = 2 \times 10^3$$

$$\text{gu} = \pi$$

And then using MATLAB R2020a with the Control System Toolbox [20], with the following state space model comprised of an input matrix B , system matrix A and output matrix C from the ODE in [14]:

$$A = \begin{bmatrix} -\frac{R_{\text{ind}}}{L_{\text{ind}}} & -\frac{1}{L_{\text{ind}}} \\ \frac{1}{C_f} & -\frac{1}{C_f \cdot R_f} \end{bmatrix} = \begin{bmatrix} -8.482E3 & -5.655E5 \\ 2.525E5 & 1.263E5 \end{bmatrix} \quad (3.16a)$$

$$B = \begin{bmatrix} \frac{\text{Gain}}{L_{\text{ind}}} \\ 0 \end{bmatrix} = \begin{bmatrix} 1.244E7 \\ 0 \end{bmatrix} \quad (3.16\text{b})$$

$$C = [0 \ 1] \quad (3.16\text{c})$$

$$G = ss \left(A, B, \begin{bmatrix} C \\ \text{zeros}(2) \end{bmatrix}, 0 \right) \quad (3.16\text{d})$$

With some further matrix augmentation and calculation the regulator calculation, in accordance with Listing E.2, yielding the following parameters for the PI controller:

$$C_{\text{PI}} = 1.5 \text{ nF} \quad (3.17\text{a})$$

$$R_{\text{PI}} = 33.3 \text{ k}\Omega \quad (3.17\text{b})$$

Where $C_{\text{PI}} = C_{14}$ and $R_{\text{PI}} = R_5$. And for the LQR:

$$R_{k_1} = 16.2 \text{ k}\Omega \quad (3.18\text{a})$$

$$R_{k_2} = 8.63 \text{ k}\Omega \quad (3.18\text{b})$$

Where $R_{k_1} = R_{18}$ and $R_{k_2} = R_{14}$. Now the values for the discrete analogue components in the PI controller and the LQR have been determined.

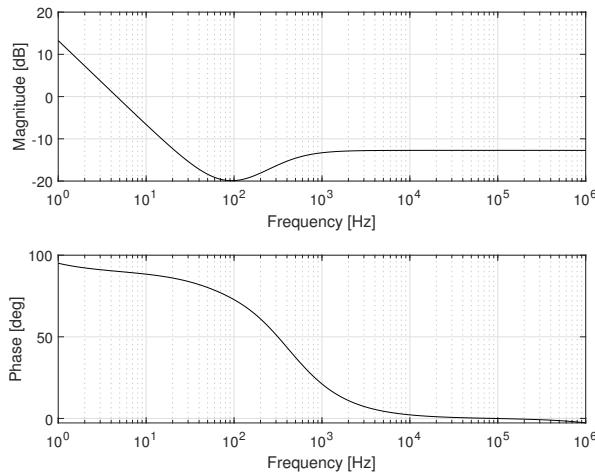


Figure 3.3: Bode plot of the designed PI controller from a small-signal analysis

Applying the synthesized values, a bode plot is seen in Figure 3.3 where the steady-state integrator is present. In the upper subfigure, the magnitude is shown in dB and in the lower subfigure, the phase is shown in degrees. The small-signal analysis that was used to obtain the bode plot above can be found in Figure C.2.

3.8 Remarks

This concludes the synthesis chapter of the report. The entire BOM based on Synthesis chapter can be found in the appendix on Table F.1. During the production phase, some modifications were made to the design, which will be explained in the following chapter.

Chapter 4: Production

This chapter will explain the process of going from a theoretical design to actual implementation. First, the system will be simulated, and the results will be reviewed. Lastly, the process of producing the physical hardware will be discussed.

4.1 Simulation

During the synthesis phase of the project, it was decided that it would be a valuable learning tool to use the understanding gained from studying the materials and theory to come up with a SPICE model that can simulate the design. For simplicity, it would be beneficial to the simulation to use ideal components rather than complex physical models. This causes the circuit simulation to compute faster (because of less complex calculations) and causes the simulation to be easier to troubleshoot. The gate driver is replaced by a buffer without hysteresis and complementary output, and the power stage is replaced by a VCVS also called an E source in LTSpice. To streamline simulation efforts by using MATLAB for carrying out the necessary synthesis calculations and inputting those component values to the simulations in LTSpice, the script Listing E.4 will export the component values to an external parameter file, import the parameters in LTspice and perform the simulation. The simulation output is imported automatically to MATLAB using the library `ltspace2matlab` [19] for post-processing and analysis. This improves workflow and makes it possible to compare various sets of parameters efficiently.

The transient simulations are performed for a length of $600\ \mu\text{s}$ with a log delay of $200\ \mu\text{s}$ to ensure a steady state. The input signal is configured with a DC component of $V_{\text{DC}} = 2.5\ \text{V}$, AC component $v_{\text{p-p}} = 900\ \text{mV}$ and frequency of $f_{\text{in}} = 10\ \text{kHz}$.

4.1.1 Open Loop

A simulation model based on the theory of each function can be seen implemented in LTSpiceXVII in the figure below:

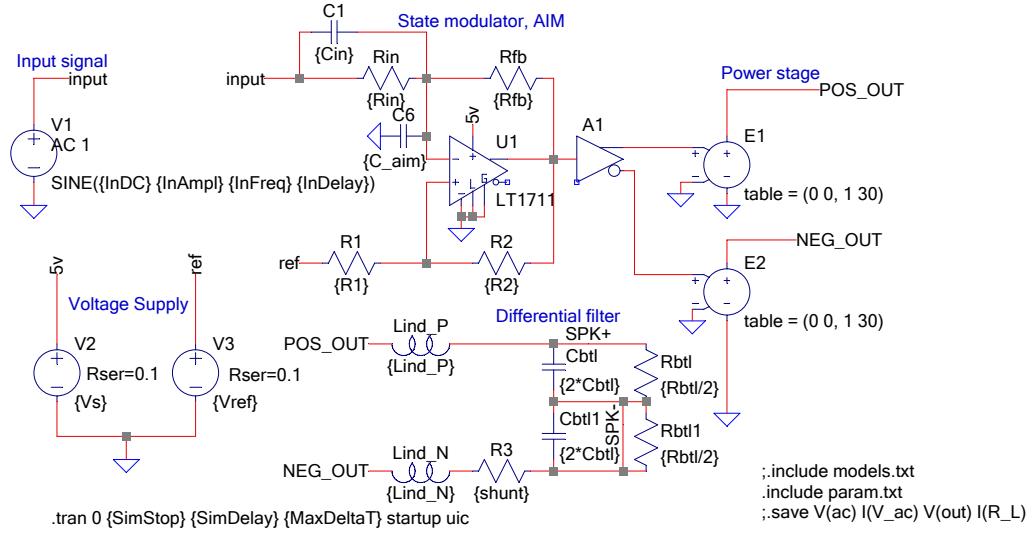


Figure 4.1: LTspice model of class-D amplifier using ideal components without feedback

Seen in Figure 4.1 is the circuit as described in the synthesis chapter, although with the gate driver circuit and power stage implemented with ideal components rather than complex SPICE component models. Upon simulating the circuit and analysing the following data is obtained: On Figure 4.2 the output of the open loop transient simulation

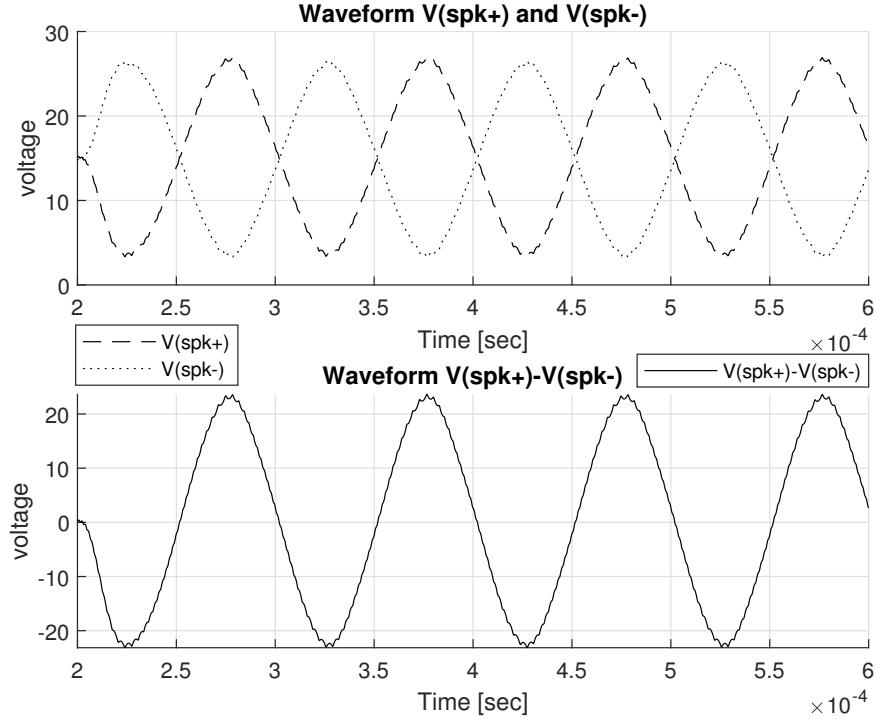
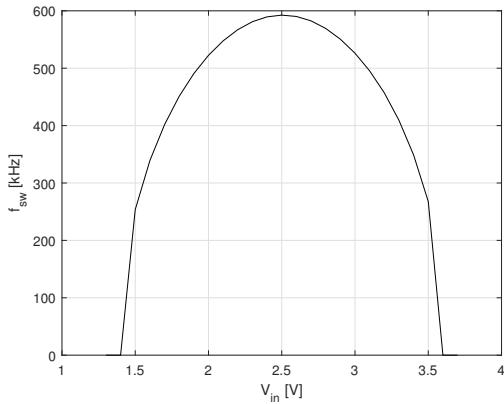


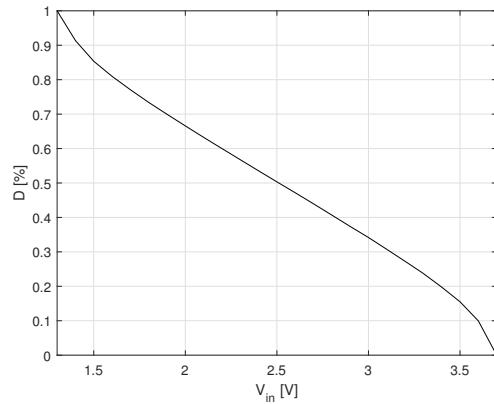
Figure 4.2: LTspice simulation output of openloop configuration

from Figure 4.1 can be seen. Note that under the x-axis of the figure, it is zeroed at 200 μ s. This is done to ensure a steady-state in the transient simulation. In the upper

subfigure the two node voltages of the bridge-tied load can be seen as described in the LTspice model in Figure 4.1. In the output signal on both subfigures some noticeable but minor output ripple can be seen. This is due to the reactive components characteristics in the output filter.



(a) f_{sw} over V_{in}



(b) D over V_{in}

Figure 4.3: Simulated f_{sw} and D over DC values of V_{in} with zero amplitude

Seen in Figure 4.3 is the simulated AIM, plotted for f_{sw} in Figure 4.3(a) and D in Figure 4.3(b). This is done with zero amplitude and a step parameter of DC input. It is noted that the switching frequency produces the expected curve according to the calculations. This varying switching frequency is a particular trait of the astable integrating modulator due to the non-linear behavior of the carrier waveform and the propagated phase delay of the self-oscillation. The duty cycle fits the theoretical model as seen in Figure 3.2(b).

4.1.2 Closed Loop

Seen in Figure 4.4 is the circuit as described in its entirety. This includes the control loop with the LQR and PI controller feedback loop from the bridge-tied load.

The output from the closed loop simulation model can be seen in Figure 4.5. Note that under the x-axis of the figure, it is zeroed at 200 μ s. This is undertaken to ensure a steady-state in the transient simulation. In the upper subfigure are the two voltage nodes on each side of the bridge-tied load and in the lower plot is the differential output signal. It is noted that the amplitude of the differential output signal is approximately half of the open loop configuration.

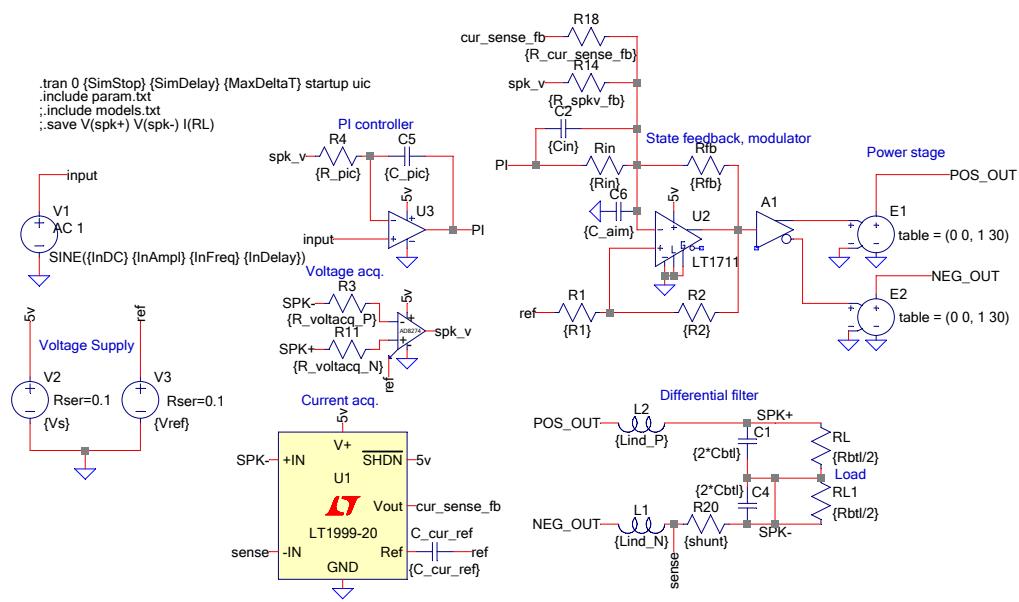


Figure 4.4: LTspice model of class-D amplifier using ideal power stage switches with a control loop

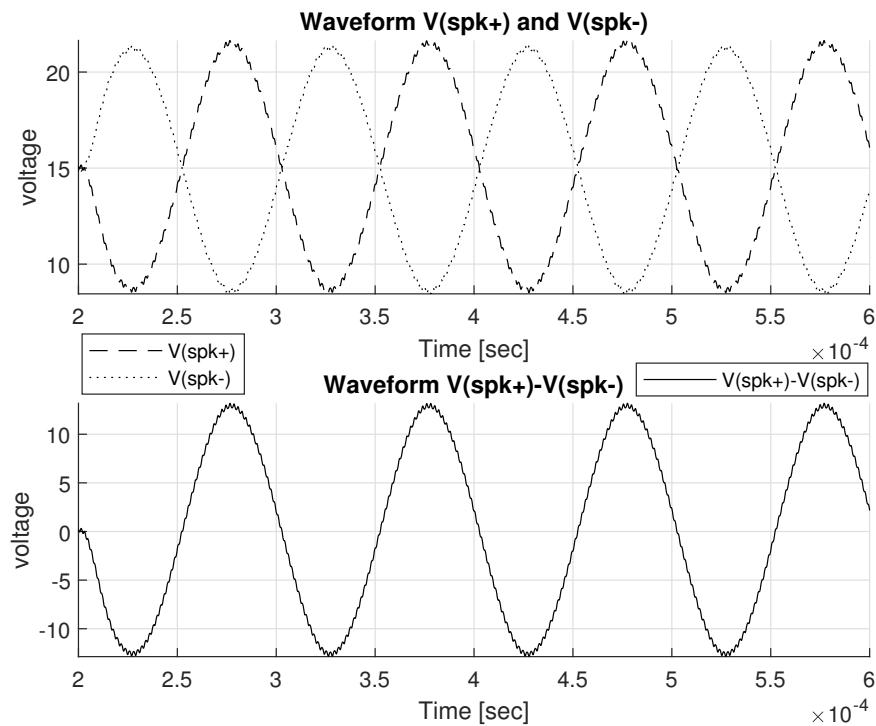


Figure 4.5: LTspice simulation output of closed loop configuration

4.2 Inductor design

During the synthesis phase, a value for the output filter inductor was obtained. Now, an inductor design must be made with regards to core material, core size and wire gauge. Based on an initial proposal, it was decided to investigate between two options being MICROMETALS, Inc. toroid cores of the T80-2 and T94-2 variants. The choice being a relatively small core size that would adequately fit the PCB in a parallel mounting position, and a material '2'-type that holds necessary linear frequency characteristics. The inductor wire gauge was chosen fairly large to retain a modest number of turns and in turn causing the winding to be easier to do by hand. Based on the datasheet [7] expressions, the calculations were made in MATLAB in accordance with Listing E.3. The calculation showing that both options are valid choices in terms of not saturating the core and yielding the following results.

For T-80-2:

$$N = 17 \text{ turns}$$

$$B = 32 \text{ mT}$$

For T-94-2:

$$N = 14.5 \text{ turns}$$

$$B = 25 \text{ mT}$$

The T-80-2 was chosen because of its smaller core size and wound by hand using 0.95 mm wire gauge from inventory.

Measurement

After winding the two coils, a validation of the coil specifications is needed. A lab test with a N4L PSM1735 frequency analyzer [22], the following inductance over frequency was measured: Seen in Figure 4.6, is a measurement sweep with the wound inductor coil under test. The upper subfigures shows inductance over frequency, and measures reasonably the expected $1.768 \mu\text{H}$ on the output filter inductor. relatively linearly until around 10 MHz where there is a peak and then a drop-off in inductance. As this frequency is significantly higher than the switching frequency of the pulse signal it is acceptable. The lower subfigure describes the resistance over frequency and is also comparatively low until it reaches 20Ω at 10 MHz. This should give an idea of the amount of heat dissipation within the output filter inductors can be negligible on the frequency range of interest.

4.2.1 Mounting method

In the PCB design a through-hole mounting was decided in the original design. However, in the project a surface mount was decided. The problem with mounting the output filter inductors in the through-hole method is that it can cause the removal to be much more difficult as well as the protrusion of the conducting wires on the opposing side of the PCB can increase EMI in the sensitive circuitry.

Seen in Figure 4.7 are two possible ways to mount the output filter inductors. In Figure 4.7(a) the two conductive wires of the inductor are inserted through the Via on the PCB and soldered on the opposing end. In Figure 4.7(b) the two wires are bent and soldered to the Via on the same side as the inductor. In this project the primary benefit of this mounting method is that it is desired to be able to test different inductors and it

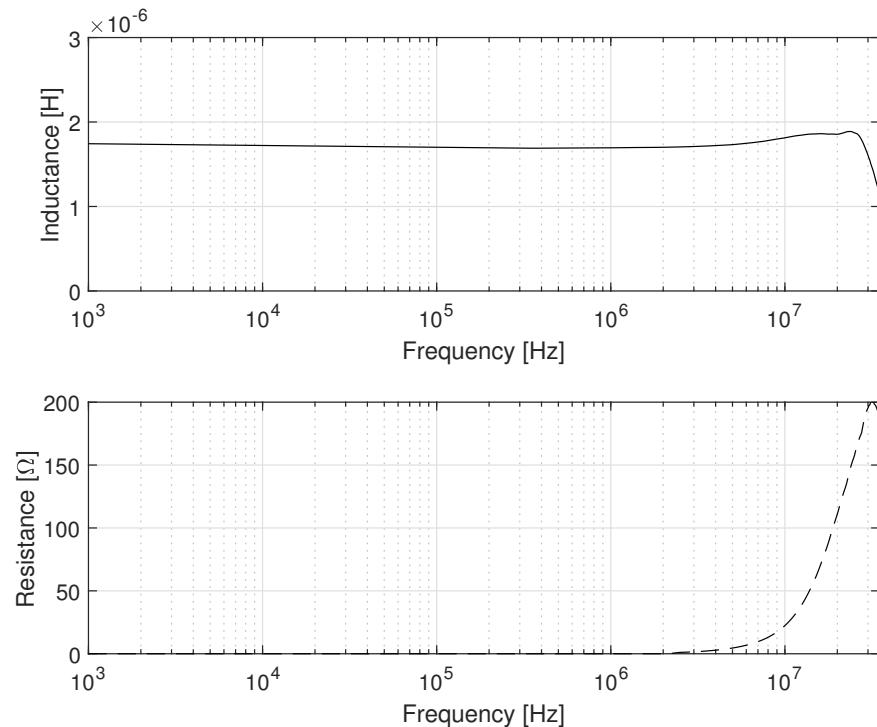


Figure 4.6: Inductor measurement over the frequency range 1 kHz to 35 MHz

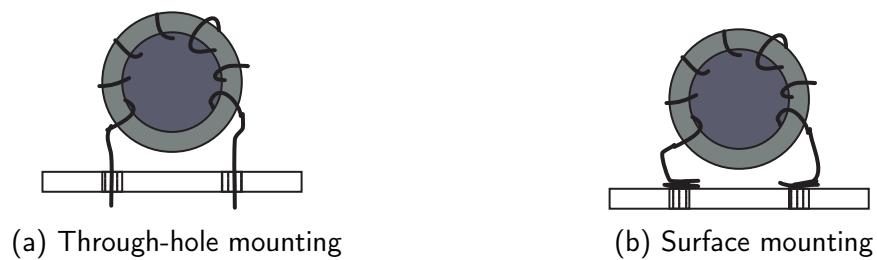


Figure 4.7: Inductor mounting sketch, not to scale

considers the possibility to remove the coil a requirement. A through-hole mounting is not ideal because the increased thermal connection becomes excessively large and the introduced heat on the copper by the soldering iron is dissipated into other areas of the PCB. Therefore, some heat restriction is required. This is knowledge that was acquired experimentally during the mounting process.

4.3 Printed Circuit Board

This section will explain the process of manufacturing the physical PCBs for the class-D amplifier. The layout file from [21] was used in this project. It is comprised of two PCBs. The first part handles the IO and in addition has the input filter, preamp and PI controller. The other PCB includes the modulation, power stage, output filter and regulation subcircuit.

4.3.1 Input-Output Printed Circuit Board

Refer to Figure 4.8 for the layout of the IO PCB.

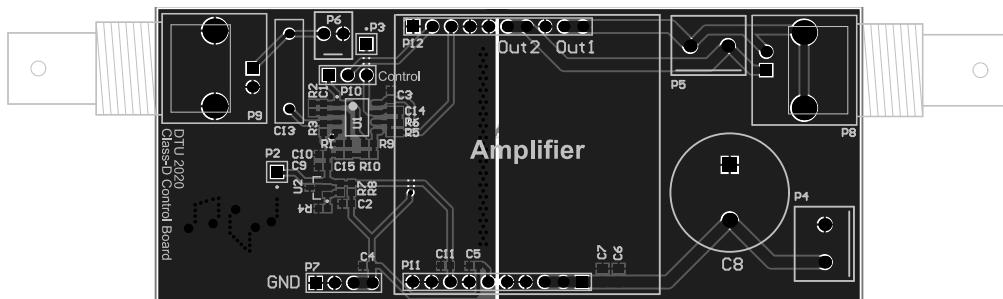


Figure 4.8: Layout of IO PCB

4.3.2 Amplifier Printed Circuit Board

Refer to Figure 4.9 for the Amplifier PCB.

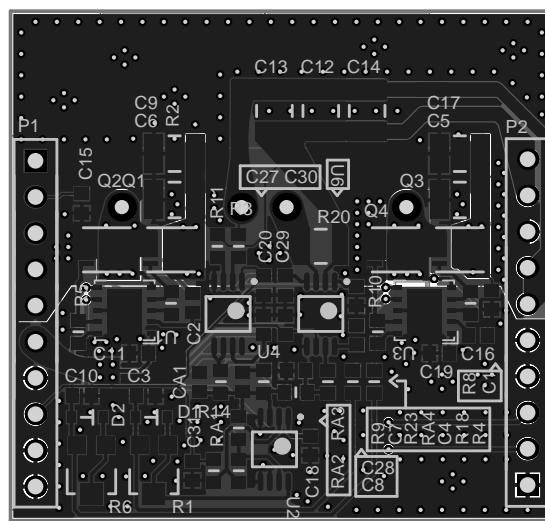


Figure 4.9: Layout of Amplifier PCB

4.3.3 Methodology

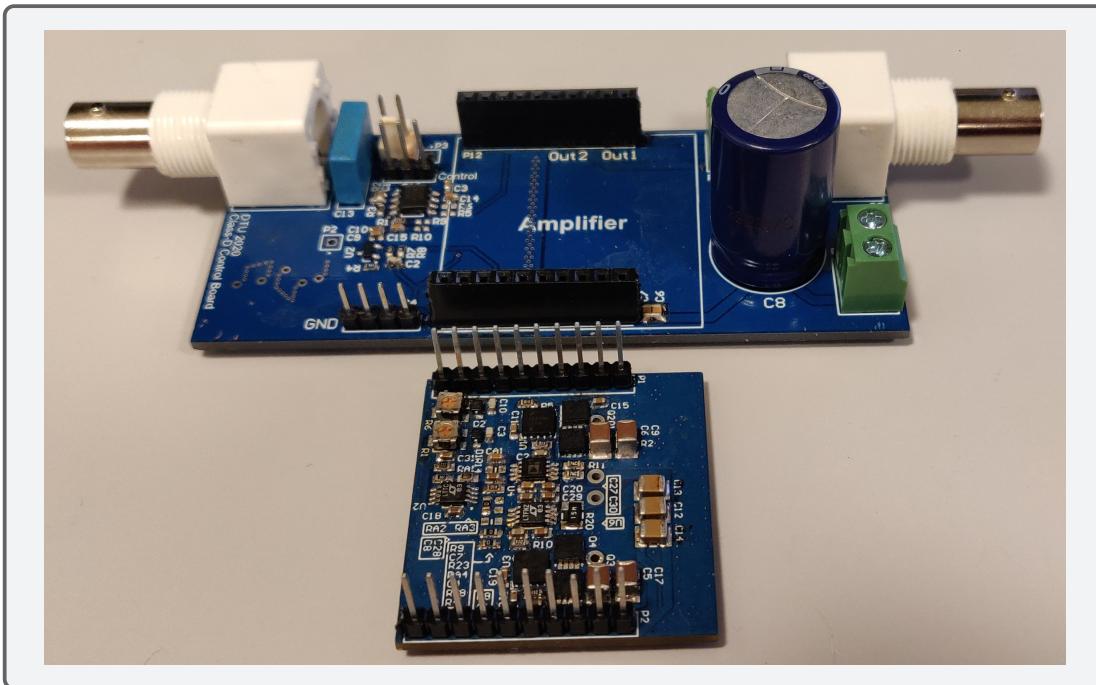


Figure 4.10: Amplifier after solder work, without output filter inductors

Seen in figure Figure 4.10 are the two amplifier PCBs. The upper PCB is the IO, preamplifier, input filter and PI regulator. The lower PCB is amplifier. The implementation is a 4-layer PCB design in Altium Designer and was manufactured professionally and sent to DTU without components. During production of the PCBs, a 63Sn/37Pb solder paste was added and SMD components were placed onto the PCB. Next the PCBs were placed in a reflow oven on the appropriate reflow cycle in accordance with the solder paste datasheet. Finally, the PCBs were inspected, cleaned and faulty soldering was corrected and through-hole components were soldered by hand.

During the production phase, some modifications were made to the original specification due to various circumstances like alternative inventory, better component choice, etc. A table with only the modifications to the BOM can be in Table 4.1.

In the table with modifications to the BOM in conjunction with Table F.1, a comprehensive list of the amplifier components and their values are found. In the modification list, some components were experimentally improved in accordance with the further analysis.

4.3.4 Remarks

After the circuits were produced, components were soldered to the PCB as described in the previous section, initial inspections revealed some cross-connections due to imperfections in the soldering process. Therefore, manual corrections had to be done on the reflow process. Following the corrections, under visual inspection the PCBs appeared to be in a suitable condition. Some DMM measurements on the Amplifier PCB were performed to verify proper connections between ICs and the copper pads. This indicated adequate solder work ready for conclusive analysis.

Circuit	Component	Value	Footprint	Rating	Reason
IO	C2,C3	120n	0603	X7R16V	100n: No inventory
IO	C4,C9,C10,C11	100n 1u	0603	X7R16V	120n: Improvement
IO	C5	1u	0603	X7R50V	X5R6.3V: No inventory
IO	C15	1.5n	0603	X7R16V	NC: Added
IO	C8	1000u	RAD-0.3in	63Vdc	1500u: No inventory
IO	R4,R7	3.01k	0603	1%	4.75k: Improvement
IO	R8	475	0603	1%	2.49k: Improvement
Power stage	C11,C19	120n	0603	X7R16V	100n: No inventory
Power stage	C1,C15	22n 1u	0603	X7R50V	120n: Improvement
Power stage	D1,D2	Diode	NA	75V 0.25A	85V 0.25A: No inventory
AIM+reg	C18,C20,C27,	120n	0603	X7R16V	100n: No inventory
AIM+reg	C28,C29,C30,C31	120n	0603	X7R16V	100n: No inventory
AIM+reg	C8	120n	0603	X7R16V	Implement
AIM+reg	RA1	2.21k	0603	1%	2.2k: No inventory

Table 4.1: Modifications to the Bill of Materials

Chapter 5: Analysis

In this chapter various test setups will be discussed for the purpose of making quantifiable measurements of the amplifier, effects of the output filters parasitic elements on the control loop among others.

5.1 Hysteresis window of modulator (Simulation)

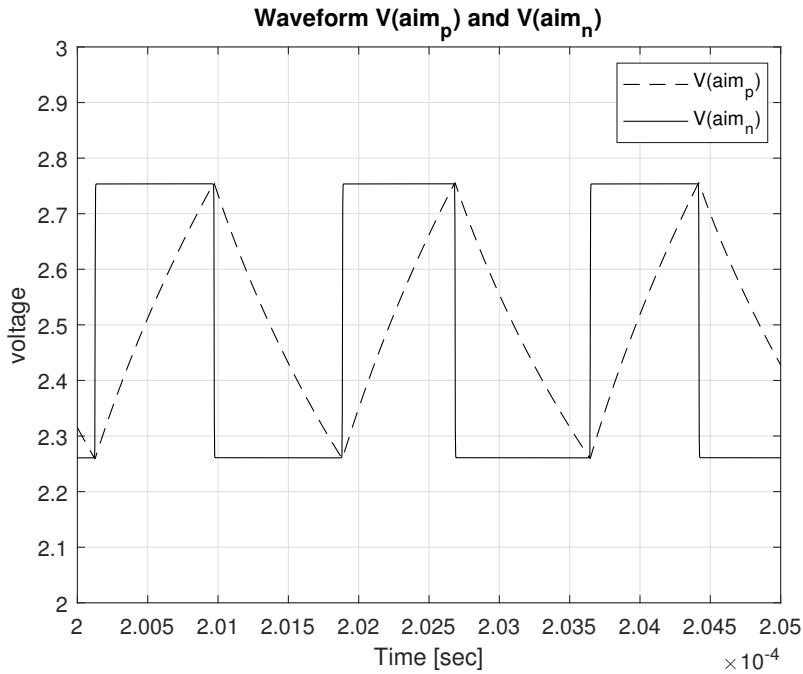


Figure 5.1: Hysteresis window on AIM

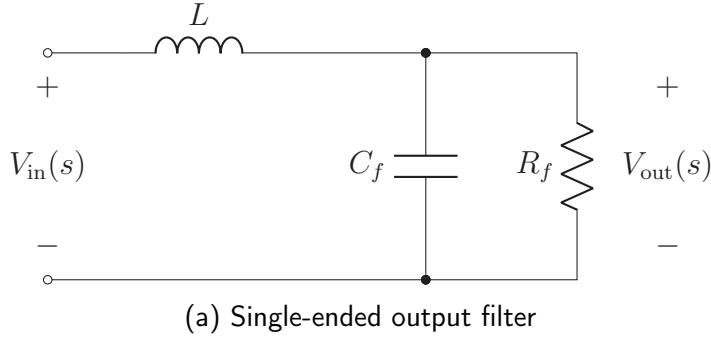
Seen in Figure 5.1 is the hysteresis window conforming to the theoretical model. The analysis is performed by inputting a DC component of 2.5 V with zero AC components. This gives a duty cycle of 50 % and an idle switching frequency of 600 kHz. It is noted that the variables V_{th_H} and V_{th_L} is seen in the square waveform alternating between 2.25 V to 2.75 V as mentioned in Equations (3.4a) and (3.4b) and the carrier waveform is seen on the dashed curve. Noted is a slight non-linear curve of the carrier waveform due to the AIM capacitor charge and discharge in each cycle.

5.2 Output filter (Calculation and Simulation)

As a class-D amplifier cannot be classified as a linear time-invariant system, it is difficult to perform a small-signal analysis of the complete circuit with regards to the influence of parasitic elements in the output filter. Therefore, the output filter with various parasitic elements will be investigated using the output stage alone.

5.2.1 Analytical approach

To make nodal analysis more convenient the filter is transformed to single-ended filter type using Equations (2.20a) to (2.20c).



Applying nodal analysis to Figure 5.2(a) yields:

$$\begin{aligned}
 H(s) &= \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{\frac{R_f}{1+s(R_f C_f)}}{sL + \frac{R_f}{1+s(R_f C_f)}} \\
 &= \frac{R_f}{R_f + sL + s^2 R_f L C_f} \\
 &= \frac{1}{1 + s \frac{L}{R_f} + s^2 L C_f}
 \end{aligned} \tag{5.1}$$

Finally, from Equation 5.1 it is seen that the transfer function has no zeros and two poles.

Inductor parasitic ESR

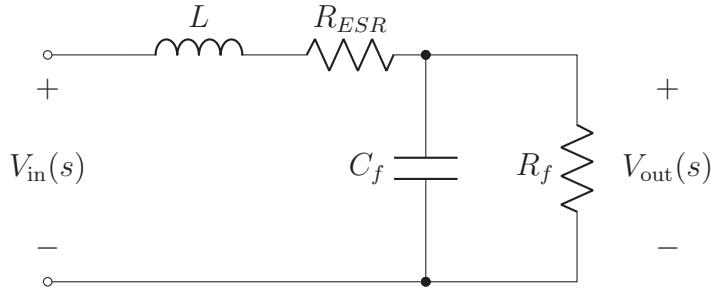


Figure 5.3: Output filter parasitic elements, addition of series resistance R_{ESR}

Seen in Figure 5.3 is a diagram of the inserted parasitic series resistance of the output filter inductor. Initial decision of numeric value of inserted parasitic resistance was an choice in desire for sufficient weight of change in behaviour and a sensibility in function. The decision was a resistance value of $300 \text{ m}\Omega$.

$$\begin{aligned}
 H(s) &= \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{\frac{R_f}{1+sR_fC_f}}{R_{\text{ESR}} + sL_{\text{ind}} + \frac{R_f}{1+sR_fC_f}} \\
 &= \frac{R_f}{(R_{\text{ESR}} + R_f) + s(L + R_f R_{\text{ESR}} C_f) + s^2 (R_f L C_f)}
 \end{aligned} \tag{5.2}$$

Looking to Equation 5.2, it is seen that the addition of a series resistance to the inductor does not cause addition of a pole or zero which is an indication that the frequency

response of the system will not be significantly altered by the series resistance of the inductor.

Inductor parasitic capacitance

Decision on an equivalent parallel capacitance of the inductor was made by calculating the resonance frequency of the inductor from earlier impedance analysis and back-calculating for solving for the capacitance using an LC-equation. The resulting value was 120 pF.

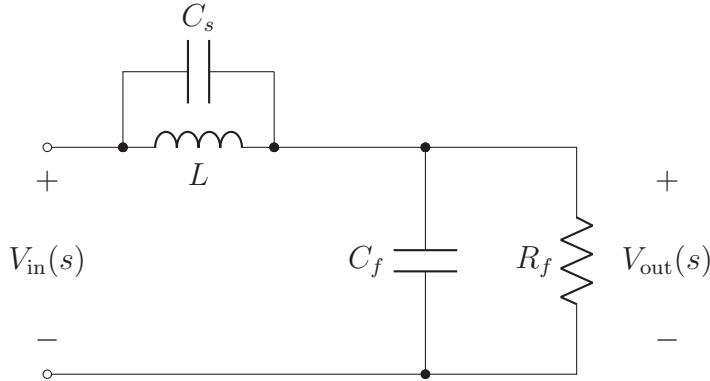


Figure 5.4: Output filter parasitic elements, addition of parallel capacitance C_s

Seen in Figure 5.4 is a diagram of inserted parallel capacitance of inductors.

$$\begin{aligned}
 H(s) &= \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{\frac{R_f}{1+sR_fC_f}}{\frac{sL}{1+s^2LC_L} + \frac{R}{1+sRC}} \\
 &= \frac{R + s^2RLC_L}{R + sL + s^2(RLC_L + RLC)}
 \end{aligned} \tag{5.3}$$

From Equation 5.3 it is seen that a zero is added in the numerator of the transfer function. This indicates a change in the overall response of the system.

Summary

In the derived expressions for transfer functions of addition of inductor series resistance and parallel capacitance, it is seen from a control loop stand point that the parallel capacitance makes the most significant change to the frequency response. The location of the zero is presumably rather high in frequency, based on the small capacitor value of 120 pF.

5.2.2 Simulation approach

Looking at Figure 5.5, different plots are seen of the small-signal output of the output filter. This figure is based of a small-signal analysis from Figure C.3. First the ideal filter is plotted and contains a relatively prominent peak around the cut-off frequency. This is by design, as the Q factor is relatively high. This resonance peak was decided to compensate for some switching losses in the power stage. It is noted that as parasitic elements are added in the inductor and capacitor, this resonance peak is lowered and will presumably cause further switching losses in the output stage. In the magnitude plot it can be seen that overall, the parasitic elements in the capacitor seem to make a larger change to the frequency response in the high-frequency range.

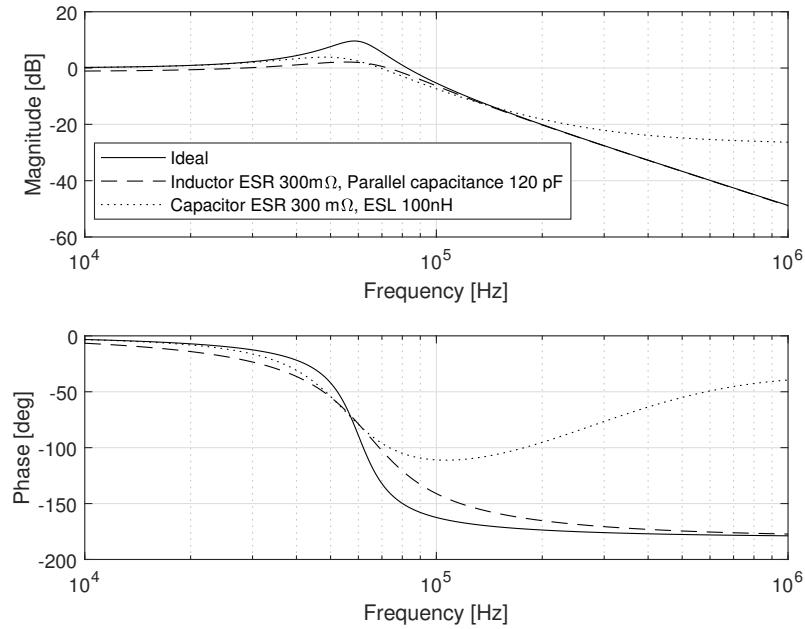


Figure 5.5: Bode plot of output filter using ideal LC filter, parasitic elements in inductor and parasitic elements in capacitor

5.3 Initial tests (Hardware)

A preliminary analysis was attempted to be made on the hardware. Unfortunately, there were stability issues with the setup. Differential voltage measurements made across the load revealed through-put of the amplified input signal, with a high-frequent oscillation superimposed. On rough estimates, the high-frequent oscillation signal appeared to be in the vicinity of the resonance frequency of the output filter. Shortly thereafter during testing, the lower half-bridge short-circuited, and reparation of the hardware was necessary. After repairs were completed on the amplifier circuit and tested to be functional, next will be some hardware analysis on the circuitry.

5.4 Control loop (Hardware)

Regulator characteristics for amplifier circuitry are determined by its converter loop transfer function. This transfer function can be illustrated by a Bode plot. This representation of magnitude and phase over a frequency spectrum gives insight into the speed of the regulation loop and the general stability of the system. To acquire the Bode plot data measurements need to be made on the circuit. This will be explained in the following sections.

5.4.1 Measurement setup

A measurement setup is implemented using a Bode 100 Vector Network Analyzer [13]. To determine the control loop parameters of an active circuit, a wideband injection transformer is required. Using the recommended typical measurement setup from Figure B.1, the following measurement setup is implemented:

Seen in Figure 5.6 is an overall block diagram of the measurement setup. The Injection

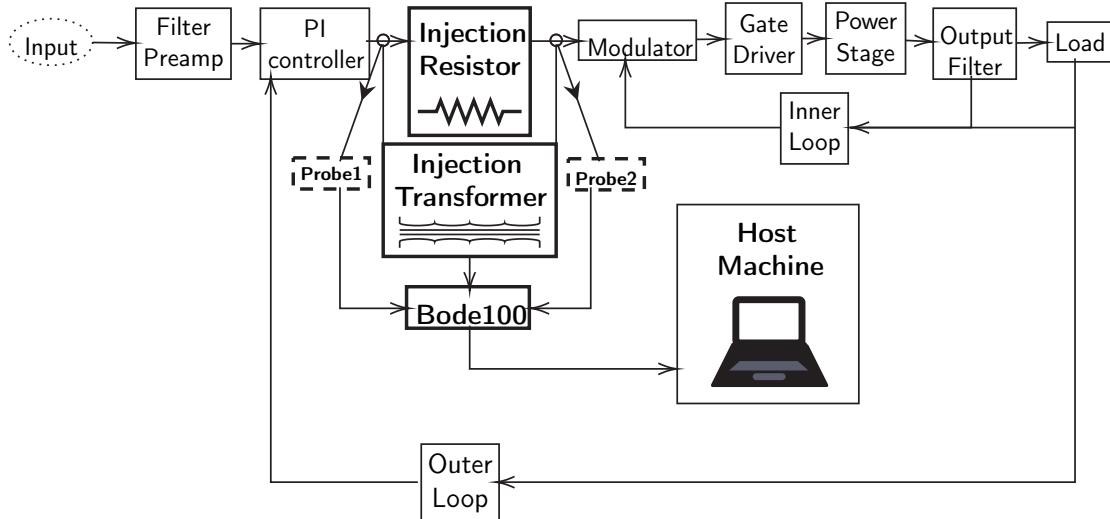


Figure 5.6: Block diagram of measurement setup for transformer injection measurement of control loop

Transformer B-WIT 100 transformer [17] is used with an injection resistor of 10Ω inserted in the feed-forward loop between the PI controller and the modulator subcircuits. Typically the injection transformer is inserted across the injection resistor in the feedback loop as per the manual diagram, but to secure the equipment from common-mode voltages, it was decided to break the loop in the low voltage circuitry between the PI controller and the modulator. A breakout board was made using a copper-clad circular perf board, connectors, a resistor and cables. In this project, any reactive characteristics from the speaker will be disregarded. In the practical measurement setup, it will be replaced by a resistive element. Choosing packages for the introduced parasitic elements was based on availability. For the inductor series resistance, three 0.1Ω was connected in series. For the inductor parallel capacitance, the chosen package was a ceramic 0603 120 pF capacitor.

The breakout board can be seen in Figure 5.7 mounted on the IO PCB of the amplifier. The two BNC connectors are for Probe 1 and Probe 2 of the Bode 100 Network Vector Analyzer. The red and black 4 mm lab connectors are for the injection transformer. Finally, the green/yellow 4 mm lab connector is for a ground reference on the analyzer probes.

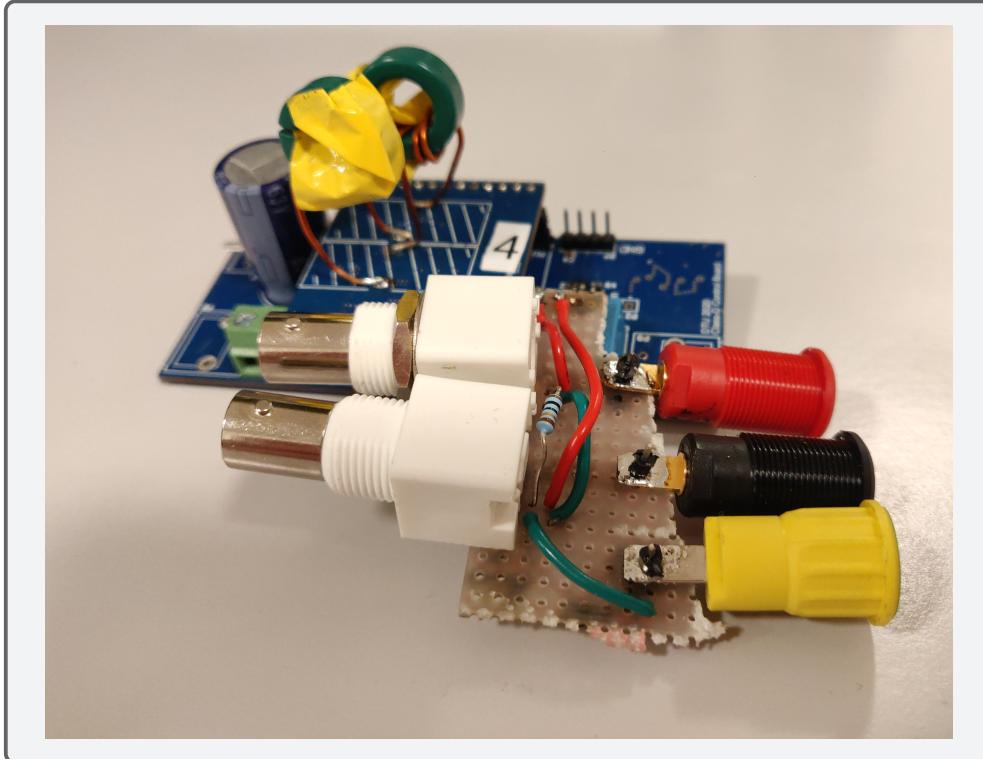


Figure 5.7: Breakout board for transformer injection measurement setup

5.4.2 Outer loop open, inner loop closed

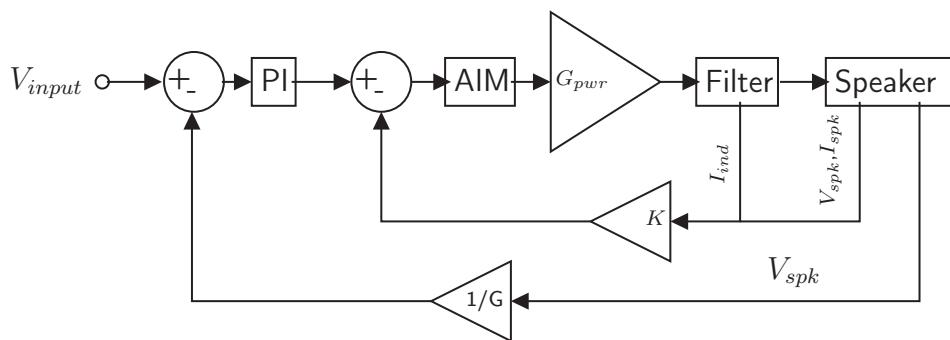


Figure 5.8: Diagram of PI-LQR controller

Seen in Figure 5.8 is the more elaborated diagram overview of the feedback loop. Observed are the inner loop (LQR) and outer loop (PI) with their respective error amplifiers. First, the system will be analysed as open PI loop and closed LQR loop. Next some parasitic elements will be introduced on the output stage, and the same analysis will be repeated with the LQR loop opened.

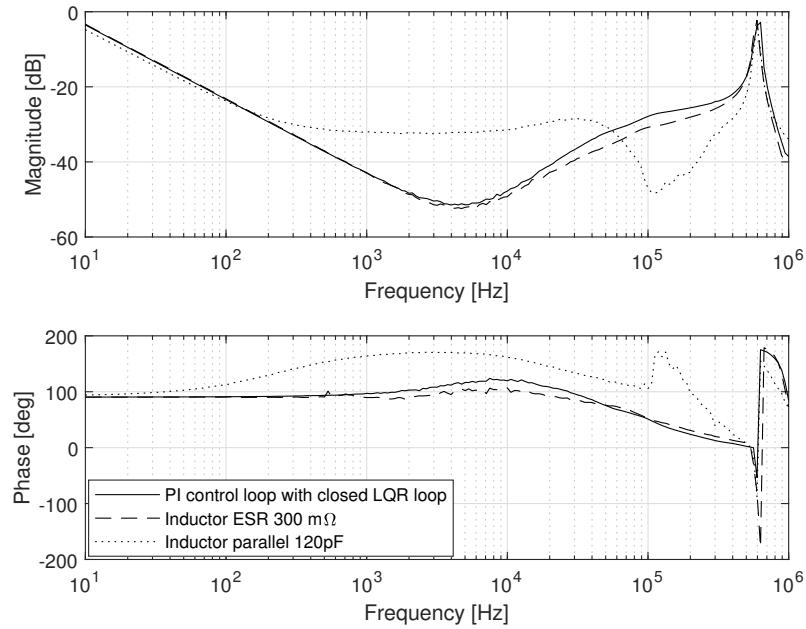


Figure 5.9: Measurement of frequency response of PI with closed LQR controller with addition of parasitic elements

Seen in Figure 5.9 are bode plots displaying the change in magnitude and phase response with addition of parasitic elements in the filter inductor.

5.4.3 Outer loop open, inner loop open

Next the inner loop (LQR) will be opened and only the PI controller will remain loop under test. The same measurements will be repeated and discussed.

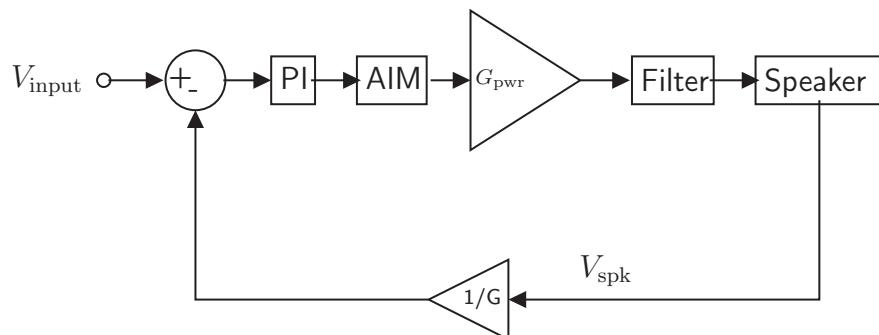


Figure 5.10: Diagram of PI controller feedback loop

Seen in Figure 5.10 is the control loop with only the outer feedback loop active. The same parameters in the test will be repeated and measured.

Parasitic elements

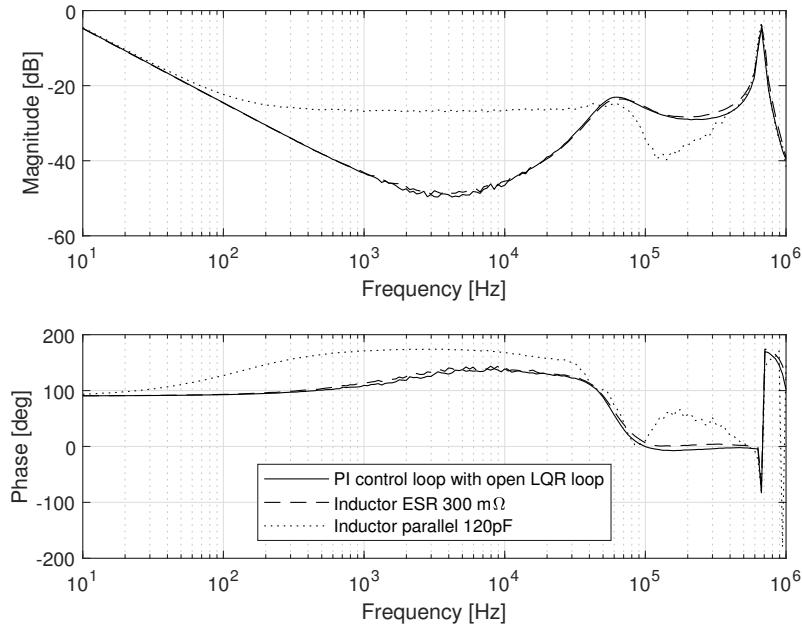


Figure 5.11: Measurement of frequency response of PI with open LQR controller with addition of parasitic elements

In Figure 5.11 is the frequency response of the outer control loop with the inner loop open.

5.4.4 Discussion

In this discussion section, the data collected from control loop measurements in the two parameterised tests will be processed using Listing E.6. Using System Identification Toolbox [24] a transfer function can be estimated to create dynamic system models from measured data.

Looking at the addition of the series resistance of the inductor there is no significant change in the frequency response. Only with the addition of a parallel capacitance the frequency band between 1 kHz to 50 kHz is changed seemingly with an addition of a zero around 300 Hz. This is expected as per the analytical investigation into the effect of the output filter transfer function with the addition of a parallel capacitor from Equations (5.1) to (5.3).

The preliminary indication looking at the measured transfer functions Figures 5.9 and 5.11 indicates the closed versus open of the LQR loop is not significantly affected by the addition of inductor parasitic elements in the low frequency band. In other words, closing the LQR loop had no mitigating effects on the parasitic elements influence on the parasitic elements. It did, however, did mitigate a discontinuity in the frequency band between 100 kHz to 500 kHz range both in the magnitude response and phase delay. This does not seem to be exclusively related to the parasitic elements introduced during the measurements, as the control loop without any added parasitic elements is also displays this characteristic.

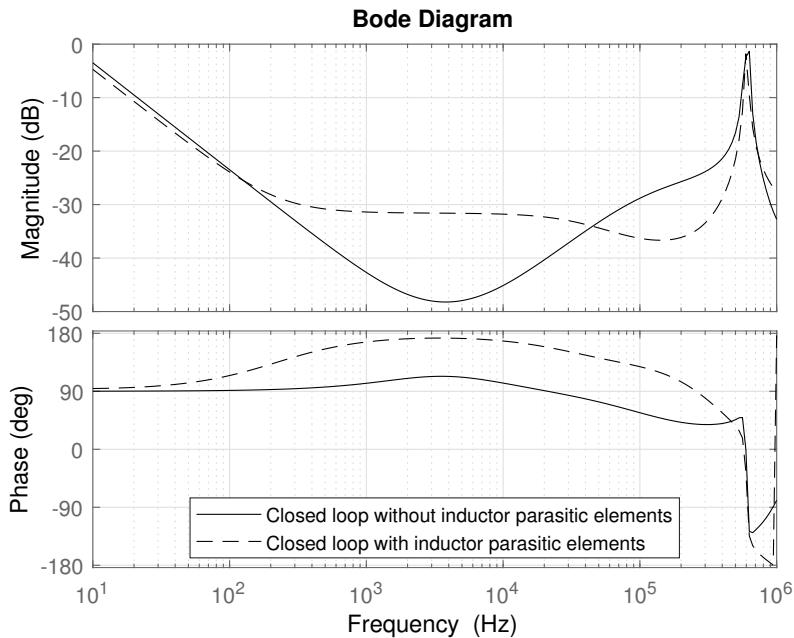


Figure 5.12: Estimated transfer functions of PI loop with closed LQR loop

In Figure 5.12 is the estimated control loop transfer functions using fourth-order transfer function estimation. It appears that the modulation frequency peak at 600 kHz has been shifted up in frequency to 4 MHz as the transfer function was estimated. This is a processing artifact but is not part of the measurement. Plausibly the estimation error could be mitigated by applying the transfer function estimation with a higher order. However, this is deemed not of significance for the parasitic element transfer function analysis.

In Figure 5.13 the transfer function of the inductor parasitic elements are estimated with a division calculation in MATLAB. As the transfer function is calculated with a function division it produces a relative transfer function to determine the frequency bands that are most affected by the parasitic elements. It is noted that particularly in the frequency band between 10 kHz to 100 kHz the parasitic elements add a significant gain of 15 dB and approximately 45° of phase shift.

As the PI control loop has a time constant $\tau_i = 50 \mu\text{s}$ and the effect of the parasitic transfer function in the higher frequencies at 100 kHz is in an interval of $10 \mu\text{s}$ it is proposed to change the PI controller time constant τ_i to an order of five times larger. This would mean adjusting the value of the PI controller resistor R_{PI} from $33 \text{ k}\Omega$ to $6.6 \text{ k}\Omega$. This would mean a more aggressive integrator with a time constant of $9.9 \mu\text{s}$.

Theoretical control loop

In Figure 5.14 the control loop is seen in its theoretical form, where C is control, P is plant, F is feedback and x and y are the input and output, respectively. When assessing the transfer function for open loop, starting on the right and moving left gives:

$$H_o = P \cdot C \cdot F \quad (5.4)$$

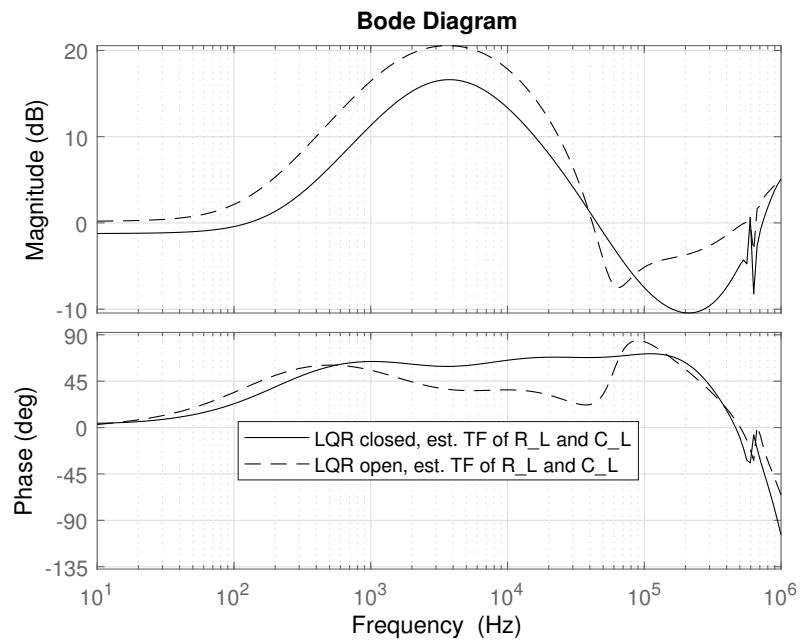


Figure 5.13: Estimation of transfer function of inductor parasitic elements on PI loop with and without LQR loop based on Figure 5.12

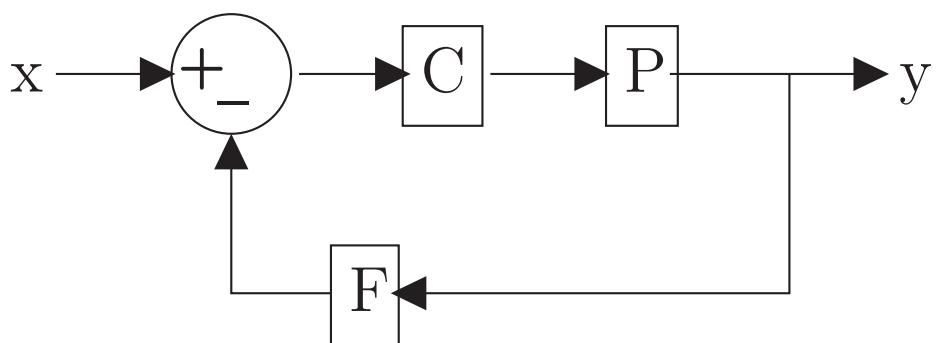


Figure 5.14: Diagram of theoretical control loop

And for the closed loop is starting on the right and moving left gives:

$$y = P \cdot C \cdot (x - F \cdot y) \quad (5.5)$$

Where $C \cdot P$ is the feed-forward and $(x - F \cdot y)$ is the feedback. Applying control loop theory from Equation 5.4 in the open loop to generating a theoretical transfer function of the system. This is accomplished using MATLAB and Simulink with the Control System Toolbox [20] with the simulation model in Figure 5.15 is used to construct an open loop transfer function of the amplifier.

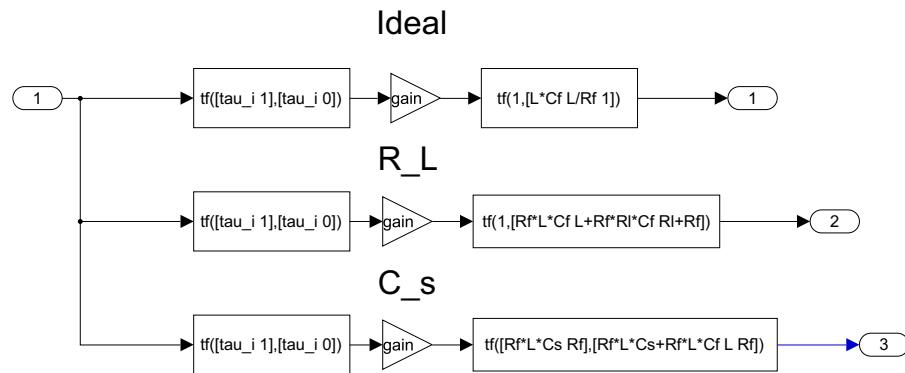


Figure 5.15: Simulink model of open loop transfer function in control loop

Using this Simulink model and the derived expressions from the output filter Equations (5.1) to (5.3) the open loop frequency response can be obtained.

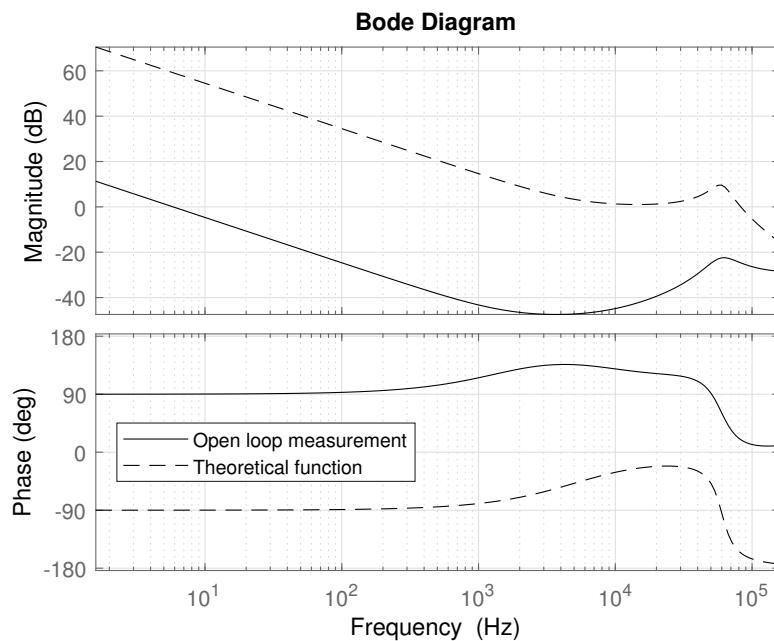


Figure 5.16: Comparison of measured transfer function and the theoretically obtained open loop transfer function of the system

Seen in Figure 5.16 is the comparison between the measured control loop using the transformer injection method and estimated with an 8th order transfer function compared with the theoretically derived expression. The increased order in the transfer function was necessary to do to obtain a meaningful comparison with the theoretical transfer function. For the purpose of validating the measurement, it seems to fit reasonably with the results that could be expected. It would appear that the measured control loop seems lower in magnitude than the actual expected transfer function level, although this could be explained when the reference level of the measuring instrument was set quite low to protect the injection transformer from overloading. This could possibly explain why there is a discrepancy in the magnitude. The difference in phase reference is probably occurred through data processing with phase wrapping performed in the analysis software.

Chapter 6: Conclusion

The overall goal of this project was to work on a class-D audio amplifier system, understand its topology and seek to investigate the influence of parasitic elements on the control loop. A class-D audio amplifier design was researched from a reference and implemented in a Spice simulation. The simulation was subject to some rudimentary analysis to better learn the functionality of the design. The output filter was subject to a small-signal analysis to model the frequency response of parasitic elements in both the inductor and capacitor. Next, a hardware implementation was built using calculated component values. The hardware implementation was applied in a parameterised testing scheme to investigate the influence of the output filter on each control loop transfer function. Validation was performed on the measurement data from a theoretical standpoint. The investigation revealed inductor parasitic elements primarily affected the outer control loop above 10 kHz but lower than 100 kHz. It would appear the LQR control loop effect on introduced parasitic elements was negligible. The LQR control loop did seem to effectively mitigate discontinuity in the frequency range in the vicinity of the modulation frequency in both magnitude and phase. Based on these findings, a proposition was considered to decrease the time-constant of the PI regulator to compensate for the parasitic elements by employing a more aggressive integrative effect on the PI controller.

6.1 Future Work

Regarding the conclusion of the investigation into parasitic elements of the capacitor, the logical next step would be to perform the proposed control loop modifications and redo the control loop analysis to see if the outer control loop has compensated for the influences of the parasitic elements. This was not possible to do due to time constraints. Secondly, it was not possible to investigate the parasitic elements of the output filter capacitor. On the topic of this project, the series inductance and series resistance would be the following subject to investigate. Regrettably, due to the form factor of the hardware, it was a laborious task to properly mount the parasitic elements in series with the output filter capacitor. Therefore, it was promptly decided to limit the scope of the investigation to the inductor parasitic elements. This is ideal for a subsequent investigation to broaden the scope of model parameters to comprehensively examine the serial resistance and inductance of the output filter capacitor. Another case for future investigation could be more thoroughly account for the inner control loop (LQR) in regards to parasitic elements. It is conceivable this can be investigated further to include parasitic elements in the state space model when designing the parameters of the inner control loop.

Chapter 7: Bibliography

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Appendix A: Circuit Schematics

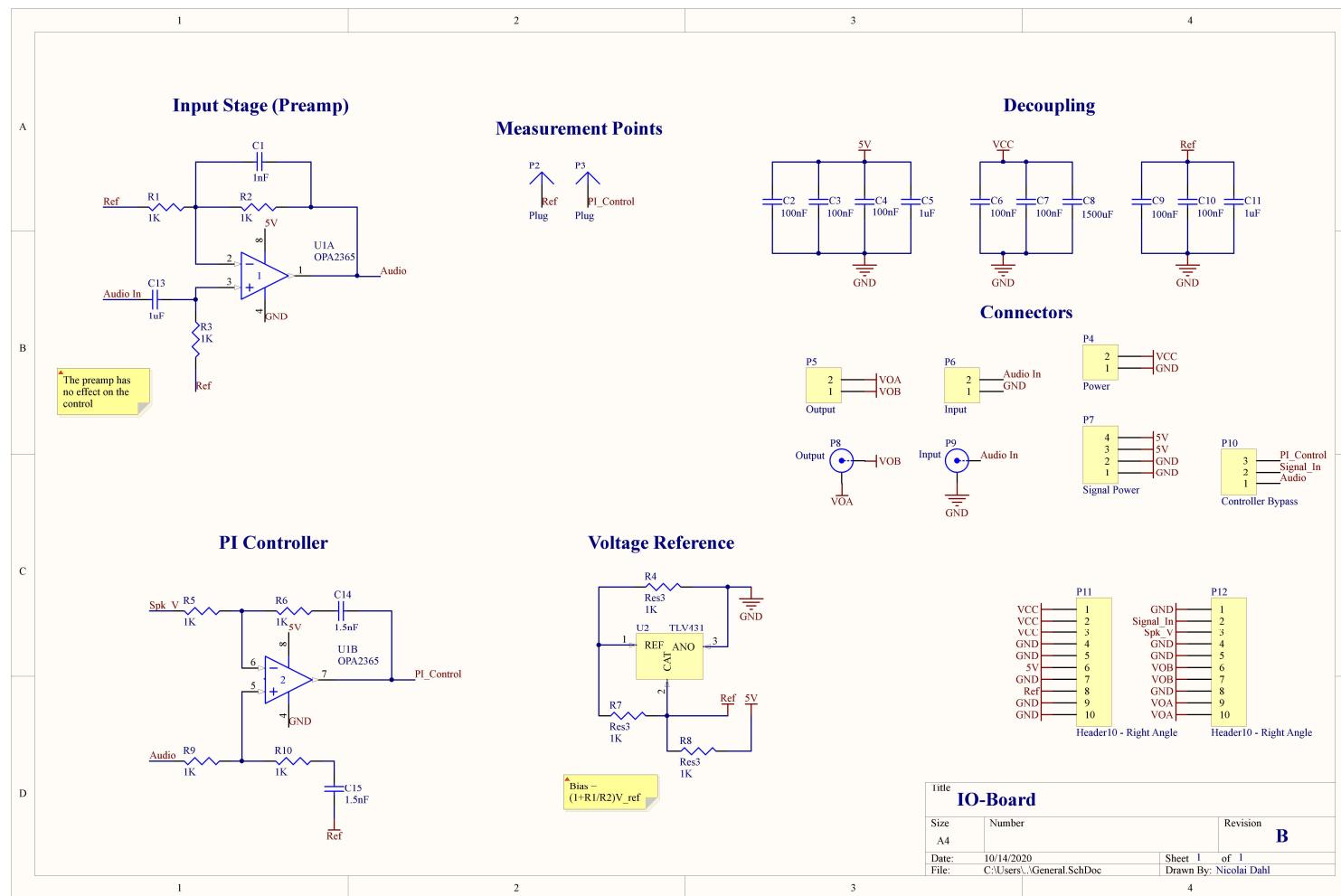


Figure A.1: Schematic of IO Board [14]

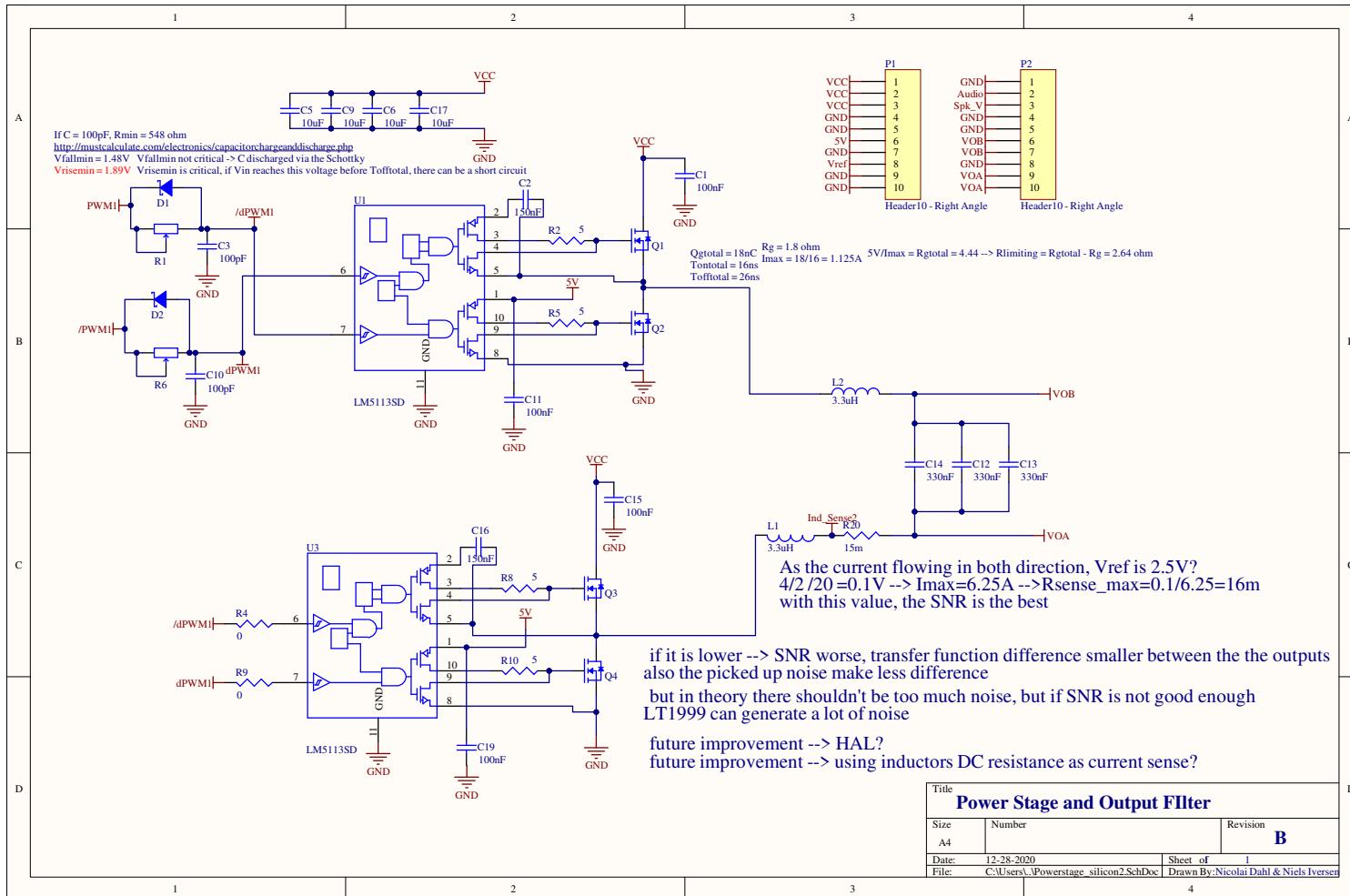


Figure A.2: Schematic of Power Stage [14]

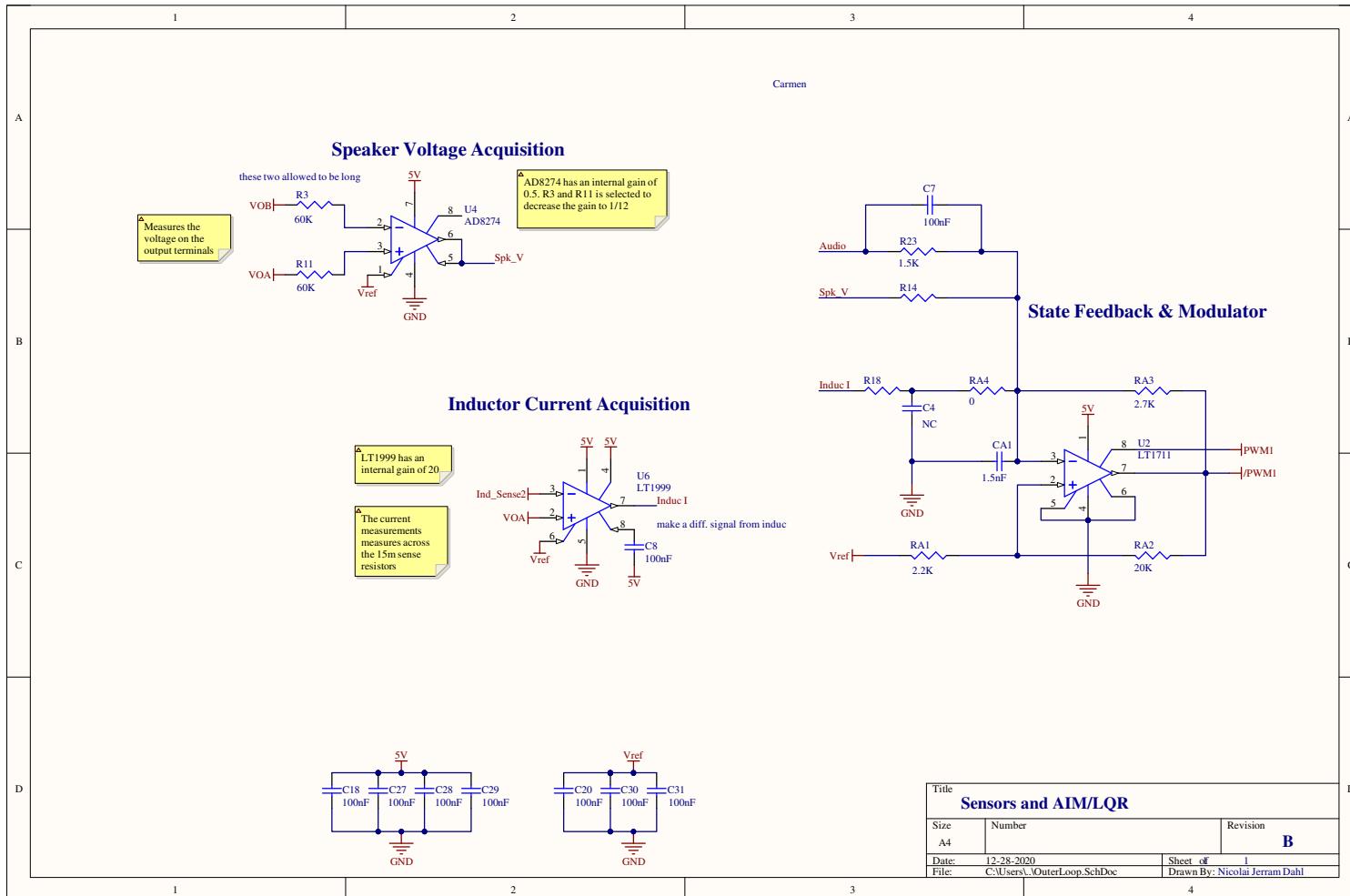


Figure A.3: Schematic of Outer Loop [14]

Appendix B: Measurement setups

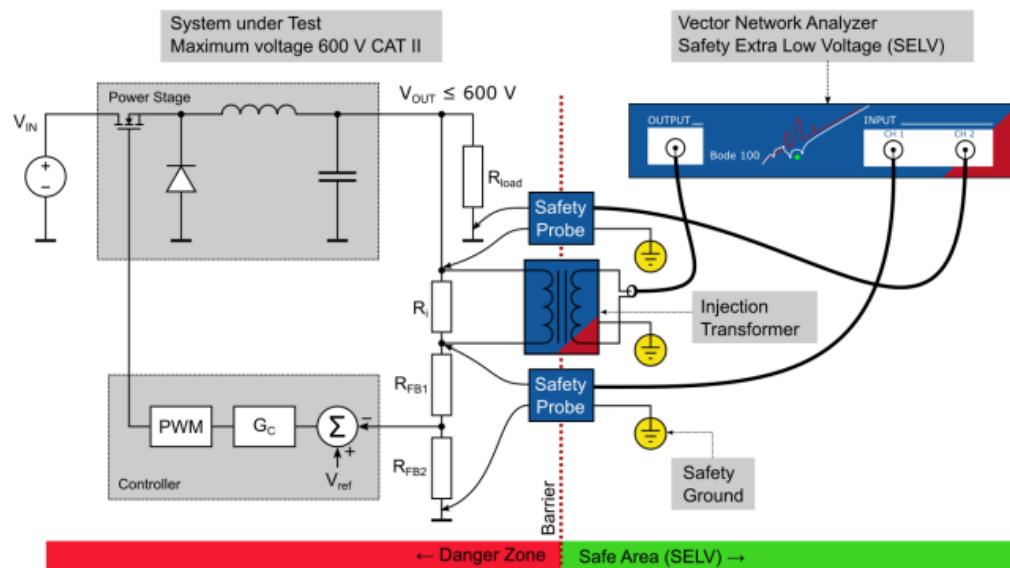


Figure 4-1: Typical measurement setup

More details and information about the loop gain measurement can be found in our application note section at: <https://www.omicron-lab.com/>

Figure B.1: Typical measurement set-up of injection transformer in feedback loop from user manual [17]

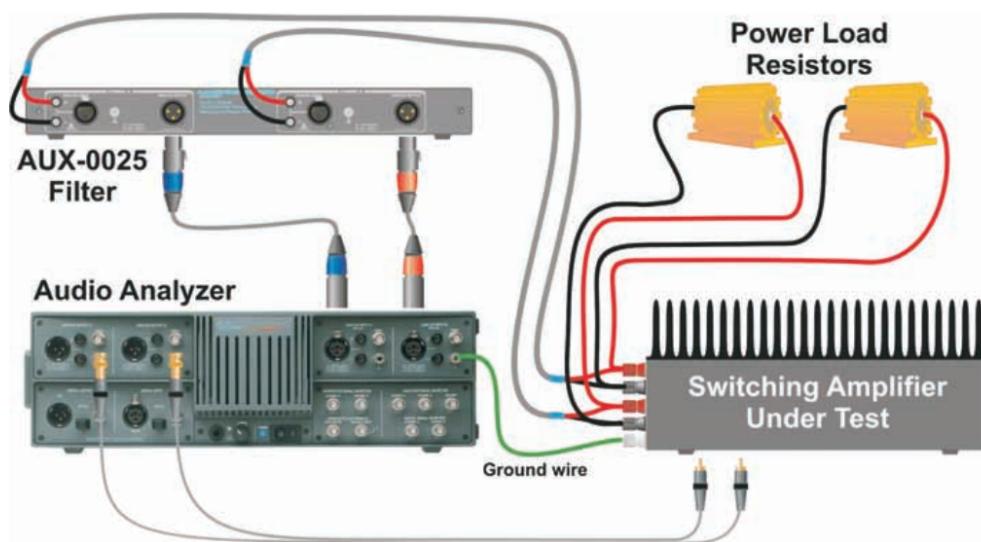


Figure 5. Recommended test setup using the AUX-0025. Note that the connections to the load are independent of the connections to the filter and analyzer.

Figure B.2: Typical measurement set-up of Audio Precision APx500 audio analyzer from white paper [2]

Appendix C: LTspice

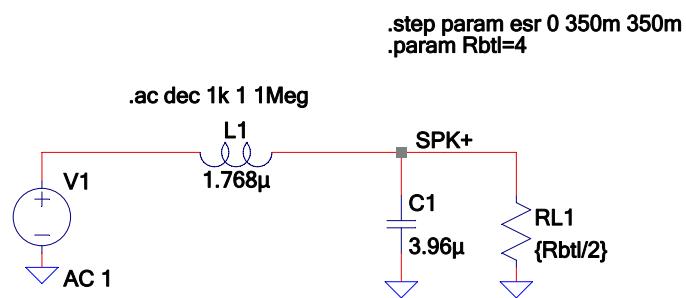


Figure C.1: Small signal analysis of output filter

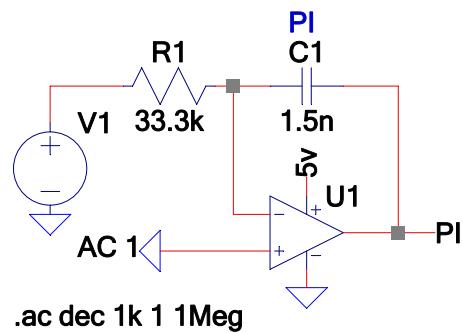


Figure C.2: Small signal analysis of PI controller

```
.param c_esl=100n c_esr=300m *step param c_esr 0 300m 300m
.param l_esr=300m c_l=120p      *.step param c_esl 0 100n 100n
```

```
.ac dec 1k 1 1Meg    .param Rbtl=4 Cctl=1.98u Lind=1.768u
```

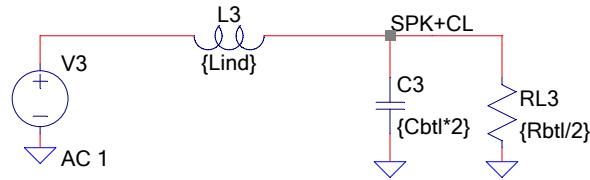
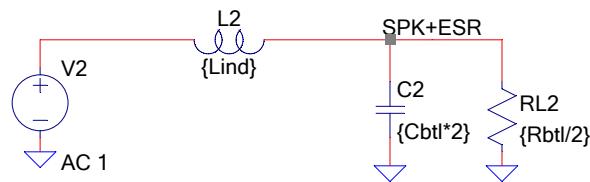
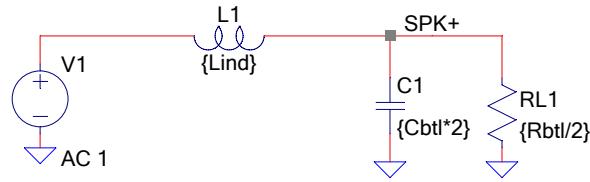


Figure C.3: Small signal analysis of output filter parasitic elements

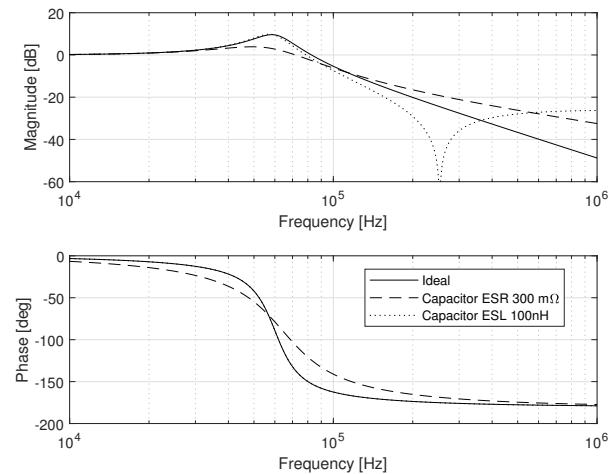


Figure C.4: Bode plot of output filter using ideal LC filter, parasitic elements in capacitor

It is noted that adding series resistance and inductance to the output capacitor results in a deviating magnitude and higher roll-off at around -25 dB in the stopband of high frequency compared to both other curves. To determine the amplitude gain:

$$10^{\frac{-25 \text{ dB}}{10}} = 5.6\%$$

meaning 5.6% of the signal is preserved on control loop that returns to the input. Based on this initial hypothesis, it is theorised that parasitic elements in the output capacitor have the greatest altering effect on the transfer function of the control loop.

Appendix D: Amplifier analysis

D.1 Efficiency (Simulation)

To assess the efficiency of the system, an analysis is performed by measuring the power being drawn from the supply and comparing it with the power being delivered to the load. The means is to calculate the efficiency η , where:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \quad (\text{D.1})$$

This is undertaken by implementing a set of SPICE parameters in the simulation, where:

$$P_{\text{in}} = P_{E1} + P_{E2} \quad (\text{D.2a})$$

$$P_{\text{out}} = V_{R_{\text{BTL}}} \cdot I_{R_{\text{BTL}}} \quad (\text{D.2b})$$

In Equation (D.2a), the sources $E1$ and $E2$ is the power stage voltage supply, a source from each half-bridge. In Equation (D.2b), the voltage across the load in the bridge-tied-load is multiplied by the current through the bridge-tied-load, it provides the output power. Analysed across an output power sweep it yields the following results:

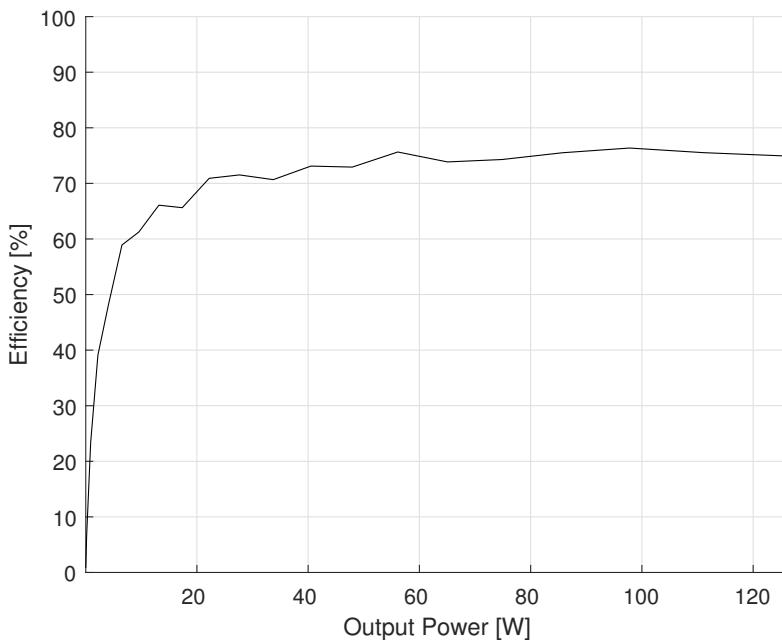


Figure D.1: Amplifier efficiency across a varying output power

As seen in Figure D.1, there is a rather low efficiency in the low output power range, but as the output power increases, the efficiency increases accordingly. Plotted are amplifier with inductor ESR used in the differential filter output from the control loop measurements. The output power seems to taper off at around 75 %, also a somewhat

low efficiency for a class-D amplifier. However, as the serial resistance of the inductor, from an efficiency standpoint, is unreasonably large. It is seen that it would impact the power stage substantially in regards to the efficiency of the amplifier. One thing to note, however, is that this analysis does not account for the low-voltage power rail for the preamplifier, modulation and control loop. This would presumably lower the efficiency slightly if taken into account.

D.2 Total Harmonic Distortion + Noise (Hardware)

A THD+N test was done to get an idea of the distortion factor. THD+N is a measurement of the harmonic distortion present in the output signal. It is defined by the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency signal. In an audio system, the lower THD+N means the more accurate representation of the input signal is obtained at the output.

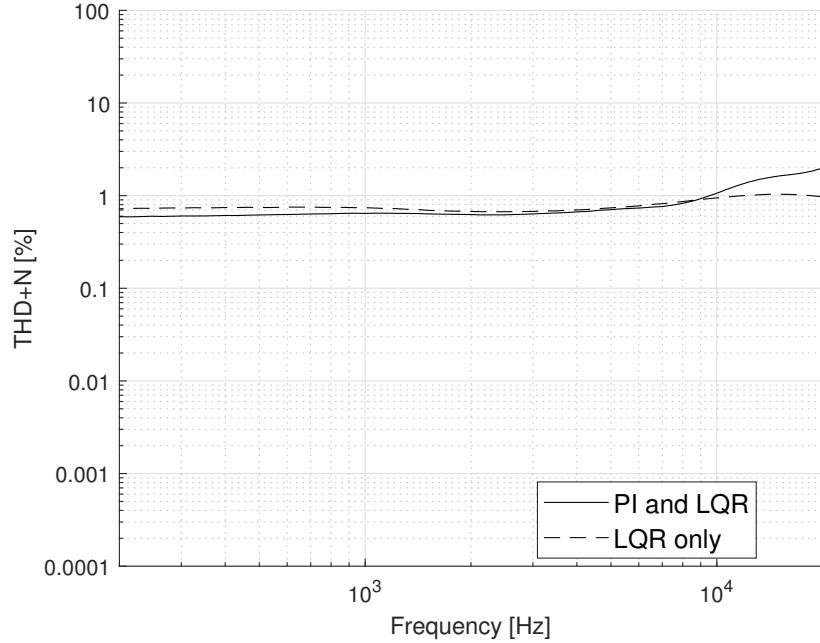


Figure D.2: THD+N of amplifier without and with feedback loop

Seen in Figure D.2 is the measured THD+N from the measurement setup with APx500 Audio Analyzer [8] in Figure B.2. In a practical sense, the analysis is performed by inputting a controlled sine wave sweep, filtering the output signal and comparing the ratio. This is described by the following expression:

$$\text{THD} + \text{N} = \frac{\sum_{n=2}^{\infty} \text{harmonics} + \text{noise}}{\text{fundamental}} \quad (\text{D.3})$$

Seen in Equation D.3 is a mathematical expression of the calculation done by the audio analyzer.

D.3 Control loop simulation

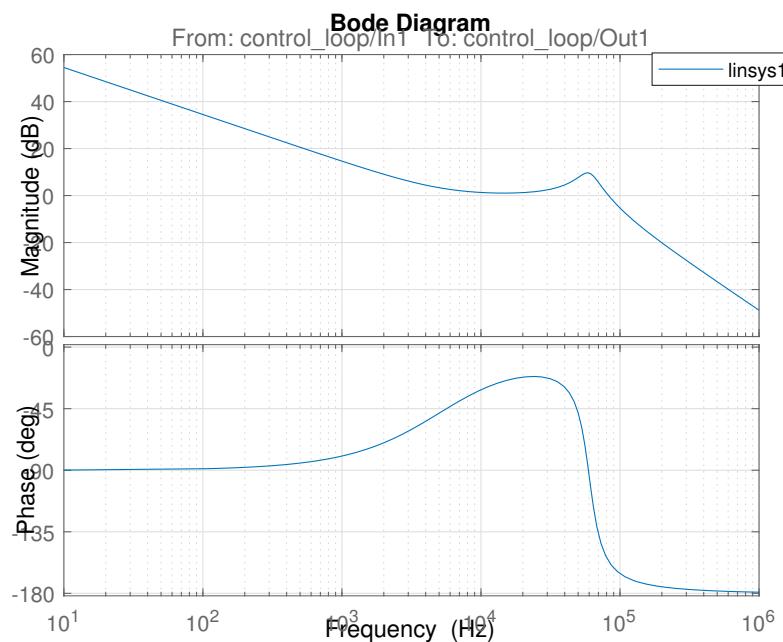


Figure D.3: Control loop figure form Simulink

Appendix E: MATLAB code

Listing E.1: SimpleModulator.m

```

1 clc; clear all; close all;
2 Simulation_Time = 1;
3 input = 1.5; % Signal frekvens
4
5 sim('PWM_modulation1',Simulation_Time)
6
7
8 % Plot switching frequency
9 figure(1)
10 hold on
11 plot(get(ans,'pwm'),'—','color','black')
12 plot(get(ans,'input'),'—','color','black')
13 plot(get(ans,'carrier'),':','color','black')
14 xlabel('Normalised time [s]')
15 ylabel('Normalised amplitude [V]');
16 legend({'PWM','Input','Carrier'},'FontSize',12,'Location','northeast')
    )
17 grid on
18 hold off

```

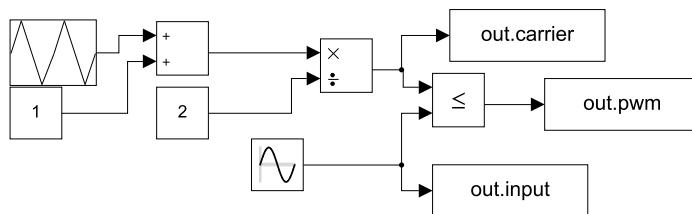


Figure E.1: Simulink model for a PWM generator

Listing E.2: Regulator Calculation.m

```

1 clc; close all; clear all
2
3 global Ai Bi Br C Ci dcg t
4 %% Insert filter values
5 Rspk = 4; %Speaker Resistance
6 Cf = 1.98*1e-6 %Filter Capacitance

```

```

7 Lind = 1.7684*1e-6      %Filter Inductance
8 Rind = 15*1e-3;          %Shunt resistance
9 gain = 25;               %Amplifier Gain
10
11 Rin = 1500;             %Input Resistor of Aim
12
13 %% Tuning Parameters
14
15 Ki = 20000; %Integrator weight
16 gu = pi; %Damping weight
17
18 %% Dynamic Model
19
20 % Converting to single-ended parameters
21 Cf = Cf*2; Rspk = Rspk/2;
22
23 % State Space Model
24 A = [-Rind/Lind, -1/Lind;
25           1/Cf, -1/(Cf*Rspk)];
26 B = [gain/Lind; 0];
27 C = [0 1];
28
29 G = ss(A, B, [C;zeros(2)], 0);
30 dcg = dcgain(G); dcg = dcg(1);
31
32 %Plotting Bode plot and Step Response
33 figure(1)
34 bode(G)
35 legend('Plant')
36 grid on
37
38 figure(2)
39 step(G)
40 legend('Plant')
41 grid on
42
43 %% Integrator Augmentation
44
45 Ai = [A,zeros(2,1);-C/gain,0];
46 Bi = [B;0];
47 Ci = [C,0];
48 Br = [0;0;1];
49
50 %% LQR — No integrator
51
52 R2 = gu;
53 R1 = C'*dcg^-2*C*2;

```

```

54 N = -dcg^-1*C';
55
56 K1 = lqr(A,B,R1,R2,N);
57 K = [K1,-Ki];
58 sys1 = ss(Ai-Bi*K,Br+Bi,[Ci;-K;0,0,-K(3)],[0;1;0])
59
60 %Plotting Bode plot and Step Response
61 % figure(1); hold on
62 % bode(sys1)
63 % legend('Plant','LQR')
64 % hold off
65
66 figure(2); hold on
67 step(sys1)
68 legend('Plant','LQR')
69 hold off
70
71 %% Controller Components
72
73 PI.C = 1.5e-9;
74 PI.R1 = 1/(PI.C*Ki);
75 PI
76
77 tau_i = PI.C*PI.R1
78
79 Kim(1) = K(1)*3.33*2; %Remember to multiply by 2 when implementing
    for BTL
80 Kim(2) = K(2)*gain;
81 LQR.Rk = abs(Rin./Kim(1:2))
82
83
84 return
85 %%
86
87 SIMTIME = 0.00005;
88 Ts = SIMTIME*1e-4;
89 t = 0:Ts:SIMTIME;
90
91 x = particleswarm(@Control_Designer, 3,[0.01;4*1e5],[5; 1e6]);
92 x(3) = 1;
93
94 R2 = x(1);
95 R1 = C'*dcg^-2*C*2;
96 N = -dcg^-1*C';
97
98 K1 = lqr(A,B,R1,R2,N);
99 K = [K1,-x(2)];

```

```

100
101 sys = ss(Ai-Bi*K,Br+Bi*x(3),[Ci;-K;0,0,-K(3)],[0;x(3);0]);
102
103 figure(3)
104 step(G,t); hold on
105 step(sys,t); hold off
106 grid on
107
108
109 %%
110 function [J] = Control_Designer(Q)
111
112 global Ai Bi Br C Ci dcg t
113
114 R2 = Q(1);
115 R1 = C'*dcg^2*C*2;
116 N = -dcg^1*C';
117
118 K = lqr(Ai(1:2,1:2),Bi(1:2),R1,R2,N);
119 K = [K,-Q(2)];
120
121 % Forming Closed-Loop System
122 sys = ss(Ai-Bi*K,Br+Bi,Ci,0);
123
124 % Calculating Step Response
125 y = step(sys,t)/dcgain(sys);
126
127 % Calculating the cost
128 J = sum((1-y).^2);
129 %J = sum(abs(1-y));
130 %J = t*abs(1-y);
131 end

```

Listing E.3: Inductor Design.m

```

1 %% Clear workspace
2 clc
3 clear all
4 close all
5
6 %% Design specifications
7 % Amplifier
8 L = 1.768e-6; % Inductance
9 V_cc = 30; % Rail-to-rail voltage
10 R_spk = 4; % Speaker load

```

```

11 I_max      = V_cc/R_spk;           % Max output current
12                                     [A]
13 %
14 core       = ['T80-2'; 'T94-2'];    % Core type
15 B_sat     = [400e-3, 400e-3];      % Max allowable flux density
16                                     [T]
17 A_ef      = [.231e-4, .362e-4];   % Effective cross-sectional area
18                                     [m^2]
19 A_L        = [5.5e-9, 8.4e-9];     % Inductance rating
20                                     [H/N^2]
21 %
22 % Core physical dimensions
23 OD         = [20.2e-3, 23.9e-3];  % Outer diameter
24                                     [m]
25 ID         = [12.6e-3, 14.2e-3];  % Inner diameter
26                                     [m]
27 Ht         = [6.35e-3, 7.92e-3];  % Height/thickness
28                                     [m]
29 l          = [5.14e-2, 5.97e-3];  %
30 %
31 %
32 % Wire specifications
33 D_wire     = 0.95e-3;             % Wire diameter
34 %
35 %%
36 % Calculations
37 vectorSize = size(core,1);
38 N          = zeros(1,vectorSize);
39 B          = zeros(1,vectorSize);
40 %
41 %
42 % Calculate required number of turns N and peak core flux B
43 for i=1:vectorSize
44     N(i)      = (L/A_L(i))^(1/2);
45     B(i)      = (L*I_max) / (A_ef(i) * N(i));
46 end
47 %
48 %
49 % Calculate minimum required wire length
50 l_wire     = zeros(1,vectorSize);
51 for i=1:vectorSize
52     r_mean   = OD(i)/2 - (OD(i)-ID(i))/4;
53     l_wire(i) = N(i) * (2*Ht(i)+ (OD(i)-ID(i)) + 4*D_wire) + 2*pi*
54         r_mean;
55 end
56 %
57 %
58 % Print results
59 fprintf('\nDESIGN SPECIFICATIONS\n')
60 fprintf(['L      = ' num2str(L*1e6) ' uH\n'])
61 fprintf(['V_cc  = ' num2str(V_cc) ' V\n'])
62 fprintf(['R_spk = ' num2str(R_spk) ' ohm\n'])

```

```

50 fprintf(['I_max      = ' num2str(I_max) ' A\n'])
51
52 for i=1:vectorSize
53     fprintf('
54     fprintf(['\nCORE ' core(i,:)\n'])
55     fprintf('parameters:\n')
56     fprintf(['B_sat      = ' num2str(B_sat(i)*1e3) ' mT\n'])
57     fprintf(['A_ef       = ' num2str(A_ef(i)*1e4) ' cm^2\n'])
58     fprintf(['A_L        = ' num2str(A_L(i)*1e9) ' nH/N^2\n'])
59     fprintf('results:\n')
60     fprintf(['N          = ' num2str(N(i)) ' turns\n'])
61     fprintf(['B          = ' num2str(B(i)*1e3) ' mT\n'])
62     fprintf(['l_wire    = >' num2str(l_wire(i)*1e2) ' cm\n'])
63     fprintf('Evaluation: ')
64     if (B(i) < B_sat(i))
65         fprintf('Valid design (B < B_sat)\n')
66     else
67         fprintf('Invalid design (B > B_sat)\n')
68     end
69 end

```

Listing E.4: Simulation Script.m

```

1 %% Clear all
2 clear all
3 close all
4 clc
5 %% Set up parameters in circuit
6 % Supply parameters
7 Vs = 5;
8 Vref = 2.5;
9 % Input signal parameters
10 InDC = 2.5;
11 InAmpl = 0.9;
12 InFreq = 10e3;
13 InDelay = 200e-6;
14 % Modulator parameters
15 Rin = 1.5e3;
16 Rfb = 2.7e3;
17 C_aim = 1.5e-9;
18 Cin = 1e-15;
19 R1 = 2.21e3;
20 % Notat: Open loop fungerer bedst med 2.2k og closed loop fungerer
21 % bedst
22 % med 1k (?)
23 R2 = 20e3;
24 % Output filter parameters
25 Lind = 1.768e-6;

```

```

25 Cctl = 1.98e-6;
26 Rctl = 4;
27 shunt = 15e-3;
28 % Control loop parameters
29 R_cur_sense_fb = 16e3;
30 R_spkv_fb = 8.3e3;
31 R_voltacq = 60e3;
32 C_cur_ref = 0.1e-6;
33 % PI controller
34 R_pic = 40e3;
35 C_pic = 1e-6;
36 % Simulation control
37 SimStop = 600e-6;
38 SimDelay = 200e-6;
39 MaxDeltaT = 5e-9;
40 % Schmitt trigger hysteresis
41 Vt = 2.5;
42 Vh = 0.05;
43
44 %% CIRCUIT: CLASSD OPEN LOOP
45 %% Export data to SPICE directive files
46 % Add circuit models
47 %FID_models = fopen('../LTspice/models.txt', 'w');
48 %fprintf(FID_models, '.model SW SW(Vt=%d)\n', V_t);
49 %fprintf(FID_models, '.model D_SW D(Ron=%d Roff=%d Vfwd=%d Vrev=%d)\n'
50 %      ', R_on_SW, R_off_SW, V_fwd_SW, V_rev_SW);
51 %fprintf(FID_models, '.model D D(Ron=%d Roff=%d Vfwd=%d Vrev=%d)\n',
52 %      R_on_D, R_off_D, V_fwd_D, V_rev_D);
53 %fclose(FID_models);
54
55 % Circuit: Class D open loop
56 path_LTSpice = '"C:/Program Files/LTC/LTspiceXVII/XVIIx64.exe"';
57 circuit_path = 'C:/Users/JeppeLaptop/Danmarks Tekniske Universitet/
58             BEng Jeppe audio amplifier control loop - General/
59             Simuleringsfiler/classd_openloop/';
60 circuit_name = 'classd_open';
61 command = ' -Run -ascii -b ';
62
63 % Add circuit parameters
64 FID_param = fopen([append(circuit_path, 'param.txt')], 'w');
65 % Define components and parameters
66 param_nam = ["Vs", "Vref", "InDC", "InAmpl", "InFreq", "InDelay", "
67             Rin", "Rfb", "C_aim", "Cin", "R1", "R2", "Cctl", "Rctl", "shunt",
68             "R_cur_sense_fb", "R_spkv_fb", "R_voltacq", "C_cur_ref", "R_pic
69             ", "C_pic", "SimStop", "SimDelay", "MaxDeltaT"];
70 param_val = [Vs, Vref, InDC, InAmpl, InFreq, InDelay, Rin, Rfb, C_aim

```

```

    , Cin, R1, R2, Cctl, Rctl, shunt, R_cur_sense_fb, R_spkv_fb,
    R_voltacq, C_cur_ref, R_pic, C_pic, SimStop, SimDelay, MaxDeltaT
];
65 % Define symmetrical components (will be printed for pos and neg
% circuit)
66 param_nam_sym = ["Lind"];
67 param_val_sym = [Lind];
68 % Export parameters to external file
69 for i=1:length(param_nam)
70     fprintf(FID_param, '.param %s = %d\n', param_nam(i), param_val(i))
71 end
72 % Export symmetrical parameters to external file
73 for i=1:length(param_nam_sym)
74     fprintf(FID_param, '.param %s_P = %d\n', param_nam_sym(i),
75             param_val_sym(i));
76     fprintf(FID_param, '.param %s_N = %d\n', param_nam_sym(i),
77             param_val_sym(i));
78 end
79 fclose(FID_param);
80 %% Simulate and import data
81 % Run LTSpice simulation
82 command = [path_LTSpice command ...
83             circuit_path circuit_name '.asc'
84 ];
85 dos(command);
86 % Import data
87 raw_data = LTspice2Matlab([circuit_path circuit_name '.raw']);
88 % Display variables
89 fprintf('var \t name\n')
90 for i=1:raw_data.num_variables
91     fprintf('%d \t %s \n', raw_data.selected_vars(i), raw_data.
92             variable_name_list{i})
93 end
94 %% Plot data
95 % Trace numbers
96 var_input = 1;
97 var_spk_p = 2;
98 var_spk_m = 3;
99
100 Open_TimeVect = raw_data.time_vect;
101 Open_varspk_p = raw_data.variable_mat(var_spk_p,:);
102 Open_varspk_m = raw_data.variable_mat(var_spk_m,:);
103 Open_input = raw_data.variable_mat(var_input,:);
104
105 figure(1)

```

```

103 subplot(2,1,1)
104 hold on
105 plot(raw_data.time_vect, raw_data.variable_mat(var_spk_p,:), '—k');
106 plot(raw_data.time_vect, raw_data.variable_mat(var_spk_m,:), ':k');
107 title(sprintf('Waveform %s and %s', raw_data.variable_name_list{
108     var_spk_p},raw_data.variable_name_list{var_spk_m}));
109 grid on
110 ylabel(raw_data.variable_type_list{var_input});
111 xlabel('Time [sec]');
112 xlim([SimDelay,SimStop]);
113 ylim([min(raw_data.variable_mat(var_input,:)),max(raw_data.
114     variable_mat(var_input,:))])
115 legend(raw_data.variable_name_list{var_spk_p}, raw_data.
116     variable_name_list{var_spk_m}, 'location','best');
117 hold off
118 subplot(2,1,2)
119 hold on
120 plot(raw_data.time_vect, (raw_data.variable_mat(var_spk_p,:)-raw_data
121     .variable_mat(var_spk_m,:)), 'k');
122 title(sprintf('Waveform %s-%s', raw_data.variable_name_list{var_spk_p
123     },raw_data.variable_name_list{var_spk_m}));
124 grid on
125 ylabel(raw_data.variable_type_list{var_spk_p});
126 xlabel('Time [sec]');
127 xlim([SimDelay,SimStop]);
128 ylim([min(raw_data.variable_mat(var_spk_p,:)-raw_data.variable_mat(
129     var_spk_m,:)),max(raw_data.variable_mat(var_spk_p,:)-raw_data.
130     variable_mat(var_spk_m,:))])
131 legend(sprintf('%s-%s', raw_data.variable_name_list{var_spk_p},
132     raw_data.variable_name_list{var_spk_m}));
133 hold off
134 %sgt = sgtitle('Open loop','Color','black');
135 %sgt.FontSize = 20;
136
137 %% CIRCUIT: CLASSD REGULATOR
138 %% Export data to SPICE directive files
139 % Add circuit models
140 FID_models = fopen('../LTspice/models.txt', 'w');
141 fprintf(FID_models, '.model SW SW(Vt=%d)\n', V_t);
142 fprintf(FID_models, '.model D_SW D(Ron=%d Roff=%d Vfwd=%d Vrev=%d)\n
143     ', R_on_SW, R_off_SW, V_fwd_SW, V_rev_SW);
144 fprintf(FID_models, '.model D D(Ron=%d Roff=%d Vfwd=%d Vrev=%d)\n',
145     R_on_D, R_off_D, V_fwd_D, V_rev_D);
146 fclose(FID_models);
147
148 % Circuit: Class D open loop
149 path_LTSpice = '"C:/Program Files/LTC/LTspiceXVII/XVIIx64.exe"';
```

```

140 circuit_path = 'C:/Users/JeppeLaptop/Danmarks Tekniske Universitet/
    BEng Jeppe audio amplifier control loop — General/
    Simuleringsfiler/classd_PI_LQR/';
141 circuit_name = 'classd_PI_LQR';
142 command = ' -Run -ascii -b ';
143
144 % Add circuit parameters
145 FID_param = fopen(append(circuit_path,'param.txt'), 'w');
146 % Define components and parameters
147 param_nam = ["Vs", "Vref", "InDC", "InAmpl", "InFreq", "InDelay", "
    Rin", "Rfb", "C_aim", "Cin", "R1", "R2", "Cctl", "Rctl", "shunt",
    "R_cur_sense_fb", "R_spkV_fb", "C_cur_ref", "R_pic", "C_pic", "
    SimStop", "SimDelay", "MaxDeltaT"];
148 param_val = [Vs, Vref, InDC, InAmpl, InFreq, InDelay, Rin, Rfb, C_aim
    , Cin, R1, R2, Cctl, Rctl, shunt, R_cur_sense_fb, R_spkV_fb,
    C_cur_ref, R_pic, C_pic, SimStop, SimDelay, MaxDeltaT];
149 % Define symmetrical components (will be printed for pos and neg
    circuit)
150 param_nam_sym = ["Lind", "R_voltacq"];
151 param_val_sym = [Lind, R_voltacq];
152 % Export parameters to external file
153 for i=1:length(param_nam)
    fprintf(FID_param, '.param %s = %d\n', param_nam(i), param_val(i)
        );
154 end
155 % Export symmetrical parameters to external file
156 for i=1:length(param_nam_sym)
    fprintf(FID_param, '.param %s_P = %d\n', param_nam_sym(i),
        param_val_sym(i));
    fprintf(FID_param, '.param %s_N = %d\n', param_nam_sym(i),
        param_val_sym(i));
157 end
158 fclose(FID_param);
159 %% Simulate and import data
160 % Run LTSpice simulation
161 command = [path_LTSpice command ''' circuit_path circuit_name '.asc''
    ];
162 dos(command);
163
164 % Import data
165 raw_data = LTspice2Matlab([circuit_path circuit_name '.raw']);
166
167 %Print variables
168 fprintf('var \t name\n')
169 for i=1:raw_data.num_variables
    fprintf('%d \t\t %s \n', raw_data.selected_vars(i), raw_data.
        variable_name_list{i})
170
171
172
173

```

```

174 end
175 %% Plot data
176 % Trace numbers
177 var_spk_p = 1;
178 var_spk_m = 2;
179 var_input = 20;
180 var_aim_n = 8;
181 var_aim_p = 10;
182
183 Regulator_TimeVect = raw_data.time_vect;
184 Regulator_varspk_p = raw_data.variable_mat(var_spk_p,:);
185 Regulator_varspk_m = raw_data.variable_mat(var_spk_m,:);
186
187 figure(2)
188 subplot(2,1,1)
189 hold on
190 plot(raw_data.time_vect, raw_data.variable_mat(var_spk_p,:), '--k');
191 plot(raw_data.time_vect, raw_data.variable_mat(var_spk_m,:), ':k');
192 title(sprintf('Waveform %s and %s', raw_data.variable_name_list{
    var_spk_p},raw_data.variable_name_list{var_spk_m}));
193 grid on
194 ylabel(raw_data.variable_type_list{var_spk_p});
195 xlabel('Time [sec]');
196 xlim([SimDelay,SimStop]);
197 ylim([min(raw_data.variable_mat(var_input,:)),max(raw_data.
    variable_mat(var_input,:))])
198 legend(raw_data.variable_name_list{var_spk_p}, raw_data.
    variable_name_list{var_spk_m}, 'location','best');
199 hold off
200 subplot(2,1,2)
201 hold on
202 plot(raw_data.time_vect, (raw_data.variable_mat(var_spk_p,:)-raw_data
    .variable_mat(var_spk_m,:)), 'k');
203 title(sprintf('Waveform %s-%s', raw_data.variable_name_list{var_spk_p}
    ,raw_data.variable_name_list{var_spk_m}));
204 grid on
205 ylabel(raw_data.variable_type_list{var_spk_p});
206 xlabel('Time [sec]');
207 xlim([SimDelay,SimStop]);
208 ylim([min(raw_data.variable_mat(var_spk_p,:)-raw_data.variable_mat(
    var_spk_m,:)),max(raw_data.variable_mat(var_spk_p,:)-raw_data.
    variable_mat(var_spk_m,:))])
209 legend(sprintf('%s-%s', raw_data.variable_name_list{var_spk_p},
    raw_data.variable_name_list{var_spk_m}));
210 hold off
211 %sgt = sgtitle('PI+LQR closed loop','Color','black');
212 %sgt.FontSize = 20;

```

```

213
214 figure(3)
215 plot(raw_data.time_vect, raw_data.variable_mat(var_aim_n,:), '-k');
216 hold on
217 plot(raw_data.time_vect, raw_data.variable_mat(var_aim_p,:), '-k');
218 title(sprintf('Waveform %s and %s', raw_data.variable_name_list{
    var_aim_p},raw_data.variable_name_list{var_aim_n}));
219 grid on
220 xlabel('Time [sec]');
221 ylabel(raw_data.variable_type_list{var_aim_p});
222 xlim([SimDelay,SimDelay+5e-6]);
223 ylim([2,3]);
224 legend(raw_data.variable_name_list{var_aim_p}, raw_data.
    variable_name_list{var_aim_n}, 'location','best');
225 hold off
226 %% Plot both open and regulator
227 figure(3)
228 hold on
229 plot(Regulator_TimeVect, (Regulator_vars_pk_p-Regulator_vars_pk_m), '-',
    'color','black');
230 plot(Open_TimeVect, (Open_vars_pk_p-Open_vars_pk_m), '-','color','blue')
    ;
231 ylabel(raw_data.variable_type_list{var_spk_p});
232 xlabel('Time [sec]');
233 xlim([SimDelay,SimStop]);
234 legend({'PI+LQR','Open loop'},'FontSize',12,'Location','best')
235 hold off

```

Listing E.5: sim matlab importer.m

```

1 %% Clear all
2 clear all
3 close all
4 clc
5 %% Set up
6 circuit_path = 'C:\Users\JeppeLaptop\Danmarks Tekniske Universitet\
    BEng Jeppe audio amplifier control loop - General\
    Simuleringsfiler';
7 circuit_name = '2020-11-24 - self oscillating class-d cleanup test
    filter_v2';
8
9 raw_data = LTspice2Matlab([circuit_path circuit_name '.raw']);
10
11 %% Plot results
12 % Display plot variables
13 fprintf('PLOT VARIABLES\nvar \t name\n')
14 for i=1:raw_data.num_variables
15     fprintf('%d \t\t %s \n', raw_data.selected_vars(i), raw_data.

```

```

    variable_name_list{i})
16 end
17
18 % Define plot variables
19 var_V_signal_in = 1; % Input voltage
20 var_v_SPKP = 2; % Switch voltage
21 var_v_SPKM = 3; % Resonant tank voltage
22 var_V_rec = 4; % Diode voltage
23 var_V_o = 5; % Output voltage
24 var_I_D = 6; % Diode current
25 var_I_L_R = 7; % Resonant tank current
26 var_I_Lf = 8; % Input current
27 var_I_o = 9; % Output current
28 var_i_SW = 10; % Switch current
29
30 %% waveforms+calculations
31 % Calculate output power and resonant component voltages
32 %V_CR = raw_data.variable_mat(var_v_SPKP,:)-raw_data.
33 %variable_mat(var_v_SPKM,:);
33 %V_LR = raw_data.variable_mat(var_v_SPKM,:)-raw_data.
34 %variable_mat(var_V_rec,:);
34 V_R_BTL = raw_data.variable_mat(var_v_SPKP,:)-raw_data.
35 %variable_mat(var_v_SPKM,:);
35
36 % Plots
37 figure(1)
38 % V_IN and v_SW
39 subplot(2,1,1)
40 plot(raw_data.time_vect, raw_data.variable_mat(var_V_signal_in,:), 'k
41 ');
41 hold on
42 %plot(raw_data.time_vect, raw_data.variable_mat(var_v_SPKP,:), 'k', '
43 %linestyle', '—');
43 hold off
44 %legend('Input voltage', 'Switch voltage')
45 grid on
46 xlim([min(raw_data.time_vect) max(raw_data.time_vect)])
47 title('Input voltage V_{IN}');
48 ylabel('Voltage [V]');
49 xlabel('Time [s]');
50 % Output voltage and diode voltage
51 subplot(2,1,2)
52 %plot(raw_data.time_vect, raw_data.variable_mat(var_V_o,:), 'k', '
53 %linestyle', '—');
53 plot(raw_data.time_vect, V_R_BTL, 'k', 'linestyle', '-');
54 hold on
55 %plot(raw_data.time_vect, raw_data.variable_mat(var_V_rec,:), 'k');

```

```

56 hold off
57 %legend('Output voltage', 'Diode voltage')
58 grid on
59 xlim([min(raw_data.time_vect) max(raw_data.time_vect)])
60 title('Output voltage across bridge-tied-load R_{L}');
61 ylabel('Voltage [V]');
62 xlabel('Time [s]');
63
64 % Export
65 fig_width = 25;
66 fig_height = 25;
67 %set(gcf,'paperunits','centimeters','Paperposition',[0 0 fig_width
68 %      fig_height]);
68 %set(gcf,'units','centimeters','Position',[0 1 fig_width fig_height])
69 ;
70 %saveas(gcf, 'figures_con/waveforms.eps', 'epsc')
71 %saveas(gcf, 'figures_con/waveforms_tuned.eps', 'epsc')
72 %% Plot preamp input filter ac
73 % load
74 circuit_path = 'C:\Users\JeppeLaptop\Danmarks Tekniske Universitet\
75     BEng Jeppe audio amplifier control loop - General\
76     Simuleringsfiler\Simuleringsarkiv\' ;
77 circuit_name = 'input_filter';
78 raw_data = LTspice2Matlab([circuit_path circuit_name '.raw']);
79 % Display variables
80 fprintf('var \t name\n')
81 for i=1:raw_data.num_variables
82     fprintf('%d \t %s \n', raw_data.selected_vars(i), raw_data.
83             variable_name_list{i})
84 end
85 var_out = 3;
86 Log_Magnitude_dB = 20*log10(abs(raw_data.variable_mat(var_out,:)));
87 Norm_Phase_Degrees = angle(raw_data.variable_mat(var_out,:))*180/pi;
88 Freq_Vect = raw_data.freq_vect;
89 figure(2)
90 subplot(2,1,1)
91 semilogx(Freq_Vect, Log_Magnitude_dB, 'k');
92 hold on
93 grid on
94 xlim([min(raw_data.freq_vect) max(raw_data.freq_vect)])
95 ylim([-20 8])
96 xlabel('Frequency [Hz]');
97 ylabel('Magnitude [dB]');
98 hold off
99 subplot(2,1,2)
100 semilogx(Freq_Vect, Norm_Phase_Degrees, 'k');

```

```

98 hold on
99 grid on
100 xlim([min(raw_data.freq_vect) max(raw_data.freq_vect)])
101 xlabel('Frequency [Hz]');
102 ylabel('Phase [deg]');
103 hold off
104 %sgt = sgtitle('PI controller frequency response','Color','black');
105 %sgt.FontSize = 20;
106 %% Plot PI ac analysis
107 % load
108 circuit_path = 'C:\Users\JeppeLaptop\Danmarks Tekniske Universitet\
    BEng Jeppe audio amplifier control loop - General\
    Simuleringsfiler\Simuleringsarkiv\' ;
109 circuit_name = 'PI_regulator_ac';
110 raw_data = LTspice2Matlab([circuit_path circuit_name '.raw']);
111 % Display variables
112 fprintf('var \t name\n')
113 for i=1:raw_data.num_variables
114     fprintf('%d \t %s \n', raw_data.selected_vars(i), raw_data.
        variable_name_list{i})
115 end
116 var_out = 1;
117 Log_Magnitude_dB = 20*log10(abs(raw_data.variable_mat(var_out,:)));
118 Norm_Phase_Degrees = angle(raw_data.variable_mat(var_out,:))*180/pi;
119 Freq_Vect = raw_data.freq_vect;
120 figure(2)
121 subplot(2,1,1)
122 semilogx(Freq_Vect, Log_Magnitude_dB, 'k');
123 hold on
124 grid on
125 xlim([min(raw_data.freq_vect) max(raw_data.freq_vect)])
126 xlabel('Frequency [Hz]');
127 ylabel('Magnitude [dB]');
128 hold off
129 subplot(2,1,2)
130 semilogx(Freq_Vect, Norm_Phase_Degrees, 'k');
131 hold on
132 grid on
133 xlim([min(raw_data.freq_vect) max(raw_data.freq_vect)])
134 xlabel('Frequency [Hz]');
135 ylabel('Phase [deg]');
136 hold off
137 %sgt = sgtitle('PI controller frequency response','Color','black');
138 %sgt.FontSize = 20;
139 %% Plot output filter frequency response
140 % load
141 circuit_path = 'C:\Users\JeppeLaptop\Danmarks Tekniske Universitet\

```

```

BEng Jeppe audio amplifier control loop - General\
Simuleringsfiler\Simuleringsarkiv\';
142 circuit_name = 'output_filter_smallsignal';
143 raw_data = LTspice2Matlab([circuit_path circuit_name '.raw']);
144 % Display variables
145 fprintf('var \t name\n')
146 for i=1:raw_data.num_variables
147     fprintf('%d \t\t %s \n', raw_data.selected_vars(i), raw_data.
148         variable_name_list{i})
149 end
150 var_out = 2;
151 var_out_l_esr = 4;
152 var_out_l_c = 6;
153 var_out_c_esr = 8;
154 var_out_c_esl = 10;
155 Log_Magnitude_dB = 20*log10(abs(raw_data.variable_mat(var_out,:)));
156 Log_Magnitude_dB_l_esr = 20*log10(abs(raw_data.variable_mat(
157     var_out_l_esr,:)));
158 Log_Magnitude_dB_l_c = 20*log10(abs(raw_data.variable_mat(var_out_l_c
159 ,:)));
160 Log_Magnitude_dB_c_esr = 20*log10(abs(raw_data.variable_mat(
161     var_out_c_esr,:)));
162 Log_Magnitude_dB_c_esl = 20*log10(abs(raw_data.variable_mat(
163     var_out_c_esl,:)));
164 Norm_Phase_Degrees = angle(raw_data.variable_mat(var_out,:))*180/pi;
165 Norm_Phase_Degrees_l_esr = angle(raw_data.variable_mat(var_out_l_esr
166 ,:))*180/pi;
167 Norm_Phase_Degrees_l_c = angle(raw_data.variable_mat(var_out_l_c,:))
168     *180/pi;
169 Norm_Phase_Degrees_c_esr = angle(raw_data.variable_mat(var_out_c_esr
170 ,:))*180/pi;
171 Norm_Phase_Degrees_c_esl = angle(raw_data.variable_mat(var_out_c_esl
171 ,:))*180/pi;
172 Freq_Vect = raw_data.freq_vect(1,:);
173 figure(2)
174 subplot(2,1,1)
175 hold on
176 semilogx(Freq_Vect, Log_Magnitude_dB, 'color', 'black');
177 semilogx(Freq_Vect, Log_Magnitude_dB_l_esr, '--', 'color', 'black');
178 semilogx(Freq_Vect, Log_Magnitude_dB_l_c, ':', 'color', 'black');
179 grid on
180 xlabel('Frequency [Hz]');
181 ylabel('Magnitude [dB]');
182 xlim([1e4 1e6])
183 set(gca, 'XScale', 'log');
184 legend('Ideal', 'Inductor ESR 300 m\Omega', 'Inductor parallel'

```

```

    capacitance 120 pF', 'location', 'best');
178 hold off
179 subplot(2,1,2)
180 hold on
181 semilogx(Freq_Vect, Norm_Phase_Degrees, 'color', 'black');
182 semilogx(Freq_Vect, Norm_Phase_Degrees_l_esr, '--', 'color', 'black')
    ;
183 semilogx(Freq_Vect, Norm_Phase_Degrees_l_c, ':', 'color', 'black');
184 grid on
185 xlim([1e4 1e6])
186 xlabel('Frequency [Hz]');
187 ylabel('Phase [deg]');
188 legend('Ideal', 'Inductor ESR 300 m\Omega', 'Inductor parallel
    capacitance 120 pF', 'location', 'best');
189 hold off
190 %sgt = sgttitle('PI controller frequency response','Color','black');
191 %sgt.FontSize = 20;
192
193 figure(3)
194 subplot(2,1,1)
195 semilogx(Freq_Vect, Log_Magnitude_dB, 'color', 'black');
196 hold on
197 semilogx(Freq_Vect, Log_Magnitude_dB_c_esr, '--', 'color', 'black');
198 semilogx(Freq_Vect, Log_Magnitude_dB_c_esl, ':', 'color', 'black');
199 grid on
200 xlim([1e4 1e6])
201 ylim([-60 20])
202 xlabel('Frequency [Hz]');
203 ylabel('Magnitude [dB]');
204 %legend('Ideal', 'Inductor ESR 300 m\Omega, C_{s} 120 pF', 'Capacitor
    ESR 300 m\Omega, ESL 100 nH', 'location', 'southwest');
205 hold off
206 subplot(2,1,2)
207 semilogx(Freq_Vect, Norm_Phase_Degrees, 'color', 'black');
208 hold on
209 semilogx(Freq_Vect, Norm_Phase_Degrees_l_esr, '--', 'color', 'black')
    ;
210 semilogx(Freq_Vect, Norm_Phase_Degrees_l_c, ':', 'color', 'black');
211 grid on
212 xlim([1e4 1e6])
213 xlabel('Frequency [Hz]');
214 ylabel('Phase [deg]');
215 legend('Ideal', 'Capacitor ESR 300 m\Omega', 'Capacitor ESL 100nH', 'location', 'best');
216 hold off
217
218

```

```

219 figure(4)
220 subplot(2,1,1)
221 semilogx(Freq_Vect, Log_Magnitude_dB, 'color', 'black');
222 hold on
223 semilogx(Freq_Vect, Log_Magnitude_dB_l_c, '—', 'color', 'black');
224 semilogx(Freq_Vect, Log_Magnitude_dB_c_esl, ':', 'color', 'black');
225 grid on
226 xlim([1e4 1e6])
227 ylim([-60 20])
228 xlabel('Frequency [Hz]');
229 ylabel('Magnitude [dB]');
230 legend('Ideal', 'Inductor ESR 300m\Omega, Parallel capacitance 120 pF
    ', 'Capacitor ESR 300 m\Omega, ESL 100nH', 'location', 'best');
231 hold off
232 subplot(2,1,2)
233 semilogx(Freq_Vect, Norm_Phase_Degrees, 'color', 'black');
234 hold on
235 semilogx(Freq_Vect, Norm_Phase_Degrees_l_c, '—', 'color', 'black');
236 semilogx(Freq_Vect, Norm_Phase_Degrees_c_esl, ':', 'color', 'black');
237 grid on
238 xlim([1e4 1e6])
239 xlabel('Frequency [Hz]');
240 ylabel('Phase [deg]');
241 hold off
242 %% Plot AIM
243 % load
244 circuit_path = 'C:\Users\JeppeLaptop\Danmarks Tekniske Universitet\
    BEng Jeppe audio amplifier control loop — General\
    Simuleringsfiler\Simuleringsarkiv\' ;
245 circuit_name = 'aim_modulator_duty_full';
246 raw_data = LTspice2Matlab([circuit_path circuit_name '.log.raw'], [])
247 ;
248 % Display variables
249 disp( sprintf('\n\nThis file contains %.0f variables:\n', raw_data.
    num_variables) );
250 fprintf('var \t name\n')
251 for i=1:raw_data.num_variables
    fprintf('%d \t\t %s \t\t %s \n', i, char(raw_data.
        variable_type_list{i}), raw_data.variable_name_list{i})
252 end
253 var_v_spk_p = 1;
254 var_v_spk_m = 2;
255 var_v_pos_out = 5;
256 var_v_neg_out = 7;
257 var_v_out = 8;
258 var_v_in = 11;
259 var_i_e1 = 41;

```

```

260 var_i_e2 = 40;
261 var_i_v1 = 42;
262 %raw_data = LTspice2Matlab([circuit_path circuit_name '.raw'], [
263     var_v_spk_p,var_v_spk_m,var_v_pos_out,var_v_neg_out,var_v_out,
264     var_v_in,var_i_e1,var_i_e2,var_i_v1]);
265 raw_data = LTspice2Matlab([circuit_path circuit_name '.raw'
266     ],[1,2,5,7,8,11,40,41,42],10);
267
268 %% Plot eff
269 % load
270 circuit_path = 'C:\Users\JeppeLaptop\Danmarks Tekniske Universitet\
271     BEng Jeppe audio amplifier control loop - General\
272     Simuleringsfiler\Simuleringsarkiv\' ;
273 circuit_name = 'aim_modulator_duty_full';
274 %para_data = readtable([circuit_path circuit_name '.eff_para.txt']);
275 %para_data = readtable([circuit_path circuit_name '.eff_esr.txt']);
276 eff_data = readtable([circuit_path circuit_name '.eff.bak.txt']);
277 eff_data = readtable([circuit_path circuit_name '.eff.txt']);
278 %para_array = table2array(para_data);
279 eff_array = table2array(eff_data);
280 %eff_array(:,1) = [];
281 %para_array(:,1) = [];
282 %s = 20;
283 %for c = 1:s
284 %    eff_array(c,:) = [];
285 %end
286 eff_array([1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20],:) =
287     [];
288 figure(4)
289 %semilogx(para_array(:,2),para_array(:,1),'k');
290 hold on
291 semilogx(eff_array(:,3),eff_array(:,2),'k');
292 grid on
293 xlim([min(eff_array(:,3)) max(eff_array(:,3))]);
294 ylim([0 100]);
295 New_XTickLabel = get(gca,'xtick');
296 set(gca,'XTickLabel',New_XTickLabel);
297 xlabel('Output Power [W]');
298 ylabel('Efficiency [%]');
299 %legend('With Inductor ESR','Without Inductor ESR','location','best')
300 ;
301 hold off
302
303 %% Plot aim fsw duty
304 circuit_path = 'C:\Users\JeppeLaptop\Danmarks Tekniske Universitet\
305     BEng Jeppe audio amplifier control loop - General\
306     Simuleringsfiler\Simuleringsarkiv\' ;

```

```

298 circuit_name = 'aim_modulator_duty_full';
299 open_data = readtable([circuit_path circuit_name '.fosc.txt']);
300 open_array = table2array(open_data);
301
302 figure(5)
303 %subplot(1,2,1)
304 plot(open_array(:,1),open_array(:,3)*1e-3,'k')
305 hold on
306 %yticks([0 100.0e3 200e3 300e4 400e3 500e3 600e3])
307 grid on
308 xlabel('V_{in} [V]');
309 ylabel('f_{sw} [kHz]');
310 hold off
311 %subplot(1,2,2)
312 figure(6)
313 plot(open_array(:,1),open_array(:,2),'k')
314 hold on
315 grid on
316 xlabel('V_{in} [V]');
317 ylabel('D [%]');
318 ylim([0 100]);
319 hold off
320 %% Plot aim duty proper
321 circuit_path = 'C:\Users\JeppeLaptop\Danmarks Tekniske Universitet\
322     BEng Jeppe audio amplifier control loop – General\
323     Simuleringsfiler\Simuleringsarkiv\' ;
322 circuit_name = 'aim_modulator_duty_full';
323 open_data = readtable([circuit_path circuit_name '.duty.txt']);
324 open_array = table2array(open_data);
325 figure(6)
326 plot(open_array(:,1),open_array(:,2),'k')
327 hold on
328 grid on
329 xlabel('V_{in} [V]');
330 ylabel('D [%]');
331 ylim([0 1]);
332 xlim([1.3 3.7]);
333 hold off
334 %% Plot THD
335 circuit_path = 'C:\Users\JeppeLaptop\Danmarks Tekniske Universitet\
336     BEng Jeppe audio amplifier control loop – General\
337     Simuleringsfiler\Simuleringsarkiv\' ;
336 circuit_name = 'aim_modulator_duty_full';
337 data = readtable([circuit_path circuit_name '.thd.log']);
338 data_array = table2array(data);
339 figure(7)
340 plot(data_array(:,1)*1e-3,data_array(:,2),'k')

```

```

341 hold on
342 grid on
343 xlabel('f_{in} [kHz]');
344 ylabel('THD [%]');
345 xlim([min(data_array(:,1))*1e-3 max(data_array(:,1))*1e-3])
346 ylim([0 max(data_array(:,2))])
347 hold off

```

Listing E.6: bode100importer.m

```

1 %% General
2 %clear all; clc; close all
3 % Load path
4 path = 'C:\Users\JeppeLaptop\OneDrive — Danmarks Tekniske Universitet
      \6. semester\Diplomingenørprojekt\Målinger\Bode 100\';
5 %% PI Open, LQR closed 4
6 % Load
7 log_name = 'xtf_0dbm_pi_open_lqr_closed_4ohm';
8 pi_open_lqr_closed_4ohm_table = readtable([path log_name '.log']);
9
10 pi_open_lqr_closed_4ohm_data = table2array(
     pi_open_lqr_closed_4ohm_table);
11 figure(1)
12 subplot(2,1,1)
13 semilogx(pi_open_lqr_closed_4ohm_data(:,1),
            pi_open_lqr_closed_4ohm_data(:,2), 'k');
14 hold on
15 grid on
16 xlim([min(pi_open_lqr_closed_4ohm_data(:,1)) max(
     pi_open_lqr_closed_4ohm_data(:,1))])
17 xlabel('Frequency [Hz]');
18 ylabel('Magnitude [dB]');
19 hold off
20 subplot(2,1,2)
21 semilogx(pi_open_lqr_closed_4ohm_data(:,1),
            pi_open_lqr_closed_4ohm_data(:,3), '--', 'color','black');
22 hold on
23 grid on
24 xlim([min(pi_open_lqr_closed_4ohm_data(:,1)) max(
     pi_open_lqr_closed_4ohm_data(:,1))])
25 xlabel('Frequency [Hz]');
26 ylabel('Phase [deg]');
27 hold off
28 %sgt = sgtitle('PI controller frequency response','Color','black');
29 %sgt.FontSize = 20;
30
31 %% PI Open, LQR closed
32 log_name = 'tf_0dbm_pi_open_lqr_closed';

```

```

33 pi_open_lqr_closed_table = readtable([path log_name '.log']);
34
35 pi_open_lqr_closed_data = table2array(pi_open_lqr_closed_table);
36 figure(2)
37 subplot(2,1,1)
38 semilogx(pi_open_lqr_closed_data(:,1), pi_open_lqr_closed_data(:,2),
39           'k');
40 hold on
41 grid on
42 xlim([min(pi_open_lqr_closed_data(:,1)) max(pi_open_lqr_closed_data
43           (:,1))])
44 xlabel('Frequency [Hz]');
45 ylabel('Magnitude [dB]');
46 hold off
47 subplot(2,1,2)
48 semilogx(pi_open_lqr_closed_data(:,1), pi_open_lqr_closed_data(:,3),
49           'color','black');
50 hold on
51 grid on
52 xlim([min(pi_open_lqr_closed_data(:,1)) max(pi_open_lqr_closed_data
53           (:,1))])
54 xlabel('Frequency [Hz]');
55 ylabel('Phase [deg]');
56 hold off
57
58 %% PI open, LQR closed 300mohm ESR
59 log_name = 'tf_0dbm_pi_open_lqr_closed_lout_300mohmESR_both';
60 pi_open_lqr_closed_L_ESR_table = readtable([path log_name '.log']);
61 pi_open_lqr_closed_L_ESR_data = table2array(
62           pi_open_lqr_closed_L_ESR_table);
63
64 figure(2)
65 subplot(2,1,1)
66 semilogx(pi_open_lqr_closed_data(:,1), pi_open_lqr_closed_data(:,2),
67           '-','color','black');
68 hold on
69 semilogx(pi_open_lqr_closed_L_ESR_data(:,1),
70           pi_open_lqr_closed_L_ESR_data(:,2), '—','color','black');
71 grid on
72 %xlim([min(pi_open_lqr_closed_L_ESR_data(:,1)) max(
73 %           pi_open_lqr_closed_L_ESR_data(:,1))])
74 xlabel('Frequency [Hz]');
75 ylabel('Magnitude [dB]');
76 legend('PI control loop with closed LQR loop', 'Added Inductor ESR 300
77           m\Omega', 'location', 'best');
78 hold off

```

```

71 subplot(2,1,2)
72 semilogx(pi_open_lqr_closed_data(:,1), pi_open_lqr_closed_data(:,3), '-','color','black');
73 hold on
74 semilogx(pi_open_lqr_closed_L_ESR_data(:,1),
75         pi_open_lqr_closed_L_ESR_data(:,3), '--','color','black');
76 grid on
77 %xlim([min(pi_open_lqr_closed_L_ESR_data(:,1)) max(
78 %    pi_open_lqr_closed_L_ESR_data(:,1))])
79 xlabel('Frequency [Hz]');
80 ylabel('Phase [deg]');
81 legend('PI control loop with closed LQR loop','Added Inductor ESR 300
82     m\Omega','location','best');
83 hold off
84
85 %% PI open, LQR closed, ESR 300 mOhm, 240pF ceramic
86 log_name = 'tf_0dbm_pi_open_lqr_closed_lout_300mohmESR_240pF_both';
87 pi_open_lqr_closed_L_ESR_Cparallel120pF_table = readtable([path
88     log_name '.log']);
89 pi_open_lqr_closed_L_ESR_Cparallel120pF_data = table2array(
90     pi_open_lqr_closed_L_ESR_Cparallel120pF_table);
91
92 figure(3)
93 subplot(2,1,1)
94 semilogx(pi_open_lqr_closed_data(:,1), pi_open_lqr_closed_data(:,2), '-','color','black');
95 hold on
96 semilogx(pi_open_lqr_closed_L_ESR_data(:,1),
97         pi_open_lqr_closed_L_ESR_data(:,2), '--','color','black');
98 semilogx(pi_open_lqr_closed_L_ESR_Cparallel120pF_data(:,1),
99         pi_open_lqr_closed_L_ESR_Cparallel120pF_data(:,2), ':','color','
100 black');
101 grid on
102 %xlim([min(pi_open_lqr_closed_L_ESR_data(:,1)) max(
103 %    pi_open_lqr_closed_L_ESR_data(:,1))])
104 xlabel('Frequency [Hz]');
105 ylabel('Magnitude [dB]');
106 %legend('PI control loop with closed LQR loop','Inductor ESR 300 m\
107     \Omega','Inductor parallel 120pF','location','best');
108 hold off
109 subplot(2,1,2)
110 semilogx(pi_open_lqr_closed_data(:,1), pi_open_lqr_closed_data(:,3), '-','color','black');
111 hold on
112 semilogx(pi_open_lqr_closed_L_ESR_data(:,1),
113         pi_open_lqr_closed_L_ESR_data(:,3), '--','color','black');
114 semilogx(pi_open_lqr_closed_L_ESR_Cparallel120pF_data(:,1),
115         pi_open_lqr_closed_L_ESR_Cparallel120pF_data(:,3), ':','color','black');
116 grid on
117 %xlim([min(pi_open_lqr_closed_L_ESR_data(:,1)) max(
118 %    pi_open_lqr_closed_L_ESR_data(:,1))])
119 xlabel('Frequency [Hz]');
120 ylabel('Phase [deg]');
121 legend('PI control loop with closed LQR loop','Inductor ESR 300 m\Omega
122     ','Inductor parallel 120pF','location','best');
123 hold off
124
```

```

    pi_open_lqr_closed_L_ESR_Cparallel120pF_data(:,3),':','color','
    black');

104 grid on
105 %xlim([min(pi_open_lqr_closed_L_ESR_data(:,1)) max(
106     pi_open_lqr_closed_L_ESR_data(:,1))])
107 xlabel('Frequency [Hz]')
108 ylabel('Phase [deg]');
109 legend('PI control loop with closed LQR loop','Inductor ESR 300 m\
    Omega','Inductor parallel 120pF','location','best');
110 hold off
111
112 %% General
113 %clear all; clc; close all
114 % Load path
115 %path = 'C:\Users\JeppeLaptop\OneDrive — Danmarks Tekniske
116 %Universitet\6. semester\Diplomingenørprojekt\Målinger\Bode
117 %100\';
118
119 %% PI, LQR open
120 log_name = 'tf_0dbm_pi_open_lqr_open';
121 pi_open_lqr_open_table = readtable([path log_name '.log']);
122
123 pi_open_lqr_open_data = table2array(pi_open_lqr_open_table);
124 figure(1)
125 subplot(2,1,1)
126 semilogx(pi_open_lqr_open_data(:,1), pi_open_lqr_open_data(:,2), 'k')
127 ;
128 hold on
129 grid on
130 xlim([min(pi_open_lqr_open_data(:,1)) max(pi_open_lqr_open_data(:,1))
131 ])
132 xlabel('Frequency [Hz]')
133 ylabel('Magnitude [dB]')
134 hold off
135 subplot(2,1,2)
136 semilogx(pi_open_lqr_open_data(:,1), pi_open_lqr_open_data(:,3),':',
137     'color','black');
138 hold on
139 grid on
140 xlim([min(pi_open_lqr_open_data(:,1)) max(pi_open_lqr_open_data(:,1))
141 ])
142 xlabel('Frequency [Hz]')
143 ylabel('Phase [deg]')
144 hold off
145 %% PI, LQR open 300mohm ESR
146 log_name = 'tf_0dbm_pi_open_lqr_open_lout_300mohmESR_both';
147 pi_open_lqr_open_L_ESR_table = readtable([path log_name '.log']);

```

```

141 pi_open_lqr_open_L_ESR_data = table2array(
142     pi_open_lqr_open_L_ESR_table);
143 figure(2)
144 subplot(2,1,1)
145 semilogx(pi_open_lqr_open_data(:,1), pi_open_lqr_open_data(:,2), '—', 'color','black');
146 hold on
147 semilogx(pi_open_lqr_open_L_ESR_data(:,1),
148     pi_open_lqr_open_L_ESR_data(:,2), '—', 'color','black');
149 grid on
150 %xlim([min(pi_open_lqr_closed_L_ESR_data(:,1)) max(
151     pi_open_lqr_closed_L_ESR_data(:,1))])
152 xlabel('Frequency [Hz]');
153 ylabel('Magnitude [dB]');
154 legend('PI control loop with closed LQR loop','Added Inductor ESR 300
155     m\Omega','location','best');
156 hold off
157 subplot(2,1,2)
158 semilogx(pi_open_lqr_open_data(:,1), pi_open_lqr_open_data(:,3), '—', 'color','black');
159 hold on
160 semilogx(pi_open_lqr_open_L_ESR_data(:,1),
161     pi_open_lqr_open_L_ESR_data(:,3), '—', 'color','black');
162 grid on
163 %xlim([min(pi_open_lqr_closed_L_ESR_data(:,1)) max(
164     pi_open_lqr_closed_L_ESR_data(:,1))])
165 xlabel('Frequency [Hz]');
166 ylabel('Phase [deg]');
167 legend('PI control loop with open LQR loop','Inductor ESR 300 m\Omega
168     ','location','best');
169 hold off
170
171 %% PI open, LQR open ESR 300 mOhm, 240pF ceramic
172 log_name = 'tf_0dbm_pi_open_lqr_open_lout_300mohmESR_240pF_both';
173 pi_open_lqr_open_L_ESR_Cparallel120pF_table = readtable([path
174     log_name '.log']);
175 pi_open_lqr_open_L_ESR_Cparallel120pF_data = table2array(
176     pi_open_lqr_open_L_ESR_Cparallel120pF_table);
177 figure(3)
178 subplot(2,1,1)
179 semilogx(pi_open_lqr_open_data(:,1), pi_open_lqr_open_data(:,2), '—', 'color','black');
180 hold on
181 semilogx(pi_open_lqr_open_L_ESR_data(:,1),

```

```

    pi_open_lqr_open_L_ESR_data(:,2), '—','color','black');
176 semilogx(pi_open_lqr_open_L_ESR_Cparallel120pF_data(:,1),
    pi_open_lqr_open_L_ESR_Cparallel120pF_data(:,2), ':','color',
    'black');
177 grid on
178 %xlim([min(pi_open_lqr_closed_L_ESR_data(:,1)) max(
    pi_open_lqr_closed_L_ESR_data(:,1))])
179 xlabel('Frequency [Hz]');
180 ylabel('Magnitude [dB]');
181 %legend('PI control loop with closed LQR loop','Inductor ESR 300 m\
    Omega','Inductor parallel 120pF','location','best');
182 hold off
183 subplot(2,1,2)
184 semilogx(pi_open_lqr_open_data(:,1), pi_open_lqr_open_data(:,3), '—',
    'color','black');
185 hold on
186 semilogx(pi_open_lqr_open_L_ESR_data(:,1),
    pi_open_lqr_open_L_ESR_data(:,3), '—','color','black');
187 semilogx(pi_open_lqr_open_L_ESR_Cparallel120pF_data(:,1),
    pi_open_lqr_open_L_ESR_Cparallel120pF_data(:,3), ':','color',
    'black');
188 grid on
189 %xlim([min(pi_open_lqr_closed_L_ESR_data(:,1)) max(
    pi_open_lqr_closed_L_ESR_data(:,1))])
190 xlabel('Frequency [Hz]');
191 ylabel('Phase [deg]');
192 legend('PI control loop with open LQR loop','Inductor ESR 300 m\Omega\
    ','Inductor parallel 120pF','location','best');
193 hold off
194


---


195 %% Comparison of parasitic elements open and closed LQR
196
197 figure(4)
198 subplot(2,1,1)
199 semilogx(pi_open_lqr_open_L_ESR_Cparallel120pF_data(:,1),
    pi_open_lqr_open_L_ESR_Cparallel120pF_data(:,2), '—','color',
    'black');
200 hold on
201 semilogx(pi_open_lqr_closed_L_ESR_Cparallel120pF_data(:,1),
    pi_open_lqr_closed_L_ESR_Cparallel120pF_data(:,2), ':','color',
    'black');
202 grid on
203 xlabel('Frequency [Hz]');
204 ylabel('Magnitude [dB]');
205 hold off
206 subplot(2,1,2)
207 semilogx(pi_open_lqr_open_data(:,1), pi_open_lqr_open_data(:,3), '—',

```

```

    'color','black');
208 hold on
209 semilogx(pi_open_lqr_closed_L_ESR_Cparallel120pF_data(:,1),
210     pi_open_lqr_closed_L_ESR_Cparallel120pF_data(:,3), ':' , 'color',
211     'black');
212 grid on
213 xlabel('Frequency [Hz]');
214 ylabel('Phase [deg]');
215 legend('PI control loop with closed LQR loop and parasitic elements',
216         'PI control loop with open LQR loop and parasitic elements',
217         'location','best');
218 hold off
219


---


220 %% Transfer function estimation
221 %% First
222 %Freq = pi_open_lqr_closed_4ohm_data(:,1);
223 %Mag_4ohm = 10.^ (pi_open_lqr_closed_4ohm_data(:,2)./20);
224 %Pha_4ohm = pi_open_lqr_closed_4ohm_data(:,3);
225 %zfr_4ohm = Mag_4ohm.*exp(1i*Pha_4ohm*pi/180);
226 %W = Freq*2*pi;
227 %Ts = 1/(2*max(Freq)); % your sampling time
228 %gfr_4ohm = frd(zfr_4ohm,W,Ts);
229 %sys=tfest(gfr_4ohm,4);
230 %[mag,ph]=bode(sys,W);
231 %[poles,zeros] = pzmap(sys);
232 % figure(5)
233 % compare(gfr_4ohm,sys)
234 % grid on
235 % figure(6)
236 % pzmap(sys)
237 % grid on


---


238 %% Load data
239
240 % Load first system
241 Freq_closed = pi_open_lqr_closed_data(:,1);
242 Mag_closed = 10.^ (pi_open_lqr_closed_data(:,2)./20);
243 Pha_closed = pi_open_lqr_closed_data(:,3);
244 zfr_closed = Mag_closed.*exp(1i*Pha_closed*pi/180);
245 W = Freq_closed*2*pi;
246 Ts_closed = 1/(2*max(Freq_closed)); % your sampling time
247 gfr_closed = frd(zfr_closed,W,Ts_closed);
248 sys_closed=tfest(gfr_closed,8);


---


249 % Parasites 1
250 Mag_closed_para = 10.^ (pi_open_lqr_closed_L_ESR_Cparallel120pF_data
251     (:,2)./20);
252 Pha_closed_para = pi_open_lqr_closed_L_ESR_Cparallel120pF_data(:,3);
253 zfr_closed_para = Mag_closed_para.*exp(1i*Pha_closed_para*pi/180);

```

```

249 gfr_closed_para = frd(zfr_closed_para,W,Ts_closed);
250 sys_closed_para=tfest(gfr_closed_para,5);
251
252 % Load second system
253 Freq_open = pi_open_lqr_open_data(:,1);
254 Mag_open = 10.^ (pi_open_lqr_open_data(:,2)./20);
255 Pha_open = pi_open_lqr_open_data(:,3);
256 zfr_open = Mag_open.*exp(1i*Pha_open*pi/180);
257 W2 = Freq_open*2*pi;
258 Ts_open = 1/(2*max(Freq_open)); % your sampling time
259 gfr_open = frd(zfr_open,W2,Ts_open);
260 sys_open = tfest(gfr_open,8);
261 % Parasites 2
262 Mag_open_para = 10.^ (pi_open_lqr_open_L_ESR_Cparallel120pF_data(:,2)
263 ./20);
264 Pha_open_para = pi_open_lqr_open_L_ESR_Cparallel120pF_data(:,3);
265 zfr_open_para = Mag_open_para.*exp(1i*Pha_open_para*pi/180);
266 gfr_open_para = frd(zfr_open_para,W2,Ts_open);
267 sys_open_para=tfest(gfr_open_para,5);
268
269 %%
270 % Display
271 % Wrap phase to [-180,180]
272 opts = bodeoptions('cstprefs');
273 opts.PhaseWrapping='on';
274 %opts.PhaseWrappingBranch=-180;
275
276 [mag2,ph2]=bode(sys_closed,W,opts);
277 [mag2_para,ph2_para]=bode(sys_closed_para,W);
278 [poles,zeros] = pzmap(sys_closed);
279 %figure(5)
280 %pzmap(sys_closed)
281 %grid on
282 figure(6)
283 %subplot(2,1,1)
284 %compare(gfr,sys2)
285 %compare(gfr_closed_para,sys2_para)
286 %grid on
287 %figure(7)
288 %subplot(2,1,2)
289 hold on
290 bode(sys_closed,W,opts,'k');
291 bode(sys_closed_para,W,opts,'—k');
292 %[mag2_para,ph2_para]=bode(sys2_para,W);
293 grid on
294 legend('Closed loop without inductor parasitic elements', 'Closed

```

```

    loop with inductor parasitic elements', 'location','best'));
295 hold off
296 figure(8)
297 hold on
298 tsum_closed= sys_closed_para/sys_closed;
299 tsum_open= sys_open_para/sys_open;
300 bode(tsum_closed,W,opts,'-k');
301 bode(tsum_open,W2,opts,'-k');
302 legend('LQR closed, est. TF of R_{L} and C_{L}', 'LQR open, est. TF
      of R_{L} and C_{L}', 'location','best');
303 grid on
304 hold off
305 %w=pi_open_lqr_closed_4ohm_data(:,1)*2*pi; %convert Hz to rad/sec
306 %gfr = idfrd(response,w,Ts);
307 %sys=tfest(gfr,4);
308 %tfest = tfest(pi_open_lqr_closed_4ohm_data,4)
309
310
311 %% TF estimation
312 opts = bodeoptions('cstprefs');
313 opts.PhaseWrapping='on';
314 opts.PhaseWrappingBranch=-180;
315 %lintf = tf([4.285e12,8.578e16],[1,1.263e5,1.428e11,0]);
316 lintf_real = tf([1.428e11,4.761e15],[1,1.263e5,1.428e11,0]);
317 lintf_rl = tf([2.142e12,4.289e16],[1,2.959e5,1.643e11,0]);
318 lintf_cs = tf([4.159e12,8.326e16],[1,1.225e5,1.386e11,0]);
319 %[lintf_mag,lintf_ph,lintf_w] = bode(lintf);
320 %lintf_mag=squeeze(lintf_mag);lintf_ph=squeeze(lintf_ph);
321 lintf_rl2 = lintf_rl/lintf_real;
322 lintf_cs2 = lintf_cs/lintf_real;
323 lintf_real2 = lintf_real*lintf_rl2*lintf_cs2;
324 figure(9)
325 hold on
326 bode(sys_open,Freq_open,opts,'-k')
327 bode(lintf_real,Freq_open,opts,'-k')
328 grid on
329 legend('Open loop measurement','Theoretical function','location',
      'best');
330 hold off

```

Listing E.7: outputfilter.m

```

1 %% Analytical calculation of transfer function in output filter with
   parasitic elements
2 close all; clc; clear all;
3 opts = bodeoptions('cstprefs');
4 opts.PhaseWrapping='on'; % Bode plot phase wrap enable
5 %opts.PhaseWrappingBranch=-180;

```

```

6 opts.Xlim=[1e4, 1e6]; % Axis limitation
7 Rctl = 4; Cctl = 1.98e-6; % Differential filter values
8 R = Rctl/2; C = Cctl*2; L = 1.768e-6; R_L = 300e-3; C_L = 120e-9; %
    Single-ended filter values
9 sys = tf([1],[L*C, L/R, 1]);
10 sys_rl = tf([R],[R*L*C, L+R*R_L*C, R_L+R]);
11 sys_cl = tf([R*L*C_L, 0, R],[R*L*C_L+R*L*C, L, R]);
12 [mag,phase,wout] = bode(sys); % Get Plot Data
13 mag = squeeze(mag); % Reduce (1x1xN) Matrix To (1xN)
14 phase=squeeze(phase); % Reduce (1x1xN) Matrix To (1xN)
15 magr2 = (mag/max(mag)).^2; % Calculate Power Of Ratio Of mag/max(mag)
16 dB3 = interp1(magr2, [wout phase mag], 0.5, 'spline'); % Find corner
    frequency
17
18 % Display
19 figure(9)
20 hold on
21 bode(sys,opts,'-k');
22 bode(sys_rl,opts,'—k');
23 bode(sys_cl,opts,:k');
24 grid on
25 legend('Ideal', 'ESR 300 m\Omega', 'Parallel capacitance 120 pF','
    location','best')
26 hold off

```

Listing E.8: controlloop.m

```

1 %clc; clear all; close all;
2
3 Cctl = 1.98e-6; Rctl = 4; L = 1.768e-6;
4 Cf = Cctl*2; Rf = Rctl/2;
5
6 C_pi = 1.5e-9; R_pi = 33e3;
7 tau_i = C_pi*R_pi;
8 gain = 30;
9
10 % Parasitic elements
11 Rl = 300e-3; Cs = 120e-9;
12
13 s = tf('s');
14
15 sim('control_loop')
16
17 %[b,a] = ss2tf(linsys1.A,linsys1.B,linsys1.C,linsys1.D)
18 %[b,a] = ss2tf(linsys1.A,linsys1.B,linsys1.C,linsys1.D); linsys1_tf =
    tf(b,a)
19
20 lntf = tf([4.285e12,8.578e16],[1,1.263e5,1.428e11,0]);

```

```
21 | lintf_rl = tf([2.142e12,4.289e16],[1,2.959e5,1.643e11,0]);  
22 | lintf_cs = tf([4.159e12,8.326e16],[1,1.225e5,1.386e11,0]);
```

Appendix F: Bill of Materials

Influence of the output filter parasitic elements on the control loop in a switch-mode audio amplifier

Circuit	Component	Value	Footprint	Rating	Description
IO	C1	1n	0603	X7R50V	Preamp
	C13	1u	RAD-0.3in	Film 40V	Preamp
	C14	1.5n	0603	X7R50V	PI controller
	C15	NC	0603	X7R50V	PI controller
	C2,C3,C4,C9,C10	100n	0603	X7R16V	Decoupling
	C5,C11	1u	0603	X5R6.3V	Decoupling
	C6,C7	100n	0805	X7R50V	Decoupling
	C8	1500u	RAD-0.3in	63Vdc	Decoupling
	P10	3-pin header	Male	250V	Controller bypass
	P11,P12	10-pin header	Female	250V	InterPCB con.
	P2,P3	1-pin header	Male	250V	Measurements
	P4,P5	2-way screw	NA	300V 15A	30V Power,Output
	P6	2-pin header	Molex KK254	500V 4A	Audio in
	P7	4-pin header	Female	250V	5V Power
	P8,P9	BNC	BNC PCB	500V	Audio in, Output
	R2	16.2k	0603	1%	Preamp
	R1,R3	2k	0603	1%	Preamp
	R4,R7	4.75k	0603	1%	Voltage ref
Power Stage	R5	33.2k	0603	NA	PI controller
	R6	0 (short)	0603	NA	PI controller
	R9	0 (short)	0603	NA	PI controller
	R10	NC	0603	NA	PI controller
	R8	2.49k	0603	1%	Voltage ref
	U1	OPA2365	SOIC-8	NA	Preamp, PI
	U2	TLV431A	SOT-23	1%	Voltage ref
	C1,C11,C15,C19	100n	0603	X7R16V	Gate driver
	P1,P2	10-pin header	Male	250V	InterPCB con.
	C2,C16	150n	0603	X5R10V	Gate driver
	C3,C10	100p	0603	NPO50V	Decoupling
	L1,L2	1.768u	Radial	NA	Output filter
	U1,U3	LM5113	WSON-10	NA	Gate driver
	R20	15m sense	1210	1% 1W	Output filter
AIM+reg	R1,R6	500	SMDtrim 3213	NA	Gate driver
	Q1,Q2,Q3,Q4	BSZ097N10NS5	TSDSON-8	NA	Power stage
	R2,R5,R8,R10	5	0603	1%	Gate driver
	R4,R9	0	0603	1%	Gate driver
	D1,D2	Diode	NA	85V 0.25A	Gate driver
	C5,C6,C9,C17	10u	1210	X7R50V	Decoupling
	C12,C13,C14	680n	1210	X7R100V	Output filter
	C18,C20,C27	100n	0603	X7R16V	Decoupling
	C28,C29,C30,C31	100n	0603	X7R16V	Decoupling
	U6	LT1999	MSOP-8	NA	Current acq.
	U4	AD8274	MSOP-8	NA	Volt acq.
	U2	LT1711	MSOP-8	NA	AIM
	C4	NC	0603	X7R16V	AIM
	C7	NC	0603	X7R16V	AIM
	C8	NC	0603	X7R16V	Cur. acq.
	CA1	1.5n	0603	X7R50V	AIM
	R14	8.66k	0603	1%	AIM
	R18	16.2k	0603	1%	AIM
	R23	1.5k	0603	1%	AIM
	R3,R11	120k	0603	1%	Voltage acq.
	RA1	2.2k	0603	1%	AIM
	RA2	20k	0603	1%	AIM
	RA3	2.74k	0603	1%	AIM
	RA4	0	0603	NA	AIM

Table F.1: Bill of Materials

Appendix G: Instruments

Function	Manufacturer	Model
Visual inspection microscope	Leica	A60
Manual soldering	Weller	WX2
Heat gun	Thermaltronics	TMT-HA600-2
SMT solder paste dispensing	Fisnar	SL101N
Reflow oven	Mistral	260
DMM	Meterman	38XR

Table G.1: List of instruments used for solder work

Function	Manufacturer	Model
Power supply	RIGOL	DP832
DMM	Agilent	34410A
Frequency response analysis	N4L	PSM1735
Audio analysis	Audio Precision	APx500
Audio analysis filter	Audio Precision	AUX-0025
Control loop analyzer	OMICRON Lab	BODE 100
Control loop injection transformer	OMICRON Lab	B-WIT 100
Passive load	Unknown	Power resistor 4Ω
Passive load	Unknown	Loudspeaker 4Ω
Active cooling	ebm	W2S107-AA01-16

Table G.2: List of instruments used for testing

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