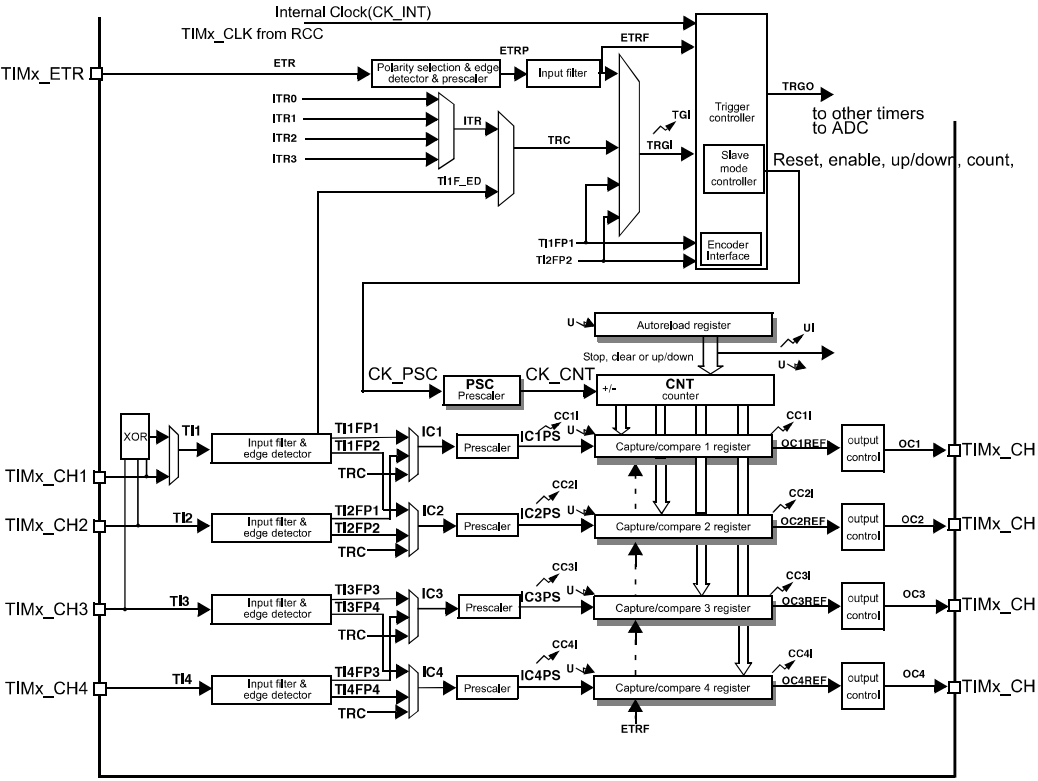


Notes:

Reg — Preload registers transferred to active registers on U event according to control bit

event

interrupt & DMA output