Process flow title:	**Minimal MOS Capacitor Process**	**Revision:**	**Rev 0.3**
Contact email:	jephin@dtu.dk	Contact name:	Jeppe Hinrichs
Contact phone:	Not applicable		
LabManager group:	Not applicable	Batch name:	TBD
Date of creation:	2025-08-15	Date of revision:	2025-08-19

Process Overview

Minimal MOS capacitor fabrication flow.

Key Specifications

- Gate oxide: 35 nm thermal SiO_2
- Gate electrode: 400 nm n+ polysilicon
- Backside contact: 400 nm aluminum

Critical Safety

- **HF handling:** Apron+gloves, face shield, no lone working, no glass beakers!
- **Furnace:** Thermal gloves for >800 °C operations
- **Metal anneal:** confirm Al spiking risk mitigated by Ti barrier, avoid $\geq$ 450 °C for Al

1 Starting Material

Substrate	Specification	Thickness	Qty
Silicon	p-type <100>, 6", 1-10 Ω·cm	500 µm ± 20 µm	5

2 Critical Layers

Layer	Material	Thickness
Gate oxide	Thermal SiO_2	35 nm
Gate electrode	n+ Poly-Si	400 nm
Back barrier/adhesion	Ti	100 nm
Back contact	Al	400 nm

3 Core Process Flow

Step	Process	Equipment	Process	Comment
0.1	(Optional) LOCOS isolation	See locos_v1.DOCX	Use if isolation is required	
1.1	Pre-oxidation clean (HF-last)	Wet bench	SC1, SC2, HF (12%), immediate furnace load	
2.1	Gate SiO_2 growth	Furnace	1000 °C, dry/wet-dry recipe to 35 nm	
3.1	Poly-Si deposition (n+ preferred)	LPCVD	620 °C, 2 h; *specify in-situ PH_3 or undoped*	
3.2	(If undoped) Poly doping + anneal	Diffusion/RTA	$POCl_3$ or P implant; anneal per spec	
4.1	Gate patterning	Aligner + Etch	Mask: capacitor; poly etch (e.g. HBr/Cl_2 ICP or TMAH)	
5.0	Backside oxide strip	Wet bench	Protect frontside; remove backside oxide with BOE/HF until bare Si exposed; leave edge exclusion	
5.1	Backside Ti deposition	Sputter	100 nm	
5.2	Backside Al deposition	E-beam/Sputter	400 nm	
5.3	Contact/forming-gas anneal	RTP/Furnace	400 °C to 450 °C, 20 min to 30 min, N_2 or 5% H_2 in N_2	

4 Critical Checks

Step	QC Verification
2.1	Oxide thickness: 35 nm ± 1 nm
3.1/3.2	Poly n+ sheet resistance: $\leq$ 30 Ω/□
4.1	Gate CD: ± 0.5 µm
5.0	Backside oxide fully removed (contact-angle change, test drop, or monitor wafer)
5.1	Backside Ti sheet resistance ≈ 0.3 Ω/□(100 nm Ti)
5.2	Backside Al sheet resistance ≈ 0.07 Ω/□(400 nm Al)
5.3	Contact anneal; contact resistance to Si governed by Ti/Si interface quality (target $<$ 1 Ω·contact)

5 Process Flow Diagram

6 Required Figures

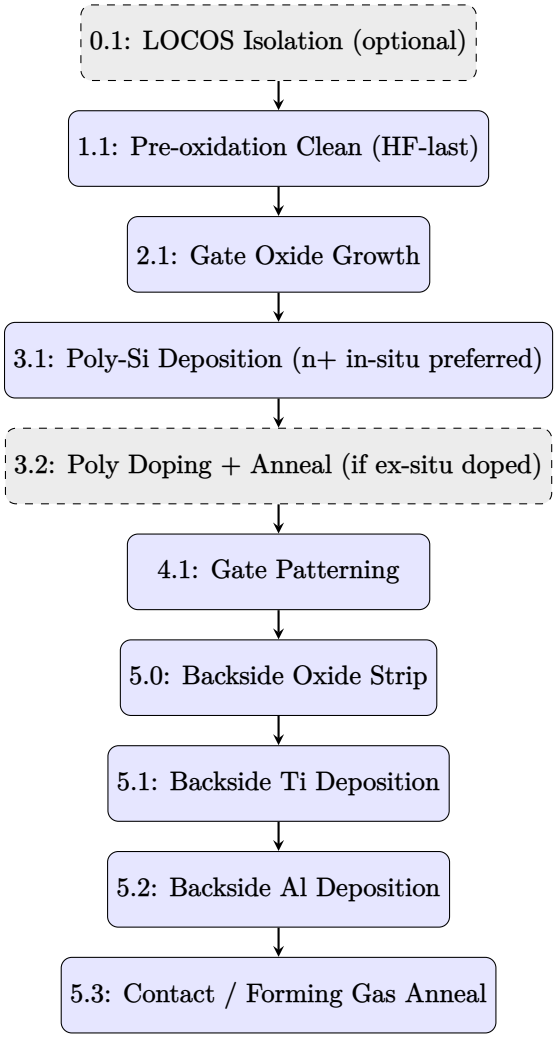
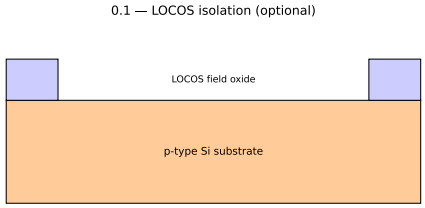


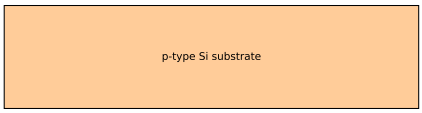
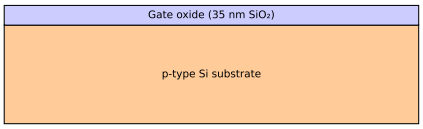
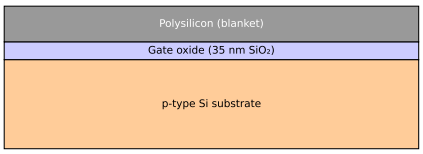
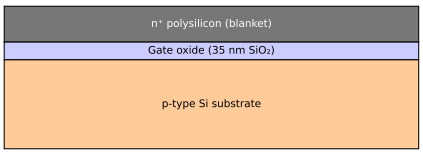
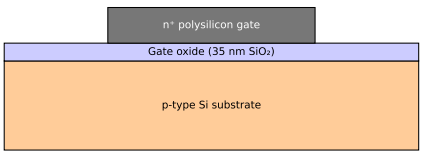
Figure 1: Process flow diagram for MOS capacitor fabrication.

Table 1:

ID	Step	Description
0	0.1	 LOCOS isolation (optional)

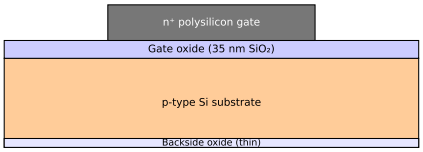
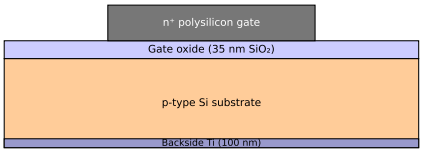
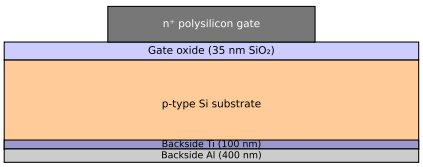
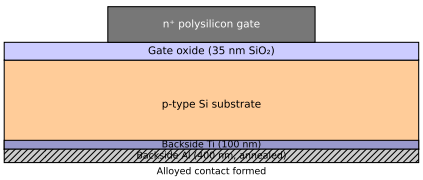
Continued on next page

Table 1: (Continued)

1	1.1	1.1 — Pre-oxidation clean (HF-last)  Pre-oxidation clean (HF-last)
2	2.1	2.1 — Gate oxide growth  Gate oxide growth
3	3.1	3.1 — Poly-Si deposition (blanket)  Poly-Si deposition (blanket)
4	3.2	3.2 — Poly doping + anneal  Poly doping + anneal
5	4.1	4.1 — Gate patterning  Gate patterning + top pad

Continued on next page

Table 1: (Continued)

7	5.0	5.0 — Backside oxide strip  Backside oxide strip
8	5.1	5.1 — Backside Ti deposition  Backside Ti deposition
9	5.2	5.2 — Backside Al deposition  Backside Al deposition
10	5.3	5.3 — Contact anneal  Contact anneal