Process flow title:	**Minimal MOS Capacitor Process**	**Revision:**	**Rev 0.3**
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Process Overview

Minimal MOS capacitor fabrication flow.

Key Specifications

- Gate oxide: 35 nm thermal SiO_2
- Gate electrode: 400 nm n+ polysilicon
- Backside contact: 400 nm aluminum

Critical Safety

- **HF handling:** Apron+gloves, face shield, no lone working, no glass beakers!
- **Furnace:** Thermal gloves for >800 °C operations
- **Metal anneal:** confirm Al spiking risk mitigated by Ti barrier, avoid $\geq$ 450 °C for Al

1 Starting Material

Substrate	Specification	Thickness	Qty
Silicon	p-type <100>, 6", 1-10 Ω·cm	500 µm ± 20 µm	5

2 Critical Layers

Layer	Material	Thickness
Gate oxide	Thermal SiO_2	35 nm
Gate electrode	n+ Poly-Si	400 nm
Back barrier/adhesion	Ti	100 nm
Back contact	Al	400 nm

3 Core Process Flow

Table 1:

Step	Process	Equipment	Parameters	Comment
0.1	(Optional) LOCOS isolation	Furnace: Oxidation (8") E1	Recipe LOCOS, pad oxide + SiN mask + field oxidation	See `locos_v1.DOCX`. Perform only if device isolation needed.
1.1	Pre-oxidation clean (HF-last)	RCA bench	RCA clean: SC1 (NH_4OH/H_2O_2), rinse, SC2 (HCl/H_2O_2), rinse, HF dip (1 % to 2 %) last, N_2 dry	Leave H-terminated surface; immediate furnace load.
2.1	Gate SiO_2 growth	Furnace: Oxidation (8") E1	Recipe DRY1000: 40 min dry oxidation + 20 min anneal at 1000 °C; target 35 nm SiO_2	Inspect oxide thickness by Ellipsometer or Filmtek; tolerance ±1 nm.
3.1	Poly-Si deposition (n+ preferred)	Furnace: LPCVD Poly-Si (6") E2	Recipe DOPEPOLY: 2 h at 620 °C, thickness ≈400 nm	If in-situ PH_3 doping is available, select doped recipe. Measure film thickness (Ellipsometer/Filmtek).
3.2	(If undoped) Poly doping + anneal	Furnace: Oxidation (8") E1 or RTP	$POCl_3$ deposition + drive-in, or P implant + anneal (Recipe ANN1000, 20 min, 1000 °C)	Required if 3.1 used undoped poly. Verify sheet resistance ≤30 Ω/□.
4.1	Gate patterning (Lithography + Poly etch)	Litho: Gamma UV coater (Seq. 1611); Aligner MLA2; Etcher Pegasus 3 DRIE	Coat: 1.5 µm resist, 30 s @ 4600 rpm, softbake 90 s at 90 °C. Expose MLA2: 375 nm, 325 mJ/cm^2, defocus 2. Develop: TMAH. Etch: HBr/Cl_2 ICP or DRIE. Strip resist in WB06.	Inspect CD with microscope; measure etch depth with DekTak. Target CD ±0.5 µm.
5.0	Backside oxide strip	Wet bench 04	Buffered HF 2 (BHF), 40 s (etch rate 75 nm/min to 80 nm/min for 35 nm oxide)	Protect frontside; leave edge exclusion. Confirm bare Si via contact angle or monitor wafer.
5.1	Backside Ti deposition	E-beam	Deposit Ti, 100 nm	Forms barrier + adhesion to Si.
5.2	Backside Al deposition	E-beam	Deposit Al, 400 nm	Back contact metal.
5.3	Contact / Forming-gas anneal	RTP2 Jipelec or Furnace	400 °C to 450 °C, 20 min to 30 min, N_2 or 5% H_2 in N_2	Stabilizes contacts. Contact resistance governed by Ti/Si interface; aim $< 1\ \Omega \cdot$ contact.

4 Critical Checks

Step	QC Verification
2.1	Oxide thickness: $35\,\text{nm} \pm 1\,\text{nm}$
3.1/3.2	Poly n+ sheet resistance: $\leq 30\ \Omega/\square$
4.1	Gate CD: $\pm\ 0.5\,\mu\text{m}$
5.0	Backside oxide fully removed (contact-angle change, test drop, or monitor wafer)
5.1	Backside Ti sheet resistance $\approx 0.3\ \Omega/\square$(100 nm Ti)
5.2	Backside Al sheet resistance $\approx 0.07\ \Omega/\square$(400 nm Al)
5.3	Contact anneal; contact resistance to Si governed by Ti/Si interface quality (target $< 1\ \Omega\cdot$contact)

5 Process Flow Diagram

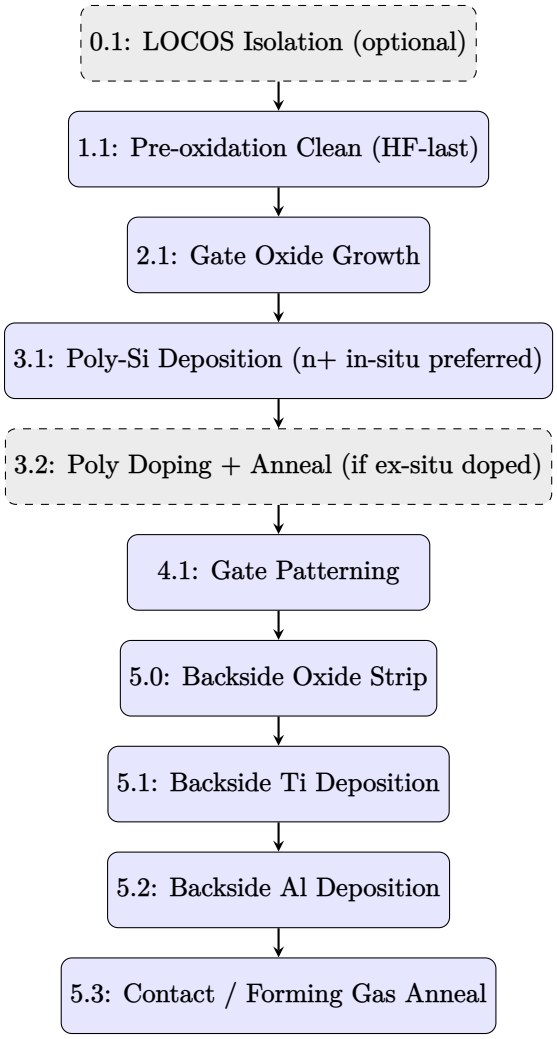


Figure 1: Process flow diagram for MOS capacitor fabrication.

6 Required Figures

Table 2:

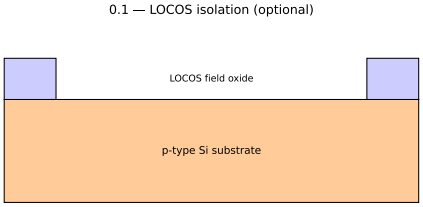
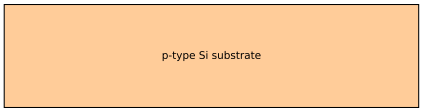
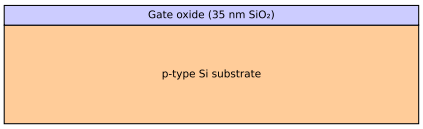
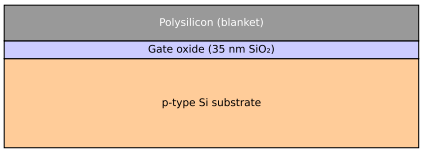
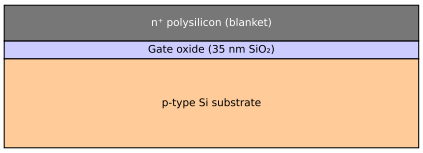
ID	Step	Description
0	0.1	 LOCOS isolation (optional)
1	1.1	 Pre-oxidation clean (HF-last)
2	2.1	 Gate oxide growth
3	3.1	 Poly-Si deposition (blanket)
4	3.2	 Poly doping + anneal

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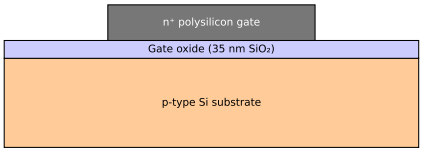
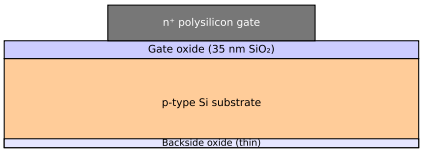
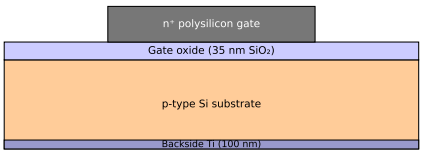
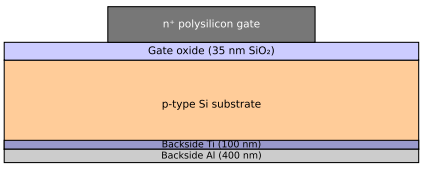
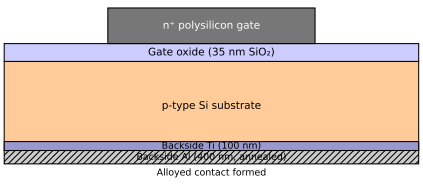
Table 2: (Continued)

5	4.1	4.1 — Gate patterning  Gate patterning + top pad
6	5.0	5.0 — Backside oxide strip  Backside oxide strip
7	5.1	5.1 — Backside Ti deposition  Backside Ti deposition
8	5.2	5.2 — Backside Al deposition  Backside Al deposition
9	5.3	5.3 — Contact anneal  Contact anneal