

Process flow title:	Minimal MOS Capacitor Process	Revision:	Rev 0.5
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Date of creation:	2025-08-15	Date of revision:	2025-08-28

Process Overview

Minimal MOS capacitor fabrication flow.

Key Specifications

- Gate oxide: 35 nm thermal SiO₂
- Gate electrode: 400 nm n+ polysilicon
- Backside contact: 400 nm aluminum

Critical Safety

- **HF handling:** Apron+gloves, face shield, no lone working, no glass beakers!
- **Furnace:** Thermal gloves for >800 °C operations
- **Metal anneal:** confirm Al spiking risk mitigated by Ti barrier, avoid ≥ 450 °C for Al

1 Starting Material

Substrate	Specification	Thickness	Box Name	Qty
Silicon	p-type <100>, 6", 1-10 Ω·cm	500 μm ± 20 μm	SP632	5

2 Critical Layers

Layer	Material	Thickness
Gate oxide	Thermal SiO ₂	35 nm
Gate electrode	n+ Poly-Si	400 nm
Back barrier/adhesion	Ti	100 nm
Back contact	Al	400 nm

3 Core Process Flow

Table 1: MOS Capacitor Process Flow

Step	Process	Equipment	Parameters	Comment
1 Dry-Ox				
1.1	Inspection	4-point probe + Thickness tool	Measure resistivity and thickness on one wafer	Verify starting material specifications.
1.2	Pre-oxidation clean	RCA bench	Standard RCA clean	Can be skipped for fresh, out-of-the-box wafers.
1.3	Gate SiO ₂ growth	Furnace: Oxidation (8") E1	Recipe: DRY1000 Oxidation time: 40 min Anneal time: 20 min	Target thickness: 35 nm.
1.4	Inspection	Ellipsometer		Verify oxide thickness.
2 Poly-Si				
2.1	Pre-deposition clean	RCA bench	Standard RCA clean	Required if wafers were stored after Step 1.
2.2	Poly-Si deposition	Furnace: LPCVD Poly-Si (6") E2	Recipe: DOPEPOLY Deposition time: 2 h	Target thickness: 400 nm.
2.3	Inspection	Filmtek / Ellipsometer		Verify poly-Si thickness.
3 Anneal Poly-Si				
3.1	Pre-anneal clean	RCA bench	Standard RCA clean	Required if wafers were stored after Step 2.
3.2	Poly-Si anneal	Furnace: Oxidation (8") E1	Recipe ANN1000: 20 min at 1000 °C	Activates dopants and improves film quality.
4 Etch gate Poly-Si				
4.1	Gate lithography: Coat	Spin Coater: Gamma UV	Sequence 1611: 1.5 µm HMDS resist. Spin: 30 s @ 4600 rpm. Softbake: 90 s @ 90 °C.	
4.2	Gate lithography: Exposure	Aligner: MLA2	Mask: gate_poly. Laser: 375 nm. Dose: 325 mJ/cm ² . Defocus: 2. Mode: Quality.	TEST exposure.
4.3	Gate lithography: Develop	Developer: TMAH UV-lithography	Sequence 3001: PEB 60 s @ 100 °C, SP 60 s.	
4.4	Litho inspection	Optical microscope	Check pattern and alignment marks	
4.5	DRIE tool preparation	DRIE – Pegasus 3	Recipe: TDESC for 5 min	Chamber conditioning step.

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Table 1: MOS Capacitor Process Flow (Continued)

Step	Process	Equipment	Parameters	Comment
4.6	Gate poly-Si etch	DRIE – Pegasus 3	Recipe: ?? Cycles: ??	Etches the 400 nm poly-Si layer.
4.7	DRIE tool clean	DRIE – Pegasus 3	Recipe: 20 min stabilization + 10 min clean	Post-process chamber cleaning.
4.8	Etch inspection	DekTak	Check step height	Verify poly-Si is etched through.
4.9	Resist strip	Wet bench 06	Strip time: ??	
4.10	Final gate inspection	DekTak	Measure heights and widths	Verify critical dimensions (CD).
5	Backside preparation			
5.1	Backside oxide strip	Wet bench 04: BHF 2	40 s (etch rate 75 nm/min to 80 nm/min)	Perform <i>immediately before</i> back metalization to ensure Si surface.
6	Backside electrode			
6.1	Backside litho: Coat	Spin Coater: Gamma UV	Sequence 2411: 1.5 μ m nLOF 2020 resist. Spin: 6000 rpm. Softbake: 120 s @ 110 °C.	
6.2	Backside litho: Expose	Aligner: MLA2	Mask: gate_electrode. Laser: 375 nm. Dose: 450 mJ/cm ² . Defocus: 0. Mode: Quality.	TEST exposure.
6.3	Backside litho: Develop	Developer: TMAH UV-lithography	Sequence 3001: PEB 60 s @ 110 °C, SP 60 s	
6.4	Litho inspection	Optical microscope	Check pattern and alignment marks	
6.5	Backside metal deposition (Ti)	Temescal	Ti: 100 nm	Serves as adhesion/barrier layer.
6.6	Backside metal deposition (Al)	Temescal	Al: 400 nm	Main backside contact metal.
6.7	Lift-off	Wet bench 07		
6.8	Post-lift-off inspection	Optical microscope		Check pattern and alignment marks.
6.9	Contact anneal	RTP2 Jipelec	Recipe: ?? Temp: ?? Time: ??	Stabilizes the Ti/Al Si contact. Avoid $\geq 450^\circ\text{C}$ (Al spiking).

4 Critical Checks

Step	QC Verification
1.3	Oxide thickness: 35 nm \pm 1 nm
3.2	Poly n+ sheet resistance: $\leq 30 \Omega/\square$
4.10	Gate CD: $\pm 0.5 \mu\text{m}$
5.1	Backside oxide fully removed (contact-angle change, test drop, or monitor wafer)
6.5	Backside Ti sheet resistance $\approx 0.3 \Omega/\square$ (100 nm Ti)
6.6	Backside Al sheet resistance $\approx 0.07 \Omega/\square$ (400 nm Al)
6.9	Contact anneal; contact resistance to Si governed by Ti/Si interface quality (target $< 1 \Omega \cdot \text{contact}$)

5 Process Flow Diagram

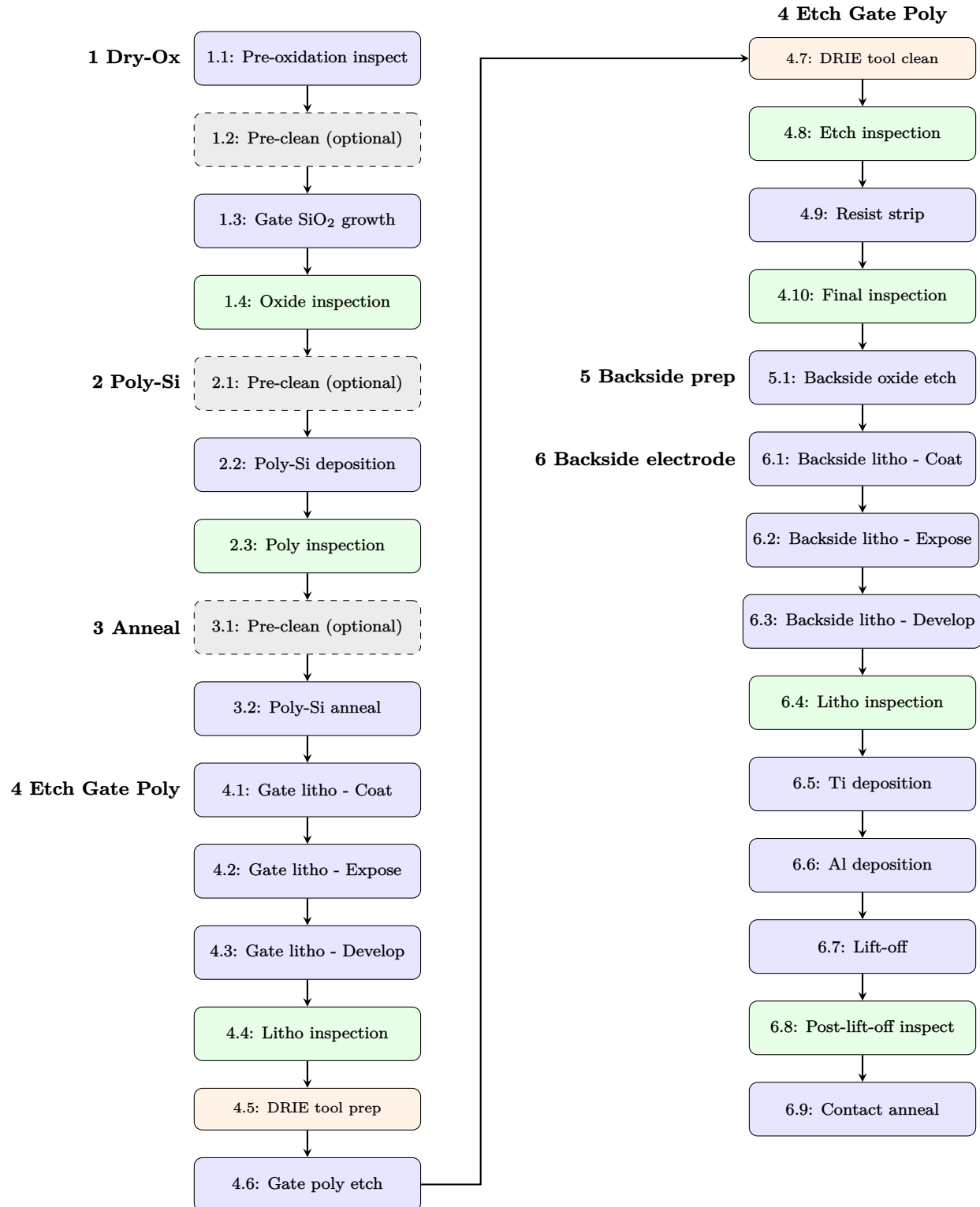


Figure 1: Process flow diagram for MOS capacitor fabrication.

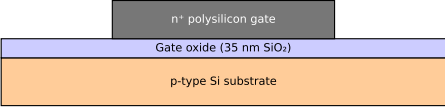
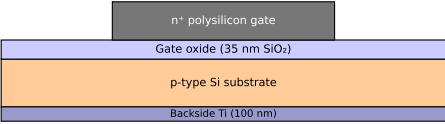
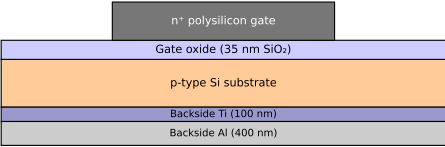
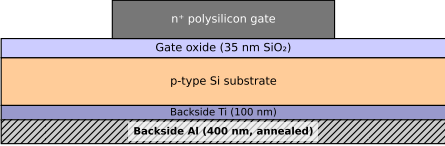
6 Required Figures

Table 2: Cross-sectional illustrations of key process steps in the MOS capacitor fabrication flow.

ID	Step	Description
1	1.1	 <p>p-type Si substrate</p> <p>Starting Si wafer</p>
1	1.3	 <p>Gate oxide (35 nm SiO₂)</p> <p>p-type Si substrate</p> <p>Gate oxide growth</p>
2	2.2	 <p>Polysilicon (blanket)</p> <p>Gate oxide (35 nm SiO₂)</p> <p>p-type Si substrate</p> <p>Poly-Si deposition (blanket)</p>
3	3.2	 <p>n⁺ polysilicon (blanket)</p> <p>Gate oxide (35 nm SiO₂)</p> <p>p-type Si substrate</p> <p>Poly-Si anneal (doped)</p>
4	4.6	 <p>n⁺ polysilicon gate</p> <p>Gate oxide (35 nm SiO₂)</p> <p>p-type Si substrate</p> <p>Gate poly etch</p>

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Table 2: Cross-sectional illustrations of key process steps in the MOS capacitor fabrication flow. (Continued)

5	5.1	<div><p>Backside oxide strip</p></div>
6	6.5	<div><p>Backside Ti deposition</p></div>
7	6.6	<div><p>Backside Al deposition</p></div>
8	6.9	<div><p>Contact anneal</p></div>