Process flow title:	**Minimal MOS Capacitor Process**	**Revision:**	**Rev 0.3**
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Process Overview

Minimal MOS capacitor fabrication flow.

Key Specifications

- Gate oxide: 35 nm thermal SiO_2
- Gate electrode: 400 nm n+ polysilicon
- Backside contact: 400 nm aluminum

Critical Safety

- **HF handling:** Apron+gloves, face shield, no lone working, no glass beakers!
- **Furnace:** Thermal gloves for >800 °C operations
- **Metal anneal:** confirm Al spiking risk mitigated by Ti barrier, avoid $\geq$ 450 °C for Al

1 Starting Material

Substrate	Specification	Thickness	Qty
Silicon	p-type <100>, 6", 1-10 Ω·cm	500 µm ± 20 µm	5

2 Critical Layers

Layer	Material	Thickness
Gate oxide	Thermal SiO_2	35 nm
Gate electrode	n+ Poly-Si	400 nm
Back barrier/adhesion	Ti	100 nm
Back contact	Al	400 nm

3 Core Process Flow

Table 1: MOS Capacitor Process Flow

Step	Process	Equipment	Parameters	Comment
1		**Dry-Ox**		
1.1	Pre-oxidation inspection	4-point probe + Thickness tool	Measure resistivity and thickness on one wafer	Verify starting material specifications.
1.2	(Optional) Pre-oxidation clean	RCA bench	Standard RCA clean	Can be skipped for fresh, out-of-the-box wafers.
1.3	Gate SiO_2 growth	Furnace: Oxidation (8") E1	Recipe DRY1000: 40 min oxidation + 20 min anneal at 1000 °C	Target thickness: 35 nm. Growth rate ca. 0.875 nm min^{-1}.
1.4	Inspection	Ellipsometer		Verify oxide thickness.
2		**Poly-Si**		
2.1	(Optional) Pre-deposition clean	RCA bench	Standard RCA clean	Required if wafers were stored after Step 1.
2.2	Poly-Si deposition	Furnace: LPCVD Poly-Si (6") E2	Recipe DOPEPOLY: 2 h deposition	Target thickness: 400 nm.
2.3	Inspection	Filmtek / Ellipsometer		Verify poly-Si thickness.
3		**Anneal**		
3.1	(Optional) Pre-anneal clean	RCA bench	Standard RCA clean	Required if wafers were stored after Step 2.
3.2	Poly-Si anneal	Furnace: Oxidation (8") E1	Recipe ANN1000: 20 min at 1000 °C	Activates dopants and improves film quality.
4		**DRIE backside**		
4.1	DRIE tool preparation	DRIE – Pegasus 3	Recipe: TDESC for 5 min	Chamber conditioning step.
4.2	Backside Si etch	DRIE – Pegasus 3	Recipe: ??; Cycles: ??	Thins the wafer from the backside.
4.3	DRIE tool clean	DRIE – Pegasus 3	Recipe: 20 min stabilization + 10 min clean	Post-process chamber cleaning.
5		**Oxide etch backside**		
5.1	Backside oxide etch	Wet bench 04: BHF 2	40 s (etch rate 75 nm/min to 80 nm/min)	Removes the 35 nm oxide from the backside.
6		**Etch gate poly**		
6.1	Gate lithography: Coat	Spin Coater: Gamma UV	Sequence 1611: 1.5 µm HMDS resist. Spin: 30 s @ 4600 rpm. Softbake: 90 s @ 90 °C.	

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Table 1: MOS Capacitor Process Flow (Continued)

6.2	Gate lithography: Expose	Aligner: MLA2	Mask: gate_poly. Laser: 375 nm. Dose: 325 mJ/cm^2. Defocus: 2. Mode: Quality.	TEST exposure.
6.3	Gate lithography: Develop	Developer: TMAH UV-lithography	Sequence 3001: PEB 60 s @ 100 °C, SP 60 s.	
6.4	Litho inspection	Optical microscope	Check pattern and alignment marks	
6.5	DRIE tool preparation	DRIE – Pegasus 3	Recipe: TDESC for 5 min	Chamber conditioning step.
6.6	Gate poly-Si etch	DRIE – Pegasus 3	Recipe: ??; Cycles: ??	Etches the 400 nm poly-Si layer.
6.7	DRIE tool clean	DRIE – Pegasus 3	Recipe: 20 min stabilization + 10 min clean	Post-process chamber cleaning.
6.8	Etch inspection	DekTak	Check step height	Verify poly-Si is etched through.
6.9	Resist strip	Wet bench 06	Strip time: ??	
6.10	Final gate inspection	DekTak	Measure heights and widths	Verify critical dimensions (CD).
7	**Backside electrode**			
7.1	Backside litho: Coat	Spin Coater: Gamma UV	Sequence 2411: 1.5 µm nLOF 2020 resist. Spin: 6000 rpm. Softbake: 120 s @ 110 °C.	
7.2	Backside litho: Expose	Aligner: MLA2	Mask: gate_electrode. Laser: 375 nm. Dose: 450 mJ/cm^2. Defocus: 0. Mode: Quality.	TEST exposure.
7.3	Backside litho: Develop	Developer: TMAH UV-lithography	Sequence 3001: PEB 60 s @ 110 °C, SP 60 s	
7.4	Litho inspection	Optical microscope	Check pattern and alignment marks	
7.5	Gate metal deposition	Temescal/E-beam	Ti: 100 nm	
7.6	Gate metal deposition	Temescal/E-beam	Al: 400 nm	
7.7	Lift-off	Wet bench 07		
7.8	Post-lift-off inspection	Optical microscope		Check pattern and alignment marks.
7.9	Contact anneal	RTP2 Jipelec	Recipe: ??; Temp: ??; Time: ??	Stabilizes the metal-silicon contact.

4 Critical Checks

Step	QC Verification
2.1	Oxide thickness: $35\,\text{nm} \pm 1\,\text{nm}$
3.1/3.2	Poly n+ sheet resistance: $\leq 30\ \Omega/\square$
4.1	Gate CD: $\pm\ 0.5\,\mu\text{m}$
5.0	Backside oxide fully removed (contact-angle change, test drop, or monitor wafer)
5.1	Backside Ti sheet resistance $\approx 0.3\ \Omega/\square$(100 nm Ti)
5.2	Backside Al sheet resistance $\approx 0.07\ \Omega/\square$(400 nm Al)
5.3	Contact anneal; contact resistance to Si governed by Ti/Si interface quality (target $< 1\ \Omega\cdot$contact)

5 Process Flow Diagram

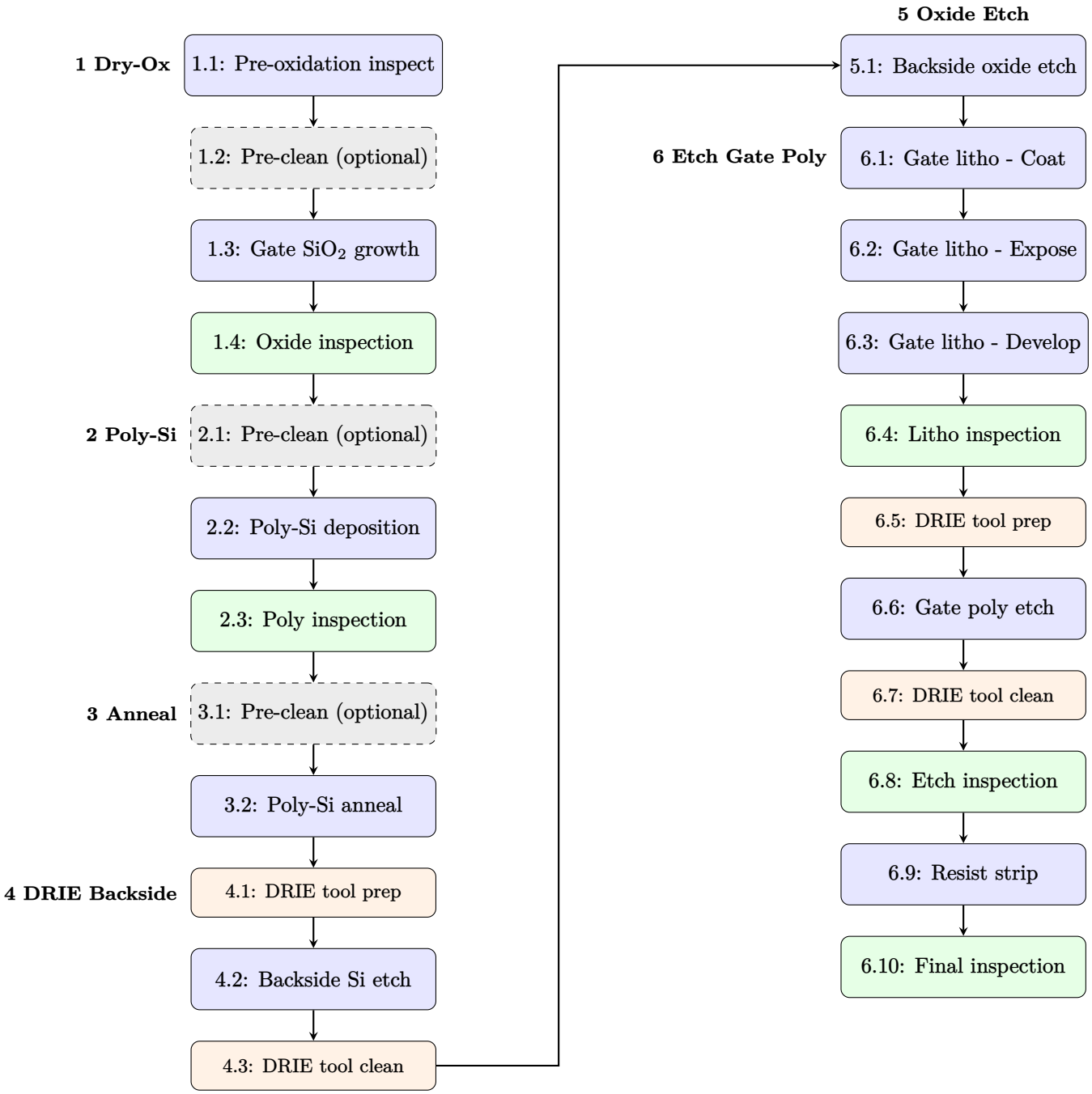


Figure 1: Process flow diagram for MOS capacitor fabrication.

6 Required Figures

Table 2:

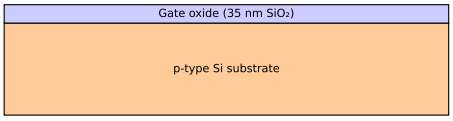
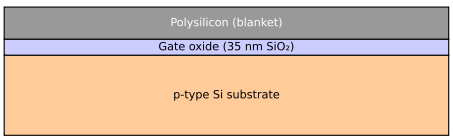
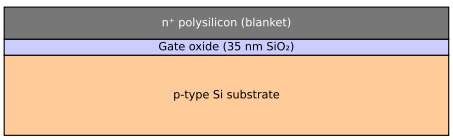
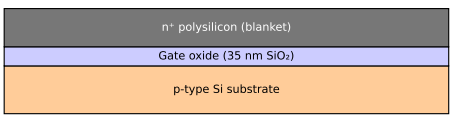
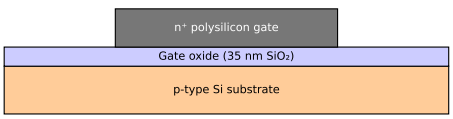
ID	Step	Description
1	1.3	 Gate oxide growth
2	2.2	 Poly-Si deposition (blanket)
3	3.2	 Poly-Si anneal (doped)
4	4.2	 Backside oxide strip
5	6.6	 Gate poly etch

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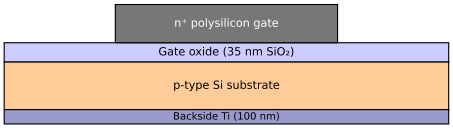
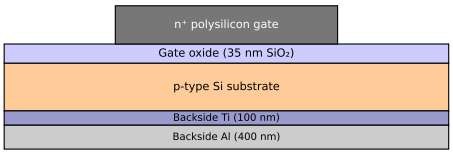
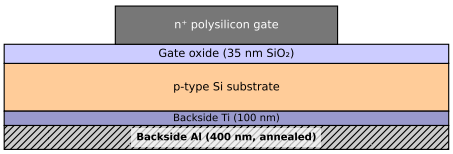
Table 2: (Continued)

6	7.5	 Backside Ti deposition
7	7.6	 Backside Al deposition
8	7.9	 Contact anneal