Process flow title:	Minimal MOS Capacitor Process	Revision:	Rev 0.5
Contact email:	jephin@dtu.dk	Contact name:	Jeppe Hinrichs
Contact phone:	Not applicable		
LabMan-ager group:	Not applicable	Batch name:	TBD
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### **Process Overview**

Minimal MOS capacitor fabrication flow.

#### **Key Specifications**

• Gate oxide:  $35\,\mathrm{nm}$  thermal  $\mathrm{SiO}_2$ 

• Gate electrode: 400 nm n+ polysilicon

• Backside contact: 400 nm aluminum

#### **Critical Safety**

• HF handling: Apron+gloves, face shield, no lone working, no glass beakers!

• Furnace: Thermal gloves for  $>800\,^{\circ}\mathrm{C}$  operations

• Metal anneal: confirm Al spiking risk mitigated by Ti barrier, avoid ≥ 450 °C for Al

#### **Starting Material** 1

Substrate	Specification	Thickness	Box Name	Qty
Silicon	p-type <100>, 6", 1-10 $\Omega$ ·cm	$500\mu\mathrm{m}\pm20\mu\mathrm{m}$	SP632	5

## **Critical Layers**

Layer	Material	Thickness	
Gate oxide	Thermal $SiO_2$	$35\mathrm{nm}$	
Gate electrode	n+ Poly-Si	$400\mathrm{nm}$	
Back barrier/adhesion	Ti	$100\mathrm{nm}$	
Back contact	Al	$400\mathrm{nm}$	

#### 3 Core Process Flow

Table 1: MOS Capacitor Process Flow

Step	Process	Comment		
$\frac{1}{1}$	Process Equipment Parameters  Dry-Ox			
1.1	Inspection	4-point probe + Thickness tool	Measure resistivity and thickness on one wafer	Verify starting material specifications.
1.2	Pre-oxidation clean	RCA bench	Standard RCA clean	Can be skipped for fresh, out-of-the-box wafers.
1.3	Gate $SiO_2$ growth	Furnace: Oxidation (8") E1	Recipe: DRY1000 Oxidation time: 40 min Anneal time: 20 min	Target thickness: 35 nm.
1.4	Inspection	Ellipsometer		Verify oxide thickness.
2			Poly-Si	
2.1	Pre-deposition clean	RCA bench	Standard RCA clean	Required if wafers were stored after Step 1.
2.2	Poly-Si deposition	Furnace: LPCVD Poly-Si (6") E2	Recipe: POLYBOR Deposition time: 2 h Target thickness: 400 nm.	ATT: Requires extensive equipment prep.
2.3	Inspection	Filmtek / Ellipsometer		Verify poly-Si thickness.
3		Ann	eal Poly-Si	
3.1	Pre-anneal clean	RCA bench	Standard RCA clean	Required if wafers were stored after Step 2.
3.2	Poly-Si anneal Furnace: Oxida- Recipe ANN1000: 20 min at tion (8") E1 1000 °C		Recipe ANN 1000: 20 min at 1000 °C	Activates dopants and improves film quality.
4		Backsid	le Poly-Si etch	
4.1	DRIE tool preparation	DRIE – Pegasus 3	Recipe: TDESC, 5 min	Chamber conditioning step.
4.2	Backside poly-Si etch	DRIE – Pegasus 3	Recipe: SF6_02_250W_0.7_0.3	Removes blanket poly- Si from backside.
4.3	DRIE tool clean	DRIE – Pegasus 3	Recipe: 20 min stabilization $+$ 10 min clean	Post-process chamber cleaning.
5		Backsi	de oxide etch	
5.1	Backside oxide etch	Wet bench 04: BHF 2	$40 \mathrm{s}$ (etch rate $75 \mathrm{nm/min}$ to $80 \mathrm{nm/min}$ )	Removes backside oxide (35 nm) prior to metal deposition.
6		Etch	gate Poly-Si	

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Table 1: MOS Capacitor Process Flow (Continued)

Sequence 1611: 1.5 µm   HMDS resist.   Spin 30 s @ 4600 rpm.   Softbake: 90 s @ 90 °C.	eters	Param	p Process Equipment		Step		
Laser: 375 mm. Dose: 325 mJ/cm². Defocus: 2. Mode: Quality.  6.3 Lithography: Develop Developer: TMAH UV-lithography Dose: 450 mJ/cm². Defocus: 2. Mode: Quality.  6.4 Inspection Optical microscope Check gate pattern and alignment marks  6.5 DRIE tool preparation DRIE – Pegasus 3 Recipe: TDESC for 5 min Chamber constep.  6.6 Poly-Si etch DRIE – Pegasus 3 Recipe: Etches the 40 SF6_02_250W_0.7_0.3 Si layer.  6.7 DRIE tool clean DRIE – Pegasus 3 Recipe: 20 min stabilization post-process cleaning.  6.8 Inspection DekTak Check step height Verify poly-Statrough.  6.9 Resist strip Wet bench 06 Strip time: 10 min Measure heights and widths Verify critics sions (CD).  7 Backside electrode  Sequence 2411: 1.5 µm nLOF 2020 resist. Spin: 6000 rpm. Softbake: 120 s @ 110 °C. Mask: gate_electrode. Laser: 375 nm. Dose: 450 mJ/cm². Description: TEST expose Defocus: 0. Mode: Quality.  7.3 Lithography: Develop Developer: TMAH UV-lithography 110 °C, SP 60 s  Check backside pattern and Dose: 325 mJ/cm². Description: Delative polonic pattern and Dose: 450 mJ/cm². TEST expose Defocus: 0. Mode: Quality.  Check backside pattern and Drivert poloric poloric pattern and Drivert poloric pattern and pattern and alignment marks  Sequence 3001: PEB 60 s @ 110 °C, SP 60 s  Check backside pattern and Drivert poloric pattern and	resist. $0 { m s} @ 46$	HMDS Spin: 3		_	: Coat	Lithography:	6.1
UV-lithography 100°C, SP 60 s.  6.4 Inspection Optical microscope	75 nm. 25 mJ/ : 2.	Laser: Dose: 3 Defocus	MLA2	Aligner: M	: Expose	Lithography:	6.2
scope alignment marks  6.5 DRIE tool preparation DRIE – Pegasus 3 Recipe: TDESC for 5 min Chamber co step.  6.6 Poly-Si etch DRIE – Pegasus 3 Recipe: SF6_02_250W_0.7_0.3 Si layer.  6.7 DRIE tool clean DRIE – Pegasus 3 Recipe: 20 min stabilization + 10 min clean + 10 min clean + 10 min clean + 10 min clean  6.8 Inspection DekTak Check step height Verify poly-S through.  6.9 Resist strip Wet bench 06 Strip time: 10 min  6.10 Final gate inspection DekTak Measure heights and widths Verify critic sions (CD).  7 Backside electrode  7.1 Lithography: Coat Spin Coater: Gamma UV  Sequence 2411: 1.5 µm nLOF 2020 resist. Spin: 6000 rpm. Softbake: 120 s @ 110 °C.  Mask: gate_electrode. Laser: 375 nm. Dose: 450 mJ/cm². Defocus: 0. Mode: Quality.  7.3 Lithography: Develop Developer: TMAH UV-lithography  7.4 Inspection Optical micro- Check backside pattern and		-		-	: Develop	Lithography:	6.3
step.  6.6 Poly-Si etch  DRIE - Pegasus 3  Recipe: SF6_02_250W_0.7_0.3  Si layer.  6.7 DRIE tool clean  DRIE - Pegasus 3  Recipe: 20 min stabilization + 10 min clean  Check step height  Verify poly-St through.  6.8 Inspection  DekTak  Check step height  Verify poly-St through.  6.9 Resist strip  Wet bench 06  Strip time: 10 min  6.10 Final gate inspection  DekTak  Measure heights and widths  Verify critic sions (CD).  7  Backside electrode  Sequence 2411: 1.5 µm nLOF 2020 resist. Spin: 6000 rpm. Softbake: 120 s @ 110 °C.  Mask: gate_electrode. Laser: 375 nm.  Dose: 450 mJ/cm². Defocus: 0. Mode: Quality.  7.3 Lithography: Develop  Developer: TMAH UV-lithography  110 °C, SP 60 s  7.4 Inspection  Optical micro-  Check backside pattern and	-		micro-	-		Inspection	6.4
SF6_02_250W_0.7_0.3 Si layer.  6.7 DRIE tool clean  DRIE - Pegasus 3  Recipe: 20 min stabilization + 10 min clean  Check step height  Verify poly-Sthrough.  Check step height  Verify poly-Sthrough.  Check step height  Verify critics sions (CD).  Third gate inspection  DekTak  Backside electrode  Sequence 2411: 1.5 µm nLOF 2020 resist. Spin: 6000 rpm. Softbake: 120 s @ 110 °C.  Mask: gate_electrode.  Laser: 375 nm. Dose: 450 mJ/cm². Defocus: 0. Mode: Quality.  Lithography: Develop  Developer: TMAH UV-lithography  Test expose  Lithography: Develop  Developer: TMAH UV-lithography  Test expose  Check backside pattern and	TDES	Recipe:	egasus 3	DRIE – P	oreparation	DRIE tool pr	6.5
+ 10 min clean cleaning.  6.8 Inspection DekTak Check step height Verify poly-Sthrough.  6.9 Resist strip Wet bench 06 Strip time: 10 min  6.10 Final gate inspection DekTak Measure heights and widths Verify critics sions (CD).  7 Backside electrode  7.1 Lithography: Coat Spin Coater: Gamma UV  Sequence 2411: 1.5 µm nLOF 2020 resist. Spin: 6000 rpm. Softbake: 120 s @ 110 °C.  Mask: gate_electrode. Laser: 375 nm. Dose: 450 mJ/cm². Defocus: 0. Mode: Quality.  7.3 Lithography: Develop Developer: TMAH Sequence 3001: PEB 60 s @ 110 °C, SP 60 s  7.4 Inspection Optical micro- Check backside pattern and	_250W_	-	egasus 3	DRIE – P		Poly-Si etch	6.6
through.  6.9 Resist strip Wet bench 06 Strip time: 10 min  6.10 Final gate inspection DekTak Measure heights and widths Verify critics sions (CD).  7 Backside electrode  7.1 Lithography: Coat Spin Coater: Gamma UV  Sequence 2411: 1.5 µm nLOF 2020 resist. Spin: 6000 rpm. Softbake: 120 s @ 110 °C.  Mask: gate_electrode. Laser: 375 nm.  Dose: 450 mJ/cm². TEST expost Defocus: 0. Mode: Quality.  7.3 Lithography: Develop Developer: TMAH UV-lithography  Test of the proper of the proper of the pattern and the pa		-	egasus 3	DRIE – P	lean	DRIE tool cle	6.7
6.10 Final gate inspection DekTak Measure heights and widths Verify critications (CD).  7 Backside electrode  7.1 Lithography: Coat Spin Coater: Gamma UV Sequence 2411: 1.5 µm nLOF 2020 resist. Spin: 6000 rpm. Softbake: 120 s @ 110 °C.  Mask: gate_electrode. Laser: 375 nm. Dose: 450 mJ/cm². Defocus: 0. Mode: Quality.  7.2 Lithography: Develop Developer: TMAH UV-lithography UV-lithography 110 °C, SP 60 s  7.4 Inspection Optical micro- Check backside pattern and	tep hei	Check s		DekTak		Inspection	6.8
To a sions (CD).    The state of the state o	ne: 10	Strip ti	n 06	Wet bench		Resist strip	6.9
7.1 Lithography: Coat  Spin Coater: Gamma UV  Sequence 2411: 1.5 µm nLOF 2020 resist. Spin: 6000 rpm. Softbake: 120 s @ 110 °C.  Mask: gate_electrode. Laser: 375 nm. Dose: 450 mJ/cm². Defocus: 0. Mode: Quality.  7.3 Lithography: Develop  Developer: TMAH UV-lithography  Developer: TMAH UV-lithography  TEST expose 110 °C, SP 60 s  Test expose 110 °C, SP 60 s  Check backside pattern and	height	Measur		DekTak	spection	Final gate ins	6.10
7.1 Lithography: Coat  Spin Coater: Spin: 6000 rpm. Softbake: 120 s @ 110 °C.  Mask: gate_electrode. Laser: 375 nm. Dose: 450 mJ/cm². Defocus: 0. Mode: Quality.  7.3 Lithography: Develop  Developer: TMAH UV-lithography  Sequence 3001: PEB 60 s @ 110 °C, SP 60 s  7.4 Inspection  Optical micro- Check backside pattern and	$\operatorname{ctrod}$	ide ele	Backs				7
7.2 Lithography: Expose Aligner: MLA2 Dose: 450 mJ/cm². TEST expose Defocus: 0. Mode: Quality.  7.3 Lithography: Develop Developer: TMAH Sequence 3001: PEB 60 s @ UV-lithography 110 °C, SP 60 s  7.4 Inspection Optical micro- Check backside pattern and	020 res 000 rpn	nLOF 2 Spin: 6		_	: Coat	Lithography:	7.1
UV-lithography 110°C, SP 60 s  7.4 Inspection Optical micro- Check backside pattern and	75 nm. 50 mJ/ : 0.	Laser: 4 Dose: 4 Defocus	MLA2	Aligner: N	: Expose	Lithography:	7.2
		-		-	: Develop	Lithography:	7.3
scope alignment marks			micro-	Optical scope		Inspection	7.4
7.5 Metal deposition (Ti) Temescal Ti: 100 nm Serves as addrier layer.	nm	Ti: 100		Temescal	ition (Ti)	Metal deposit	7.5

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Table 1: MOS Capacitor Process Flow (Continued)

Step	Process	Equipment	Parameters	Comment
7.6	Metal deposition (Al)	Temescal	Al: 400 nm	Main backside contact metal.
7.7	Lift-off	Wet bench 07		
7.8	Inspection: Post-lift-off	Optical microscope		Check pattern and alignment marks.
7.9	Contact anneal	C4 Al-anneal	Standard recipe 20 min	Stabilizes the Ti/Al Si contact. Avoid $\geq$ 450 °C (Al spiking).

# 4 Critical Checks

Step	QC Verification
1.3	Oxide thickness: $35 \mathrm{nm} \pm 1 \mathrm{nm}$ (ellipsometer, monitor wafer)
2.2	Poly-Si thickness: $400 \mathrm{nm} \pm 20 \mathrm{nm}$ (ellipsometer/Filmtek)
3.2	Poly n+ sheet resistance: $\leq 30 \ \Omega/\Box$ (4-point probe)
6.6	Gate CD: $\pm$ 0.5 µm (optical inspection / DekTak)
5.1	Backside oxide fully removed (contact-angle test drop, ellipsometer, or monitor wafer)
7.5	Backside Ti sheet resistance $\approx 0.3~\Omega/\Box~(100\mathrm{nm}~\mathrm{Ti})$
7.6	Backside Al sheet resistance $\approx 0.07~\Omega/\Box~(400\mathrm{nm}~\mathrm{Al})$
7.9	Contact anneal; contact resistance to Si governed by Ti/Si interface quality (target $< 1~\Omega \cdot \text{contact}$ )

## 5 Process Flow Diagram

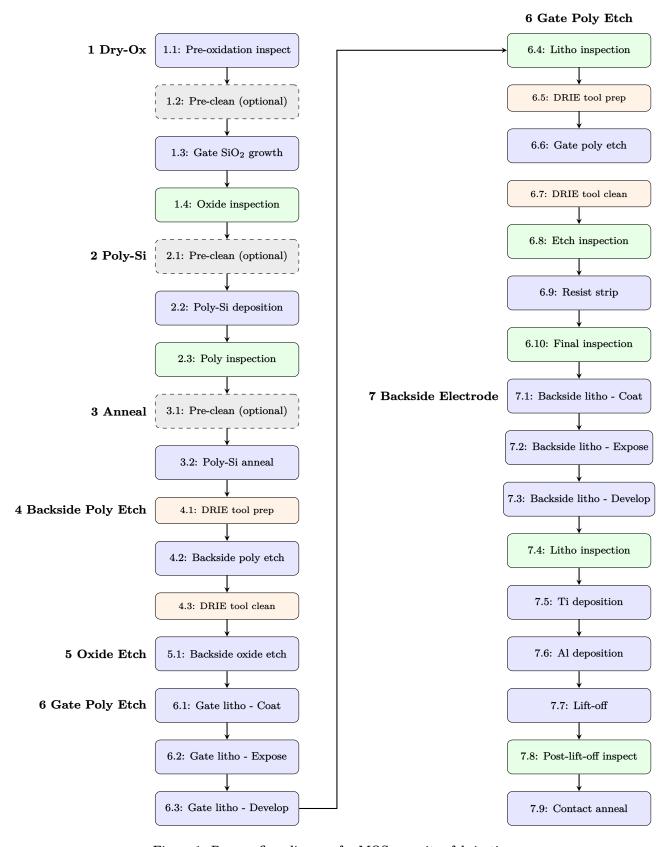


Figure 1: Process flow diagram for MOS capacitor fabrication.

# 6 Required Figures

Table 2: Cross-sectional illustrations of key process steps in the MOS capacitor fabrication flow.

ID	Step	Description
1	1.1	p-type SI substrate
		Starting Si wafer
1	1.3	Gate oxide (35 nm SiO <sub>2</sub> )  p-type Si substrate
		Gate oxide growth
		Gave onthe growth
2	2.2	Polysilicon (blanket)  Gate oxide (35 nm SiOx)  P-type SI substrate  Poly-Si deposition (blanket)
3	3.2	Poly-Si anneal (doped)
		r ory-or annear (doped)
4	4.2	n* polysilicon (blanket)  Gate oxide (35 nm SiO <sub>2</sub> )  p-type Si substrate
		Backside Poly-Si etched
		Continued or and area

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Table 2: Cross-sectional illustrations of key process steps in the MOS capacitor fabrication flow. (Continued)

5	5.1	Gate oxide (35 nm SiO <sub>2</sub> )  p-type Si substrate  Backside oxide etched
6	6.6	Gate Poly–Si patterned
7	7.5	Gate oxide (35 nm SiO <sub>2</sub> )  p-type Si substrate  Backside Ti (100 nm)  Backside Ti deposition
8	7.6	Gate oxide (35 nm SiO <sub>2</sub> )  p-type SI substrate  Backside Ti (100 nm)  Backside Al (400 nm)  Backside Al deposition
9	7.9	Gate oxide (35 nm SiO <sub>2</sub> )  p-type SI substrate  Backside Ti (100 nm)  Backside contact annealed