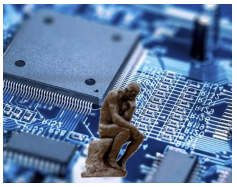
POLITECNICO DI TORINO

Dipartimento di Elettronica e Telecomunicazioni



DIGITAL SYSTEMS ELECTRONICS

Academic year 2022 - 2023

LABORATORY NR. 02

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GROUP 20

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The members of the group listed above declare under their own responsibility that no part of this document has been copied from other documents and that the associated code is original and has been developed expressly for the assigned project.

Contents

This lab objective is to get familiar with controlling the 7-segments displays built on the board by turning on and off the switches 9-0. In particular, it is required to make the symbols on those shifts and also learn how to implement an adder and a subtractor that has a visual output. This is also the first lab that requires the structural approach to correctly code the circuits.

1. Controlling a 7-segment display

DESIGN ENTRY:
The input dimension is 3 bit-wide, the switches from 0 to 2 are used to change the output visualised on the HEX0 display. The possible output values are ‘H’, ‘E’, ‘L’ and ‘O’. We have decided to use ‘H’ as the default value (when c1c0 = “00”) and the c2 switch is not used in this design (in order to minimise the work needed to adapt to other parts).

FUNCTIONAL SIMULATION:
There were a small number of inputs, so we decided to test all on both ModelSim and the physical board. In the first case the values were forcefully assigned, however on the board the physical switches are used.

SYNTHESIS:
The code works as intended, turning on or off the appropriate segments of the first 7-segment display. The code has been modified however, as the 7-segment display uses the vector input to block the display of segments and we thought it was doing the contrary.

2. *Multiplexing the 7-segment display output*

DESIGN ENTRY:
The circuit needs has been implemented with a 15 bit-wide input, where the switches 0 and 1 are used to choose a word from the following (HELLO, CELLO, CEPPO and FEPPO) and the switches from 2 to 4 are used to shift the letters of the chosen word according to the given truth-table.

The 7 letters used in the project are coded with a 3 bit-wide input. The codes are given in the comments of the file. As such, we comply with a 15 bit-wide input giving a 5 letters word.

This part has been implemented with lots of files, the main file is named “part2.vhd”.
The file named “char7_seg.whd” contains the bit sequences to display the inputs, meanwhile the files “shifter_15in_1b.vhd” and “shifter_15in_3b.vhd” are used to respectively shift the word and the letters of the chosen one.

FUNCTIONAL SIMULATION:
The test part has been divide in two section: the first one to settle down if all the different words were displayed, so we forcefully assigned values to the SW 1-0, then we tested the shifting part by assigning all the possible combination to the SW 4-2 and seeing the output to the “FEPPO” word.

SYNTHESIS:
The code is almost working as intended, only one of the five patterns is not displaying the word correctly shifted.

3. *Binary to Decimal Converter*

DESIGN ENTRY:
A structural approach is taken to tackle the design. The comparator is used to compare v and m, and circuitA

FUNCTIONAL SIMULATION:
To test the B2D converter, we use the input SW. A functioning circuit should give the expected numbers on both HEX1 and HEX0. The test gives the expected displayed values (as an example, SW = “0001” => HEX1 = 0, HEX0 = 1), thus validating the circuit.

SYNTHESIS:
The design works as intended, displaying the 10^1 numbers on HEX1 and 10^0 numbers on the other one.

4. Binary-to-BCD Converter

DESIGN ENTRY:
This circuit is reusing the precedent one and expands the system to a 6 bit wide input with one other circuit named CircuitB. We follow the plan presented, but we introduce on top of it a priority encoder which is essentially a 8 to 3 bit multiplexer with a choice system. It is using for the occasion some 2 to 1 multiplexers and another circuit which simulates the max function.

FUNCTIONAL SIMULATION:
In the simulation, we essentially assume that the system is working as the previous one (minus some changes), explaining the quasi-copy of “part3_tb”. The test gives the expected results above 15 (that were previously coded).

SYNTHESIS:
After some troubles getting the circuit design past the “Analysis” part, we have finally succeeded to get a working Binary-to-BCD Converter. Without exceptions, the circuit reacts to the switches being turned on, giving the decimal numbers on the 2 HEX displays.