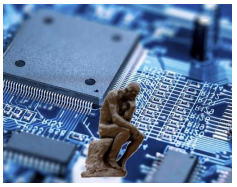
POLITECNICO DI TORINO

Dipartimento di Elettronica e Telecomunicazioni



DIGITAL SYSTEMS ELECTRONICS

Academic year 2022-2023

LABORATORY NR. 1

DUE DATE: March 27, 2022
DELIVERY DATE: March 21, 2022

GROUP 20

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The members of the group listed above declare under their own responsibility that no part of this document has been copied from other documents and that the associated code is original and has been developed expressly for the assigned project.

Contents

The first lab works as an introductory lesson to the work environment of VHDL, ModelSim and Intel Quartus Prime. The document is structured as individual and separate parts, replicating the lab structure.

1. Controlling the LEDs

DESIGN ENTRY

A 10 bit wide vector of switches is used to light up a 10 bit wide vector of leds. This serves more for properly discovering ModelSim and Intel Quartus Prime Lite than design in itself.

FUNCTIONAL SIM

Multiple sets of 10 bits are forcefully assigned to the switches to see if leds are correctly answering.

SYNTHESIS

It is working as intended, as long as we properly set the pin assignment in Intel Quartus Prime.
Every led copies the state of the led assigned to it.

2. 2-to-1 Multiplexer

DESIGN ENTRY

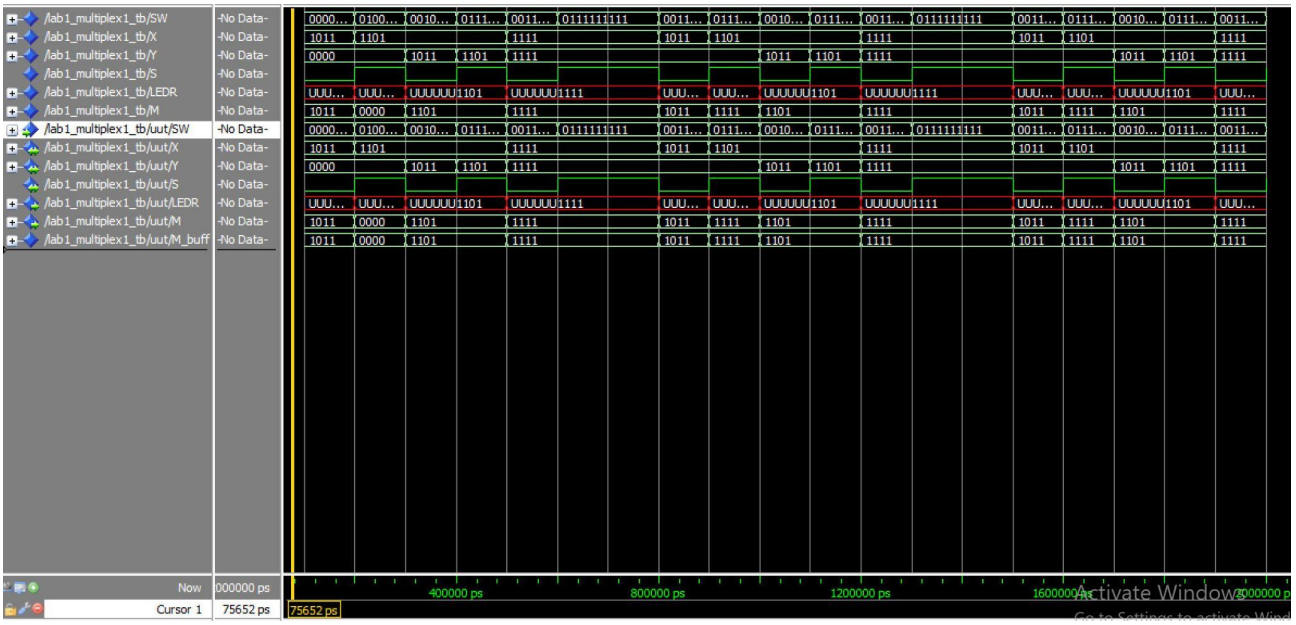
The 2-to-1 multiplexer has 2 4 bit-wide inputs where switches play the input part and the leds play the visualisation of the output. The inputs, such as the control inputs or the values, are unconditionally connected to the switches. A buffer named “M_buff” is used to assign to both the leds and the output M the value of the mux.

FUNCTIONAL SIM

In order to properly test the component, every input is tested by triggering the switches (virtually, values are forcefully assigned). One at a time, a chosen set of leds given a chosen set of switches is expected to turn on. We chose first to see if leds[4_7] and led[0_3] were properly turned on when the respective switches were triggered. The selector input behaviour is tested thereafter, with 2 sets (“1011” and “1101”)

SYNTHESIS

The program works as intended, lighting up the appropriate leds when the right switches are used. However, an additional led (led 5) is also lighting up when the switches[3_0] are on during the test on the board. We don’t know the reason for this additional behaviour.



Waves of the testbench of the 2-to-1 mux

3. *5-to-1 Multiplexer*

DESIGN ENTRY

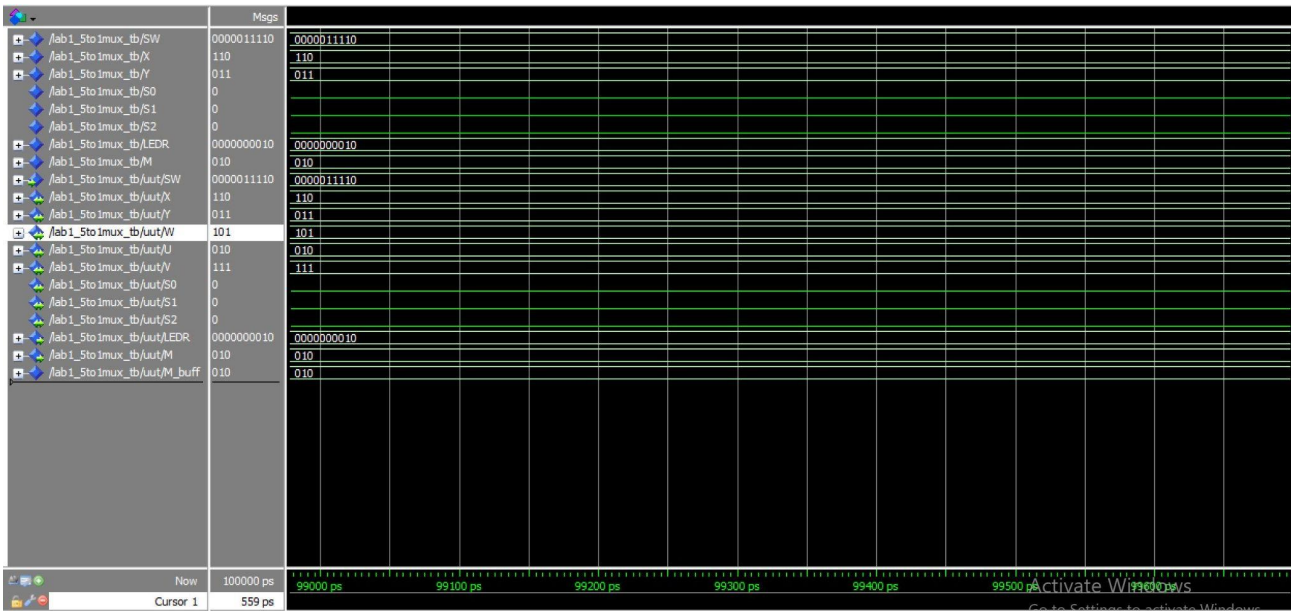
The 5-to-1 multiplexer has five 3 bit-wide inputs, the switches Sw_2-0 are the inputs and the leds are used to visualise the resulting output. A buffer named “M_buff” is used in order to assign to the output the value of the multiplexer.

FUNCTIONAL SIMULATION

The code has been tested both on the virtual environment and on the physical hardware. First the code has been tested virtually forcefully assigning the values in order to see the corresponding output, then we used the same approach described in the 2-to-1 mux for testing the code on the hardware (using only 3 switches instead for 4 as described in the “DESIGN ENTRY” section)

SYNTHESIS

The program has the expected behaviour according to the requirements, the corrects leds where turning on by triggering the switches according to the given truth table.



Waves of the testbench of the 5-to-1 mux