Open Cell Library in 15nm FreePDK Technology

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ABSTRACT

This paper presents the $15nm$ FinFET-based Open Cell Library (OCL) and describes the challenges in the methodology while designing a standard cell library for such advanced technology node. The $15nm$ OCL is based on a generic predictive state-of-the-art technology node. The proposed cell library is intended to provide access to advanced technology node for universities and other research institutions, in order to design digital integrated circuits and also to develop cell-based design flows, EDA tools and associated algorithms. Developing a $15nm$ standard cell library brings out design challenges which are not present in previous technology nodes. Some of these challenges include double-patterning for both metal and poly layers, a very restrictive set of physical design rules, and the demand for lithography-friendly patterns. This paper discusses the development of the library considering the challenges associated with advanced technology nodes.

Categories and Subject Descriptors

B.7.2 [**Hardware, Integrated Circuits**]: Design Aids; B.6.3 [**Hardware, Logic Design**]: Design Aids

General Terms

Design, Experimentation, Performance

Keywords

Standard cell Library, FinFET, Predictive Technology, Digital Integrated Circuit, ASIC Design

1. INTRODUCTION

Cell-based design is a widely adopted design methodology in current application-specific integrated circuit (ASIC) and system-on-chip (SOC) designs. This methodology is mainly based on standard cell libraries, which can be roughly defined as collections of basic building blocks that can be used to synthesize circuits. The use of cell libraries offers shorter design time and increases the circuit reliability, in the sense that the design process is less error-prone considering that the cells are pre-designed and verified. Most of cell-based designs rely on commercial cell libraries, which usually have restricted access, specially for advanced nodes. Due to those restrictions, both universities and other institutions have difficulties in having access to the information needed to perform research on EDA and design for advanced technology nodes.

Previous works have presented predictive standard cell libraries for educational and research purposes. In 2008, the open cell library $45nm$ (also known as FreePDK45) was released [26]. Since then, a considerable number of researchers have been using this library [5,8,36] . However, albeit its extensive use, the $45nm$ library does not correspond to a state-of-the-art technology node anymore, since there are new emerging technologies and devices, as FinFETs [15]. Synopsys also offers two generic standard cell libraries (also referred to as educational design kits): the $90nm$ and $32/28nm$ libraries [12, 31]. However, Synopsys' initiatives also do not represent state-of-the-art technologies anymore.

Since 2001, the International Technology Roadmap for Semiconductors (ITRS) has pointed out that FinFETs [15] are a promising technology for transistor scaling beyond CMOS limits [17]. Intel started using FinFETs in 2011, with the production of processors in $22nm$ technology [1,16]. Research efforts have been made to enable FinFET technologies, in order to continue the advances both in Moore's law and in Koomey's law [9, 11, 19–21, 27, 28, 35]. Recent works have also presented predictive technology models for high-performance and low-standby power FinFETs transistors in $20/16/14/10/7nm$ technology nodes [29, 30].

In this work, we present the $15nm$ FinFET based Open Cell Library (OCL) and we also describe the challenges in the methodology while designing a standard cell library for an advanced technology node. The $15nm$ OCL is based on a generic $15nm$ predictive state-of-the-art process design kit, the FreePDK15 [4]. The $15nm$ OCL can be downloaded in [24]. The proposed cell library is intended to provide access to advanced technology node for universities and other research institutions, in order to design digital integrated circuits and also to develop cell-based design flows, EDA tools and associated algorithms. Developing a $15nm$ standard cell library brings out design challenges which are not present in previous technology nodes. Some of these challenges include double-patterning for both metal and poly layers, a very restrictive set of physical design rules, and the

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demand for lithography-friendly patterns. This paper also discusses how the challenges associated to advanced technology nodes have affected the development of OCL.

This paper is organized as follows. In Section 2, the library content is presented. Section 3 discusses the main library characteristics, such as its architecture, design methodology and modeling. Section 5 describes the synthesis results of a public-domain design using the proposed library. In Section 6, future works are discussed. Section 7 outlines the conclusions.

2. LIBRARY CONTENT

In this section, we present the content released in the 15*nm* OCL, describing the set of cells and available views. The usual design flow needs to perform some tasks beyond combinational and sequential synthesis. Examples of these tasks are scan-chain insertion to yield circuit observability, clock tree synthesis and sizing of buffers. The proposed library was thought to be a small (but complete) cell set able to treat all these cell-based design demands.

The proposed library consists of 76 cells, covering 21 unique logic functions that commonly appear in circuits. Sequential cells as flip-flops, scan flops and latches were also included. Other cells include antenna, tie high, tie low, and filler cells.

Most of combinational cells are available in two different drive strengths (*X1* and *X2*). Driver cells, as inverters and different kinds of buffers (regular, clock and tri-state), are available in a wide range of drive strengths (from *X1* to *X16*). The list of all available cells and the respective drive strengths are presented in Appendix A, at the end of this paper.

The proposed library is being released with all necessary views to perform the usual tasks involved in commercial flows for integrated circuit design. The available views are presented in Table 1.

Table 1: List of available views released in the 15*nm* Open Cell Library.

View Name	File Extension	View Description
Technology Library	.lib	Provide logic, timing, power and area information of the cells in the library
Geometric Library	.lef	Provide information about the physical layout of the library in plain text, including design rules and abstract information about the cells
Simulation Library	.v	Provide a behavioral information of the cells for simulation intents
Cell Layouts	.gds	Provide information about planar geometric shapes, text labels, and other layout information in a binary format
Cell Netlists	.spi	Provide an instance-based transistor netlist, representing instances, nets, and some attributes
OpenAccess	.oa	Provide a database containing layouts and netlists

3. LIBRARY CHARACTERISTICS AND DESIGN CHALLENGES

This section presents the main characteristics of the proposed library. The following subsections introduce a general overview on its main features, its architecture, design methodology and modeling. Besides the characteristics, we also describe the challenges in the methodology while designing a standard cell library for such advanced technology node. Some fundamentals of the library were defined early, in conjunction with the design rules and fabrication technology definition for the PDK [4]. Details of FreePDK15 predictive technology are beyond the scope of this paper. For a detailed description of the PDK, we refer the reader to [3] and [4].

3.1 Library Overview

The 15*nm* OCL is based on multi-gate FinFET transistors, available in the target FreePDK15 technology [4]. The move from two- to three-dimensional transistors introduces several design challenges, including modeling. Figure 1 illustrates a 3D view of the 15*nm* PDK FinFET device. FinFETs originated in the 90s, when researchers were looking into possible successors to the planar transistor. FinFETs were proposed as a new structure for the FET transistor that would reduce leakage current [15]. FinFET technology takes its name from the fact that the FET structure used looks like a set of (radiator) fins when viewed. The peculiar gate structure present in a FinFET device provides a better electrical control over the channel, helping to reduce the leakage current and overcoming other short-channel effects. Given the control of the channel by the gate, the leak current is very small, thus reducing considerably the static leakage. This allows the use of lower threshold voltages, which improves the switching frequency and decreases the power consumption. FinFETs can also be implemented with two electrically independent gates, which allow the development of designs with low-power gates [28].

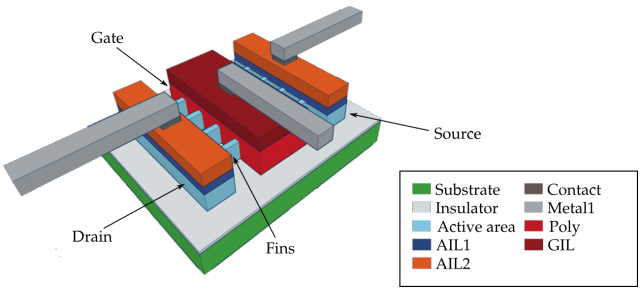

Figure 1: 3D view of the FreePDK 15*nm* transistor

The optical lithography process is an important aspect when designing a $15nm$ FinFET-based standard cell library. The target FreePDK15 technology adopts a double patterning technique as its predictive lithography process [3, 4]. Double patterning is a technique used in the lithography step that defines the features of integrated circuits at advanced process nodes. This technique is applied since the $32nm$ technology node , once enhancement techniques as as Optical Proximity Correction (OPC) were not compensating all diffraction errors and the photoresist started to blur [14]. In this library, the double patterning plays a vital role, both to poly-silicon and metal layers. This is due to the fact that most foundries are still using $193nm$ immersion lithography process [23]. The double patterning also imposes a regular layout, due to the poly-silicon arrangement. The line patterns formed by the regular poly-silicon reduces the number of exposures needed in the lithography process. Among different double patterning techniques, FreePDK15 adopts Self-Aligned Double Patterning (SADP) [2], as it has the lower overlay issues and it is well suited for further scaling [37].

Increasing the overall regularity in the circuit also poses difficulties in the layout. One of them occurs because some cells in the library have transistor networks in which the N-network are not dual to the P-network. In order to generate a valid network respecting the regularity constraints, the cell layout requires the insertion of gaps. In this case, the regular poly layers only controls one (NMOS or PMOS) FinFET, differently from a normal poly gate, which controls a pair of FinFETs. Figure 2 illustrates the layout of the D Flip-Flop labeled *DFFRNQ_X1*, in which it is possible to identify gaps where the poly layer controls just one FinFET (either PMOS or NMOS).

The very restrictive design rules of FreePDK15 also impose the need for dummy poly gates that do not control any FinFET. The poly layers are required to be repeated at regular intervals. Additionally, only two gate terminals can be placed in neighbor polys (depending on the transistor width). Some cells in the library require more than two gate terminals to be placed in subsequent neighbor poly layers. Due to this reason, one dummy poly layer that is not controlling FinFET transistors has to be inserted to isolate sequences of at most two neighbor gate terminals, in order to respect gate terminal separation design rules. Examples of dummy gates are also illustrated in Figure 2.

3.2 Library Architecture

In order to be used together, as the building blocks of a circuit, cells have to share some common characteristics to constitute a library. These shared characteristics among the cells are thought to allow routing of power rails by abutment, as well as sharing of wells and diffusion regions. The name commonly attributed to this set of standard positions and dimensions to be respected by the cells from a library is the library template. Figure 3 shows the template adopted in the OCL design. Beyond the physical template, the library shared characteristics include naming convention, physical design template, choice of available functions, drive-strength definitions, electrical and physical design guidelines, that some authors define as the library architecture [7]. This

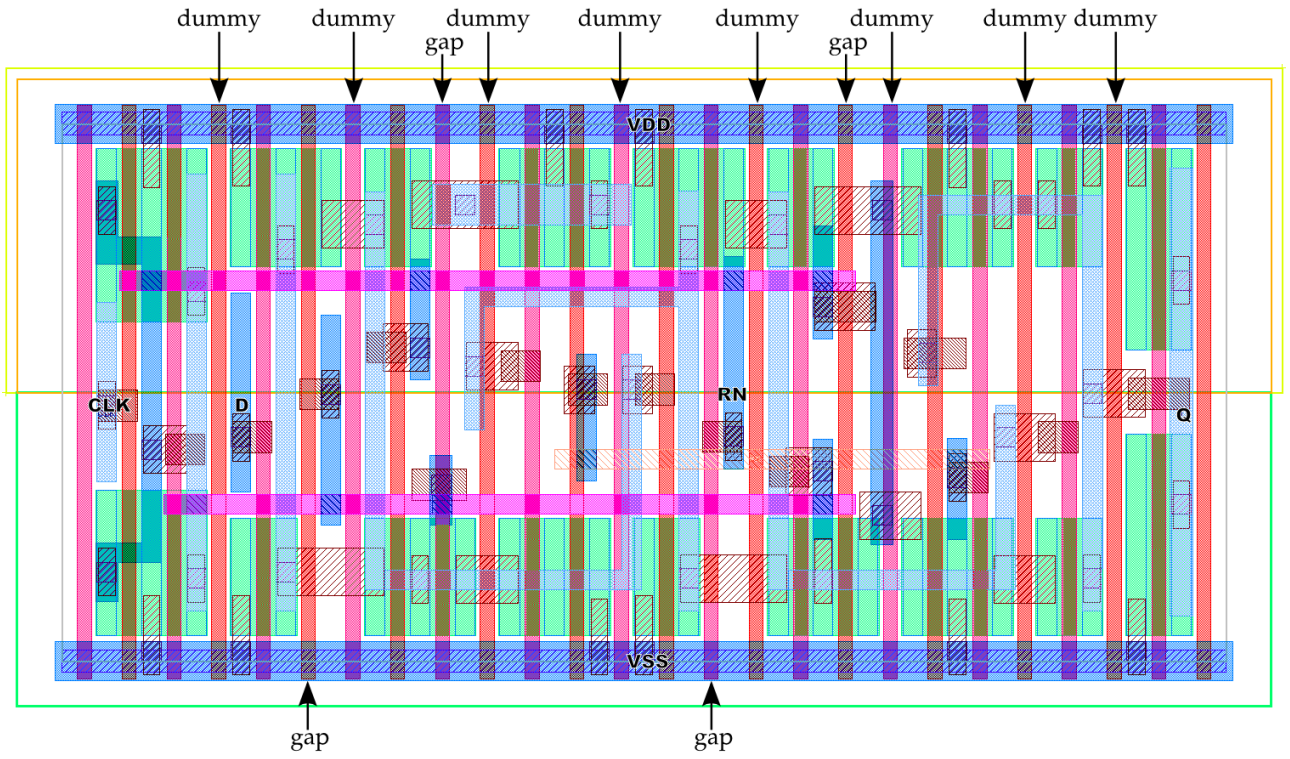

Figure 2: Layout of a D Flip-Flop with asynchronous reset containing 8 dummy gates, 4 gaps and 2 lines of metal2

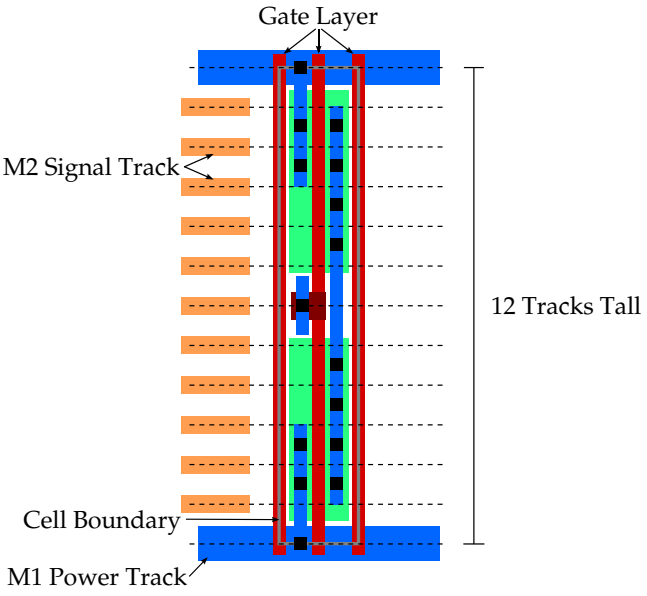

Figure 3: OCL cell physical template.

architectural specification is what distinguishes a standard cell library from a random collection of cells.

The chosen naming convention aims to inform the user about the main characteristics of the cell, while still being simple. For the combinational cells, the format is the name of the logic function and the number of inputs separated by an underscore and the drive strength (e.g. an AND with 4 inputs and drive strength of X2 has the name *AND4_X2*). The sequential cells have a similar definition. For instance, a scan D Flip-Flop with negated set, Q output and *X1* drive strength was named *SDFFSNQ_X1*. For cells that are neither combinational or sequential, the names chosen reflect the role in the library. The drive strength suffix only appears in these cells if it is meaningful.

The OCL cell physical template is illustrated in Figure 3. The developed cells are 12 metal 2 (M2) tracks tall, while the width is variable, but corresponds to an integer number of regular gate layers. This architecture features two wide metal 1 (M1) power tracks and eleven M2 tracks for internal signal routing.

The internal routing of the cells was designed to achieve acceptable levels of resistance and capacitance, while minimizing both cell area and the use of upper levels of metal. An example of adopted measures to minimize levels of resistance and capacitance while routing cells is to use as less as possible the so-called local interconnection layers, such as AIL1, AIL2 and GIL [3, 4]. The levels of resistance and capacitance are minimized when avoiding these layers due to their electrical properties. With relation to avoid upper levels of metal layers, among all 76 released cells, only 6 of them (around 8%) are using M2 for internal routing. There is no M3 being used inside the cells. All interconnection pins are in M1.

3.3 Cell Design Methodology

The library design was performed with the help of Nangate Library Creator [25], considering the device characteristics, design rules and constraints for the 15nm predictive technology. This subsection presents details about the methodology applied to design the proposed cells, such as the adopted P/N ratios, the transistor sizing approaches and a detailed description on the applied internal routing methodology.

The correct sizing of a standard cell is achieved by properly setting the number of N-type fins and P-type fins that produce almost equal rise and fall times, being equivalent to the P/N ratio. The P/N ratios were computed based on carrier mobility. In advanced technology nodes, it is possible to enhance the carrier mobility by straining the substrate [34]. This mobility enhancement increases the hole mobility, approximating the current capability of N and P transistors. As this feature can be observed in the 15nm technology model applied in this library, [4, 30], the P/N size ratio and fin ratio adopted for single-stage cells is 1.

When considering the transistor sizing, we adopted different approaches for single and multi-stage cells. As the library has less than 100 cells, more time could be invested to optimize each cell individually. The transistor sizing for single-stage cells (NAND, NOR, INV, AOI, OAI) were defined considering the regular layout structure of this technology. The adopted criteria was to increase transistor widths while avoiding transistor folding in order to maximize the cell performance without area drawbacks.

For multi-stage cells, we tried to apply the same single-stage criteria, additionally regarding the internal cell routability. In the cells with simple transistor networks (AND, OR, MUX, XOR, XNOR), performance could be maximized without routability problems. For complex cells, as half-adders, full-adders, and sequential cells, the sizing of each transistor pair was adjusted to yield internal cell routing while avoiding the use of upper levels of metal layers, without sacrificing performance whenever possible. In some layouts, so-called local interconnection layers (such as AIL2) were used to route close connection points in order to prevent metal 2 usage.

4. LIBRARY CHARACTERIZATION

This section presents the timing and power characterizations performed in the proposed library. For both timing and power characterization, we adopted the model of single input switching, where only one input signal switches at a time.

The 15nm OCL is characterized with three different timing delay models: (1) Non-Linear Delay Model (NLDM); (2) Effective Current Source Model (ECSM); and (3) Composite Current Source (CCS). In the following, we present a brief overview on these characterization models. Afterwards, details on the 15nm OCL timing and power characterization are presented.

4.1 Characterization Models

The Non-Linear Delay Model (NLDM) [18] is a voltage-based model that relies on input signal slopes and output capacitive loads. Such information is obtained from electrical simulations (Spice) and provided through the Liberty file in a look-up table (LUT) format. During the static timing analysis (STA), the gate delay characteristics of each instantiation are provided by these LUTs to compose the critical delay paths. Notice that the timing LUTs must be available for each input-to-output delay arc. A similar procedure based on LUTs is applied to the dynamic power consumption

analysis, whereas the static power (leakage) is evaluated for each gate input vector. As rarely the conditions of each gate instantiation match the LUT parameters (input slope and output load), the applied delay value is obtained through the interpolating of weighted average from LUT neighboring values. The gate output capacitive load considered in NLDM is most valid for old technology nodes, where the resistive and inductive effects in interconnection wiring can be neglected. However, the continuous process shrinking has emphasized the resistive behavior of wires impacting the STA accuracy. To overcome such a trouble, the concept of 'effective capacitance' was introduced [13]. However, the NLDM model still fails to consider some non-linearities such as the Miller effect [33]. Part of these challenges are treated by current-based models [10].

The Effective Current Source Model (ECSM) is a current-based model proposed by Cadence [6]. Current sources are able to consider more non-linear transistor switching behaviors. These source models also allow an accurate modeling of interconnections, which are even more complex in nanometer designs. Current sources also have additional granularity to reflect sensitivities like Miller capacitance, input transition times and output load. In ECSM, the concept of LUTs for gate delay characterization with different input slopes and output loads is still applied. However, instead of specific delay values at each LUT position, the gate output voltage waveform is described through a data vector. This waveform is segmented corresponding to the size of the vector and resulting in a trade-off between accuracy and data volume.

The Composite Current Source (CCS), also a current-based model, was proposed by Synopsys [32]. The main difference from ECSM is that the gate output current waveform is characterized instead of the output voltage performed by ECSM. An interesting improvement provided by CCS model was the extension of this kind of modeling to noise and power analysis, besides timing. However, there are still some practical accuracy limitations. Both ECSM voltage and CCS current waveforms are sampled with far fewer points from reference simulator's output, typically 1% to 10% of the reference points.

4.2 Timing Characterization

The $15nm$ OCL presents different characterization results considering these three timing models: NLDM, ECSM and CCS. Each model has five characterization corners: slow, typical, fast, low temperature and a worst case, which considers a low temperature characterization. The OCL also includes a functional library, containing only the cell functionality. All models use a 9x9 LUT dimension for timing. For ECSM, the output voltage waveform is presented in a 3D LUT, with a 9x9 table storing an array with up to 12 values. In the CCS case, the output current waveform is also presented in a 3D LUT, now with a 9x9 table storing an array with up to 17 values for fast and typical corners, while the worst corner has at most 20 values.

Notice that the NLDM is provided for convenience. However, since the OCL is an advanced node library and some discussed effects are not effectively modeled in NLDM, the use of a current-based model is recommended. Using NLDM model might require a large safety margin affecting the overall timing and power estimation.

4.3 Power Characterization

The main objective of a power characterization is to model both leakage and internal power of the standard cells. The leakage (or static power) is the power consumed by the gate when it is not switching. The internal power is related with the short-circuit power consumption and dynamic power of the diffusion capacitors at the output pin of the cell. The overall power consumption is evaluated by summing up the leakage power, internal power, and switching power (consumed when charging and discharging the load capacitance).

The NLDM- and ECSM-based power characterizations have a similar methodology for power characterization. In the OCL characterization for these models, we measure the leakage power by multiplying the supply voltage to the average current flowing out from the Vdd terminal, considering neither input nor output signal transition. The internal power is estimated differently for combinational and sequential cells. When taking combinational cells into account, the internal power is measured by subtracting the switching energy at the load capacitance from the total energy consumption when output signal transits. For sequential cells, we measured the internal power by considering the switching power of output, input and clock pins. The resulting characterizations of both NLDM- and ECSM-based models are presented by the $15nm$ OCL as a 9x9 LUT.

The CCS-based power characterization differs from NLDM- and ECSM-based models. The modelling for power based on CCS characterizations assumes the leakage power as a leakage current. The internal power is modeled as an internal current, which is derived from the dynamic current by subtracting the switching component. This way, we measured the leakage currents with simple DC analysis. The dynamic current is measured with transient analysis, capturing a current waveform for each combination of input transition time and output loads. The resulting dynamic current characterization of the CCS-based model is presented by the $15nm$ OCL as a 9x9 table storing an array with up to 15 values.

5. SYNTHESIS RESULTS

The benchmark chosen as case study in order to evaluate the proposed library is an OpenCore floating point unit [22]. This design implements the four basic arithmetic operations: sum, subtraction, multiplication and division. It respects the IEEE 754 standard for double precision (64 bit) floating point, and has 136 input pins and 70 output pins.

The benchmark was synthesized using a commercial tool. Besides the synthesis, we performed Place & Route. We compared results of the same benchmark using the $45nm$ OCL library. As the $45nm$ OCL has more cells than $15nm$ OCL, the extra cells were removed in order to have a fair comparison. Table 2 shows information about the used libraries and compares the area, delay and power consumption obtained for the circuit synthesized with the two libraries. The reduction column, when applicable, shows the reduction that the $15nm$ OCL circuit presented, compared to the $45nm$ OCL counterpart. The $15nm$ OCL circuit was able to reduce the total area (considering routing) by almost one order of magnitude, when compared to the $45nm$ implementation. The timing results show that the $45nm$ OCL had some difficulties to achieve the timing closure, for a target frequency of $1GHz$. Indeed, the $45nm$ OCL used more than 1500 buffers and inverters than $15nm$ OCL. As the $15nm$

Table 2: Results for OpenCore FPU benchmark

	15nm	45nm	Reduction
Library Characteristics			
Operation Voltage (V)	0.8	1.1	N/A
Operation Frequency (GHz)	1.0	1.0	N/A
Characterization Corner	Typical	Typical	N/A
Area Results			
Total Area (μm^2)	21706.92	211068.87	89.7%
Cell Area (μm^2)	15437.17	68566.29	77.5%
#Cells	31442	36583	14.1%
Timing Results			
Timing Slack (ps)	307.5	0	N/A
Power Results			
Leakage Power (mW)	0.542	1.365	60.3%
Dynamic Power (mW)	37.767	94.919	60.2%
Total Power (mW)	38.309	96.284	60.2%

had some slack, we increased the operation frequency and were able to achieve $5GHz$, for the $15nm$ implementation. Regarding the power consumption, both leakage and dynamic power were reduced to one third, compared against $45nm$ OCL. This reduction is also caused by the smaller operation voltage of $15nm$ compared to $45nm$.

6. FUTURE WORK

The presented library contains a functionally complete set of cells, meaning it can be used to successfully synthesize circuits with commercial flows. As future work, this set can be enhanced. We plan to develop a larger set of combinational cells, including complex cells (e.g. AOI, OAI) with more inputs. A wider set of sequential cells will also be implemented, adding cells with asynchronous inputs, scan chain support and different sizing. For multi-stage cells, the transistor size of first stage can be downsized to consume less power, with no significant drawbacks in cell delay. Another interesting enhancement is the support of different gate-length versions of the library (14, 16 and $20nm$). Finally, libraries characterized with different V_t would be necessary, in order to synthesize circuits aiming low power and/or high performance.

Both layout versus schematic (LVS) and layout parasitic extractions (PEX) files are not yet available. Also, some technology files are missing, such as design rule manual, design rule checking deck, and capacitance tables. These will be included as soon as they are made available by the FreePDK15 alliance.

7. CONCLUSIONS

This paper introduced the $15nm$ FinFET-based Open Cell Library (OCL). The library content, characteristics and characterization were presented. Together with its main characteristics, we also described the challenges in the methodology while designing a standard cell library for such advanced technology node. Some of these challenges include double-patterning for both metal and poly layers, a very restrictive set of physical design rules, and the demand for lithography-friendly patterns. The $15nm$ OCL can be downloaded in [24]. The proposed cell library is intended to provide access to advanced technology node for universities and other research institutions, in order to design digital integrated circuits and also to develop cell-based design flows, EDA tools and associated algorithms. In order to validate the proposed cell library, an OpenCore design using the $15nm$ OCL was successfully synthesized.

8. ACKNOWLEDGEMENTS

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APPENDIX

A. LIST OF AVAILABLE CELLS IN THE 15NM OPEN CELL LIBRARY

COMBINATIONAL CELLS			
Cell Name	*#In*	*Boolean Function*	*Drive Strengths*
BUF	1	$O = A$	X1, X2, X4, X8, X12 and X16
INV	1	$O =!A$	X1, X2, X4, X8, X12 and X16
AND2	2	$O = A * B$	X1 and X2
AND3	3	$O = A * B * C$	X1 and X2
AND4	4	$O = A * B * C * D$	X1 and X2
OR2	2	$O = A + B$	X1 and X2
OR3	3	$O = A + B + C$	X1 and X2
OR4	4	$O = A + B + C + D$	X1 and X2
NAND2	2	$O =!(A * B)$	X1 and X2
NAND3	3	$O =!(A * B * C)$	X1 and X2
NAND4	4	$O =!(A * B * C * D)$	X1 and X2
NOR2	2	$O =!(A + B)$	X1 and X2
NOR3	3	$O =!(A + B + C)$	X1 and X2
NOR4	4	$O =!(A + B + C + D)$	X1 and X2
MUX2	3	$O = A*!Sel + B * Sel$	X1
XOR2	2	$O = A \oplus B$	X1
XNOR2	2	$O =!(A \oplus B)$	X1
AOI21	3	$O =!((A * B) + C)$	X1 and X2
AOI22	4	$O =!((A * B) + (C + D))$	X1 and X2
OAI21	3	$O =!((A + B) * C)$	X1 and X2
OAI22	4	$O =!((A + B) * (C + D))$	X1 and X2
FA	3	$S = A \oplus B \oplus Cin$, $Cout = A \oplus B * Cin + A * B$	X1
HA	2	$S = A \oplus B$, $Cout = A * B$	X1
SEQUENTIAL CELLS			
Cell Name	*#In*	*Description*	*Drive Strengths*
DFFRNQ	3	D flip-flop with asynchronous $!reset$	X1
DFFSNQ	3	D flip-flop with asynchronous $!set$	X1
SDFFRNQ	5	D flip-flop with scan and asynchronous $!reset$	X1
SDFFSNQ	5	D flip-flop with scan and asynchronous $!set$	X1
LHQ	2	High enable Latch	X1
ADDITIONAL CELLS			
Cell Name	*#In*	*Description*	*Drive Strengths*
CLKBUF	2	Clock buffer	X1, X2, X4, X8, X12 and X16
TBUF	2	Tri-state buffer	X1, X2, X4, X8, X12 and X16
FILL	-	Filler cell	X1, X2, X4, X8 and X16
CLKGATETST	3	Clock gate with test pin	X1
ANTENNA	-	Antenna cell	-
FILLTIE	-	Cell to tie the wells	-
TIEH	-	Tie-high cell	-
TIEL	-	Tie-low cell	-