RMIT UNIVERSITY

School of Engineering

EEEET 2257 – ENGINEERING DESIGN 2

LAB 2: PRINTED CIRCUIT BOARD (PCB) DESIGN WITH ALTIUM DESIGNER

Aim

The primary aim of this laboratory is to gain familiarity with the following concepts:

- Create schematic symbols for new components.
- Define PCB footprints for components.
- Creating a custom PCB board size
- Placement of board mounting holes and defining a keep out region/layer
- Configure and transfer schematic capture design to PCB layout.
- Circuit partition and placement
- Routing
- Design Rules Check

Software

- *Altium Designer* software package

1. Introduction

The aim of this laboratory exercise is to give students experience in PCB layout design process using Altium Designer software package, including schematic capture, component footprint creation, schematic to PCB layout transfer, components placement, routing and running design rules check.

2. PCB layout of a BJT controlled Voltage regulator

2.1. Schematic Capture

The following schematic represents a BJT controlled voltage regulator circuit. The circuit is fed with a ***45 V input unregulated voltage***. The output, which is taken between ***V.out+ and V.out-***, is regulated to 8V and can be adjusted using ***V.ref***.

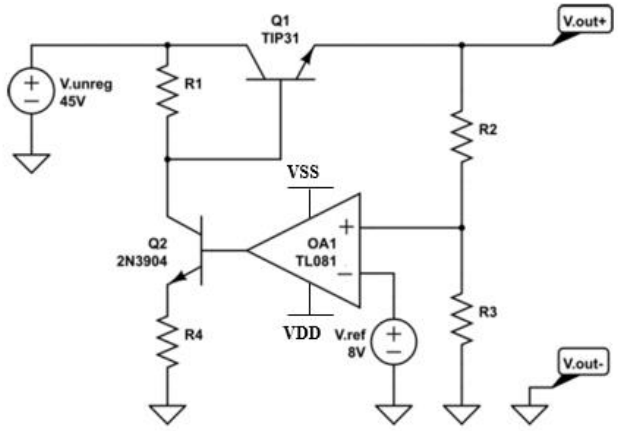


Figure 1: BJT Regulated Power Circuit.

In Altium, construct a schematic of the above circuit. Use the parts listed in the table below.

Table 1: List of components used in the BJT regulated power circuit.

Schematic label	**Design Item ID**	**Description**	**Library (*.IntLib)**	**Value**
R1, R2, R3, R4	Res1	Resistor	Miscellaneous Devices	1 kΩ
Q1	NPN	NPN Bipolar Transistor	Miscellaneous Devices	
Q2	2N3904	NPN General Purpose Amplifier	Miscellaneous Devices	
OA1 TL081	Op Amp	FET Operational Amplifier	Miscellaneous Devices	
V.unreg	Custom	2-pin terminal block	Custom library	45V
V.ref	Custom	2-pin terminal block	Custom library	8 V
VDD	Custom	2-pin terminal block	Custom library	10 V
VSS	Custom	2-pin terminal block	Custom library	-10 V

Notes:

- Components can be mirrored by pressing ‘X’ (vertical) or ‘Y’ (horizontal) while holding the selected component (holding left mouse button).
- Component can be rotated by pressing ‘Space bar’ while holding the selected component.
- Q1 transistor TIP31 is not explicitly available in the Altium library. It can be replaced by a generic model of an NPN transistor.
- Similarly, TL081 can be replaced by an NPN General Purpose Amplifier.

- Make sure you change the components annotations/designator accordingly.

When completed, your schematic should look similar to the schematic shown below:

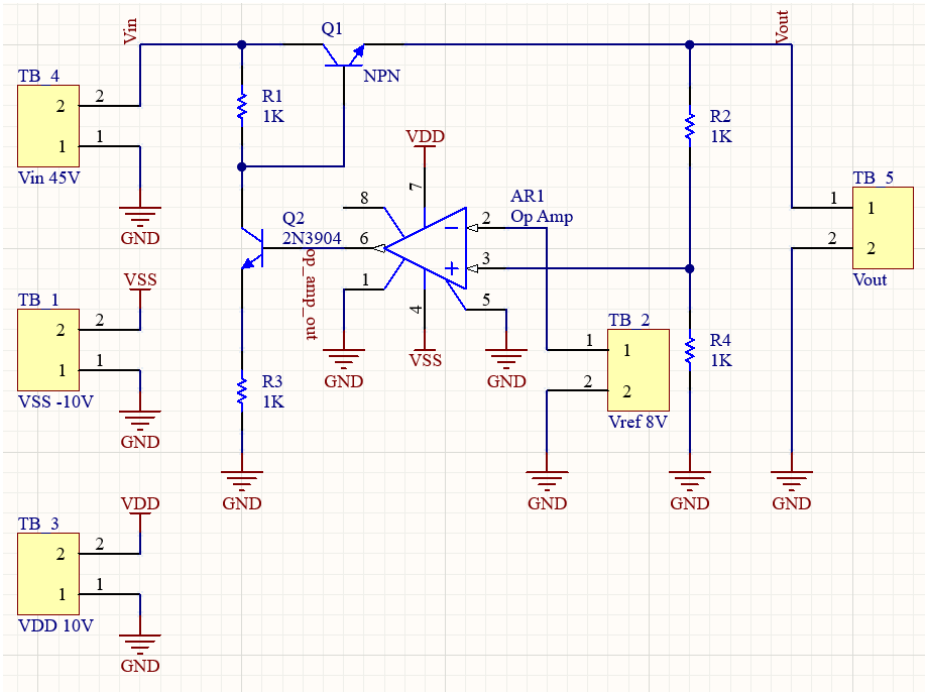


Figure 2: The schematic capture of the BJT-controlled Voltage Regulator circuit.

2.2. Create a custom symbol

As you notice, we will not be able to complete the schematic of the circuit since the symbol for the 2-pin terminal block used to capture the input/output voltages is missing. In a physical circuit board, the 'input', 'op-amp positive/negative voltages', and 'voltage reference' are also connected using terminal blocks (or headers/connectors). Default libraries in Altium do not include such type of components. Therefore, we need to create a custom symbol for this component (see Figure 3 for its physical representation). To do this, you can follow these steps:

Figure 3: 2-Pin Terminal Block

- Create a new schematic library: **Right-click** on the current project → **Add New to Project → Schematic Library**
- Create a new component 'Terminal_block_2p'. You can come up with your own words for Item ID, Designator, and Comment for the component.

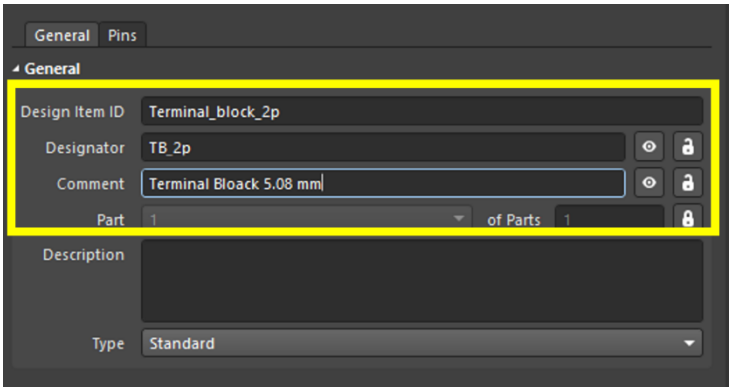


Figure 4: Defining a new component.

- You can use any shape/symbol to represent the terminal block. A rectangle can be added by selecting **Place → Rectangle**.
- Since the terminal block has 2 pins, we need to add 2 pins to the symbol accordingly. Go to **Place → Pins** or click on the Pins icon in the shortcut menu. Make sure you fill the Designator and Name field with suitable text.

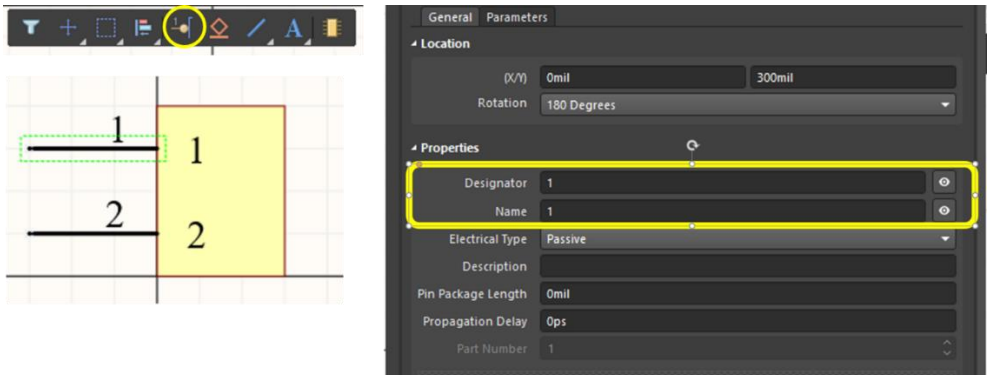


Figure 5: Adding pins for the component.

- Finally, make sure you save the schematic library in the same folder of your project.

Now you can complete the schematic by adding the new/custom schematic library at the output voltage.

2.3. PCB layout design

STEP 1: COMPONENTS FOOTPRINT ASSIGNMENT

Before transferring the circuit to the PCB layout design document, it is mandatory to assign each component with a correct footprint. The footprint should be checked against the component datasheet to make sure its dimension is correct.

- The component footprint can be changed by selecting the component, in the **Properties** tab, scrolling down to the footprint section, and clicking Add.

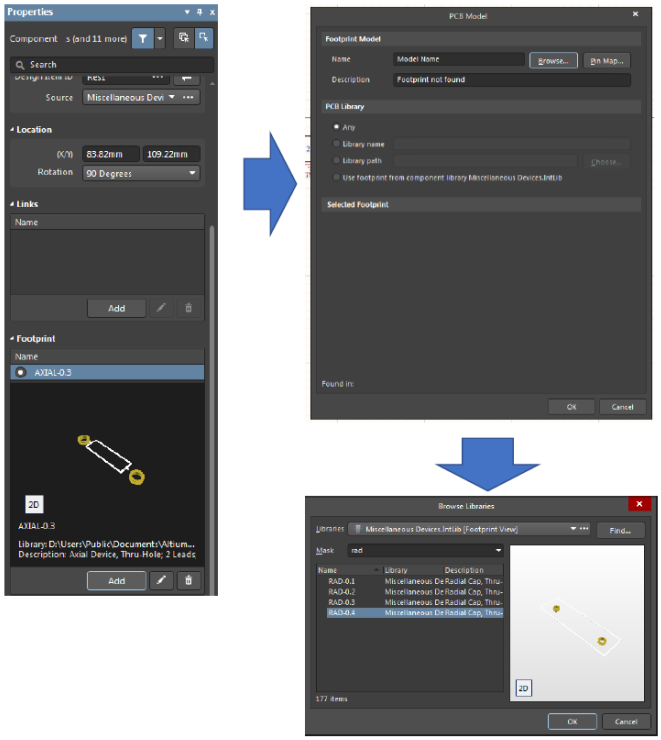


Figure 6: Assigning a component's footprint

- You will notice that there is no footprint available for voltage sources. We also need to create a custom footprint for the terminal block (steps shown in the below section)
- Change the footprint of the components to the following standard footprints:

Table 2: Selected footprints of the circuit components

Component	**Footprint**
R1, R2, R3, R4	AXIAL-0.3
Q1 Transistor	TO-220-AB
Q2 Transistor	TO-92A
OA1 TL081	DIP-8
Terminal_block_2p	Custom footprint

STEP 2: CUSTOM FOOTPRINT CREATION

It is often found that the available footprints that come with the Altium software package are very limited and sometimes they are incorrect/inappropriate for your PCB layout design. Therefore, it is essential to carefully check and correct the footprint before sending it out for fabrication. In the event that the component footprint is not available, you will have to create your own PCB footprint.

When creating a component footprint, its dimension should be checked against the datasheet provided by the manufacturer.

In this circuit, consider creating a custom footprint for the terminal block. Figure 7 shows the dimension of the block.

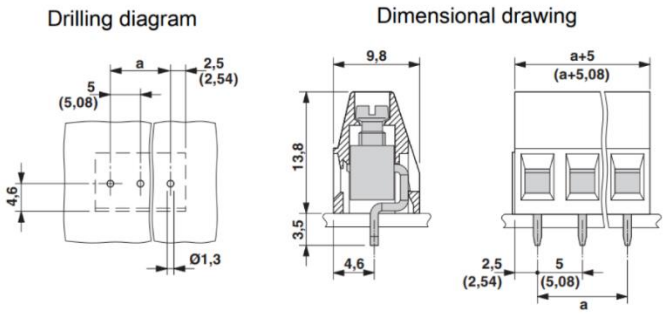


Figure 7: Dimension of a 2-pin terminal block (in mm)

From Fig. 7, it could be seen that the distance between two pins is ~ 5.08 mm and the hole size is 1.3 mm. It is also noted that the casing of the terminal block will take some space when you attach it to the board. As a result, when creating the footprint, you have to define extra space for this component, and it can be done by defining a silkscreen area (or preserved area). Follow these steps to create a custom footprint for the terminal block:

- Create a new PCB library: **File → Library → PCB Library.**
- Create a new Library component and rename it ***Terminal_Block_2P.***
- Place two pads in the locations (0, 0) and (200, 0). Notes 200 mils = 5.08 mm.

Figure 8: Two pads of the terminal block placement

- Select each pad and change the **Hole Size** to 55 mils (1.3 mm). Change the pad **Size and Shape** X/Y to 100 mill/100 mil.
- Draw an artwork (silkscreen) representing the occupied area of the component. Make sure the **Top overlay** layer is selected when drawing an artwork (see Figure 9)
- Save the PCB library to the current folder.
- Update the footprint for **TB_2p** to a footprint you just created. It can be done by selecting the component, from the **Property** panel, **Footprint→ Add → Footprints → Browse** and select the newly created footprint.
- Save the schematic capture file.

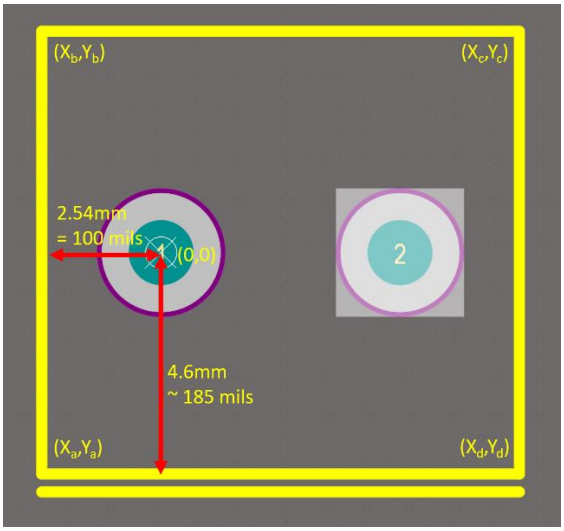


Figure 9: Defining occupied area of the 2pin terminal footprint

STEP 3: CREATE A NEW PCB

- Right-click to the project folder → **Add New to Project → PCB**.
- Make sure you save the PCB layout file in the same project folder before progressing further

STEP 4: DEFINE A CUSTOM BOARD SIZE

To define a custom size for your PCB board, you can use **Line** via the **Design** menu to draw the shape you want for the board. For example, let's set the board to a square shape with a dimension of 2000 × 2000 mils **(Note: 1 mil (thou) = 1/1000 inch)**.

- Select the **Top Overlay** as a working layer.

Figure 10: Select Top Overlay as the working layer

- Select **Place → Line** and from the origin, draw a square with a side length of 2000 mils. Note that the origin is the point where X and Y is 0. The origin can be set/redefine by selecting **Edit → Origin → Set**. If it is too difficult to draw a line exactly at 2000 mils,

you might need to increase the snap grid size by selecting **Edit → Grids → Set Global Snap Grid** or pressing **Ctrl+Shift+G**.

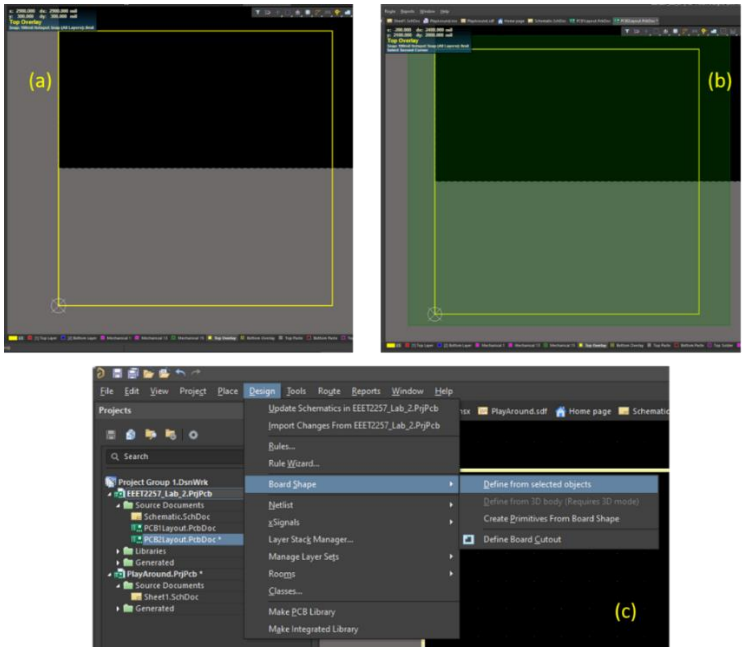


Figure 11: Set board dimensions.

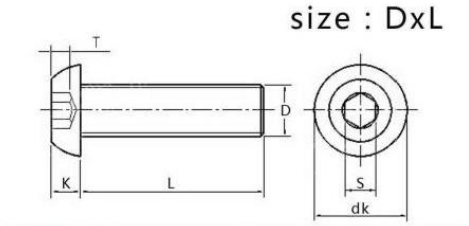
- Select the defined square object then select **Design → Board Shape → Define from selected object.**

STEP 5: PLACEMENT OF BOARD MOUNTING HOLES AND KEEP-OUT LAYER

In the PCB design process, it is important to consider how the PCB will be mounted into a protective case. If the PCB is being attached using screws, appropriate holes need to be planned and placed at the correct locations.

- In this lab, we will need to place 4 holes in the corners of the boards so it can be screwed to the case using M3 Panhead screw as shown in Figure 3. The hole size is 3 mm (118.11 mils) and the head diameter is 5.6 mm (220.472 mils). We will use slightly larger hole size (125 mils).

- To add screw holes to the board, select **Place → Pad** then place them to the workspace. The dimensions of a pad can be adjusted via the **Properties** panel as shown in the Figure 12.



D thread diameter	thread pitch	L	dk	K	S	T
M2 (2mm)	0.4mm	3-16mm	3.4mm	1.3mm	1.3mm	0.8mm
M3 (3mm)	0.5mm	4-50mm	5.6mm	1.5mm	2.0mm	1mm

Figure 12: Typical M3 hole size

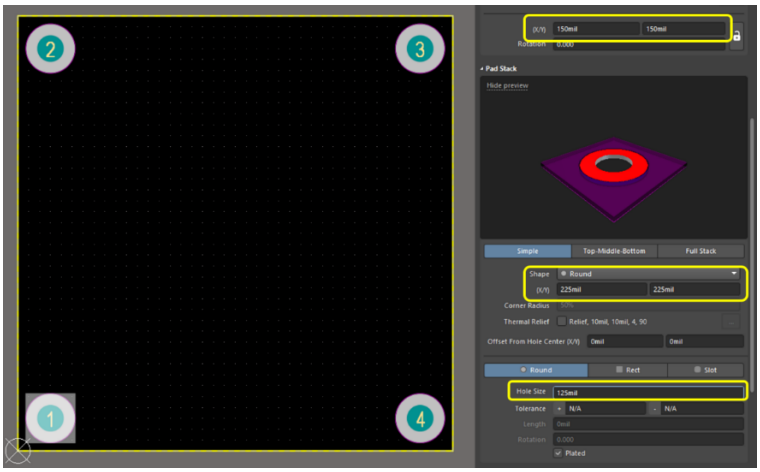


Figure 13: Pads placement

- In order to avoid routing in the neighborhood of the screw heads, a keep-out layer needs to be defined for these holes. To do this, select the **Keep-Out Layer** as the working layer. Then select **Place → Keepout → Track**. Draw a keep-out track as shown in Figure 14.

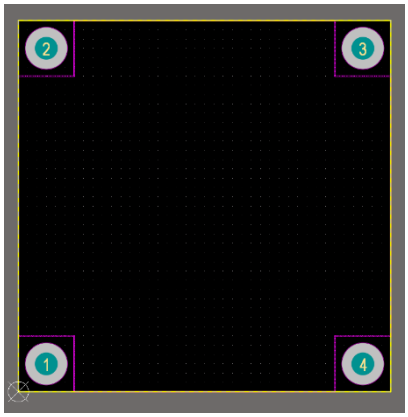


Figure 14: Defining keep-out layer

STEP 6: TRANSFER SCHEMATIC TO PCB

At this stage, we can transfer the schematic capture to the actual layout by:

- Select **Design → Import Changes From** …

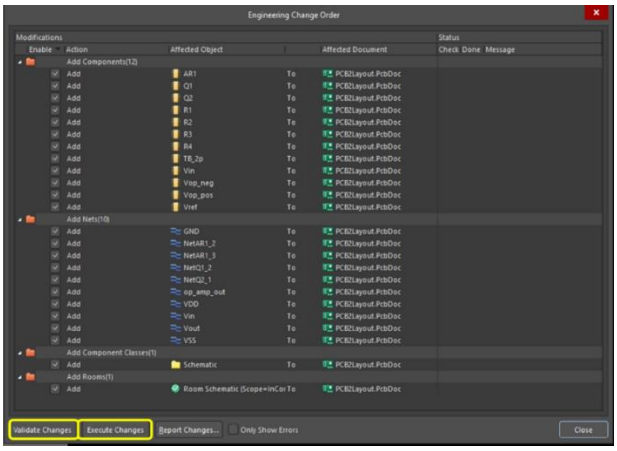


Figure 15: Engineering Change Order

- The PCB footprints of the components are placed to the right of the PCB outline with a rat's nest connection as shown below:

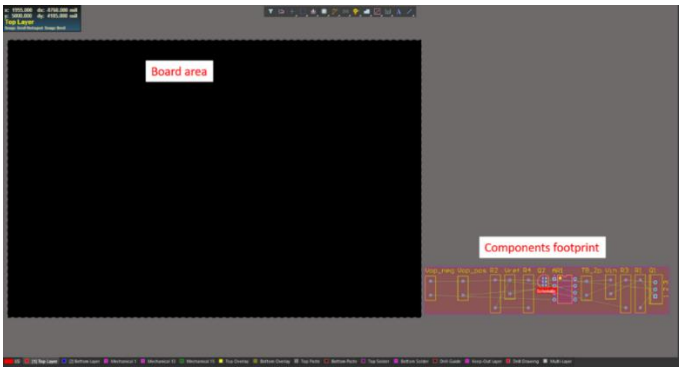


Figure 16: Components placed outside PCB outline.

STEP 7: UPDATE PCB LAYOUT

It is often that during the PCB layout design, additional components might need to be included in the schematic. An example is the placement of decoupling/bypass capacitors.

Note: Decoupling/bypass capacitor is typically placed at the power supply terminals to filter/minimize impacts of noise in the supply rails.

- Place two capacitors C_1 and C_2 at the V_{SS}, V_{DD} (see Figure 17).
- Update the footprint of C_1 and C_2 to RAD-0.1.
- Update the PCB layout document **Design → Update PCB Document → Execute Changes.**

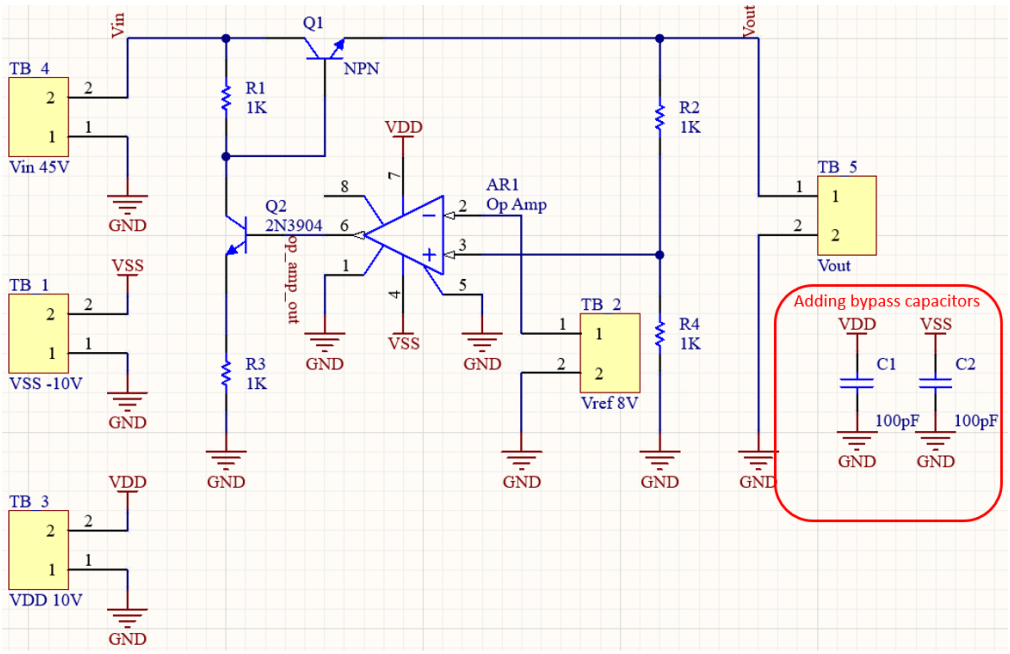


Figure 17: Updated schematic with bypass capacitors

STEP 8: PLACING COMPONENTS ON THE PCB

Component placement is an important process in PCB design. Efficient component placement will significantly simplify the layout job and provide good electrical performance for your circuit. There is no absolute method for component placement. However, there are a few basics rules:

- Divide and place the circuit into functional blocks.
- Identify critical tracks and route them first (i.e. power track, signal track).
- Place and route the building blocks separately.
- Route the remaining signal and power connection between blocks.
- Adjust/tidy up the layout.
- Run Design Rule Check (DRC).

2.8.1. Circuit Partition

Consider the circuit of the BJT-controlled voltage regulator. It can be basically divided into 2 blocks; power- and control-block (see Figure 18). The **power block** will mainly carry high current signals, while the **control block** should be dealing with small current signals.

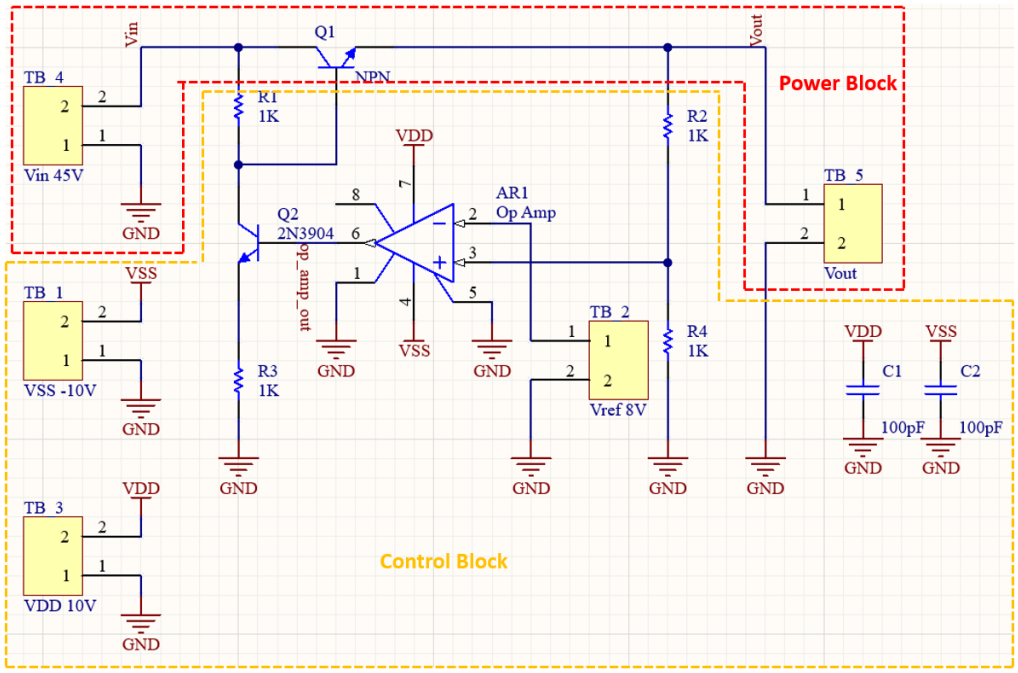


Figure 18: Circuit partition

2.8.2. Placement of input and output connectors

Input and output connectors should be placed on the edge of the board. It is usual to place the input connector on one side of the board and the output on the other side.

2.8.3. Placement of high current components

The transistor Q1 will carry most of the current. This must be placed between the input and output pins such that the track length can be minimized as much as possible.

2.8.4. Placement of similar components

One of the best practices when placing similar components is having ICs in the same direction, resistors in neat columns, polarized capacitors in the same orientation. However, electrical parameters should take precedence over nicely lined up components. i.e. make sure your layout circuit works first before polishing it up.

STEP 9: DEFINING AND MANAGING DESIGN RULES

There are many rules and practices to design a good PCB. During the design, it is important to keep the rules given by PCB manufacturers. Some practices are given below:

- ***Routing width:*** minimum routing width, minimum distance between routes, etc. In *Altium*, there is a design rule tool to check these limits.
- ***Use wider routes for power supply and ground:*** routing width affects the resistance of the track. Therefore tracks carrying a significant amount of current should be wider to minimize the voltage drop through wires.

- ***Avoid 90-degree routing connection:*** rout wires with large angles (more than 135 degrees) to avoid manufacturing problems.
- ***Board outline:*** do not place wires or holes very near to the board outline since they can be damaged during the cutting process.
- ***Drill holes:*** always use a bigger hole than the diameter of the pin. Datasheets usually contain the recommended drill hole size.

Note: To set design rules in Altium, select **Design → Rules.** Consider setting these rules for this lab exercise

Table 3: PCB Design Rules

Item	Rule	Remark
Number of Layers	2	Top-layer as a ground plane
Maximum PCB Size (Dimension)	50.8 mm × 50.8 mm (2000 mil × 2000 mil)	
Min Signal Track Width	0.5 mm/20 mil	
Min Power Track Width	1 mm/40 mil	You can define a new rule for power track
Min Spacing	0.5 mm/20 mil	Track to track, track to pad, pad to pad, pad to copper plane
Hole Sizes	0.2-6.3 mm (10-240 mil)	Min hole size is 0.2 mm, max is 6.3 mm
Power Plane Clearance	0.76 mm/30 mil	
Hole to Hole Clearance	0.254 mm/10 mil	
Silk to Silk Clearance	0.254 mm/5 mil	
Silk to Solder Mask	0.254 mm/5 mil	

Note: ***An example how to minimum clearance between all tracks, pads, and components***

- To set clearance between the tracks, select **Design → Rules.**
- Double click on **Electrical** category to expand it.
- Double click on **Clearance** type to display clearance rules.
- Finally click on the rule named **Clearance** – see Figure 19.
- Set minimum clearance to 20 mil.

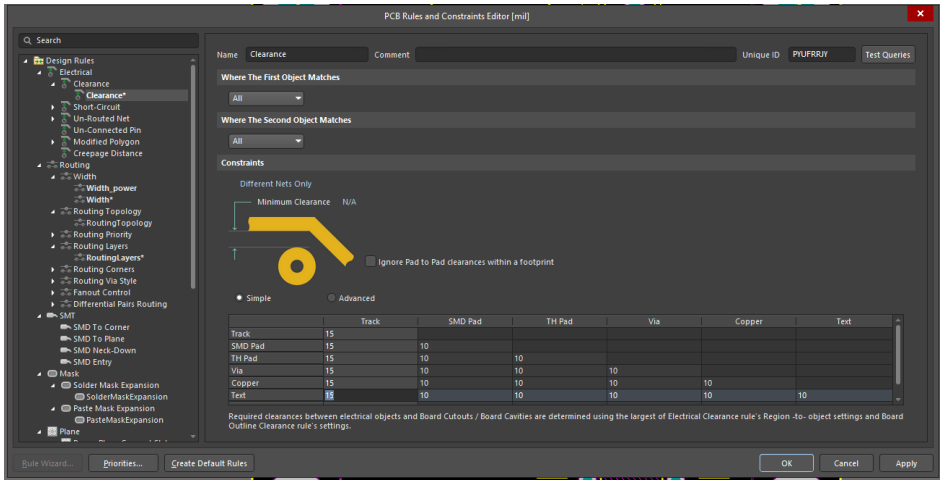


Figure 19: Setting the Minimum Clearance value

STEP 10: ROUTING THE BOARD

- Confirm that the grid is appropriate for routing. To change the grid, press **Ctrl+G** to open the Cartesian Grid Editor, type the value into the field and click OK to close the dialog.
- Check which layers are currently visible by looking at the Layer Tabs at the bottom of the workspace. Click on the layer you want to be your active layer for routing.
- To perform routing, select **Place → Track** or press **Ctrl+W**. Click to a pad and follow the rat's nest connection to place a trace between the pins of a component. Make sure you avoid 90^{o} angle connection.
- Since we will set up the GND plane later, you should leave the GND terminal disconnected.
- Continue to route all the connections on the board as shown below.

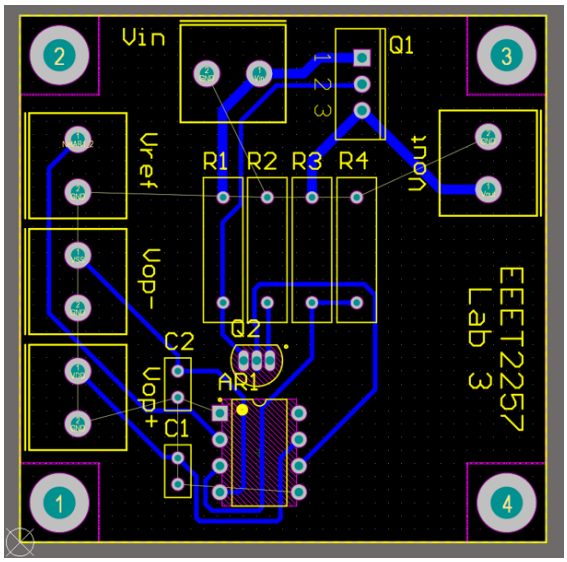


Figure 20: A complete PCB layout

- It is common to perform manual routing for critical tracks when designing the PCB layout. Less critical tracks routing can be done by the auto-routing function. Auto-routing can be done by selecting **Route → Auto Route → All**. The auto-router will route on both the top and bottom layers, red tracks on the top layer, blue on the bottom layer. The layers that are used by the auto-router are specified in the Routing Layers design rule, which defaults to top and bottom layers.

STEP 11: POLYGON POUR

A ground plane (GND) can be created using the polygon pour function.

- Select **Top Layer**
- Select **Place → Polygon Pour**
- Place the polygon along the boundary of **the Keep-Out Layer**
- Select the polygon and assign **Net to *GND***, make sure **Layer set to Top Layer** and **Remove Dead Copper** is checked.
- After implementing the polygon pour, the layout should look like in Figure 22. In case you need to modify the layout, to update the polygon pour, it needs to be repoured. It can be done by **selecting the polygon → right-click → Polygon Actions → Repour All**.

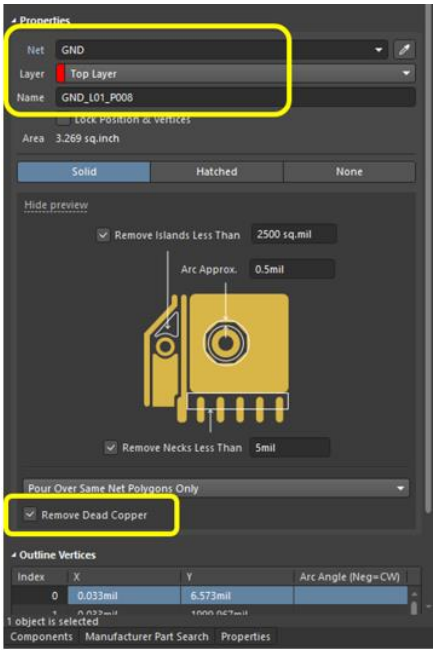


Figure 21: Polygon Pour settings

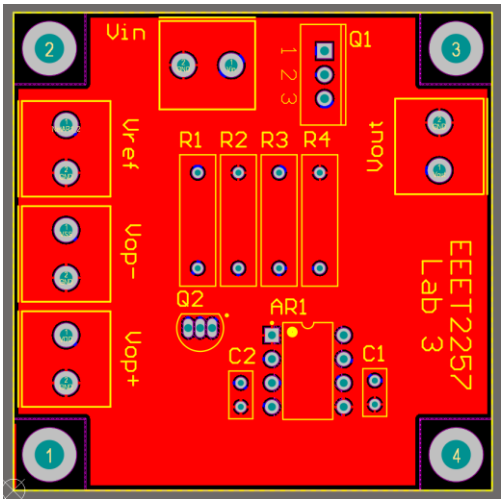


Figure 22:Polygon Pours for a ground plane.

STEP 12: PCB DESIGN RULE VERIFICATION (DRC)

The DRC functionality performs validation of the PCB artwork with the predefined design rules. Violation of the design rules will be informed for correcting. The design rules should be set based on recommendations from your PCB manufacturers. The design should pass DRC before sending out for fabrication.

Design Rule Check can be performed via **Tools → Design Rule Check → Run Design Rule Check.** The Design Rule Verification Report is created and appeared in a new tab in the workspace.

Verify that your design does not have critical errors:

- Clearance constraint – may be caused due to overlapping component footprints which may result in insufficient space to place components during soldering.
- Short-circuit constraint – components being short-circuited due to placement or large track widths
- Un-routed nets – unconnected components during the routing process.

Note: Refer to Altium documentation online if further information is required on other types of errors that may be shown in the design rule check.

If there is any violation in the report, make sure you correct them all and re-run DRC.

STEP 13: VIEWING THE PCB IN 3D

The 3D view of the PCB layout can be checked by selecting **View → 3D Layout Mode** or pressing **"3"**. The 3D layout might be useful since it can give you an idea of the fabricated PCB.

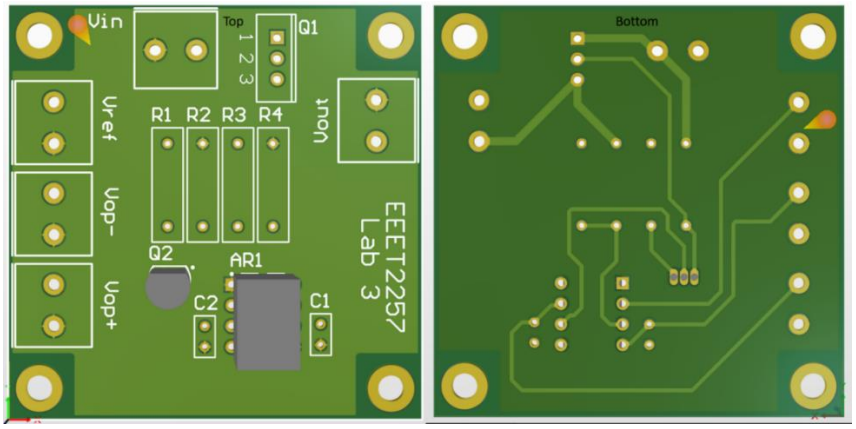


Figure 23: 3D-view of the BJT voltage regulator circuit

3. PCB layout of a low-pass filter

Design the layout for a low-pass filter circuit. Use the components listed in the table given below.

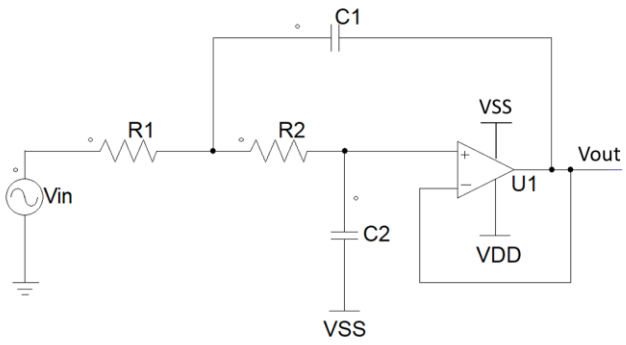


Figure 24: Schematic of the filter circuit

Schematic label	Design Item ID	Description	Library (*.IntLib)	Value	Footprint
R1	Res1	Resistor	Miscellaneous Devices	100 kΩ	RAD-0.4
R2	Res1	Resistor	Miscellaneous Devices	100 kΩ	RAD-0.4
C1	Cap	Capacitor	Miscellaneous Devices	112 pF	RAD-0.3
C2	Cap	Capacitor	Miscellaneous Devices	56 pF	RAD-0.3
U1	LF411CN	Low Offset, Low Drift JFET Input Operational Amplifier, 8-pin MDIP	NSC Amplifier		DIP-8
Vin	2-pin connector	2-pin block terminal	Custom	12 V, 1 kHz	Custom footprint
Vout	2-pin connector	2-pin block terminal	Custom		Custom footprint
VSS	2-pin connector	2-pin block terminal	Custom	-10 V	Custom footprint
VDD	2-pin connector	Custom	Custom	10 V	Custom footprint

Hints:

- The op-amp LF411 might not be found in the installed libraries. You will need to download the library **"NSC Operational Amplifier.IntLib"** for this component. The link is available at: https://techdocs.altium.com/display/ALEG/Legacy+Libraries . Download the library from ***National Semiconductor***. The **"NSC Operational Amplifier.IntLib"** should be inside the package.
- Refer to lab 1 notes on how to add a library to your working project.
- Recommended board size: 1200 mil × 1200 mil. However, you are encouraged to make it as compact as you can.
- The board should have 4 holes at the corners so that it can be attached to a protective case. Use M3 Panhead screws for these holes and make sure you define the Keep-Out layer for them.
- Use a ground plane for your design.
- The design must follow the design rules set in Table 3. Make sure your design passes DRC.

4. Assessment

- **This is an individual task.**
- You are required to submit the schematic files (**.SchDoc**) and layout files (**.PcbDoc**) of the two circuits. Please zip them to a folder and upload it on Canvas. Name your folder as **s1234567_name_lab2.zip** (replace 1234567 and name with your student ID and your first name).
- The due date is **FRIDAY Week 6 before 11:59 pm.**
- Marking criteria for the PCB design:
    - **Schematic capture**: Is the connection correct?
    - **Component placement**: How compact is the PCB? Are components placed in a logical arrangement?
    - **Component footprint**: Is the footprint correct?
    - **PCB design**: How neat is the component layout? Appropriate track widths for different signal types?
    - **DRC**: Has the design rule been defined correctly? Does the design pass DRC?

Hiep N. Tran 11/07/2022