Special Purpose Registers for Init and Config

1

```
//Power up SPI

LPC_SC->PCONP
```

2

```
//set PCLK
LPC_SC->PCLKSEL0
```

3

```
// Enable Slave SPI nCS

LPC_GPIO0->FIODIR
LPC_GPIO0->FIOSET
```

4

```
// Perform init

LPC_PINCON-
>PINSEL0
```

5

```
//init CR0 and CR1 registers

LPC_SSP1->CR0
LPC_SSP1->CR1
```

6

```
// set ssp clock rate

LPC_SSP1->CPSR = 8;
```

SSP Init and Config

PCONP Power Control for Peripherals Register

1

```
//Power up SPI

LPC_SC->PCONP
```

Table 14. System control registers, pp 31; Table 46, PCONP contains control bits to turn on/off individual peripheral controller for power saving purpose, pp. 64

2

```
//set PCLK
LPC_SC->PCLKSEL0
```

Table 40. PCKSEL0 Peripheral Clock Selection register 0, pp, Table 42, pp. 58 bit selection table

Bit	Symbol
17:16	PCLK_SPI
19:18	-
21:20	PCLK_SSP1
23:22	PCLK_DAC

Table 46, PCONP

Bit	Symbol
6	PCPWM1
7	PCI2C0
8	PCSPI
9	PCRTC
10	PCSSP1

3

```
// Enable Slave SPI nCS

LPC_GPIO0->FIODIR
LPC_GPIO0->FIOSET
```

4

```
// Perform init

LPC_PINCON-
>PINSEL0
```

8.5.1 Pin Function Select register 0, PINSEL0 register selects the multiplexed functions of the lower half of Port 0. pp 117

Bit = 10

11:10	P0.5[1]	TD2
13:12	P0.6	SSEL1
15:14	P0.7	SCK1

C-Code for SSP Init and Config

```
void initSSP1(void){
    //power up spi1
    LPC_SC->PCONP |= (1<<10);
    //01 PCLK_peripheral = CCLK.. 01, since it's CCLK/1
    LPC_SC->PCLKSEL0 &= ~(3<<20);
    LPC_SC->PCLKSEL0 |= (1<<20);

    //P0.6 is used as a GPIO output and acts as a Slave select
    LPC_GPIO0->FIODIR |= (1<<6);
    LPC_GPIO0->FIOSET = (1<<6);
    //P0.7:9 init
    LPC_PINCON->PINSEL0 &= ~((3<<18)|(3<<16)|(3<<14));
    LPC_PINCON->PINSEL0 |= ((2<<18)|(2<<16)|(2<<14));
    //data size set to 8 bits
    LPC_SSP1->CR0 = 0x07;
    //or AT45 flash SI pin latched on the rising edge of SCK, while output data
    //on the SO pin is always clocked out on the falling edge of SCK.
    //MS=0 (Master), SSE =1
    LPC_SSP1->CR1 = 0x2;
    LPC_SSP1->CPSR = 8; //SCK Frequency for Continuous Read(Low Freq) is 33Mhx max. here we are setting it
below it.
}
```

1

2

3

4

5

6

CR0 for SSP Init and Config

Table 371: SSPn Control Register 0 (SSP0CR0 - address 0x4008 8000, SSP1CR0 - 0x4003 0000) bit description, pp 431

6	CPOL		
	Clock Out Polarity		
7	CPHA		
	Clock Out Phase		
15:8	SCR		
	Serial Clock Rate		
31:8	-		

3:0	DSS		
		0011	4-bit transfer
		0100	5-bit transfer
		0101	6-bit transfer
		0110	7-bit transfer
		0111	8-bit transfer
		1000	9-bit transfer
		1001	10-bit transfer
		1010	11-bit transfer
		1011	12-bit transfer
		1100	13-bit transfer
		1101	14-bit transfer
		1110	15-bit transfer
		1111	16-bit transfer
5:4	FRF		Frame Format.
		00	SPI
		01	TI