CMPE 125 Lab 4 Assignments

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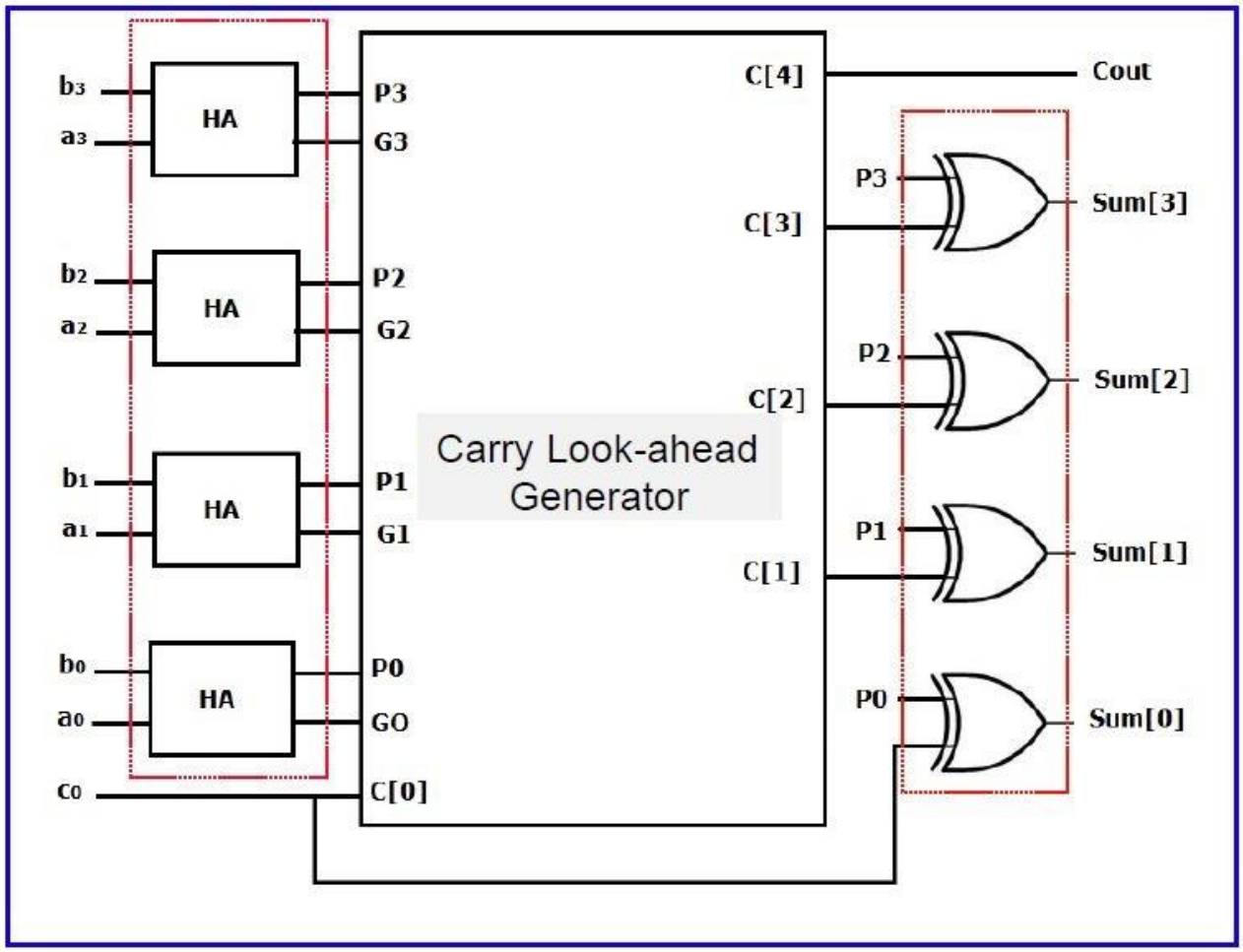
Hierarchical Design of a CLA Adder

Purpose:

1) To be familiar with the structured and hierarchical design methodology
2) To be familiar with the design/verification/validation flow and EDA tools

Tasks:

1. Design and verify a 4-bit Carry Look-Ahead unsigned adder
   a) Design the adder using half adders, a custom-designed carry look-ahead generator, as well as glue logics, as the building blocks. Write structural Verilog design code that reflect the hierarchical design methodology discussed in class.
   b) Write a **self-checking Verilog testbench** to functionally verify the designed CLA adder.
2. Design and verify a 4-bit "inferred" unsigned adder
   a) Design another version of the 4-bit binary adder via more abstract, functional Verilog description. Specifically, the adder is directly inferred by the Verilog operator '+', instead of using structural-level descriptions.
   b) Functionally verify this adder using the same Verilog testbench developed in Task 1.
3. Validate the 4-bit CLA adder using the Nexys4 DDR FPGA board. This time you do need to include a *xdc* file to run the implementation tool, with the following I/O constraints:
   - use the eight DIP-switches for inputs *A* and *B*
   - use one of the push buttons for the *Carry-In* signal and display it on one of the on-board 7-segment LEDs
   - display *A* on the left half and *B* on the right half of the on-board LEDs, respectively
   - display *SUM* (the sum) on two of the on-board 7-segment LEDs



Contents of Report:

1) Cover page
2) A list of successfully accomplished tasks
3) System schematics (including functional building blocks, their interconnections, and signals) for the CLA adder
4) Commented Verilog design code for both the CLA adder and the "inferred" adder
5) Test plan (i.e., how to verify the designed adders) and the corresponding Verilog testbench code (with necessary comments)
6) Captured verification results (waveforms and/or simulation log files)
7) Validation (hardware prototyping) setup and observed results
8) Detailed descriptions of the task(s) you cannot, or did not accomplish, including reason(s) and/or your analysis.

Report checklist

Follow the "CMPE 125 Lab Report Guidelines" document on Canvas.

Your report should include these sections:

- Cover page *(with name, SID, and the Lab Record filled out with your name, TA's name, and lab demo score)*

- Introduction *(1 paragraph)*

- Design methodology *(1 paragraph)*
    - Block diagrams:
    - Task 1:
        - Adder (overall module)
        - Half-adder
        - Carry look-ahead generator
        - XOR as block diagram, NOT gate-level diagram.
    - Task 2:
        - Inferred adder

  NOTE: Block diagrams must follow the lab report guidelines.

- Test plan for simulation *(1 paragraph)*
    - **No waveforms** as we are using self-checking test benches.
    - Console output from simulator (as a picture).

- Test plan for FPGA board *(1 paragraph)*
    - Include photograph of FPGA board showing results with a caption that clearly labels the state of the switches and LEDs.

- Conclusion *(1 paragraph)*
    - In addition if you could not complete any part of the lab explain clearly what went wrong and how you could have remedied the problem.

- Appendix
    - Any tables or other diagrams go here that don't fit in the other sections.

- Source code
    - Use a fixed-width font such as Courier New for the source code.
    - Clearly label the file name of each source file you include.
    - Include **all** source code you used in the project, including constraints.