CmpE 110

Digital Electronics

Class Notes

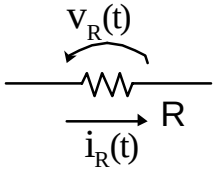
By
Dr. Ahmet Bindal

Revised August 2008

CHAPTER I. RLC NETWORKS

A. BASIC CONCEPTS ON PASSIVE ELEMENTS

Resistance:

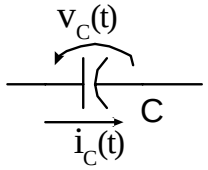


$v_R(t) = R\ i_R(t)$

£ $[v_R(t)] = V_R(s) = R$ £ $[i_R(t)] = R\ I_R(s)$

$$Z_R(s) = \frac{V_R(s)}{I_R(s)}$$

Capacitance:



$$i_C(t) = C\ \frac{dvc(t)}{dt}$$

£ $[i_C(t)] = I_C(s) = C$ £ $[\frac{dvc(t)}{dt}]$

Laplace transform: $F(s) = \int_0^\infty f(t)e^{-st}dt$

Thus:

£ $[\frac{dvc(t)}{dt}] = \int_0^\infty \frac{dvc(t)}{dt}e^{-st}dt = \int_0^\infty e^{-st}dvc(t)$

But,

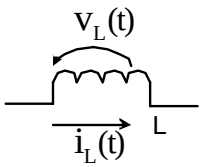
$$\int_0^\infty e^{-st}dvc(t) = e^{-st}vc(t)\Big|_0^\infty - \int_0^\infty vc(t)(-s)e^{-st}dt = [0 - vc(0)] + s\int_0^\infty vc(t)e^{-st}dt = sV_C(s) - v_C(0)$$

Then:

£ $[ic(t)] = C[sV_c(s) - v_c(0)] = sCV_c(s)$

Thus, $Z_C(s) = \frac{1}{sC}$

Inductor:



$$v_L(t) = \frac{di_L(t)}{dt}$$

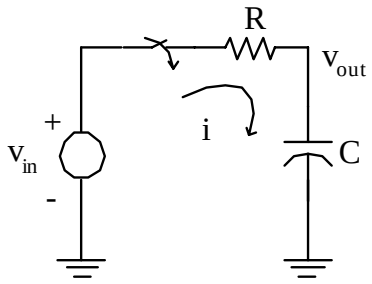
$$£[\, v_L(t)] = V_L(s) = L\, £[\frac{di_L(t)}{dt}\,] = L\,[sI_L(s) - i_L(0)] = sL\, I_L(s)$$

$$Z_L(s) = sL$$

B. TIME-DOMAIN ANALYSIS OF PASSIVE NETWORKS

(i) RC Circuits

Integrator:



$$V_{in} = Ri + v_{out}$$

$$i = C\,\frac{dvout}{dt}$$

$$\frac{dVin}{dt} = R\frac{di}{dt} + \frac{i}{C}$$

$$\frac{di}{dt} + \frac{i}{RC} = \frac{1}{R}\frac{dVin}{dt}$$

General Solution:

$$\frac{di}{dt} + \frac{1}{RC}i = 0$$

Characteristic equation:

$$s + \frac{1}{RC} = 0 \Rightarrow s = -\frac{1}{RC}$$

$$i_g = Ae^{st} = Ae^{-\frac{t}{RC}}$$

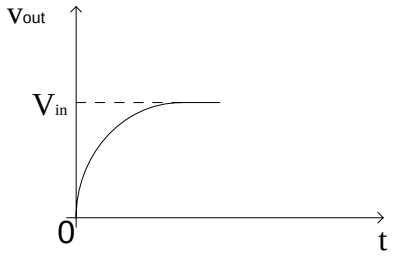
$$i_p = 0$$

$$i(t) = i_g(t) + i_p(t) = Ae^{-\frac{t}{RC}}$$

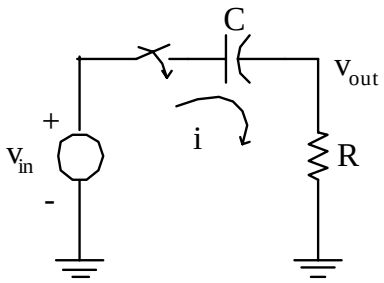
$$v_{out} = \frac{1}{C}\int_0^t i dt = \frac{1}{C}\left(\frac{V_{in}}{R}\right)\int_0^t e^{-\frac{t}{RC}} dt$$

$$= \frac{V_{in}}{RC} e^{-\frac{t}{RC}} \left(-RC\right)\Big|_0^t = -V_{in}\left[e^{-\frac{t}{RC}} - 1\right]$$

$$v_{out} = V_{in}\left[1 - e^{-\frac{t}{RC}}\right]$$



Differentiator



$$V_{in} = v_c + v_{out}$$

$$0 = \frac{dv_c}{dt} + R\frac{di}{dt}$$

$$0 = \frac{i}{C} + R\frac{di}{dt}$$

$$\frac{di}{dt} + \frac{1}{RC}i = 0$$

But, the characteristic equation: $s + \frac{1}{RC} = 0$

$$i(t) = i_g(t) + i_p(t) = Ae^{st} + 0$$

$$i(t) = Ae^{st} = Ae^{-\frac{t}{RC}}$$

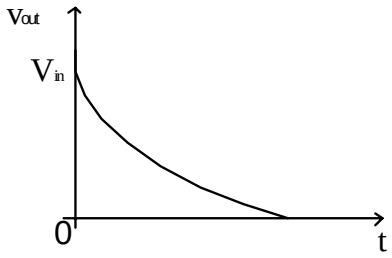
$$v_{out} = Ri(t) = ARe^{-\frac{t}{RC}}$$

But, $v_c(0) = 0 \Rightarrow v_{out}(0) = V_{in}$

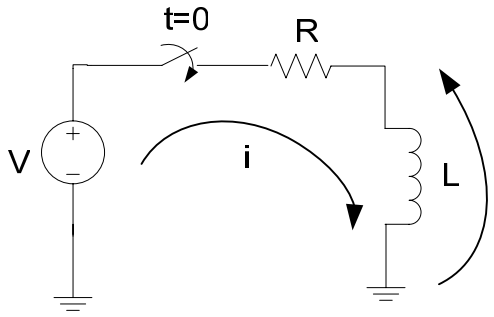
$$V_{in} = AR$$

Thus, $A = \frac{V_{in}}{R}$

Thus, $v_{out} = V_{in}e^{-\frac{t}{RC}}$



(ii) RL Circuits



$V = v_R + v_{out}$

$v_R = Ri$ Ohms law

$v_L(t) = L\frac{di}{dt}$ Lorentz Law

$V = Ri + L\frac{di}{dt}$

$\frac{di}{dt} + \frac{R}{L}i = \frac{V}{L}$

To solve the general solution (the homogeneous part) use Laplace Transform:

$\mathcal{L}\left[\frac{di}{dt} + \frac{R}{L}i\right] = 0$

$I(s)S + \frac{R}{L}I(s) = 0$

$I(s)\left[S + \frac{R}{L}\right] = 0$

$I(s) \neq 0$

$\therefore \left[S + \frac{R}{L}\right] = 0$

$S = \frac{-R}{L}$

$i(t) = Ae^{\frac{-R}{L}t}$

To solve the particular solution:

Look at the degree of the particular portion.

$\frac{V}{L}$ is a constant, so substitute $i_p = K$ into

$$\frac{di_p}{dt} + \frac{R}{L} i_p = \frac{V}{L} \qquad \rightarrow \qquad 0 + \frac{R}{L} K = \frac{V}{L}$$

$$K = \frac{V}{R}$$

Now put the general and particular solutions together:

$$i(t) = Ae^{\frac{-R}{L}t} + \frac{V}{R}$$

Now solve for A by using the initial condition $i(0) = 0$:

$$i(0) = A + \frac{V}{R} = 0 \qquad \rightarrow \qquad A = \frac{-V}{R}$$

$$\therefore i(t) = \frac{V}{R} - \frac{V}{R} e^{\frac{-R}{L}t} = \frac{V}{R}\left(1 - e^{\frac{-R}{L}t}\right)$$

Use Lorentz Law to solve for v_{out}

$$v_{out} = L\frac{di}{dt}$$

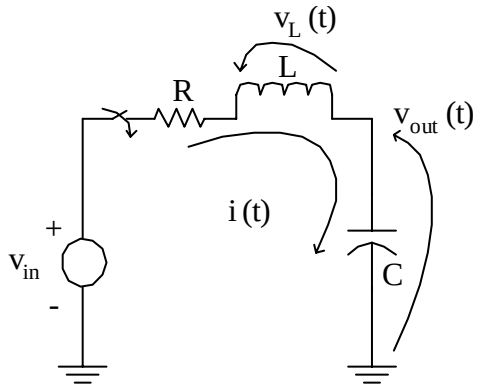
$$v_{out} = L\frac{d\left(\frac{V}{R}\left(1 - e^{\frac{-R}{L}t}\right)\right)}{dt} = L\frac{V}{R}\left(0 - e^{\frac{-R}{L}t} \cdot \left(\frac{-R}{L}\right)\right) = Ve^{\frac{-R}{L}t}$$

RESULTS:

$$i(t) = \frac{V}{R}\left(1 - e^{\frac{-R}{L}t}\right)$$

$$v_{out} = Ve^{\frac{-R}{L}t}$$

(iii) RLC Circuits



$$V_{in} = Ri(t) + v_L(t) + v_{out}(t)$$

$$v_L(t) = L\frac{di(t)}{dt} \text{ and } i(t) = C\frac{dv_{out}(t)}{dt}$$

$$V_{in} = Ri(t) + L\frac{di}{dt} + v_{out}(t)$$

Differentiating both sides yields:

$$0 = R\frac{di}{dt} + L\frac{d^2i}{dt^2} + \frac{dv_{out}}{dt} = R\frac{di}{dt} + L\frac{d^2i}{dt^2} + \frac{i}{C}$$

Characteristic equation: $s^2 + \frac{R}{L}s + \frac{1}{LC} = 0$

$$s_{1,2} = \frac{-\frac{R}{L} \pm \sqrt{\frac{R^2}{L^2} - \frac{4}{LC}}}{2} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

Let $\alpha = \frac{R}{2L}$ and $\omega_0 = \frac{1}{\sqrt{LC}}$

$$s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2}$$

$i(t) = A e^{s_1 t} + B e^{s_2 t}$ $\leftarrow$ find A & B

At $t = 0^-$, $i_L(0^-) = i(0^-) = 0$

Since the current through the inductor cannot change suddenly, $i_L(0^+) = i(0^+) = 0$

Thus, $i(0) = 0 = A + B$

$A = -B$

We need another initial condition to find A and B explicitly.

Evaluate $\frac{di(t)}{dt}$:

$$\frac{di(t)}{dt} = A\, s_1 e^{s1t} + A\, s_2 e^{s2t} = A\,(s_1 e^{s1t} - s_2 e^{s2t})$$

However, at $t = 0^-$ $v_{out}(0^-) = 0$ and $v_R(0^-) = i(0^-)\,R = 0$

When the switch is closed the voltage across the capacitor and the current through the inductor cannot change instantaneously

Thus: $v_{out}(0^+) = 0$ and $v_R(0^+) = i(0^+)\,R = 0$

$$V_{in} = v_L(0^+) = L\left.\frac{di}{dt}\right|_{t=0^+}$$

Then:

$$\frac{V_{in}}{L} = A(s_1 - s_2)$$

$$A = \frac{V_{in}}{L(s_1 - s_2)} \qquad B = -\frac{V_{in}}{L(s_1 - s_2)}$$

$$i(t) = \frac{V_{in}}{L(s_1 - s_2)}\left(e^{s1t} - e^{s2t}\right)$$

$$v_{out} = V_{in} - i\,R - L\frac{di}{dt}$$

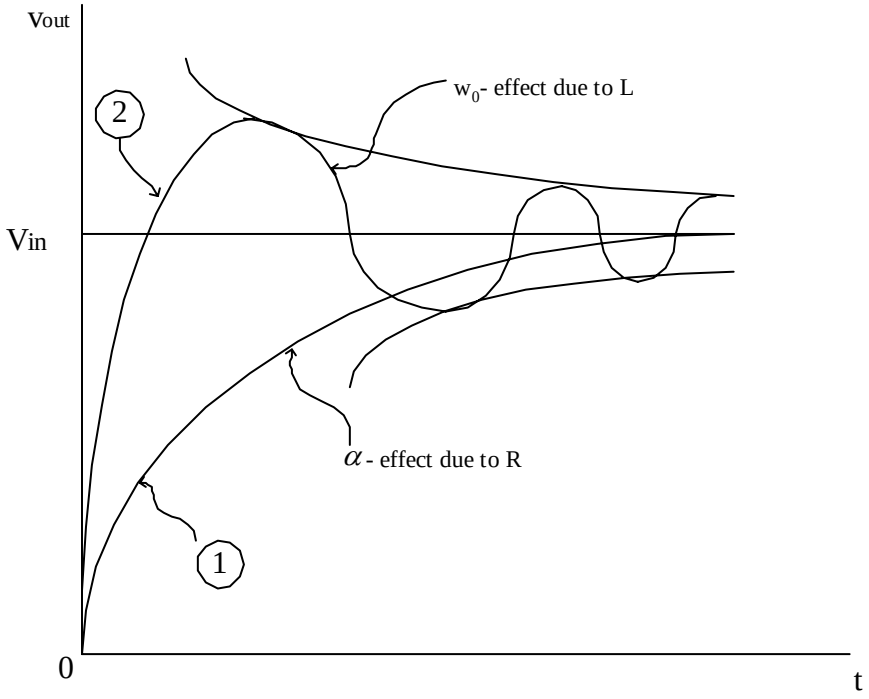
where, $$\frac{di}{dt} = \frac{V_{in}}{L(s_1 - s_2)}\,(s_1 e^{s1t} - s_2 e^{s2t})$$

$$v_{out} = V_{in} - \frac{V_{in}\,R}{L(s_1 - s_2)}\left(e^{s1t} - e^{s2t}\right) - \frac{V_{in}}{(s_1 - s_2)}(s_1 e^{s1t} - s_2 e^{s2t})$$

$$v_{out} = V_{in}\left[1 - \frac{e^{s1t}}{(s_1 - s_2)}\left(\frac{R}{L} + s_1\right) + \frac{e^{s2t}}{(s_1 - s_2)}\left(\frac{R}{L} + s_2\right)\right]$$

where, $s_1 = -\alpha - \sqrt{\alpha^2 - \omega_0^{\,2}}$ and $s_2 = -\alpha + \sqrt{\alpha^2 - \omega_0^{\,2}}$

$$s_1 - s_2 = -2\sqrt{\alpha^2 - \omega_0^{\,2}}$$



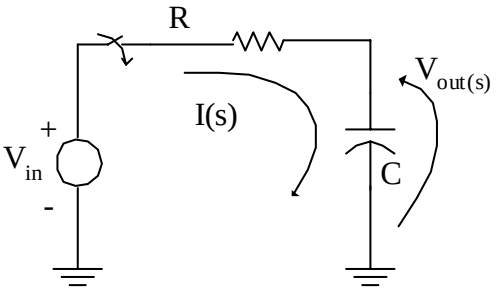
Case 1 is undershoot.

Case 2 is overshoot with dampening effect.

C. FREQUENCY-DOMAIN ANALYSIS OF PASSIVE NETWORKS

(i) RC Circuits

Integrator



Since there is a switch in the circuit, V_{in} is considered a step function with respect to time and it is valid for t > 0.
Thus, taking the Laplace transform of V_{in} yields:

$$V_{in}(s) = \int_0^\infty V_{in} e^{-st} dt = V_{in} \int_0^\infty e^{-st} dt = \frac{V_{in}}{s}$$

Then, KVL dictates:

$$\frac{Vin}{s} = I(s)\left[R + \frac{1}{sC}\right] = I(s)\frac{(sRC+1)}{sC}$$

$$Vout(s) = I(s)\frac{1}{sC} = \frac{1}{\cancel{sC}}\ \frac{\text{Vin}}{\text{s}}\ \frac{\cancel{sC}}{(sRC+1)}$$

$$Vout(s) = \frac{Vin}{RC}\ \frac{1}{s\left(s+\frac{1}{RC}\right)}$$

But, $\frac{1}{s\left(s+\frac{1}{RC}\right)} \equiv \frac{A}{s} + \frac{B}{s+\frac{1}{RC}}$ $\qquad A\left(s+\frac{1}{RC}\right) + Bs \equiv 1$ $\qquad s(A+B) + \frac{A}{RC} \equiv 1$

Thus:

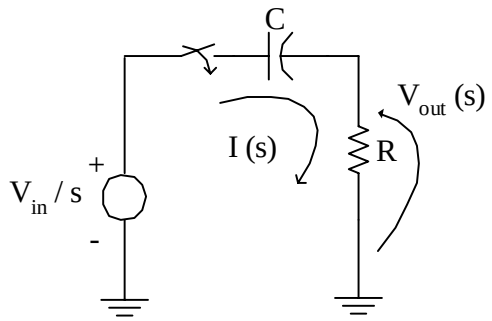
$A + B = 0$ and $\frac{\text{A}}{\text{RC}} = 1$ yields

$A = RC$ and $B = -RC$

$$Vout(s) = \frac{Vin}{RC}\left[\frac{RC}{s} - \frac{RC}{\left(s+\frac{1}{RC}\right)}\right] = Vin\left[\frac{1}{s} - \frac{1}{\left(s+\frac{1}{RC}\right)}\right]$$

$$vout(t) = Vin\ \pounds^{-1}\left[\frac{1}{s} - \frac{1}{\left(s+\frac{1}{RC}\right)}\right] = Vin\left(1 - e^{-\frac{t}{RC}}\right)$$

Differentiator



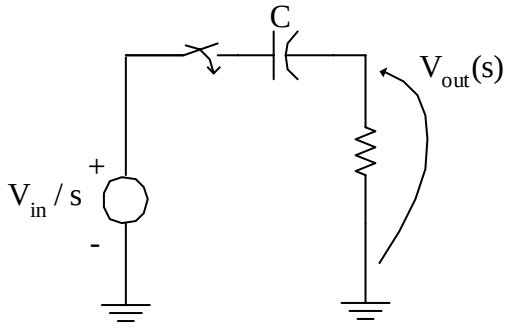
$$\frac{V_{in}}{s} = I(s)\left[R + \frac{1}{sC}\right] = I(s)\frac{(sRC+1)}{sC}$$

$$V_{out}(s) = I(s)R = \frac{\cancel{RC}}{\cancel{RC}} \frac{V_{in}}{\left(s + \frac{1}{RC}\right)} = \frac{V_{in}}{\left(s + \frac{1}{RC}\right)}$$

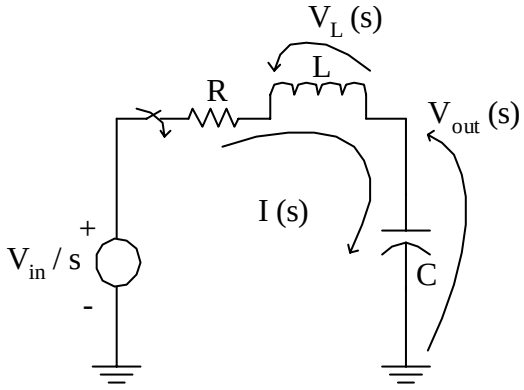
$$v_{out}(t) = V_{in}\ \mathcal{L}^{-1}\left[\frac{1}{s + \frac{1}{RC}}\right] = V_{in}\ e^{-\frac{t}{RC}}$$

Homework:

Find $v_{out}(t)$ by performing frequency-domain analysis



(ii) RLC Circuits



Assuming that $v_{out}(0) = 0$ V and $i(0) = 0$.

$$\frac{V_{in}}{s} = I(R + sL + \frac{1}{sC})$$

$$V_{out} = \frac{I}{sC}$$

$$\frac{V_{in}}{s} = sCV_{out}(R + sL + \frac{1}{sC})$$

$$\frac{V_{in}}{s} = V_{out}(RCs + s^2LC + 1)$$

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{LC}}{s(s^2 + \frac{R}{L}s + \frac{1}{LC})}$$

Solving $(s^2 + \frac{R}{L}s + \frac{1}{LC})$ yields:

$$s_{1,2} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} \quad \text{or} \quad s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0{}^2}$$

Where, $\alpha = \frac{R}{2L}$ and $\omega_0 = \frac{1}{\sqrt{LC}}$

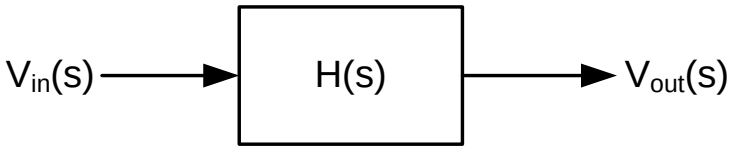
$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{LC}}{s(s-s_1)(s-s_2)} \equiv \frac{K}{s} + \frac{M}{(s-s_1)} + \frac{N}{(s-s_2)}$$

$$v_{out}(t) = \left(K + Me^{s_1 t} + Ne^{s_2 t}\right)V_{in} \quad \text{for } t \geq 0\,.$$

Where, $K = 1$, $M = \frac{s_2}{s_2 - s_1}$ and $N = \frac{s_1 - 2s_2}{s_2 - s_1}$

(iii) STABILITY

Transfer Function



$$V_{out}(s) = V_{in}(s) \cdot H(s)$$

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)}$$

The transfer function, H(s), can be described as follows.

$$H(s) = \frac{N(s)}{D(s)}$$

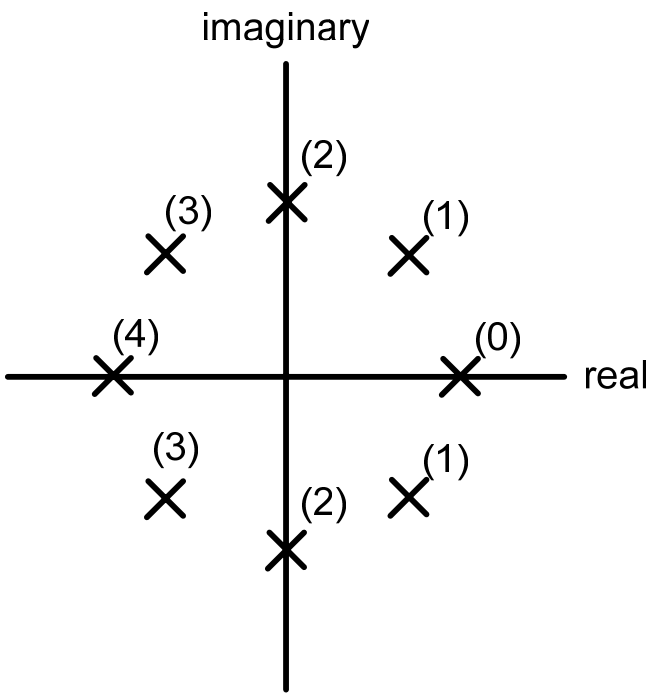
When N(s) = 0, the solution gives us the zeros.
When D(s) = 0, the solution gives us the poles and also tells us the stability of the circuit.

Poles

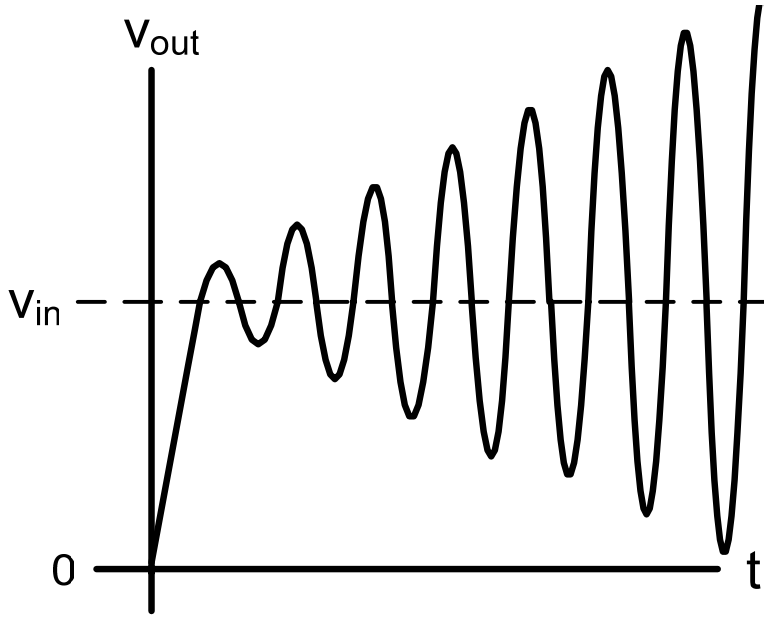
When solving for D(s) = 0, the solution should result in the following form:

$$s = \alpha + \omega j$$

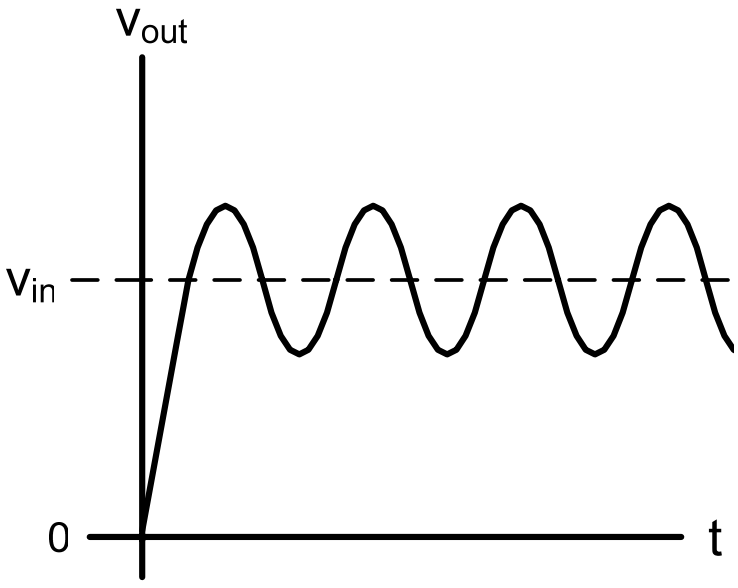
where α is the real component and ω is the imaginary component. These solutions (there could be more than one solution for s) can then be plotted real vs. imaginary.



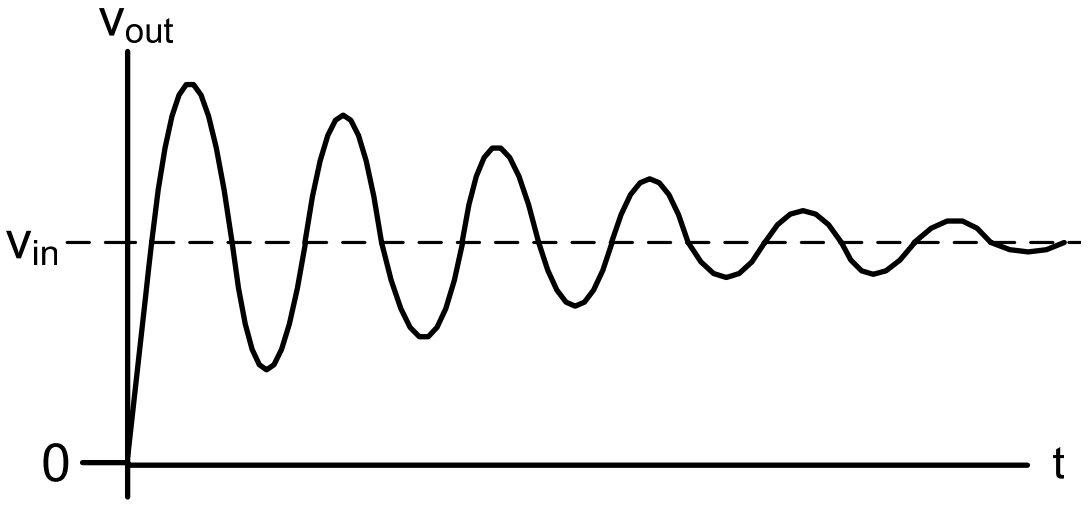
Poles to the right of the imaginary axis shown as (0) and (1) are unstable causing the resulting waveforms similar to the following:

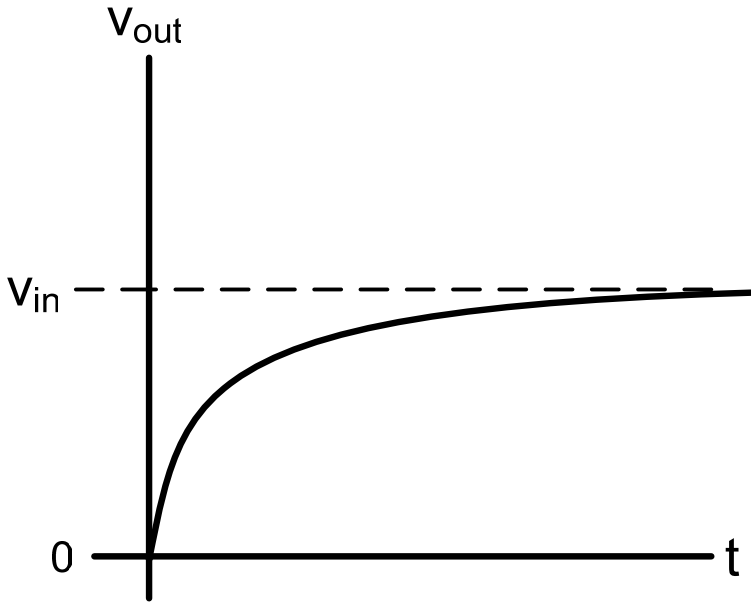


Poles that lay on the imaginary axis shown as (2) are oscillatory causing waveforms similar to the following:

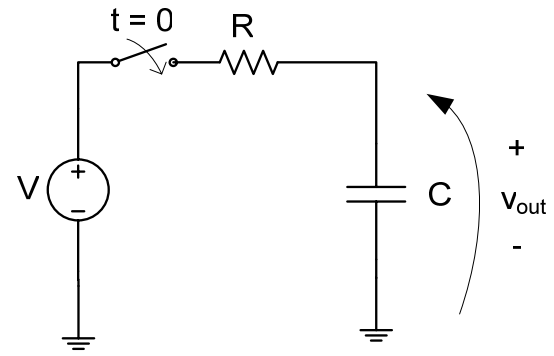


Poles to the left of the imaginary axis shown as (3) and (4) are stable causing the resulting waveforms similar to the following:

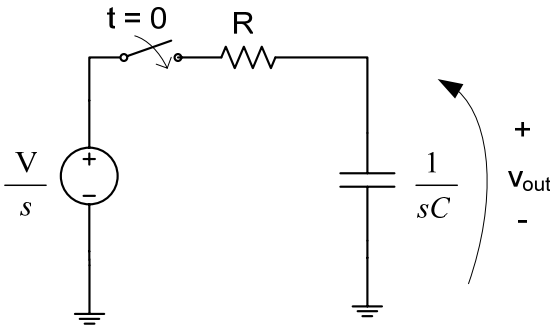




Example 1



We first transform the circuit with Laplace.



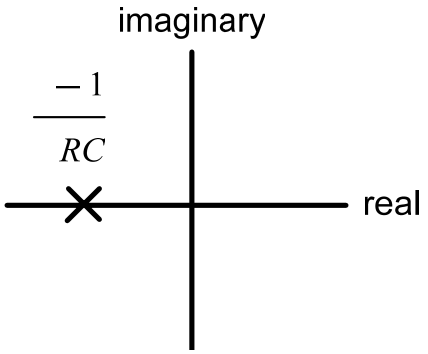
$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} = \frac{1}{sRC + 1} = \frac{1}{RC\left(s + \frac{1}{RC}\right)}$$

Now, to find the pole(s).

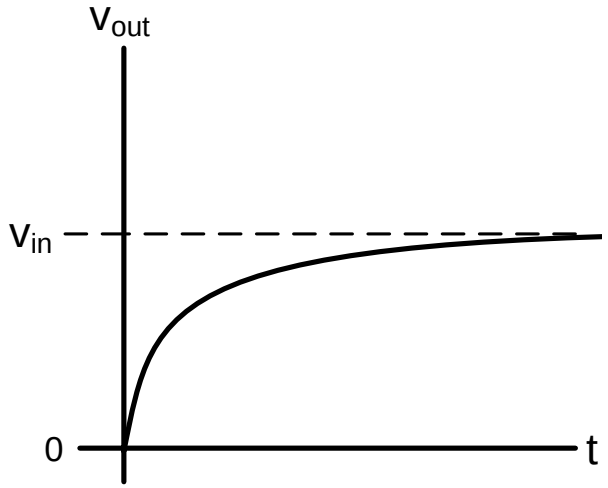
$$N(s) = RC\left(s + \frac{1}{RC}\right) = 0$$

$$s = \frac{-1}{RC}$$

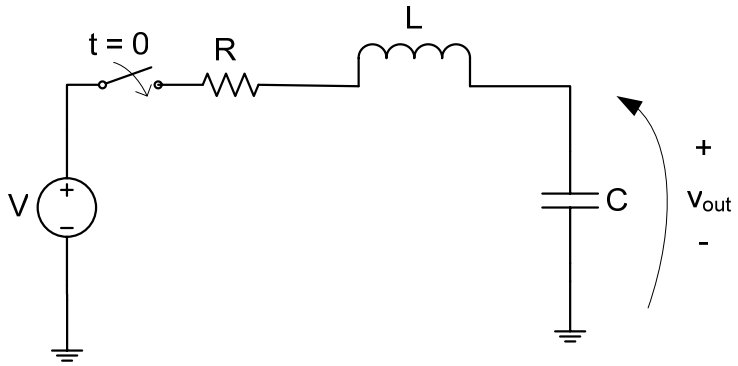
Plot this pole.



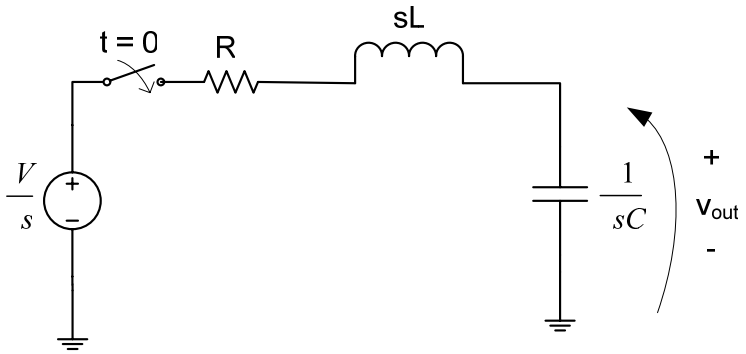
From the position of the pole, we know that the circuit is stable and the waveform would look as follows:



Example 2



We first transform the circuit into s-domain with Laplace.



$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{1}{sC}}{R + sL + \frac{1}{sC}} = \frac{1}{s^2CL + sRC + 1}$$

Now, to find the pole(s).

$$N(s) = s^2CL + sRC + 1 = 0$$

$$s_{1,2} = \frac{-RC \pm \sqrt{(RC)^2 - 4CL}}{2CL} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \left(\frac{1}{\sqrt{CL}}\right)^2}$$

$$s_1 = -\alpha_0 + \sqrt{\alpha_0^{\,2} - \omega_0^{\,2}}$$

$$s_2 = -\alpha_0 - \sqrt{\alpha_0^{\,2} - \omega_0^{\,2}}$$

where

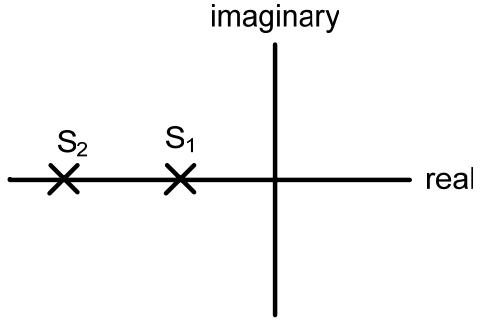
$$\alpha_0 = \frac{R}{2L}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

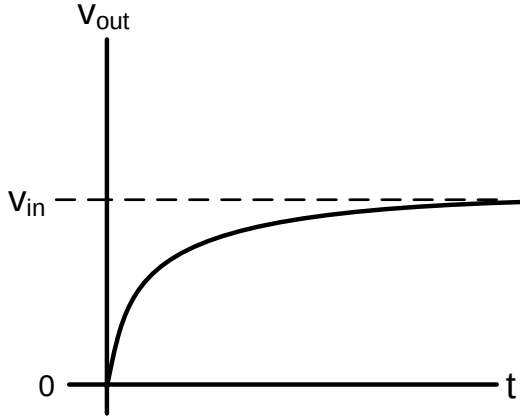
Assuming that L, R, and C are not zero and not negative there are three possible solutions.

$\alpha_0 < \omega_0$ → There is not imaginary part.

Plot these poles.

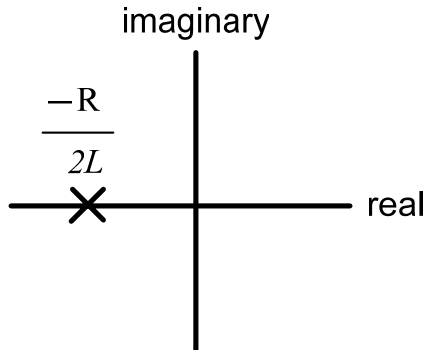


From the position of the pole, we know that the circuit is stable and the waveform would look as follows:

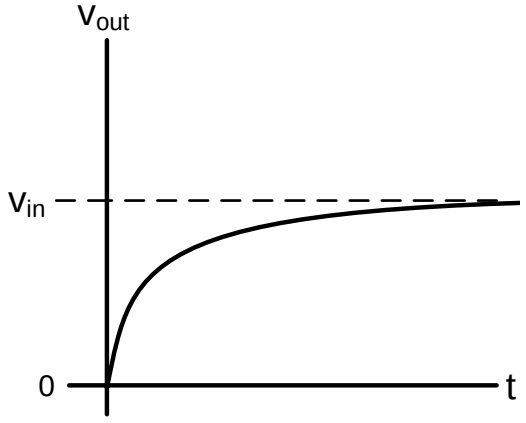


$\alpha_0 = \omega_0$ → There is not imaginary part.

Plot this pole.

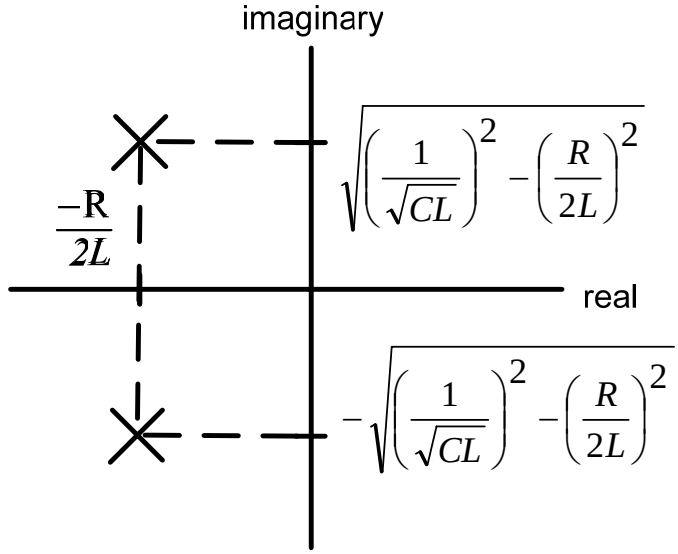


From the position of the pole, we know that the circuit is stable and the waveform would look as follows:

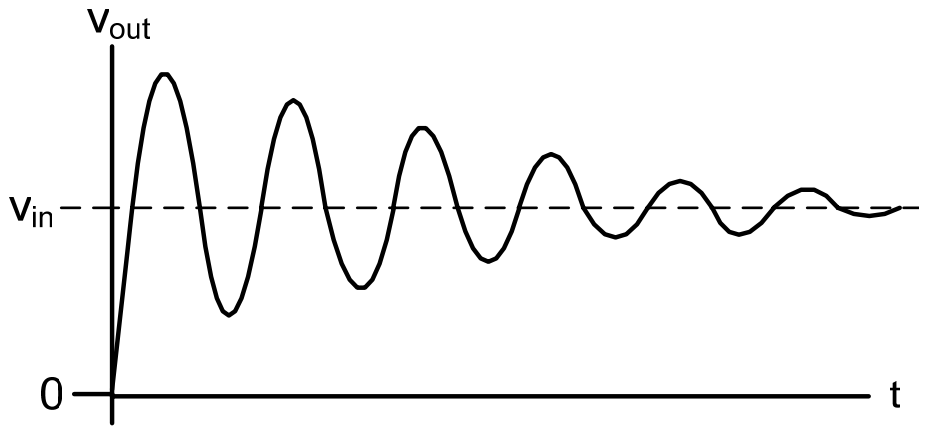


$\alpha_0 > \omega_0$ → There is an imaginary part.

Plot these poles.



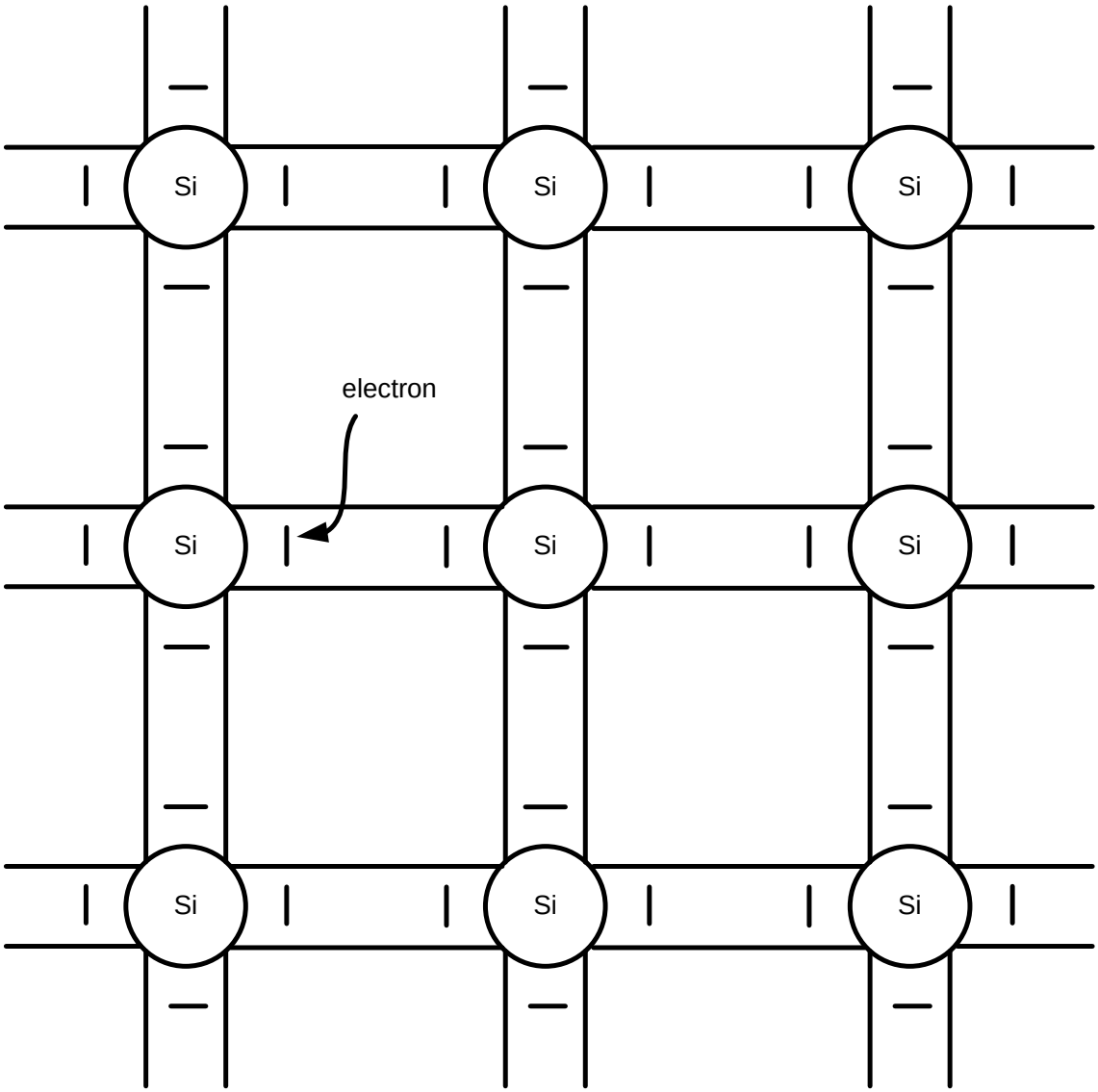
From the position of the pole, we know that the circuit is stable and the waveform would look as follows:



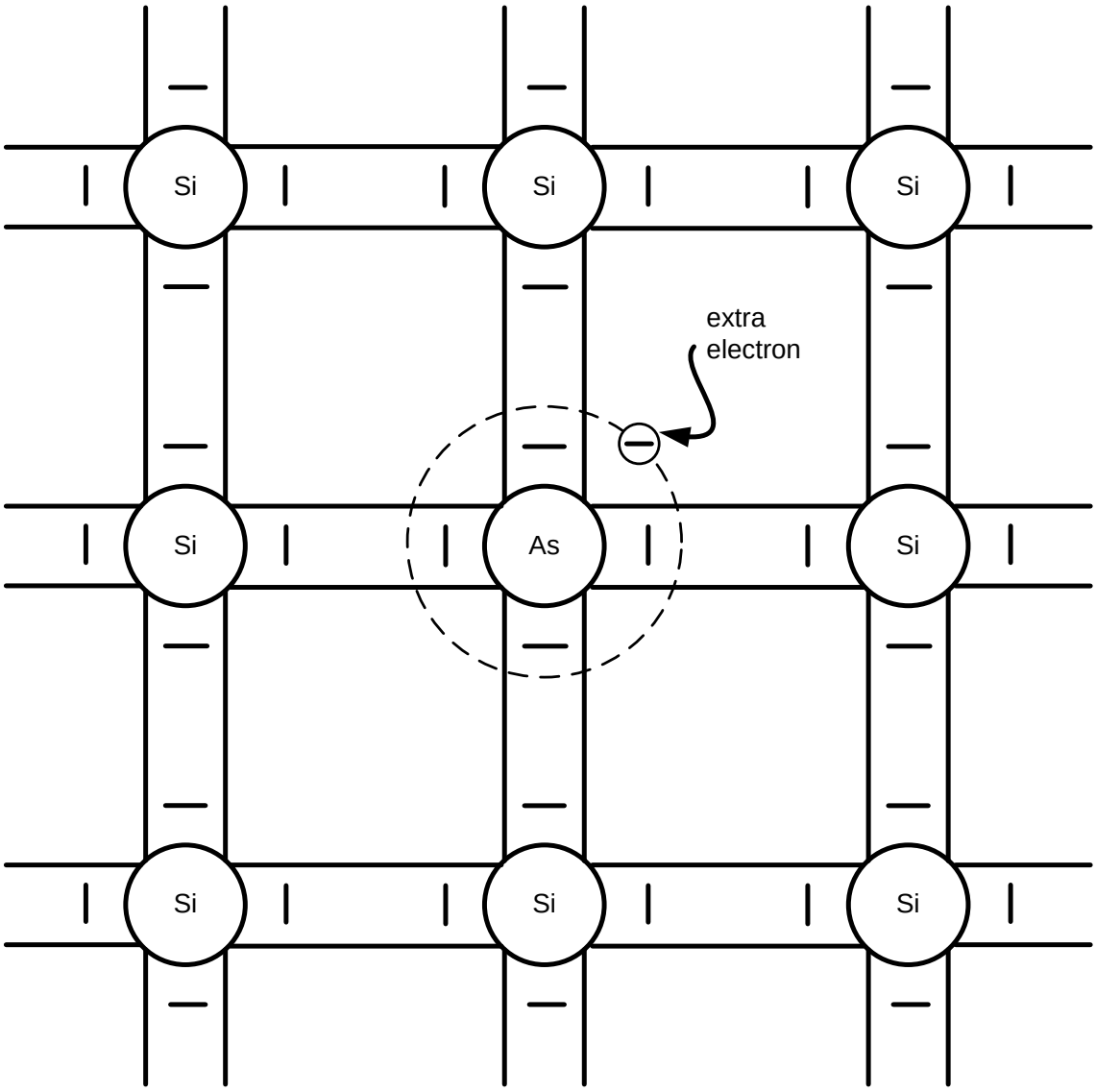
CHAPTER II. FUNDAMENTALS OF CMOS CIRCUITS

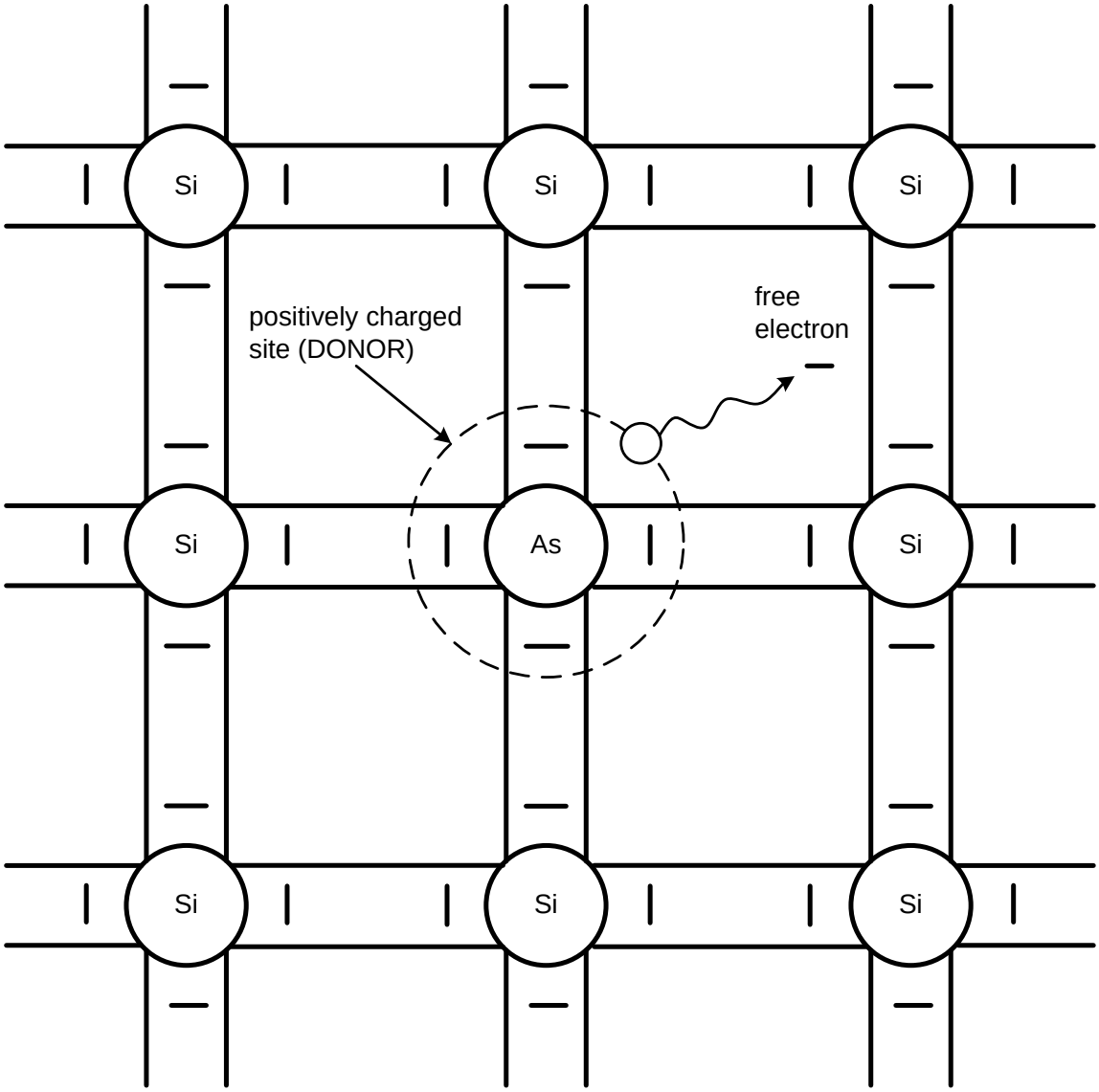
A. BRIEF THEORY OF SEMICONDUCTORS

INTRINSIC SEMICONDUCTOR

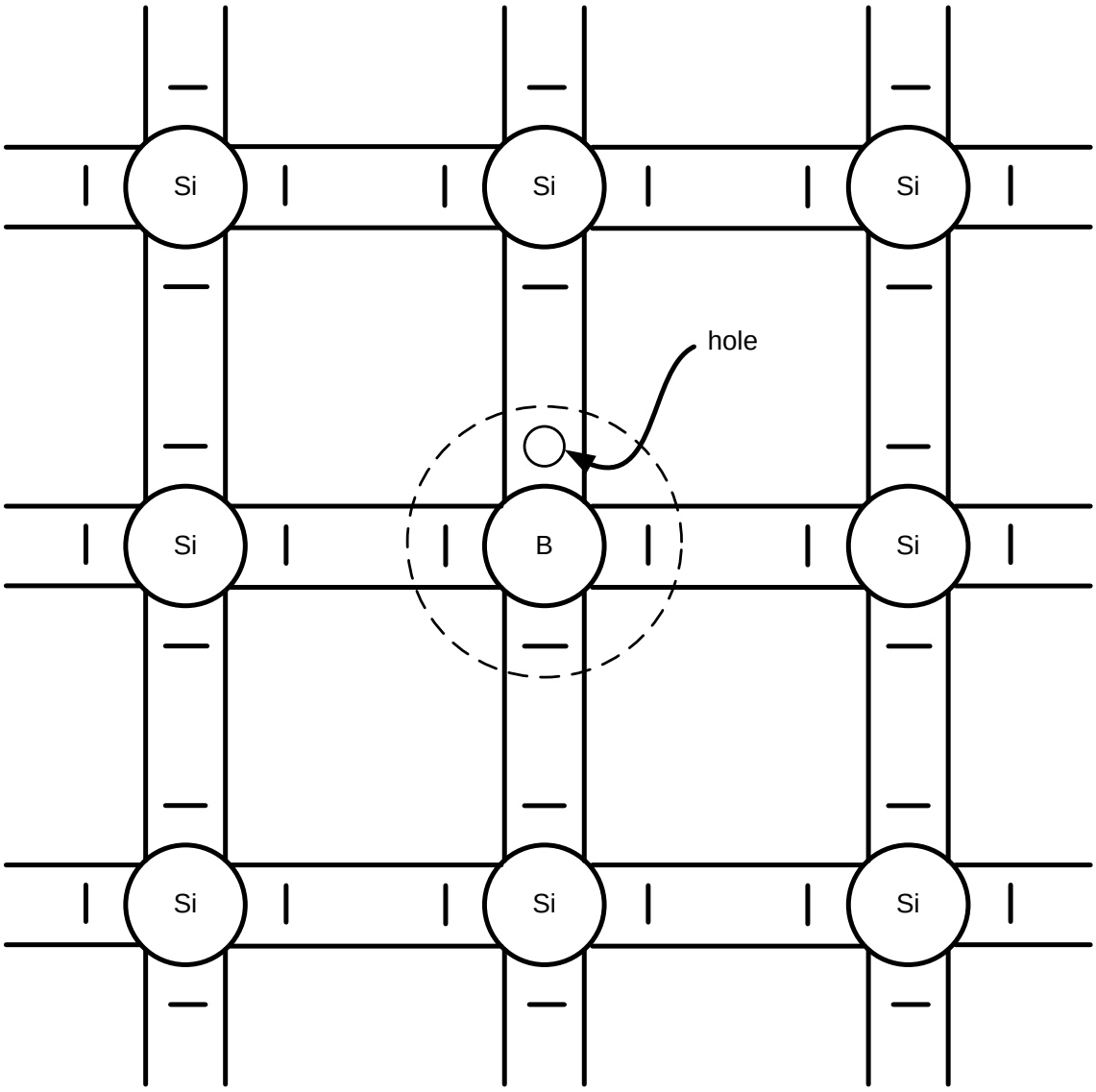


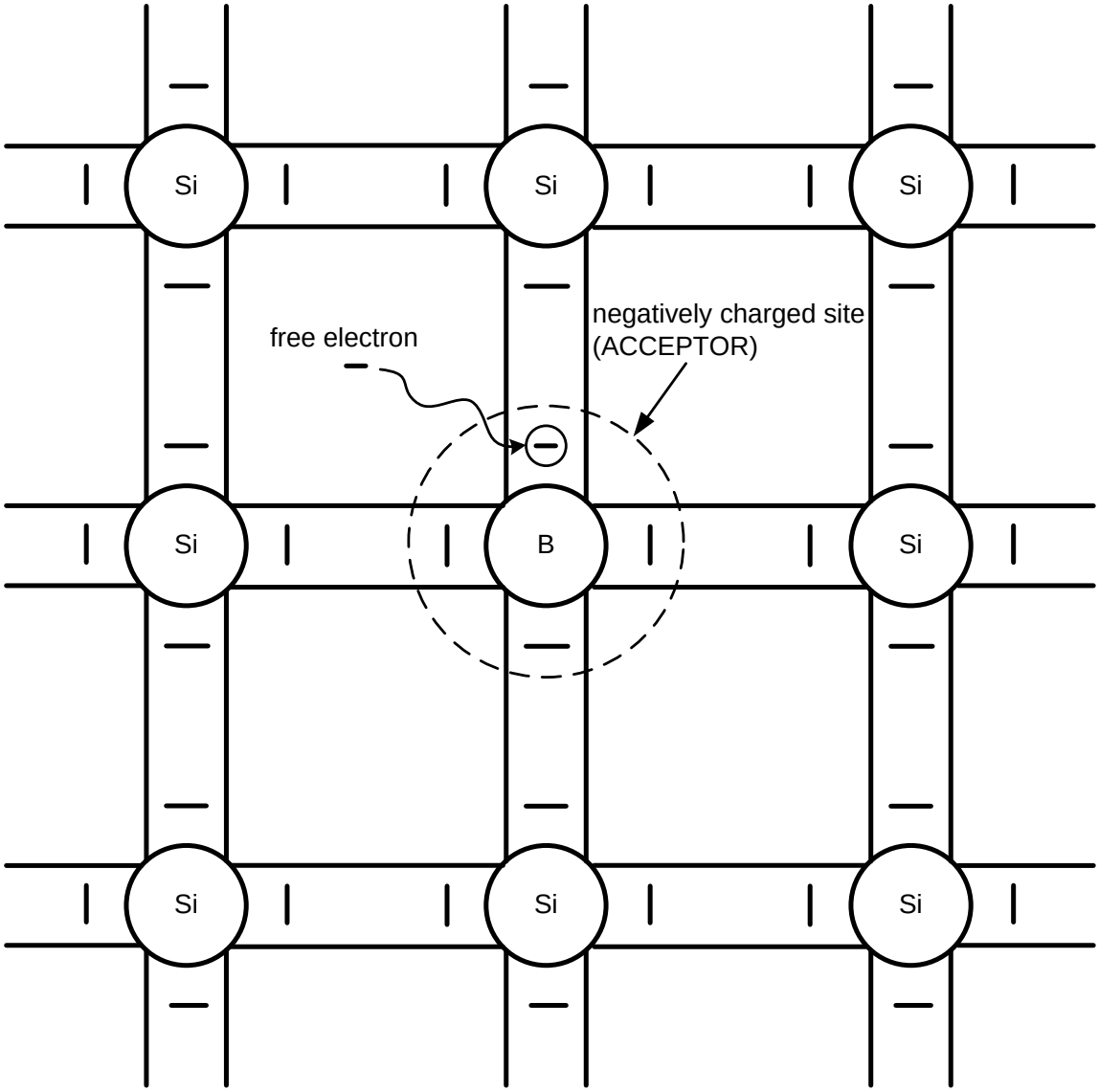
N-TYPE EXTRINSIC SEMICONDUCTOR



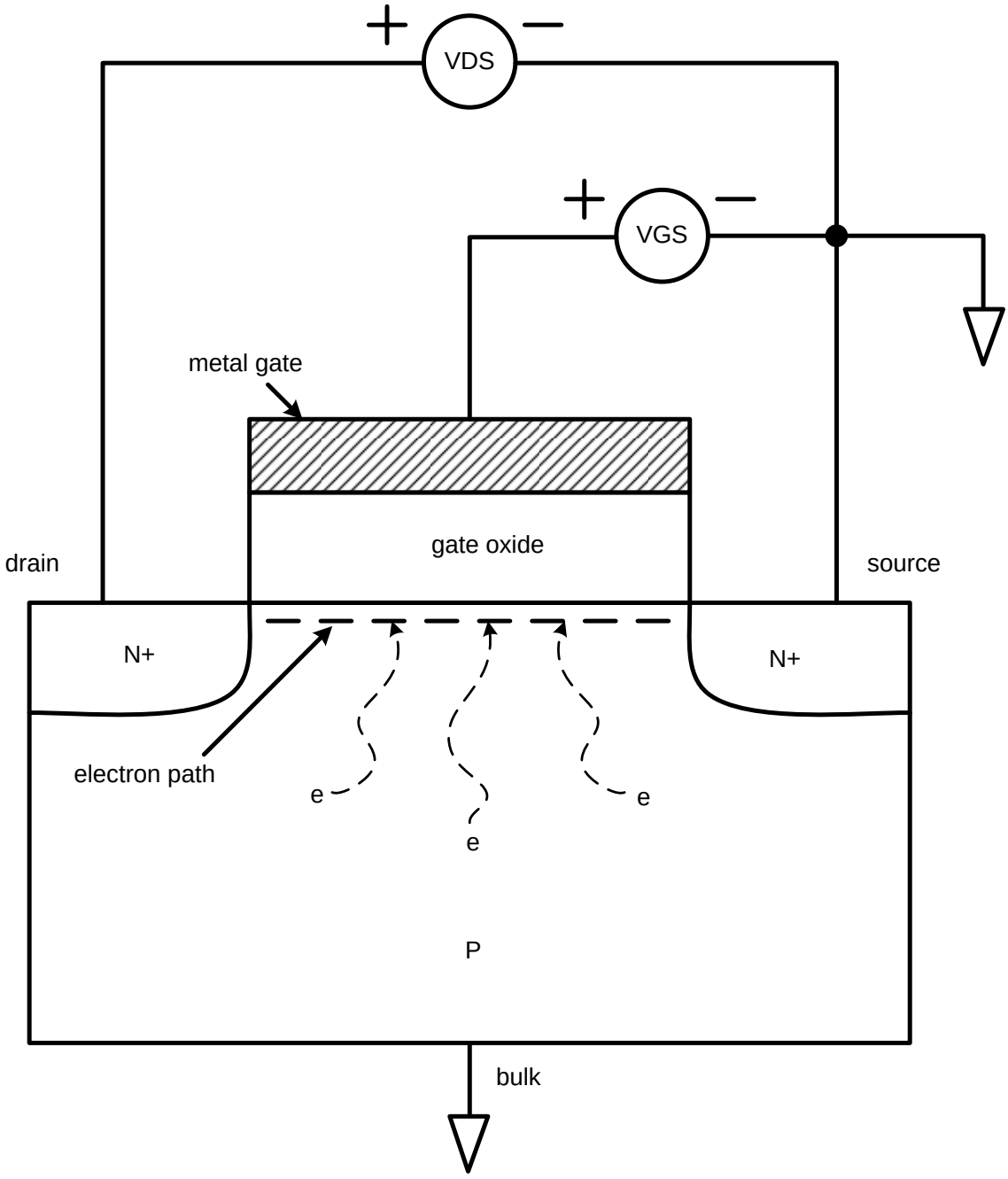

Si
Si
Si
positively charged
site (DONOR)
free
electron
Si
As
Si
Si
Si
Si

P-TYPE EXTRINSIC SEMICONDUCTOR

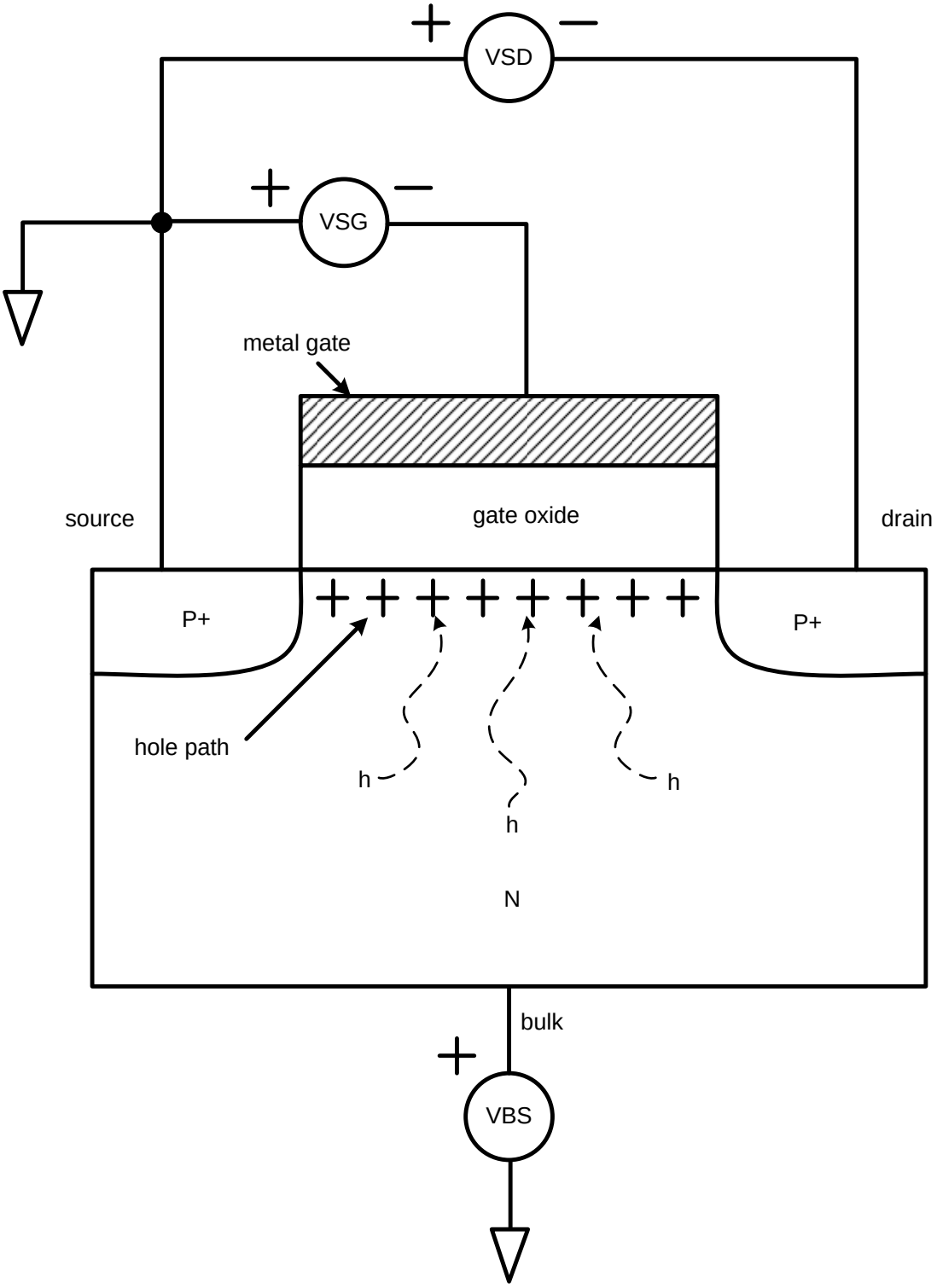



Si
Si
Si
free electron
negatively charged site
(ACCEPTOR)
Si
B
Si
Si
Si
Si

N-type Metal Oxide Semiconductor Field Effect Transistor (NMOSFET)

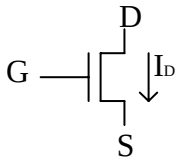


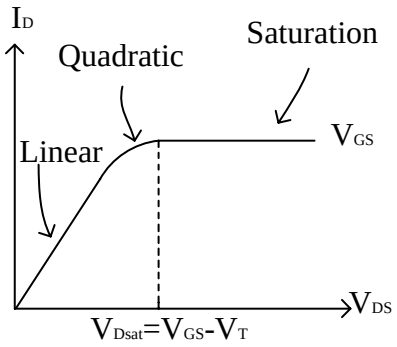
P-type Metal Oxide Semiconductor Field Effect Transistor (PMOSFET)



B. MOSFET CHARACTERISTICS

(i) NMOSFET



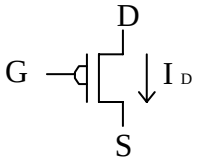


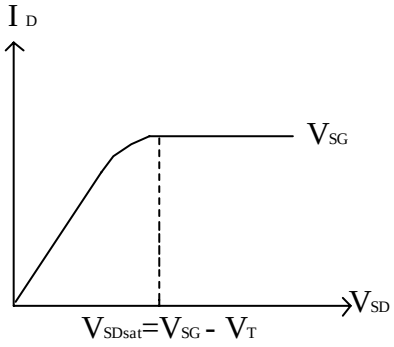
$$I_D = \frac{\mu_n C_{ox} W_n}{L}\left[\left(V_{GS} - V_{Tn}\right)V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

$$I_D \cong \frac{\mu_n C_{ox} W_n}{L}\left[\left(V_{GS} - V_{Tn}\right)V_{DS}\right]$$ linear region for small V_{DS}

$$I_D = \frac{\mu_n C_{ox} W_n}{2L}\left(V_{GS} - V_{Tn}\right)^2$$ for $V_{DS} \geq V_{Dsat} = V_{GS} - V_{Tn}$ saturation region for large V_{DS}

(ii) PMOSFET





$$I_D = \frac{\mu_p C_{ox} W_p}{L}\left[\left(V_{SG} - V_{Tp}\right)V_{SD} - \frac{{V_{SD}}^2}{2}\right]$$

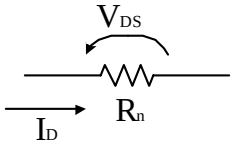
$$I_D \cong \frac{\mu_p C_{ox} W_p}{L}\left[\left(V_{SG} - V_{Tp}\right)V_{SD}\right]$$ linear region for small V_{SD}

$$I_D = \frac{\mu_p C_{ox} W_p}{2L}\left(V_{SG} - V_{Tp}\right)^2$$ for $V_{SD} \geq V_{SDsat} = V_{GS} - V_{Tp}$ saturation region for large V_{SD}

C. LARGE SIGNAL EQUIVALENT CIRCUIT OF MOSFETS

(i) NMOSFET LARGE SIGNAL EQUIVALENT CIRCUIT

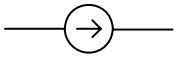
For small $V_{DS} \Rightarrow$



$$R_n = \frac{V_{DS}}{I_D} = \frac{1}{\frac{\mu_n C_{ox} W_n}{L}\left(V_{GS} - V_{Tn}\right)}$$

$$R_n = \frac{1}{K_n\left(V_{GS} - V_{Tn}\right)} \quad \text{where } K_n \cong \frac{\mu_n C_{ox} W_n}{L}$$

For large $V_{DS} \Rightarrow$

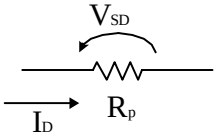


$$I_{Dsat} = \frac{K_n}{2}\left(V_{GS} - V_{Tn}\right)^2$$

If $V_{GS}=V_{DD}$ & $V_{Tn} \cong 0.2V_{DD}$ then: $R_n = \frac{1}{0.8K_nV_{DD}}$ & $I_{DSAT} = 0.32K_nV_{DD}^{\ 2}$

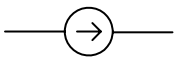
(ii) PMOSFET LARGE SIGNAL EQUIVALENT CIRCUIT

For small $V_{SD} \Rightarrow$



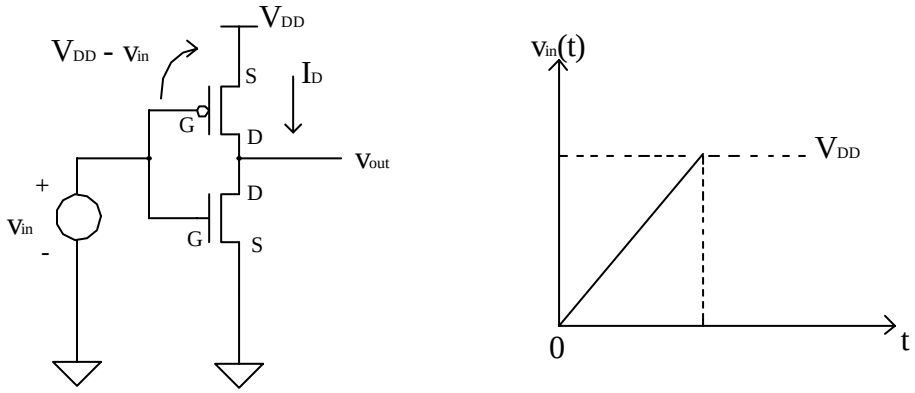
$$R_p = \frac{1}{K_p\left(V_{SG} - V_{Tp}\right)} \quad \text{where } K_p = \frac{\mu_p C_{ox} W_p}{L}$$

For large $V_{SD} \Rightarrow$

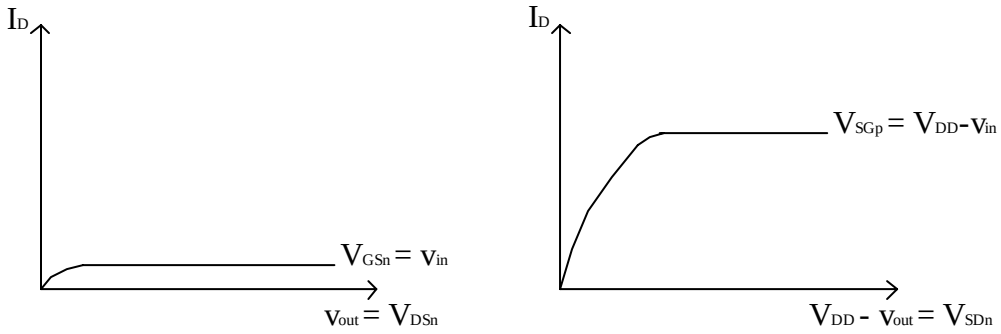


$$I_{DSAT} = \frac{K_p}{2}\left(V_{SG} - V_{Tp}\right)^2$$

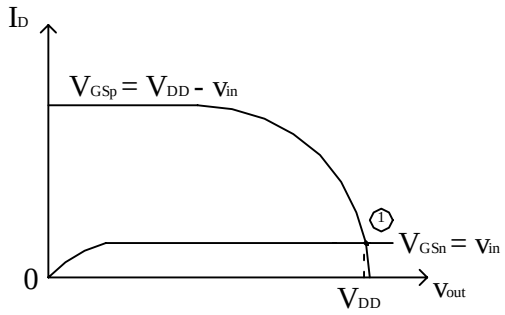
D. Complementary MOS (CMOS) Inverter Static Characteristics



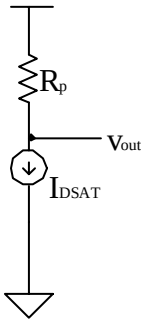
(i) For Small values of v_{in} (t)



Overlapping these two curves on top of each other yields:
$v_{out} = V_{DSn} = V_{DD}$ when $V_{SDp} = 0$
$v_{out} = 0$ when $V_{SDp} = V_{DD}$



At ① pfet is in linear region
nfet is in saturation region

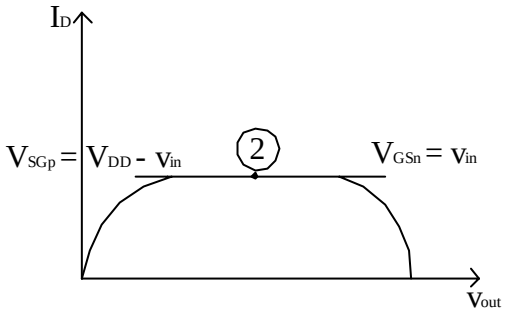


$$v_{out} = V_{DD} - R_p I_{DSAT} \quad \text{where } R_p = \frac{1}{K_p\left(V_{SGp} - V_{Tp}\right)} = \frac{1}{K_p\left(V_{DD} - v_{in} - V_{Tp}\right)}$$

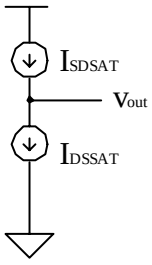
$$I_{DSAT} = \frac{K_n}{2}\left(V_{GSn} - V_{Tn}\right)^2 = \frac{K_n}{2}\left(v_{in} - V_{Tn}\right)^2$$

$$v_{out} = V_{DD} - \frac{K_n}{2K_p}\frac{\left(v_{in} - V_{Tn}\right)^2}{\left(V_{DD} - v_{in} - V_{Tp}\right)}$$

(ii) For some intermediate value of $v_{in}(t)$



At (2) both pfet & nfet are in saturation region



$$I_{SDSAT} = \frac{K_p}{2}\left(V_{SGp} - V_{Tp}\right)^2$$

$$I_{DSSAT} = \frac{K_n}{2}\left(V_{GSn} - V_{Tn}\right)^2$$

But, $I_{SDSAT} = I_{DSSAT}$ gives $\frac{K_p}{K_n} = \frac{\left(V_{GSn} - V_{Tn}\right)^2}{\left(V_{SGp} - V_{Tp}\right)^2}$

Substituting $V_{GSn} = v_{in}$ and $V_{SGp} = V_{DD} - v_{in}$

$$\sqrt{\frac{K_p}{K_n}} = \frac{\left(v_{in} - V_{Tn}\right)}{\left(V_{DD} - v_{in} - V_{Tp}\right)}$$

We had $K_p = \frac{\mu_p C_{ox} W_p}{L}$ and $K_n = \frac{\mu_n C_{ox} W_n}{L}$

$$\sqrt{\frac{\mu_p W_p}{\mu_n W_n}} = \frac{v_{in} - V_{Tn}}{V_{DD} - v_{in} - V_{Tp}}$$

Assume that $\mu_n \cong 2\mu_p$ & $V_T = V_{Tn} = V_{Tp}$

$$\sqrt{\frac{\mu_p W_p}{2\mu_p W_n}} = \frac{v_{in} - V_T}{V_{DD} - v_{in} - V_T} = \sqrt{\frac{W_p}{2W_n}} = R$$

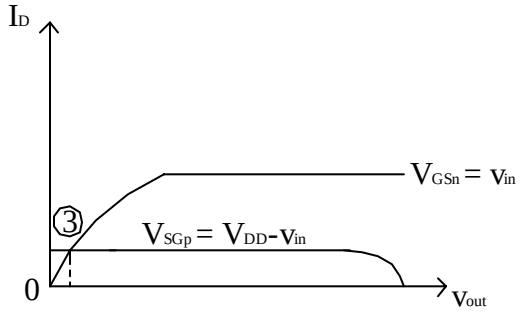
$v_{in} - V_T = R\left(V_{DD} - v_{in} - V_T\right)$ yields $v_{in}\left(1+R\right) = V_T\left(1-R\right) + RV_{DD}$

$$v_{in} = \frac{R\left(V_{DD} - V_T\right) + V_T}{1+R}$$

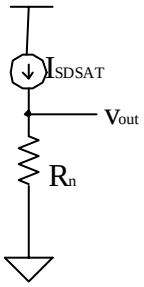
if $W_p = 2W_n \Rightarrow$ R=1 $\Rightarrow v_{in} = \frac{V_{DD}}{2}$

if $W_p = W_n \Rightarrow$ R=0.71 $\Rightarrow v_{in} \cong 0.41V_{DD}$

(iii) For large values of $v_{in}(t)$



At ③ nfet is in linear region
pfet is in saturation region



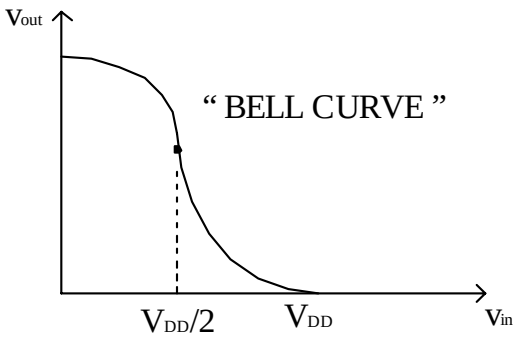
$v_{out} = R_n I_{SDSAT}$

Where, $R_n = \dfrac{1}{K_n\left(V_{GSn} - V_{Tn}\right)} = \dfrac{1}{K_n\left(v_{in} - V_T\right)}$

$$I_{SDSAT} = \frac{K_p}{2}\left(V_{SGp} - V_{Tp}\right)^2 = \frac{K_p}{2}\left(V_{DD} - v_{in} - V_{Tp}\right)^2$$

$$v_{out} = \frac{K_p}{2K_n}\frac{\left(V_{DD} - v_{in} - V_{Tp}\right)^2}{\left(v_{in} - V_{Tn}\right)}$$

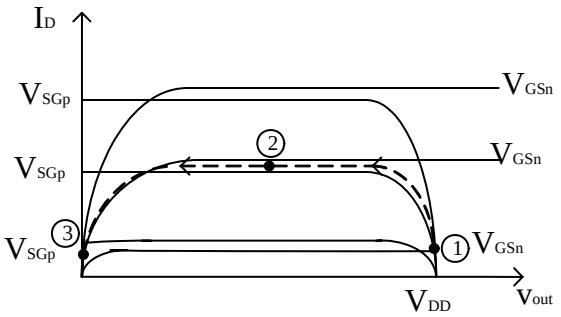
Plotting v_{out} in terms of v_{in} yields:



For $v_{in} < V_{DD}/2$

$$v_{out} = V_{DD} - \frac{K_n}{2K_p}\frac{\left(v_{in} - V_{Tn}\right)^2}{\left(V_{DD} - v_{in} - V_{Tp}\right)}$$

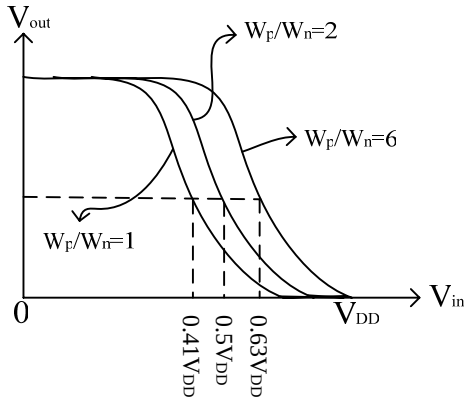
For $v_{in} > V_{DD}/2$ $v_{out} = \dfrac{K_p}{2K_n}\dfrac{\left(V_{DD} - v_{in} - V_{Tp}\right)^2}{\left(v_{in} - V_{Tn}\right)}$



As v_{in} approaches from 0 to V_{DD} then the quiescent point (operating point) of the the inverter transverses the DASHED ARC from ① to ③ through ② in I_D vs. v_{out} curve. As v_{in} approaches from V_{DD} to 0, the quiescent point of the inverter follows the DASHED ARC from ③ to ①.

Now, let's plot the BELL CURVE for different values of $\frac{W_p}{W_n}$:

$\frac{W_p}{W_n}$	v_{in} at ②
1	0.41 V_{DD}
2	0.5 V_{DD}
3	0.55 V_{DD}
4	0.58 V_{DD}
6	0.63 V_{DD}



Observe the following:

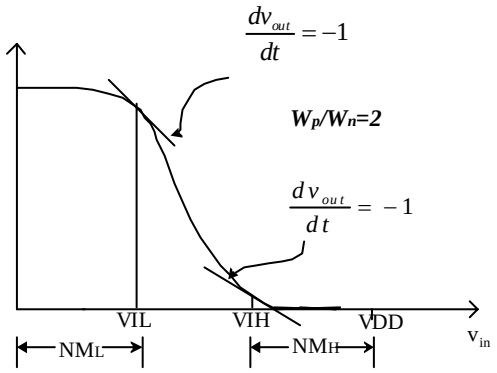
- When $\frac{W_p}{W_n} = 1$ (strong nfet weak pfet) <u>small</u> increases in v_{in} quickly turns the nfet on, and v_{out} starts decreasing towards 0.

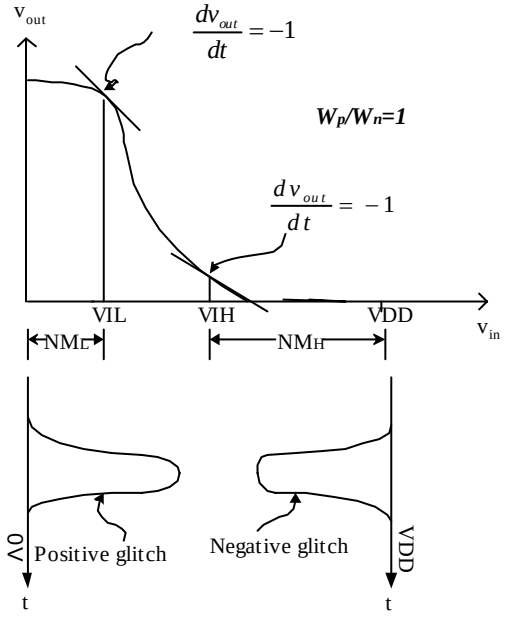
- When $\frac{W_p}{W_n} = 6$ (strong pfet weak nfet) large increases in v_{in} cannot turn on the nfet, v_{out} delays to decrease towards 0.

E. NOISE MARGIN OF THE INVERTER

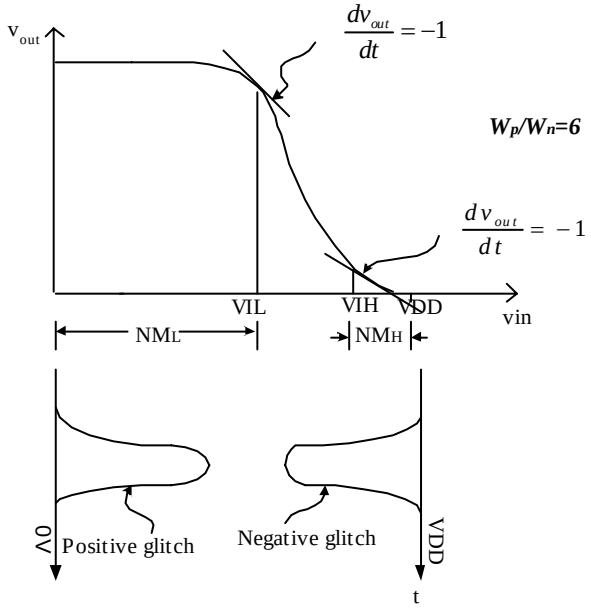
Noise margin of the inverter is defined as the value of the input voltage, v_{in}, at $\frac{dv_{out}}{dt} = -1$.

Thus, from the BELL curve:





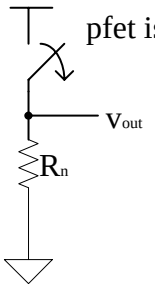
When nfet is stronger with respect to pfet (W_p/W_n=1) in an inverter, then small input voltages at v_{in} can easily turn on the nfet. Therefore, the inverter with W_p/W_n=1 has low noise margin or noise immunity for positive glitches at its input. But, the same inverter exhibits high noise immunity for negative glitches at its input.



For an inverter with W_p/W_n=6, the inverter exhibits high noise immunity for positive glitches & low noise immunity for negative glitches.

F. CMOS Inverter Dynamic Characteristics

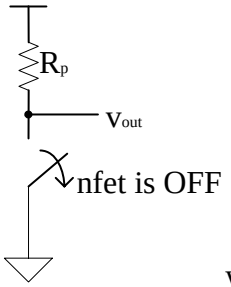
If v_{in} is changed from 0 to V_{DD} without any transition time (rise time = 0 sec), the pfet is turned OFF, and nfet is put in the linear region and shows resistive characteristics.



$$\text{When } v_{in} = V_{DD} \Rightarrow R_n \cong \frac{1}{K_n\left(V_{DD} - V_{Tn}\right)}$$

Assume $V_{Tn} \cong 0.2V_{DD}$ $\qquad R_n \cong \dfrac{1}{0.8K_nV_{DD}}$

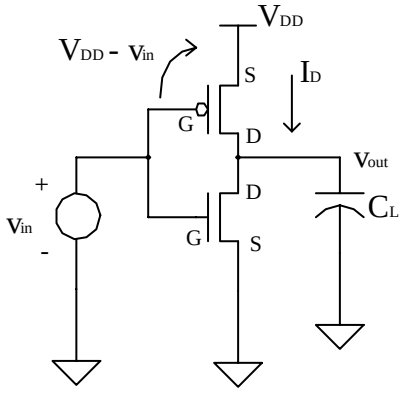
Now, if v_{in} is switched back from V_{DD} to 0 without any transition time, this time nfet is turned off and pfet is put in the linear region and shows resistive characteristics.



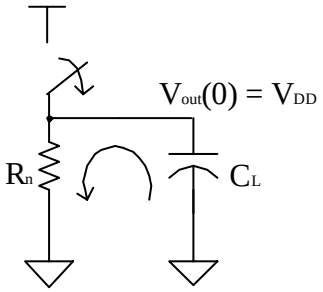
when v_{in}=0 $\quad \Rightarrow R_p \cong \dfrac{1}{K_p\left(V_{DD} - V_{Tp}\right)}$

Assume $V_{Tp} \cong 0.2V_{DD}$ and $R_p \cong \dfrac{1}{0.8K_pV_{DD}}$

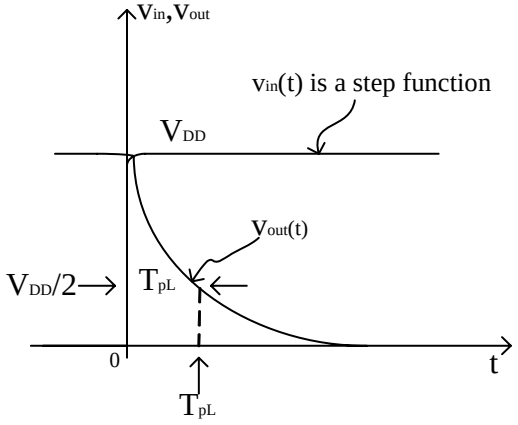
This analysis aids to derive the propagation delay of the inverter with a load capacitor, $C_{L,}$ at its output.



When v_{in} changes from 0 to V_{DD}, then nfet turns ON and pfet turns OFF.



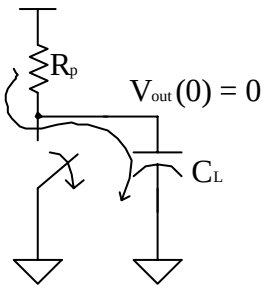
$$v_{out} = V_{DD}\, e^{-\frac{t}{R_n C_L}}$$



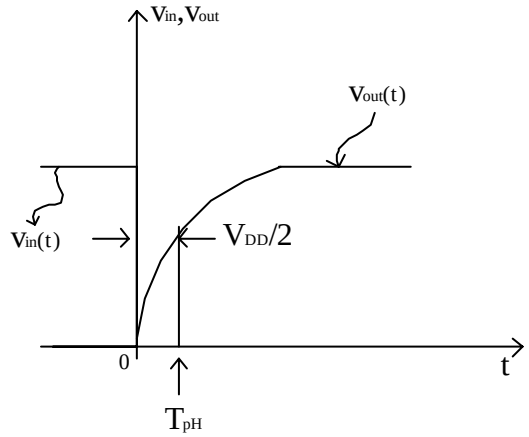
$$v_{out} = \frac{V_{DD}}{2} = V_{DD}\, e^{-\frac{T_{pL}}{R_n C_L}}$$

$T_{pL} = R_n C_L \ln 2 = 0.69\, R_n C_L$ (low-going propagation delay)

When v_{in} goes from V_{DD} to 0, then nfet is turned OFF and pfet is turned ON.



$$v_{out} = V_{DD}(1 - e^{-\frac{t}{RpC_L}})$$



$T_{pH} = 0.69\, R_p C_L$ (high-going propagation delay)

Example: Compare T_{PL} & T_{PH} for $\frac{W_p}{W_n} = 1, 2, 4$ (assume $V_T = V_{Tn} = V_{Tp} = 0.2V_{DD}$)

Solution: $R_n = \frac{1}{K_n(V_{DD} - V_T)} = \frac{1}{0.8V_{DD}K_n}$

$$R_p = \frac{1}{0.8V_{DD}K_p}$$

Where,

$$K_n = \frac{\mu_n C_{ox} W_n}{L}$$

$$K_p = \frac{\mu_p C_{ox} W_p}{L}$$

$$T_{PL} = 0.69 R_n C_L = \frac{0.86C_L}{V_{DD}K_n} = \frac{0.86C_L}{V_{DD}\, 2\mu_p C_{ox} W_n} L$$

$$T_{PH} = \frac{0.86C_L}{V_{DD}K_p} = \frac{0.86C_L}{V_{DD}\mu_p C_{ox} W_p} L$$

Let;

$$M = \frac{0.86C_L}{V_{DD}\mu_p C_{ox}} L \quad \Rightarrow \; T_{PL} = \frac{M}{2W_n}$$

$$T_{PH} = \frac{M}{W_p}$$

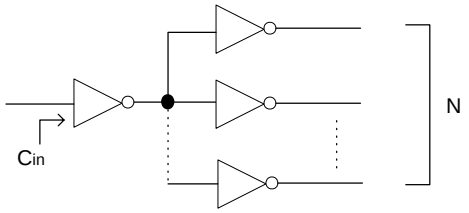
For

$\frac{W_p}{W_n} = 1$ (strong nfet, weak pfet) $\Rightarrow \; T_{PL} = \frac{M}{2W_n}$, $T_{PH} = \frac{M}{W_n} \; \Rightarrow \; T_{PL} = \frac{T_{PH}}{2}$

$\frac{W_p}{W_n} = 2$ (equal nfet and pfet) $\Rightarrow \; T_{PL} = \frac{M}{2W_n}$, $T_{PH} = \frac{M}{2W_n} \; \Rightarrow \; T_{PL} = T_{PH}$

$\frac{W_p}{W_n} = 4$ (weak nfet, strong pfet) $\Rightarrow T_{PL} = \frac{M}{2W_n}$, $T_{PH} = \frac{M}{4W_n}$ $\Rightarrow T_{PL} = 2T_{PH}$

FANOUT



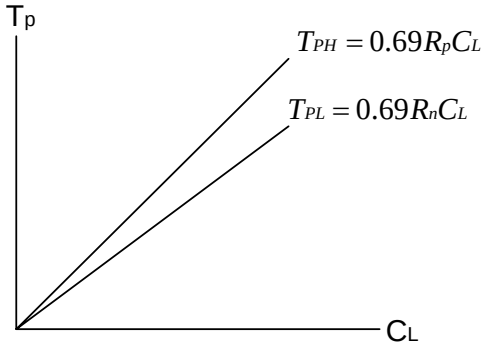
Fanout of a gate (inverter in this case) is the number of identical gates at the output of this gate.

Thus = C_L =N C_{in} where N = fanout.

Therefore,

$T_{PL} = 0.69 R_n C_L = 0.69 N\ R_n C_{in}$

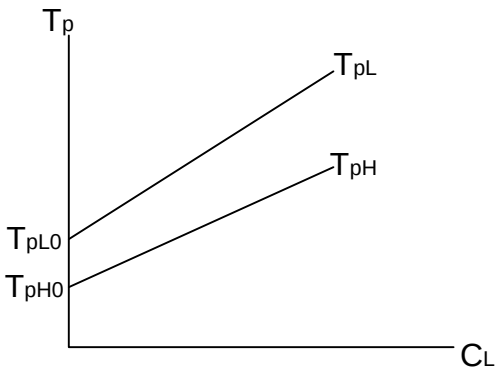
$T_{PH} = 0.69 R_p C_L = 0.69 N\ R_p C_{in}$



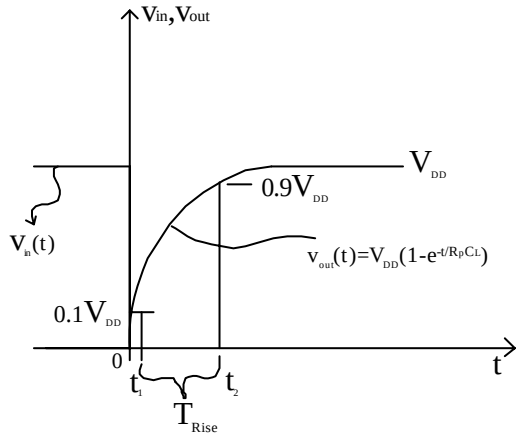
IMPORTANT OBSERVATION

T_p changes linearly with C_L. That means more output capacitance (fan-out) linearly produces propagation delay.

Note that, T_p= 0 when C_L =0 F. However, this is impossible because every inverter has an intrinsic load capacitor due to source/drain contact capacitance even though the external load capacitor, C_L, may not exist. Therefore, if one assumes C_L as a physical capacitance due to gate fanout or wiring, the practical T_p vs C_L will be as follows.



G. Rise Time & Fall Time



$$v_{out}\big|_{t=t1} = 0.1\ \cancel{V_{DD}} = \cancel{V_{DD}}\left(1 - e^{-\frac{t_1}{R_p C_L}}\right)$$

$$0.1 - 1 = -e^{-\frac{t_1}{R_p C_L}}$$

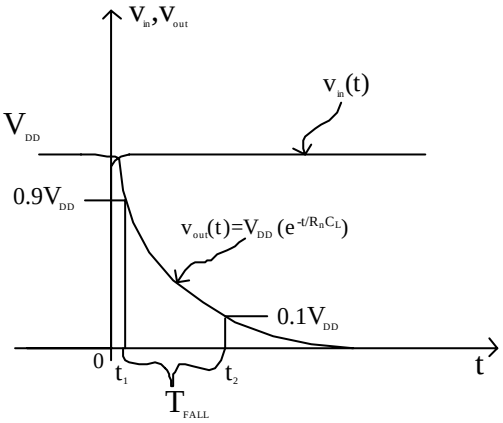
$$t_1 = -R_p C_L \ln 0.9 = 0.1 R_p C_L$$

$$v_{out}\big|_{t=t2} = 0.9\ \cancel{V_{DD}} = \cancel{V_{DD}}\left(1 - e^{-\frac{t_2}{R_pC_L}}\right)$$

$$0.9 - 1 = -e^{-\frac{t_2}{R_pC_L}}$$

$$t_2 = -R_pC_L \ln 0.1 = 2.3\ R_pC_L$$

$$T_{RISE} = t_2 - t_1 = 2.2\ R_pC_L$$



$$v_{out}\big|_{t=t1} = 0.9\cancel{V_{DD}} = \cancel{V_{DD}}\left(e^{-\frac{t_1}{R_nC_L}}\right)$$

$$t_1 = -R_nC_L \ln 0.9 = 0.1\ R_nC_L$$

$$v_{out}\big|_{t=t2} = 0.1\cancel{V_{DD}} = \cancel{V_{DD}}\left(e^{-\frac{t_2}{R_nC_L}}\right)$$

$$t_2 = -R_nC_L \ln 0.1 = 2.3\ R_nC_L$$

$$T_{FALL} = 2.2\ R_nC_L$$

<u>Example:</u> Compare T_{RISE}, T_{FALL} for $\frac{W_p}{W_n} = 1$, 2 and 4. Assume $V_T \approx 0.2V_{DD}$

Solution: $R_n = \frac{1}{0.8V_{DD}K_n}$ & $R_p = \frac{1}{0.8V_{DD}K_p}$

$$K_n = \frac{\mu_n C_{ox} W_n}{L} = \frac{2\mu_p C_{ox} W_n}{L}$$
$$K_p = \frac{\mu_p C_{ox} W_p}{L}$$

$$R_n = \frac{1}{0.8V_{DD}\mu_n C_{ox}} \frac{1}{2W_n} \qquad R_p = \frac{1}{0.8V_{DD}\mu_p C_{ox}} \frac{1}{W_p}$$

Let $P \equiv \frac{L}{0.8V_{DD}\mu_p C_{ox}}$ then $R_n = \frac{P}{2W_n}$ & $R_p = \frac{P}{W_p}$

For $\frac{W_p}{W_n} = 1$ then $T_{RISE} = (2.2\ C_L P)\frac{1}{W_n}$ *and* $T_{FALL} = (2.2\ C_L P)\frac{1}{2W_n}$

therefore $T_{RISE} = \frac{T_{FALL}}{2}$

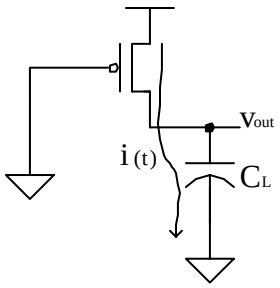
For $\frac{W_p}{W_n} = 2$ then $T_{RISE} = (2.2\ C_L P)\frac{1}{2W_n}$ *and* $T_{FALL} = (2.2\ C_L P)\frac{1}{2W_n}$

therefore $T_{RISE} = T_{FALL}$

For $\frac{W_p}{W_n} = 4$ then $T_{RISE} = (2.2\ C_L P)\frac{1}{4W_n}$ *and* $T_{FALL} = (2.2\ C_L P)\frac{1}{2W_n}$

therefore $2T_{RISE} = T_{FALL}$

H. Power Consumption



$P = \frac{1}{T}\int_0^T i(t)v_{out}(t)dt$ power spent to charge C_L.

$i = C_L \frac{dv_{out}}{dt}$

Then,

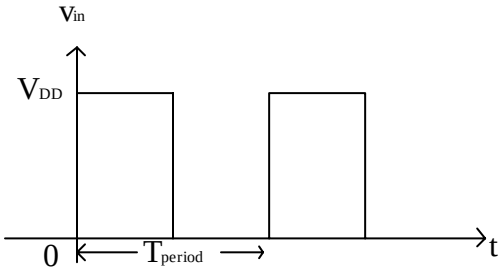
$$P = \frac{1}{T}\int_0^T C_L \frac{dv_{out}}{\cancel{dt}} v_{out}(t)\cancel{dt}$$

$$= \frac{C_L}{T}\ \frac{v_{out}^{\ 2}}{2}\ \Big|_0^{V_{DD}} = \frac{C_L}{T}\ \frac{V_{DD}^{\ 2}}{2}$$

Therefore,

Power changes LINEARLY with C_L and QUADRATICALY with $V_{DD.}$

If we have a periodic input waveform:

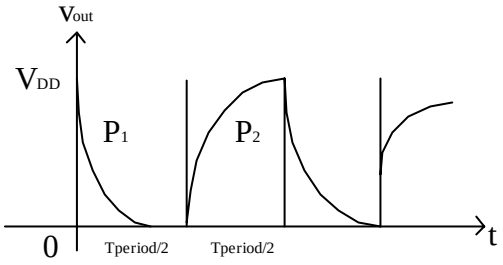


$$P_1 = \frac{1}{\left(\frac{T_{period}}{2}\right)} \int_0^{\frac{Tperiod}{2}} C_L\, v_{out}\, dv_{out}$$

$$P_2 = \frac{1}{\left(\frac{T_{period}}{2}\right)} \int_{\frac{Tperiod}{2}}^{Tperiod} C_L\, v_{out}\, dv_{out}$$

$$P = P_1 + P_2 = \frac{C_L}{T_{period}}\ \frac{V_{DD}^{\ 2}}{2} = \frac{1}{2} C_L V_{DD}^{\ 2} f$$

Therefore power changes LINEARLY with frequency.



I. TECHNOLOGY SCALING

Example: Compare 0.5μ technology with t_{ox}=100A , 3.3V @ 100 MHz with 0.1μ technology with t_{ox}=50A , 1V @ 5 GHz.

Keep $\frac{W_p}{W_n} = K$ the same in both technologies.

Solution:

$$C_L = C_{ox}(W_n + W_p)L = C_{ox}(K+1)W_n L$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \Rightarrow C_L = \frac{\varepsilon_{ox}(K+1)}{t_{ox}} W_n L$$

For 0.1μ $C_{L=0.1u} = \frac{\varepsilon_{ox}(K+1)}{50A^0} W_n (0.1\mu)$

0.5μ $C_{L=0.5u} = \frac{\varepsilon_{ox}(K+1)}{100A^0} 5W_n (0.5\mu)$

$$P_{L=0.1u} = \frac{1}{2} C_{L=0.1u} V_{DD\ L=0.1u}^{\ 2} f_{L=0.1u}$$

$$= \frac{1}{2} \frac{\varepsilon_{ox}(K+1)}{50A^0} W_n (0.1\mu)\ (1\text{V})^2 (5000MHz)$$

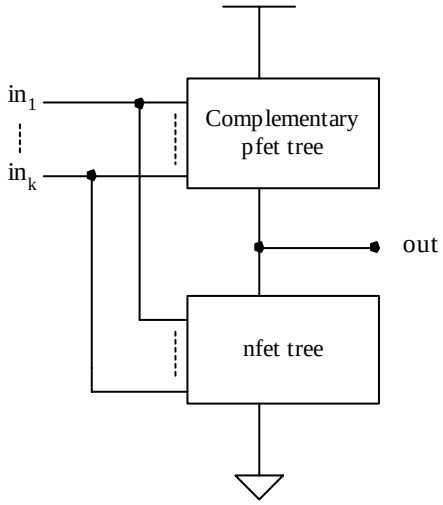
$$P_{L=0.5u} = \frac{1}{2} \frac{\varepsilon_{ox}(K+1)}{100A^0} 5W_n (0.5\mu)\ (3.3\text{V})^2 (100MHz)$$

$$\frac{P_{L=0.1u}}{P_{L=0.5u}} = \left(\frac{100A^0}{50A^0}\right)\left(\frac{1}{5}\right)\left(\frac{0.1\mu}{0.5\mu}\right)\left(\frac{1V}{3.3V}\right)^2\left(\frac{5000MHz}{100MHz}\right) = 0.368$$

Therefore, there is room to increase V_{DD}.

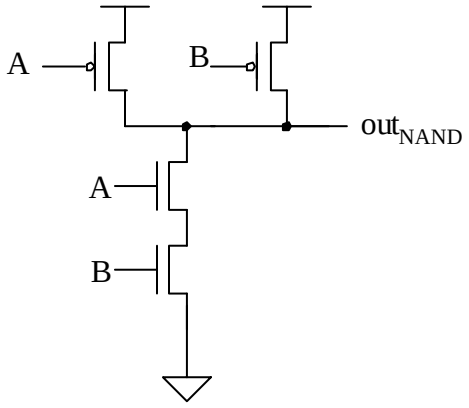
CHAPTER III. CMOS LOGIC

A. CMOS GATE STRUCTURE



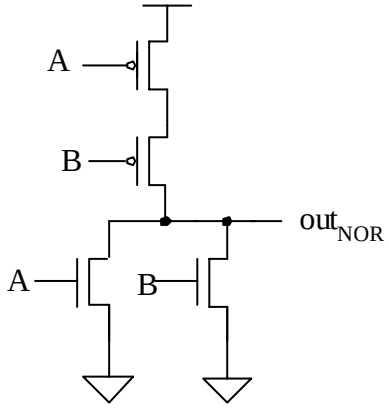
The nfet tree is formed between the output & ground to produce a logic function at the output. The pfet tree is formed between V_{DD} & output to replicate the complementary version of the nfet tree.
In a pfet tree, parallel nfet interconnects are converted into serial pfet interconnects and serial nfet interconnects are converted into parallel pfet interconnects.

(i) 2-Input NAND Gate



A	B	out_{NAND}	Comments
0	0	1	$pfet_A$ on, $pfet_B$ on
0	1	1	$pfet_A$ on only
1	0	1	$pfet_A$ on only
1	1	0	$nfet_A$ on, $nfet_B$ on

(ii) 2-Input NOR Gate

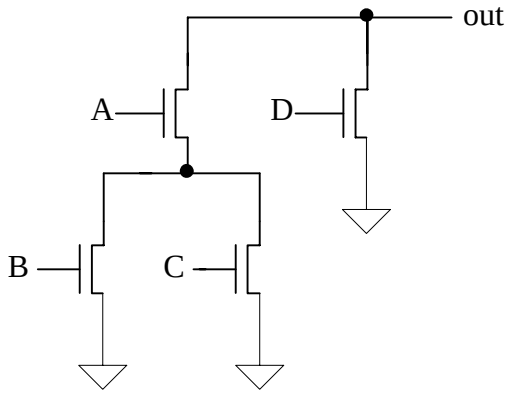


A	B	out_{NOR}	Comments
0	0	1	$pfet_A$ on, $pfet_B$ on
0	1	0	$nfet_A$ on only
1	0	0	$nfet_A$ on only
1	1	0	$nfet_A$ on, $nfet_B$ on

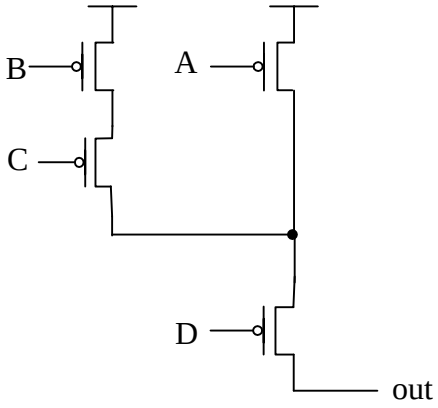
B. Building Complex Function Gates

Example: out= $\overline{D + A(B + C)}$

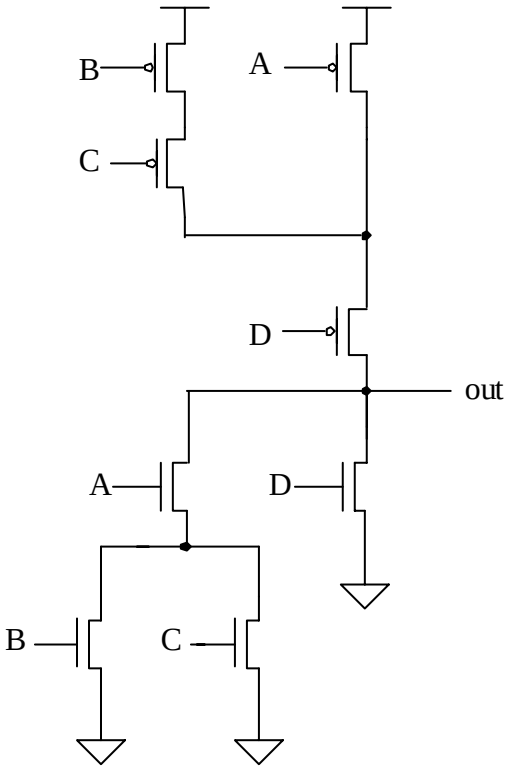
Form nfet tree first:



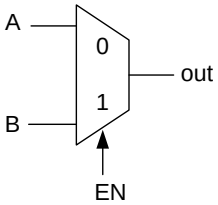
Form pfet tree second:



Combine nfet & pfet Trees

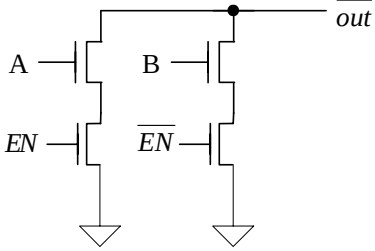


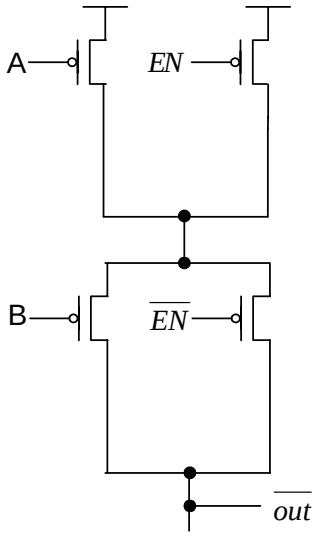
Example:



$$out = A.EN + B.\overline{EN}$$

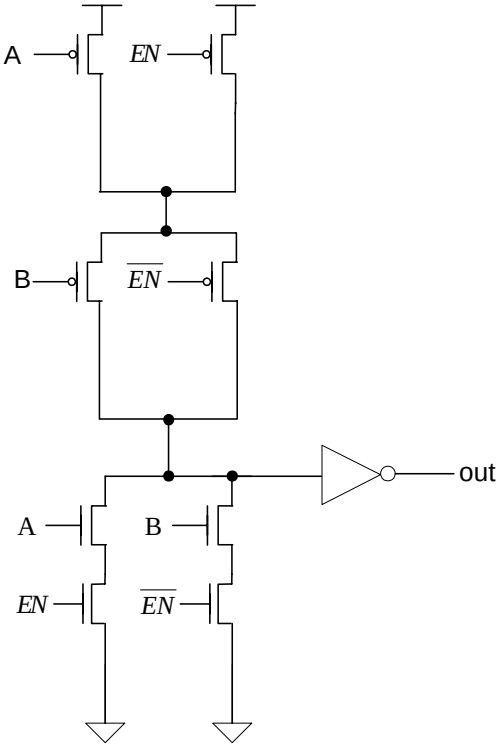
First obtain $\overline{out} = \overline{A.EN + B.\overline{EN}}$





nfet-tree pfet-tree

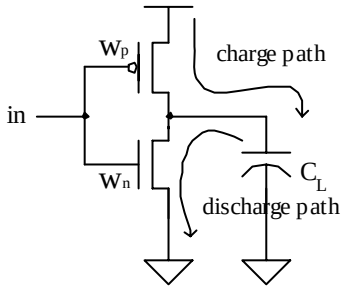
Now combine nfet tree, pfet tree &inverters to form out.



C. Fundamentals of Transistor Sizing

Transistor sizing is achieved by determining the maximum charge & discharge paths.

(i) Inverter



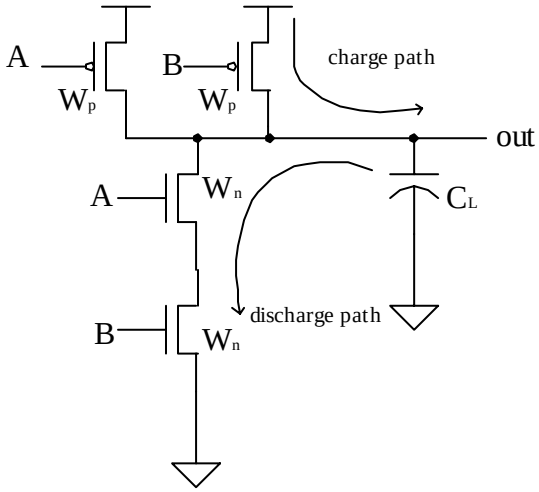
$$R_n = \frac{P}{2W_n} \quad \text{and} \quad R_p = \frac{P}{W_p}$$

$T_{PH} = 0.69\, R_p C_L$ (rise delay)

$T_{PL} = 0.69\, R_n C_L$ (fall delay)

If we want $T_{PH} = T_{PL}$ (relative)
Then,
$0.69\, R_p C_L = 0.69\, R_n C_L \Rightarrow R_p = R_n$
Or $W_p = 2W_n$

(ii) 2- Input NAND Gate



From critical charge path:

$T_{PH} = 0.69\, C_L R_{peq}$ (rise delay)

$T_{PL} = 0.69\, C_L R_{neq}$ (fall delay)

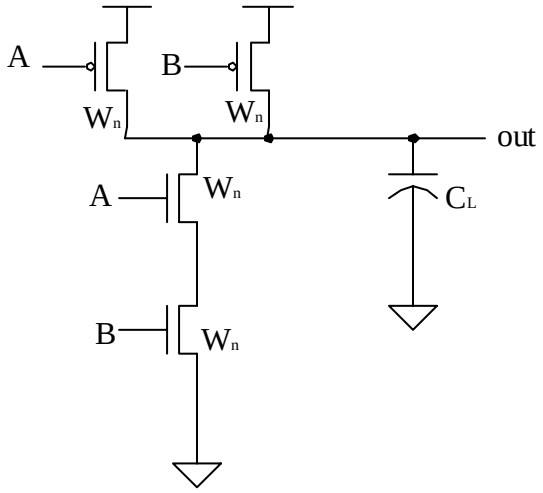
$$R_{peq} = R_p = \frac{P}{W_p}$$

$$R_{neq} = R_n + R_n = 2\frac{P}{2W_n} = \frac{P}{W_n}$$

(i) If we want $T_{PH} = T_{PL} \Rightarrow R_{peq} = R_{neq}$

$$\frac{P}{W_p} = \frac{P}{W_n} \Rightarrow W_p = W_n$$

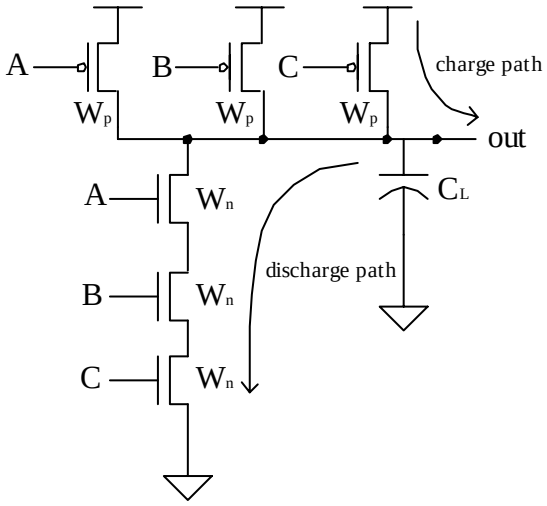
Thus:



(ii) If we want $T_{PH} = 2T_{PL} \Rightarrow R_{peq} = 2R_{neq}$

$$\frac{P}{W_p} = 2\frac{P}{W_n} \Rightarrow W_p = \frac{W_n}{2}$$

(iii) 3-Input NAND Gate



T_{PH} =0.69 C_L R_{peq} (rise delay)

T_{PL} =0.69 C_L R_{neq} (fall delay)

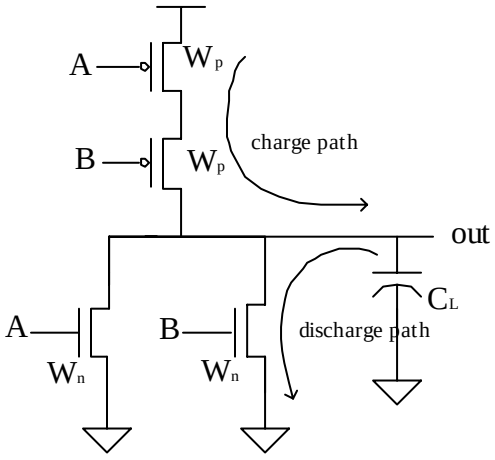
$$R_{peq} = R_p = \frac{P}{W_p}$$

$$R_{neq} = R_n + R_n + R_n = 3\frac{P}{2W_n}$$

Therefore, if we want $T_{PH} = T_{PL} \Rightarrow R_{peq} = R_{neq} \Rightarrow \frac{P}{W_p} = \frac{3}{2}\frac{P}{W_n}$

$$W_p = \frac{2}{3} W_n$$

(iv) 2- Input NOR Gate



$T_{PH} = 0.69\ C_L R_{peq}$ (rise delay)

$T_{PL} = 0.69\ C_L R_{neq}$ (fall delay)

$$R_{peq} = R_p + R_p = \frac{2P}{W_p}$$

$$R_{neq} = R_n = \frac{P}{2W_n}$$

$$T_{PH} = T_{PL} \Rightarrow \quad R_{peq} = R_{neq}$$

$$\frac{2P}{W_p} = \frac{P}{2W_n}$$

$$W_p = 4W_n$$

(v) $out = \overline{D + A(B + C)}$

$T_{PH} = 0.69\ C_L R_{peq}$ (rise delay)

$T_{PL} = 0.69\ C_L R_{neq}$ (fall delay)

$$R_{peq} = R_p + R_p + R_p = 3R_p = \frac{3P}{W_p}$$

$$R_{neq} = R_n + R_n = 2R_n = \cancel{2}\,\frac{P}{\cancel{2}W_n} = \frac{P}{W_n}$$

If we want $T_{PH} = T_{PL} \Rightarrow R_{peq} = R_{neq} \Rightarrow \frac{3\cancel{P}}{W_p} = \frac{\cancel{P}}{W_n}$

$$W_p = 3W_n$$

To find W_{p2}, W_{n2} and W_{n3} :

$$R_{p2} = 2R_p = 2\frac{P}{W_p} \Rightarrow \frac{P}{W_{p2}} = \frac{2P}{W_p}$$

$$W_{p2} = \frac{W_p}{2} = \frac{3}{2}W_n$$

$$R_{n2} = R_n \Rightarrow$$

$$W_{n2} = W_n$$

$$R_{n3} = R_n + R_n = \cancel{2}\,\frac{P}{\cancel{2}W_n} = \frac{P}{W_n} \Rightarrow \frac{P}{2W_{n3}} = \frac{P}{W_n}$$

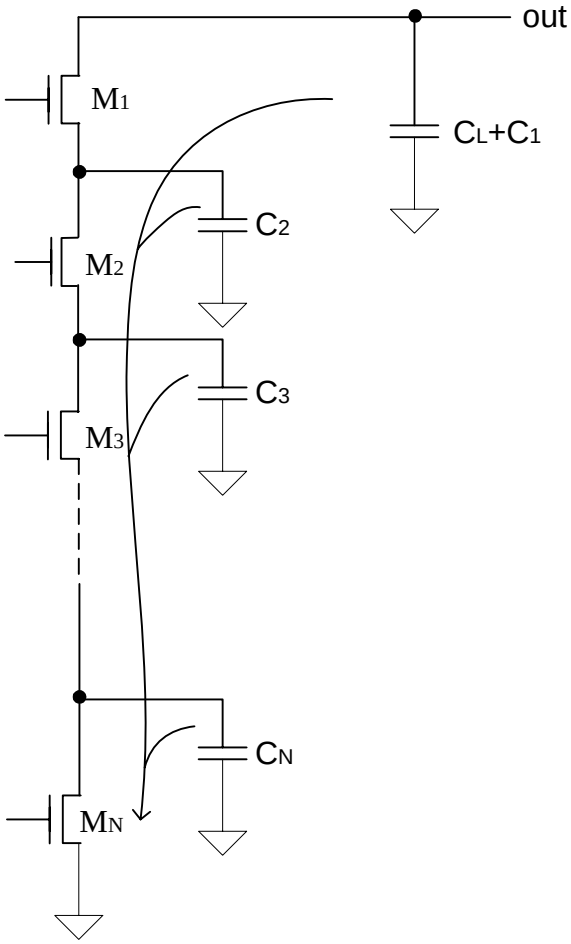
$$W_{n3} = \frac{W_n}{2}$$

Therefore, all the other charge and discharge paths will be equal to the critical charge and discharge paths, respectively.

D. MORE ACCURATE DELAY CALCULATION, ELMORE DELAY

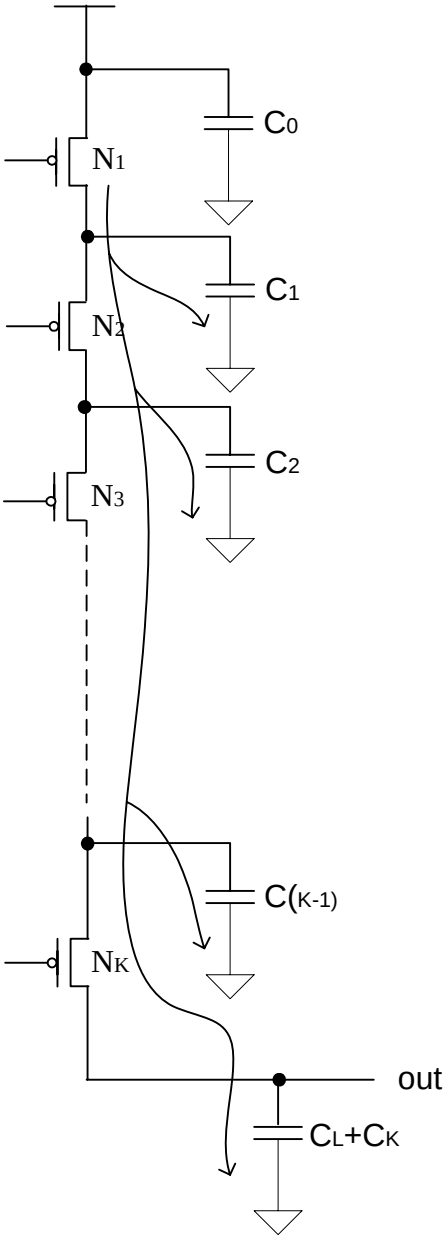
When we were calculating T_{pH} & T_{pF} earlier, we did not take the intrinsic source/drain capacitances in the delay calculation. Elmore delay calculation considers these intrinsic capacitances in the following manner:

nfet tree:



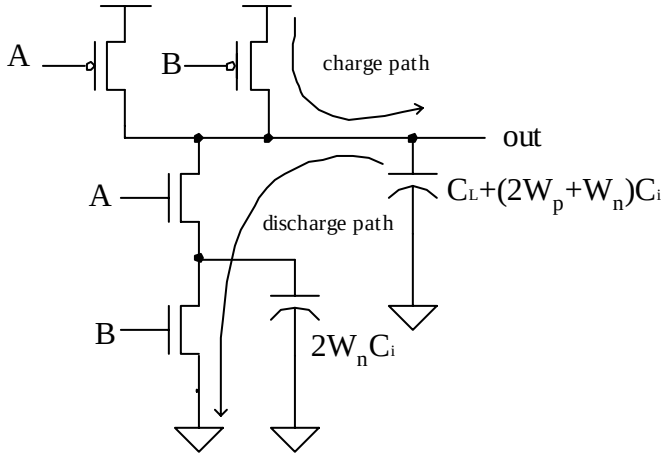
$$T_{pL} = 0.69\{(C_L + C_1)\left(R_{n1} + R_{n2} + R_{n3}..... + R_{nN}\right)$$
$$+C_2\left(R_{n2} + R_{n3} + R_{n4}..... + R_{nN}\right)$$
$$+C_3\left(R_{n3} + R_{n4} + R_{n5}..... + R_{nN}\right)$$
$$+.....$$
$$+C_N R_{nN}\}$$

pfet tree:



$$T_{pH} = 0.69\{0.C_0$$
$$+R_{p1}C_1$$
$$+\left(R_{p1}+R_{p2}\right)C_2$$
$$+\left(R_{p1}+R_{p2}+R_{p3}\right)C_3$$
$$+.....$$
$$+\left(R_{p1}+R_{p2}+.....+R_{pk}\right)(C_L+C_K)\}$$

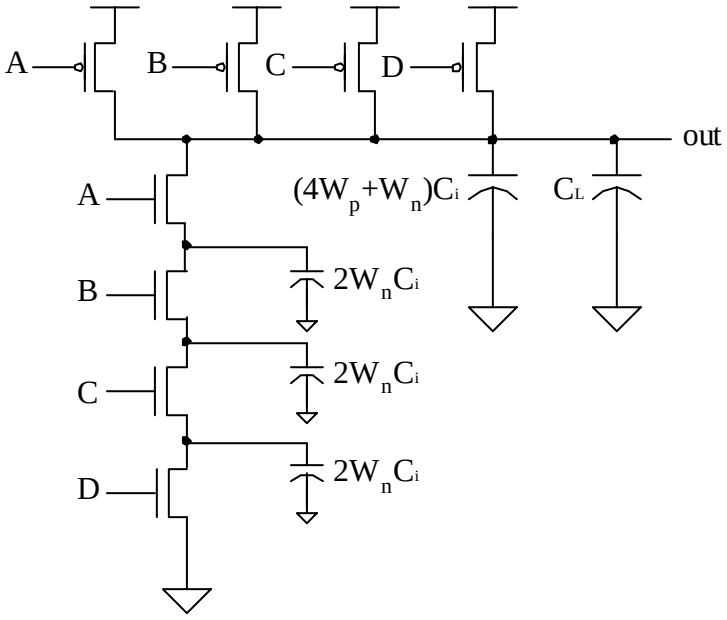
Example: Determine Elmore delays for 2 NAND with intrinsic S/D capacitance, C_i.
Let C_i be the capacitance per transistor width.
For practical purposes, each transistor has a separate C_i at its source and drain junctions.



$$T_{pH} = 0.69(C_L + C_i(2W_p + W_n))R_p$$

$$T_{pL} = 0.69\left[(C_L + C_i(2W_p + W_n))\left(R_n + R_n\right) + 2C_iW_nR_n\right]$$

Example: Determine Elmore delays for 4 NAND with intrinsic S/D cap=C_i



$$T_{pH} = 0.69(C_L + (4W_p + W_n)C_i)R_p$$

$$T_{pL} = 0.69\{(C_L + (4W_p + W_n)C_i)\left(R_n + R_n + R_n + R_n\right)$$
$$+2W_nC_i\left(R_n + R_n + R_n\right)$$
$$+2W_nC_i\left(R_n + R_n\right)$$
$$+2W_nC_iR_n\}$$

$$T_{pL} = 0.69R_n(C_L + 16(W_p + W_n)C_i)$$

If we want:

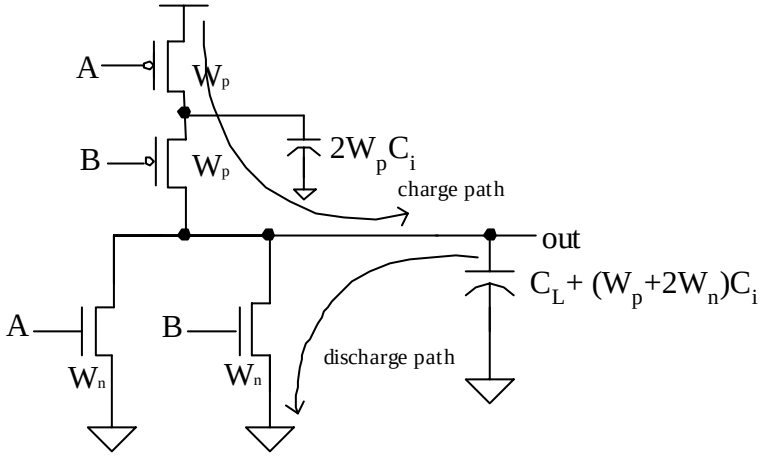
$$T_{pH} = T_{pL} \Rightarrow (C_L + (4W_p + W_n)C_i)R_p = (C_L + 16(W_p + W_n)C_i)R_n$$

$$R_p = \frac{P}{W_p},\ R_n = \frac{P}{2W_n} \text{ and } W_n = W$$

$$W_p = \frac{-(8WC_i + C_L) + \sqrt{(8WC_i + C_L)2 + 128WC_i(C_L + WC_i)}}{32C_i}$$

If $C_i \to 0 \quad \Rightarrow W_p = \frac{W_n}{2}$ as expected.

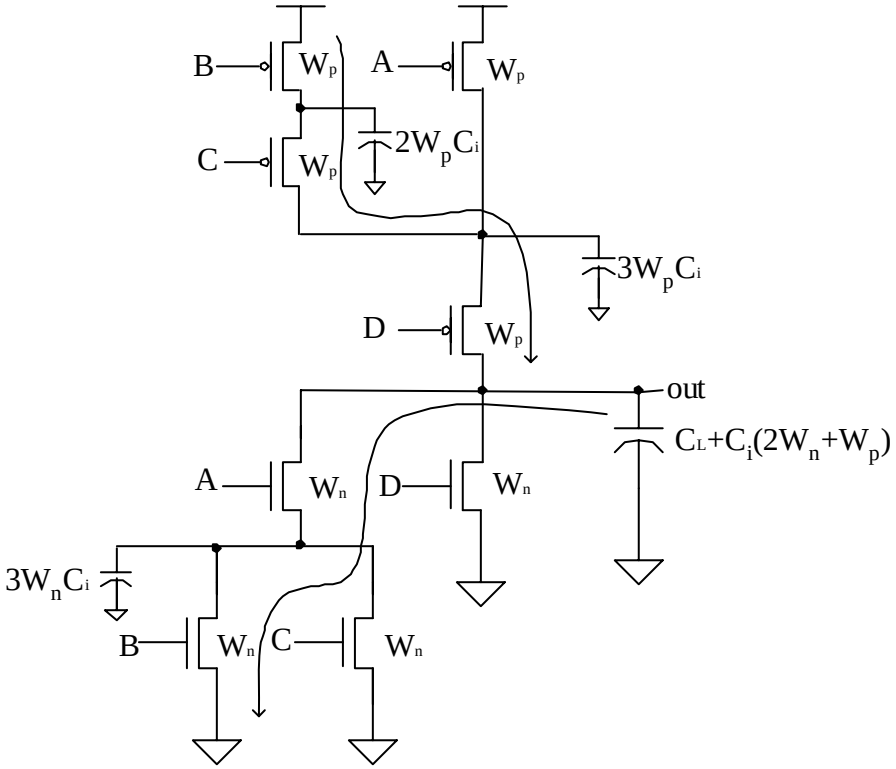
Example: Determine Elmore delays for 2 NOR with intrinsic S/D cap=C_i.



$$T_{pH} = 0.69\left[2R_pW_pC_i + \left(R_p + R_p\right)[C_L + (W_p + 2W_n)C_i]\right]$$

$$T_{pL} = 0.69[C_L + (W_p + 2W_n)C_i]R_n$$

Example: Determine Elmore delays for Out = $\overline{D + A(B + C)}$

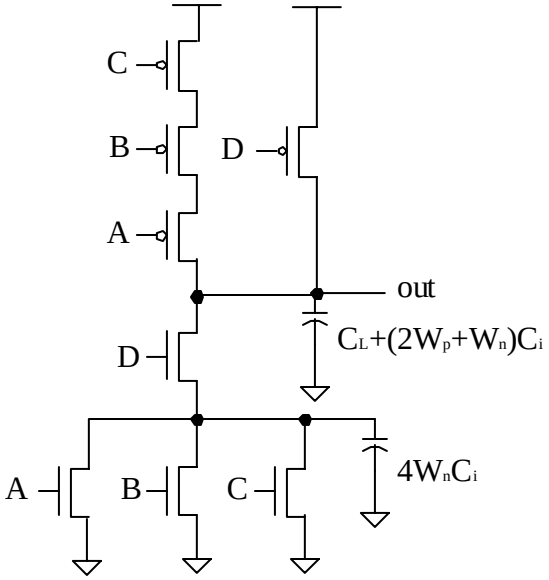


$$T_{pH} = 0.69\left[2R_pW_pC_i + 3(R_p + R_p)W_pC_i + (R_p + R_p + R_p)(C_L + C_i(2W_n + W_p))\right]$$

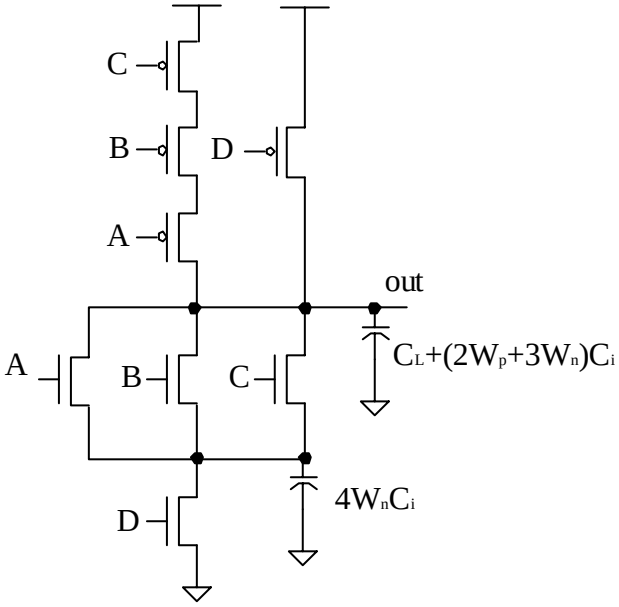
$$T_{pL} = 0.69\left[(R_n + R_n)(C_L + C_i(2W_n + W_p)) + 3R_nW_nC_i\right]$$

E. INTERCONNECT DESIGN STRATEGIES TO REDUCE ELMORE DELAYS

Consider $out = \overline{(A+B+C)D}$. There are 2 ways to implement this:



Implementation #1



Implementation #2

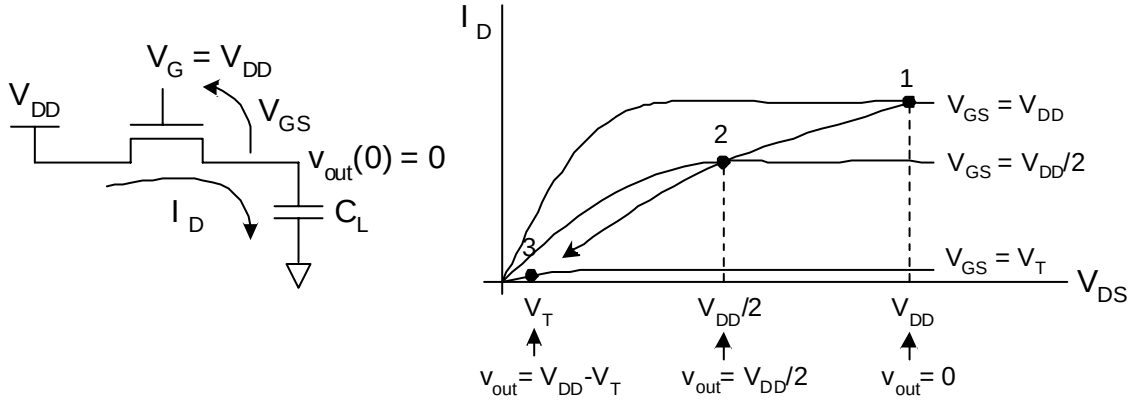
$$T_{PL1} = 0.69\left\{[C_L + (2W_p + W_n)C_i](R_n + R_n) + 4W_nC_iR_n\right\}$$
$$T_{PL2} = 0.69\left\{[C_L + (2W_p + 3W_n)C_i](R_n + R_n) + 4W_nC_iR_n\right\}$$

Therefore, $T_{PL1} < T_{PL2}$. Therefore, choose the implementation #1

CHAPTER IV. PASS-TRANSISTOR LOGIC

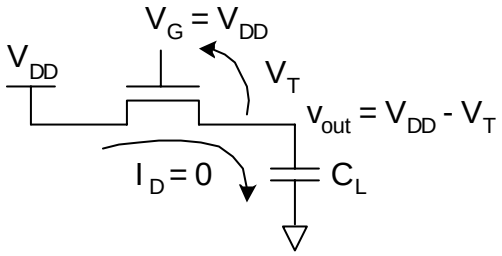
A. ISSUES WITH PASS TRANSISTOR LOGIC

(i) Problem with nfet

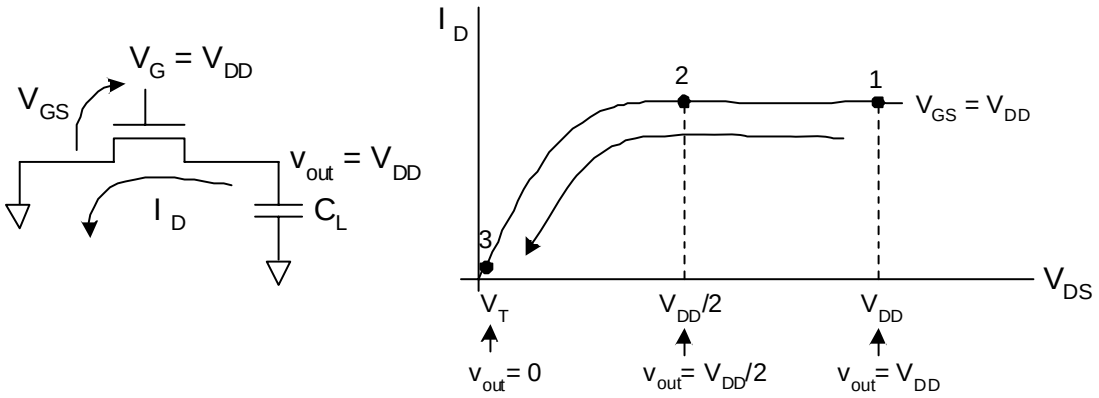


When $V_G = V_{DD}$ and $V_D = V_{DD}$ are applied to the nfet in the above circuit, the initial voltage across the load capacitor, C_L, is zero. Therefore, initially $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}$. This condition induces a maximum current through the nfet (case 1). As this current charges the output capacitor, C_L, and the output voltage rises, the current through the nfet declines steadily (case 2). When $v_{out} = V_{DD} - V_T$, the current through the nfet reaches sub-threshold level, which is practically zero (case 3).
Therefore, a logic 1 is applied to the drain (input) of an nfet, one can never reach the full V_{DD} at the source (output); the maximum attainable value is always $V_{DD} - V_T$.

Final form:

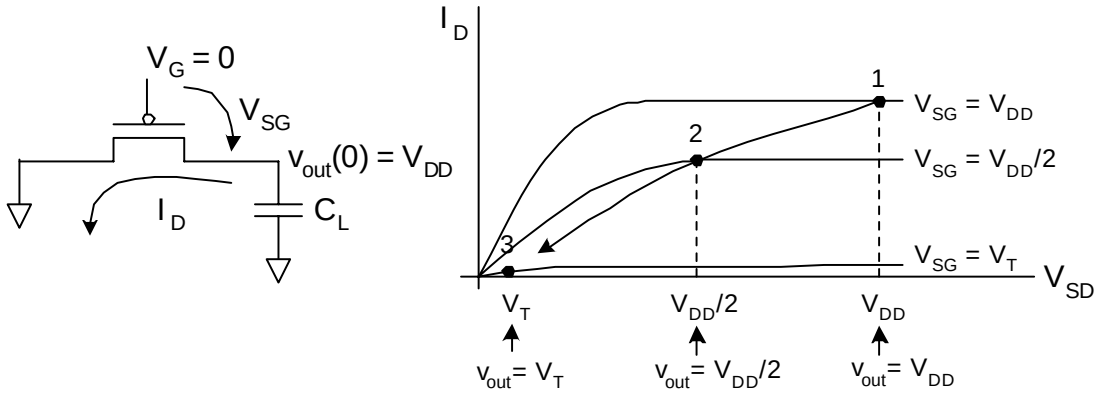


Any problem if we apply ground instead of V_{DD}?



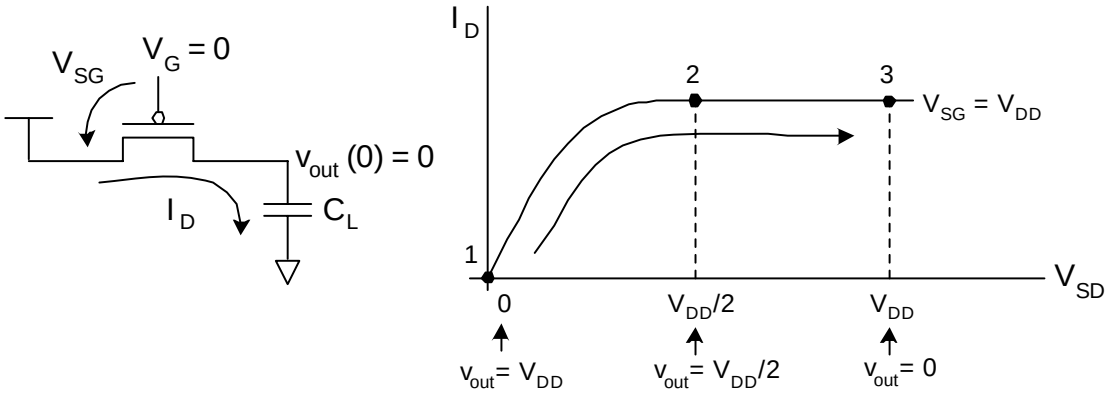
With the above bias across the nfet, output capacitor is discharged completely, and v_{out} reaches 0 since $V_{GS} = V_{DD}$ at all times. Therefore, if a logic 0 is applied to the source (input) of an nfet, a logic zero is obtained at the drain (output).

(B) Problem with pfet



When $V_G = 0$ and $v_{out}(0) = V_{DD}$ are applied to the pfet in the above circuit, the initial $V_{SG} = V_{DD}$ and $V_{SD} = V_{DD}$. This condition induces a maximum current through the pfet (case 1). As this current discharges the output capacitor, C_L, and the output voltage decreases, the current through the nfet declines steadily (case 2). When $v_{out} = V_T$, the current through the pfet reaches sub-threshold level, which is practically zero (case 3). Therefore, a logic 0 is applied to the drain (input) of a pfet, one can never reach 0 at the source (output); the minimum attainable value is always V_T.

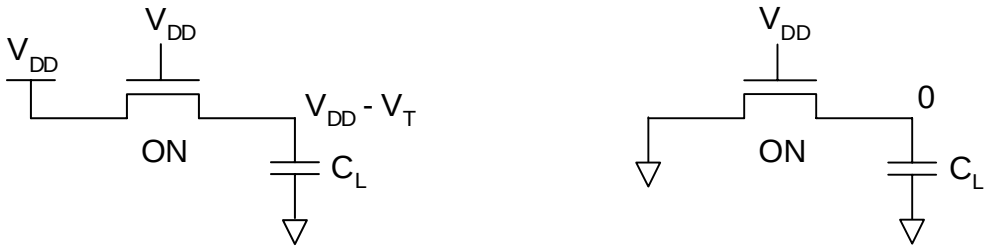
Any problem if we apply V_{DD} instead of 0 ?



With the above bias across the pfet, output capacitor gets charged completely, and v_{out} reaches V_{DD} since $V_{SG} = V_{DD}$ at all times. Therefore, if a logic 1 is applied to the source (input) of a pfet, a logic 1 is obtained at the drain (output).

CONCLUSIONS:

(1)



result: nfet transmits logic 0 OK when it is ON.

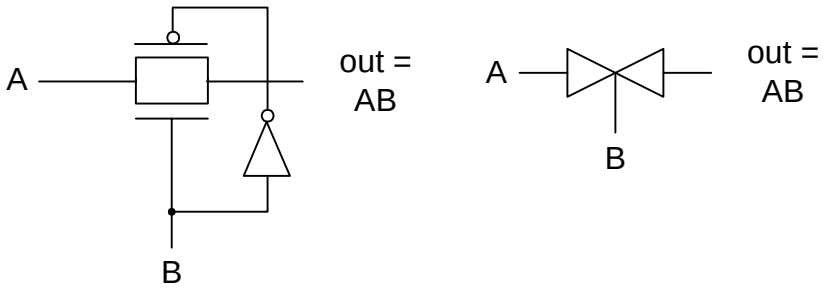
(2)

result: pfet transmits logic 1 OK when it is ON.

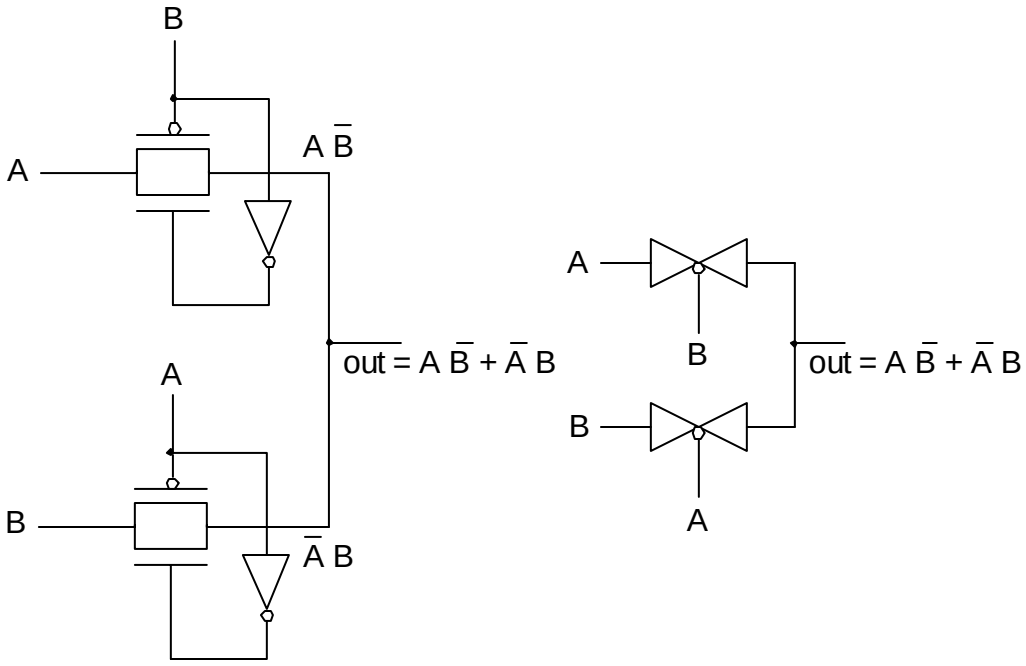
Because of the level shifting problem in nfet and pfet for V_{DD} and 0, respectively, transmission gate is developed.

B. TRANSMISSION GATES

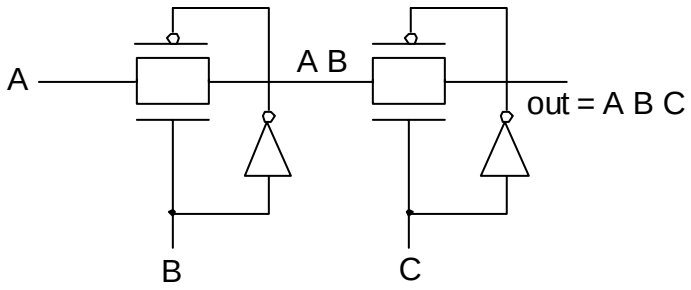
The transmission gate is the parallel combination of nfet and pfet with an inverter.



Example: $out = A \oplus B = A\overline{B} + \overline{A}B$

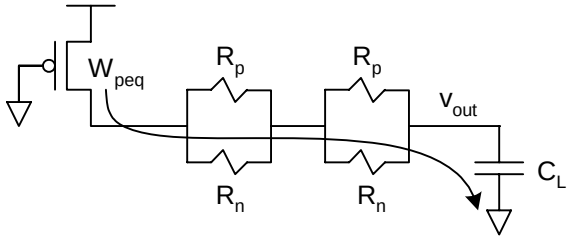


What about $out = ABC$?



Even though one gets a functionally correct output, one of the biggest drawbacks of serial transmission gate is that it generates a “slow node” at the output due to high series resistance. The charge path:

The change path:



Where,

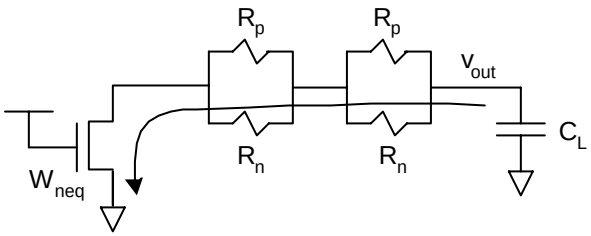
$$R_p = \frac{P}{W_p}$$

$$R_n = \frac{P}{2W_n}$$

$$\frac{R_n R_p}{R_n + R_p} = \frac{P}{W_p + 2W_n}$$

$$T_{RISEslow} = 2.2C_L(R_{peq} + 2\frac{R_p R_n}{R_p + R_n}) = 2.2C_L P(\frac{1}{W_{peq}} + \frac{2}{W_p + 2W_n})$$

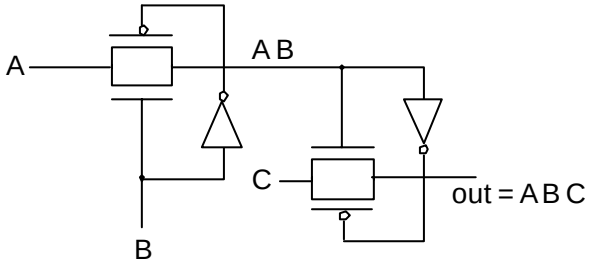
The discharge path:

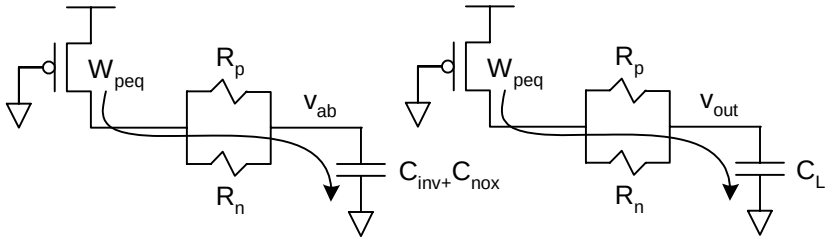


$$T_{FALLslow} = 2.2C_L P(\frac{1}{2W_{neq}} + \frac{2}{W_p + 2W_n})$$

Therefore, more serial transmission gate induces more $\frac{1}{W_p + 2W_n}$ - term, which results in generating slower output node at v_{out}.

To prevent the slow node formation signals need to be buffered by going to the gate of the next transistor rather than its drain (or source):





$$T_{RISEab} = 2.2P(C_{inv} + C_{nox})(\frac{1}{W_{peq}} + \frac{1}{W_p + 2W_n}) < T_{RISEslow}$$

$$T_{RISEout} = 2.2P(C_{inv} + C_{nox})(\frac{1}{W_{peq}} + \frac{1}{W_p + 2W_n}) < T_{RISEslow}$$

Similarly,

$$T_{FALLab} = 2.2C_L P(\frac{1}{2W_{neq}} + \frac{1}{W_p + 2W_n}) < T_{FALLslow}$$

$$T_{FALLout} = 2.2C_L P(\frac{1}{2W_{neq}} + \frac{1}{W_p + 2W_n}) < T_{FALLslow}$$

Example: Full adder design using transmission gates

$$Sum = A \oplus B \oplus C_{in} = \overline{\overline{A \oplus B \oplus C_{in}}} = \overline{\overline{(A \oplus B)}\,\overline{C_{in}} + (A \oplus B)C_{in}}$$

Thus,

$$Sum = \overline{(AB + \overline{A}\,\overline{B})\,\overline{C_{in}} + (A\overline{B} + \overline{A}B)C_{in}}$$

$$C_{out} = AB + C_{in}(A \oplus B) = AB + C_{in}(A\overline{B} + \overline{A}B)$$