Dr. Almet BINDAL

$$\frac{VoD = IV}{Vout}$$

$$\frac{VoD}{Vout}$$

$$\frac{VoD}{Vout}$$

$$\frac{Vout}{Vout}$$

Mp=100 cm²/Jec Cox=6.9x10⁷ F/cm VTp=0.2V

At t=0 Vout=0V > plot Vout(t) according to the transistor parameters above. How long does it take for Vout to reach 1V? Show your calculations clearly.

60 pts (a) Implement the circuit without using an output invoter.

(b) Assume $T_R = \frac{T_F}{2} \Rightarrow size the transistors according to a minimum geometry of 1 m.$

NOTE = Implement 4 so that you get minimal vise and fall times.

$$Mp = 100 \text{ cm}^2 / \text{sce}$$

$$Cox = \frac{60x}{tox} = \frac{3.9 \times 8.85 \times 10^{-14}}{50 \times 10^{-8}} = 6.9 \times 10^{-7} \text{ F/cm}^2$$

(a)
$$Y = A(B+CD) \Rightarrow \overline{Y} = \overline{A} + \overline{(B+CD)}$$

= $\overline{A} + \overline{B} \cdot (\overline{C} + \overline{D})$

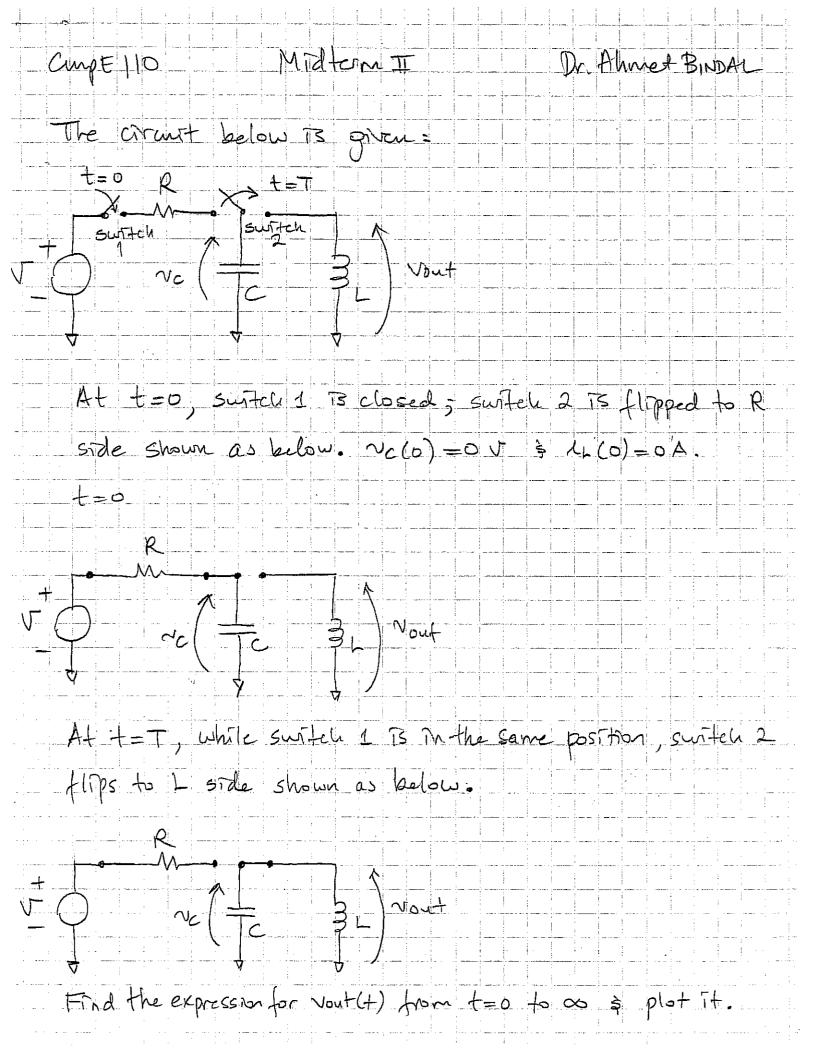
$$\frac{1}{2} \frac{1}{2} \frac{1}$$

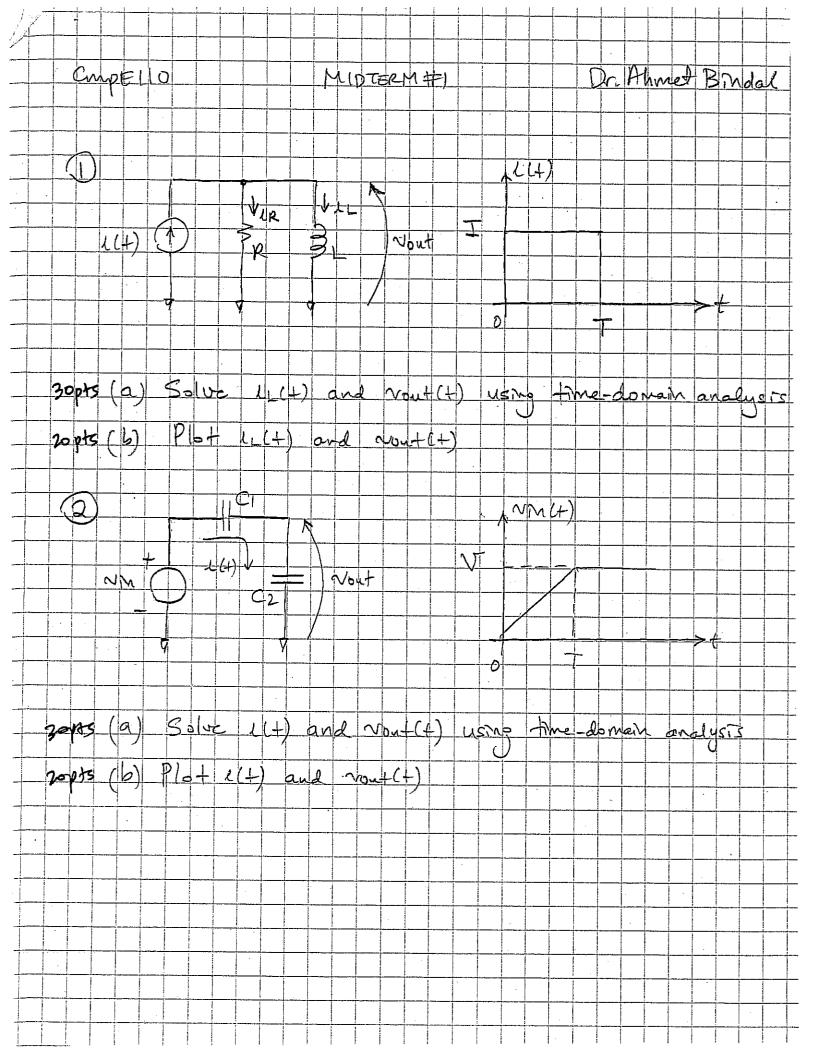
TF = 2,2 Rpeq CL = 2,2 CL
$$2R_N = 2.2$$
 CL $2\frac{p}{2W_N}$

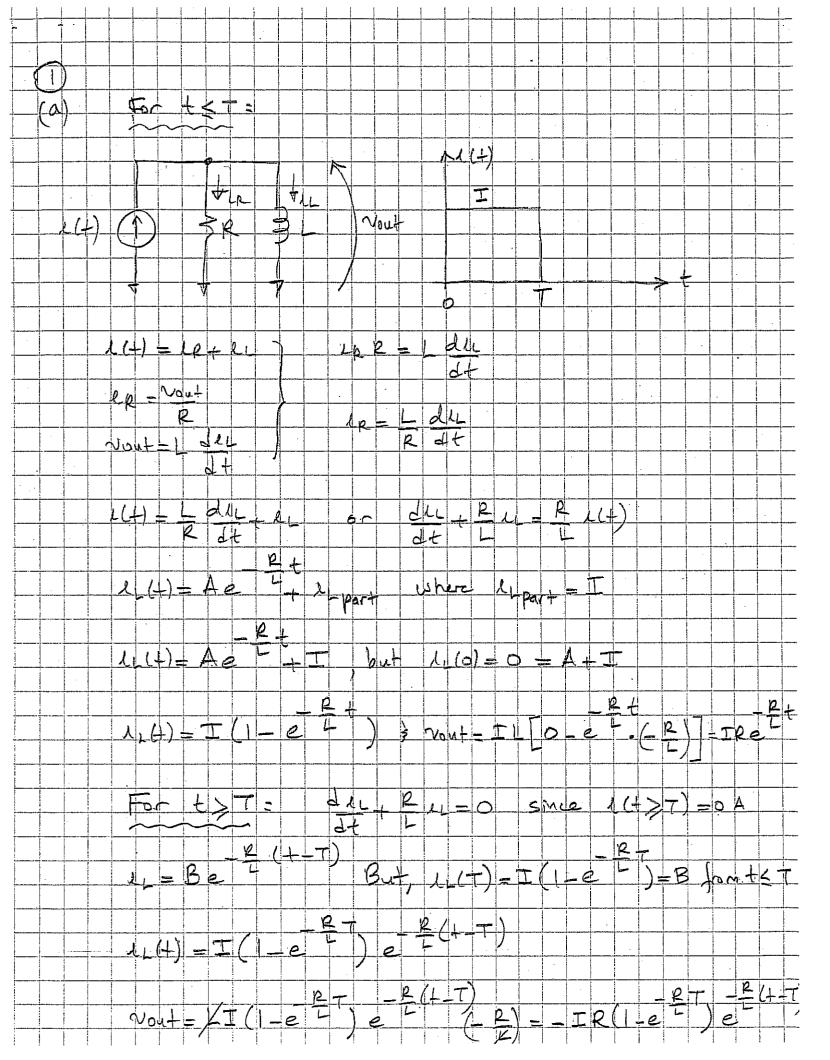
TR = 2,2 Rpeq CL = 2,2 CL $3R_P = 2.2$ CL $3\frac{p}{W_P}$

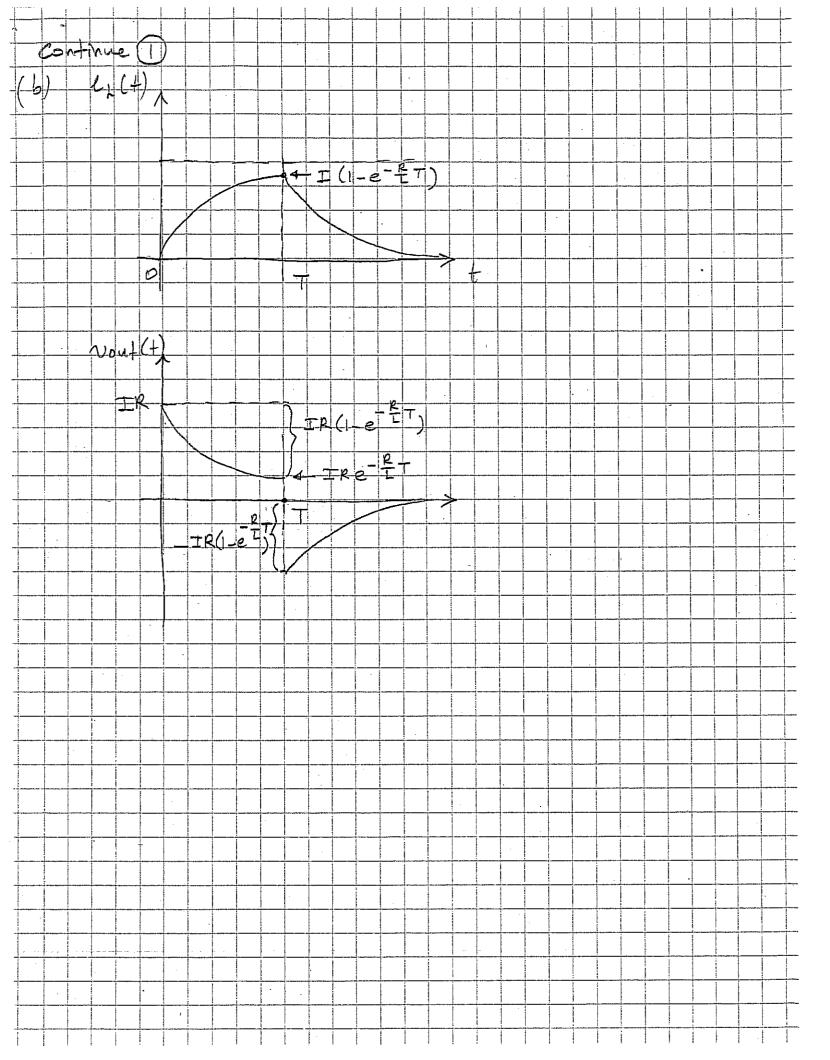
TR = $\frac{T_F}{2} \Rightarrow \frac{3}{W_P} = \frac{1}{2} \cdot \frac{1}{W_N} \Rightarrow \frac{W_P = 6W_N}{2}$

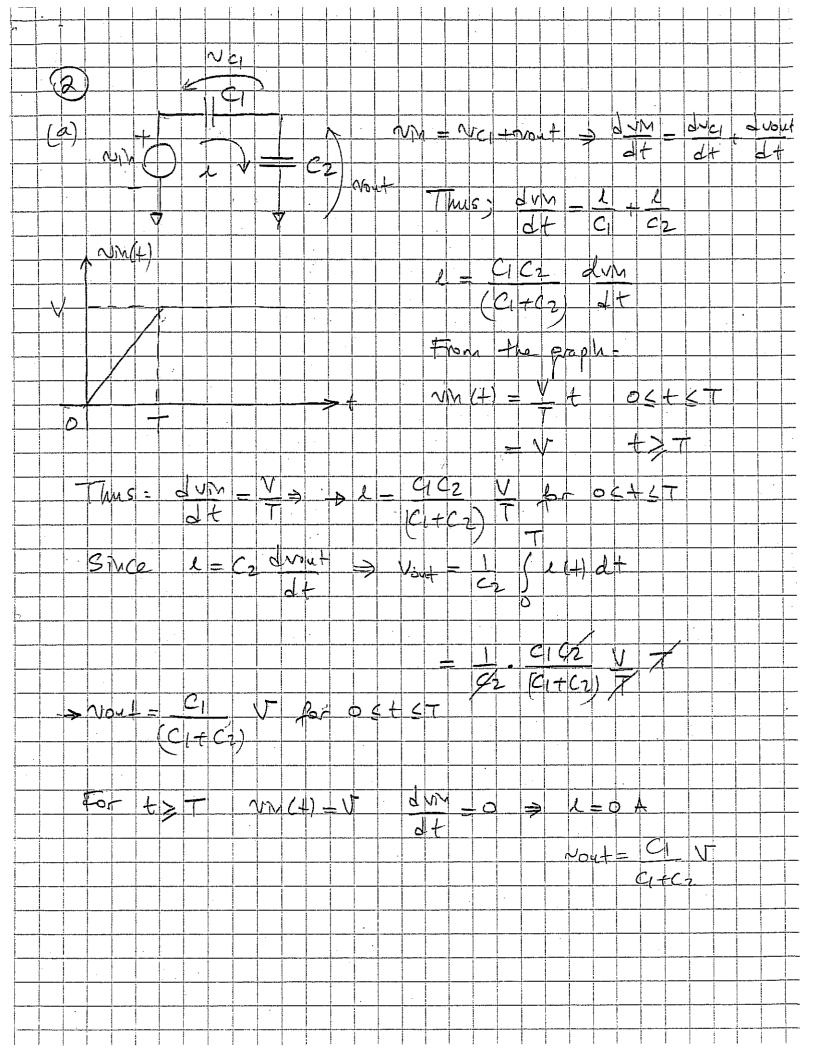
Minimum geometry To $1 \mu = \frac{1}{2} \mu$
 $\frac{W_P}{W_P} = \frac{1}{2} \mu$

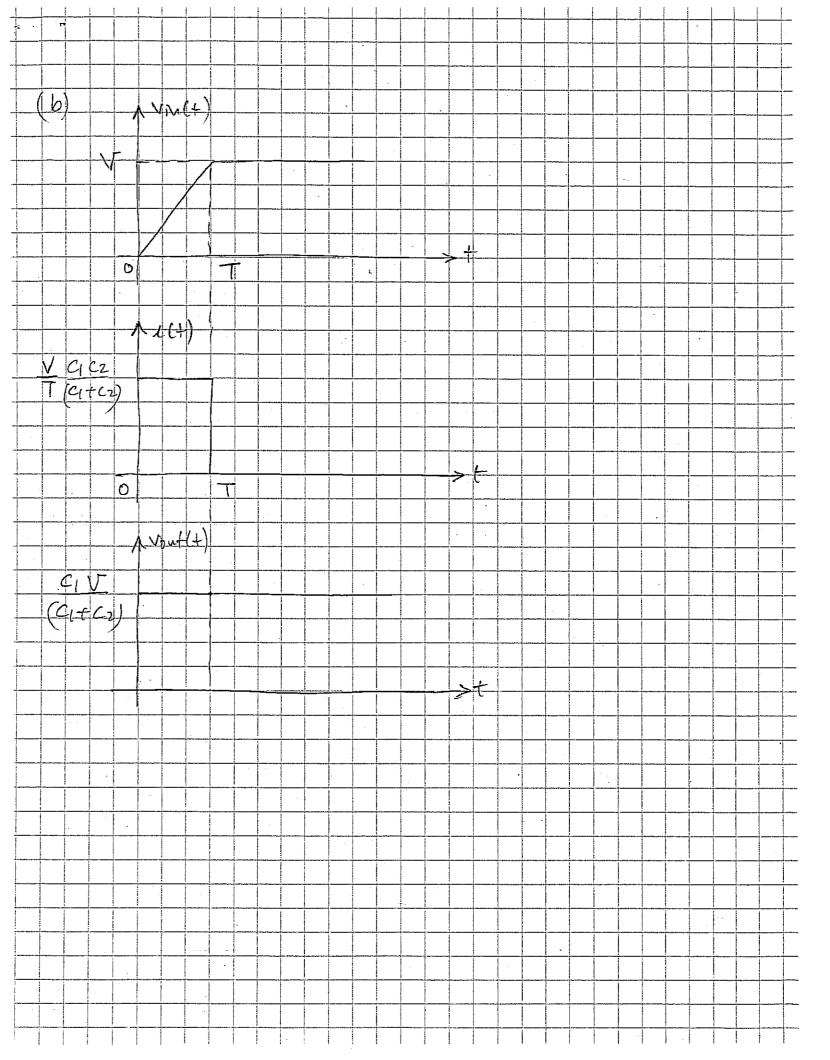


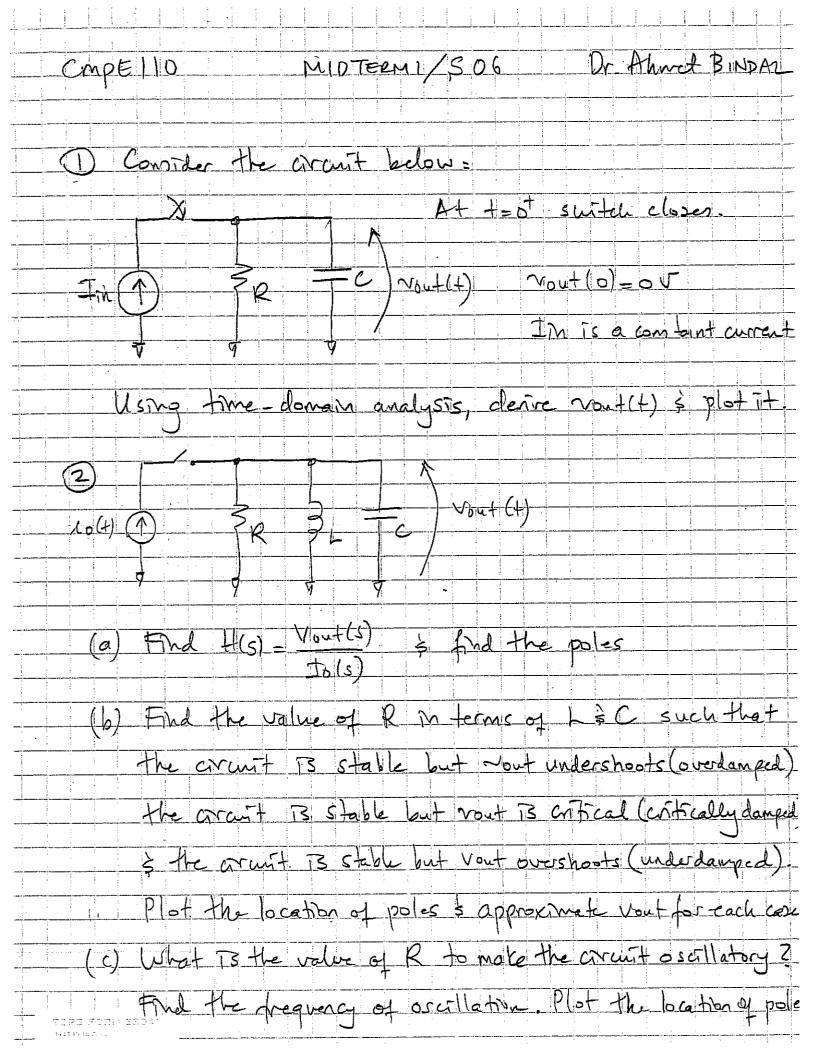


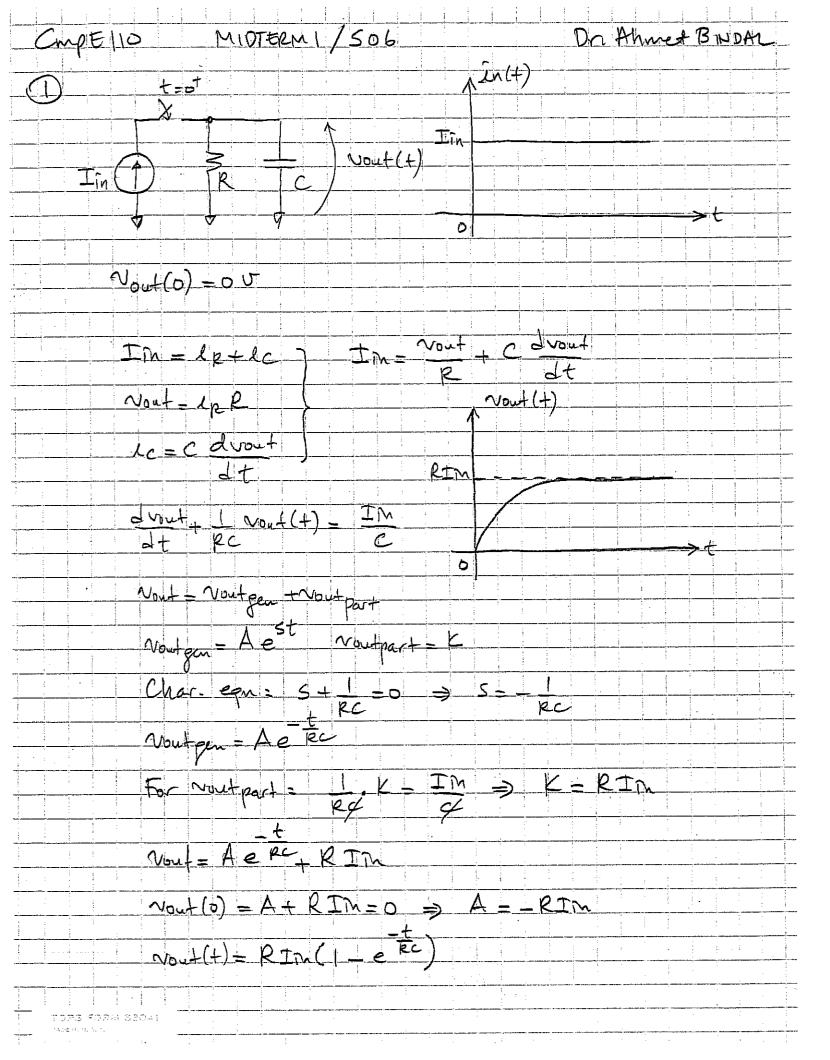


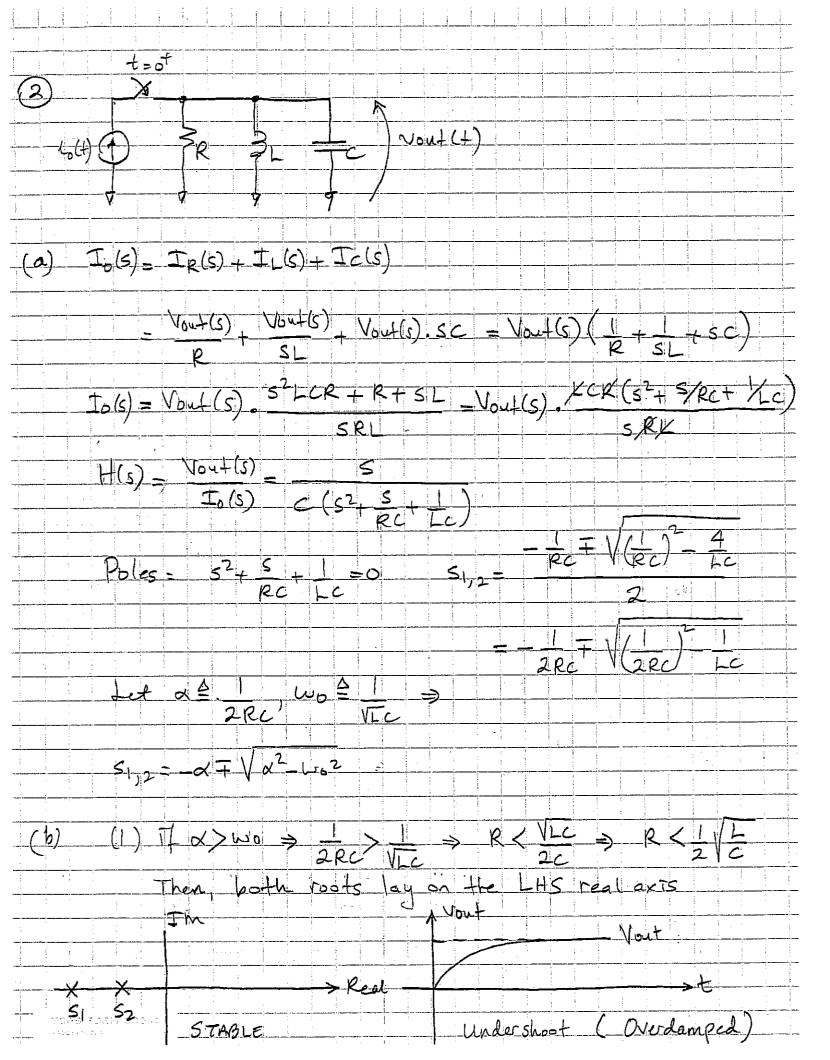


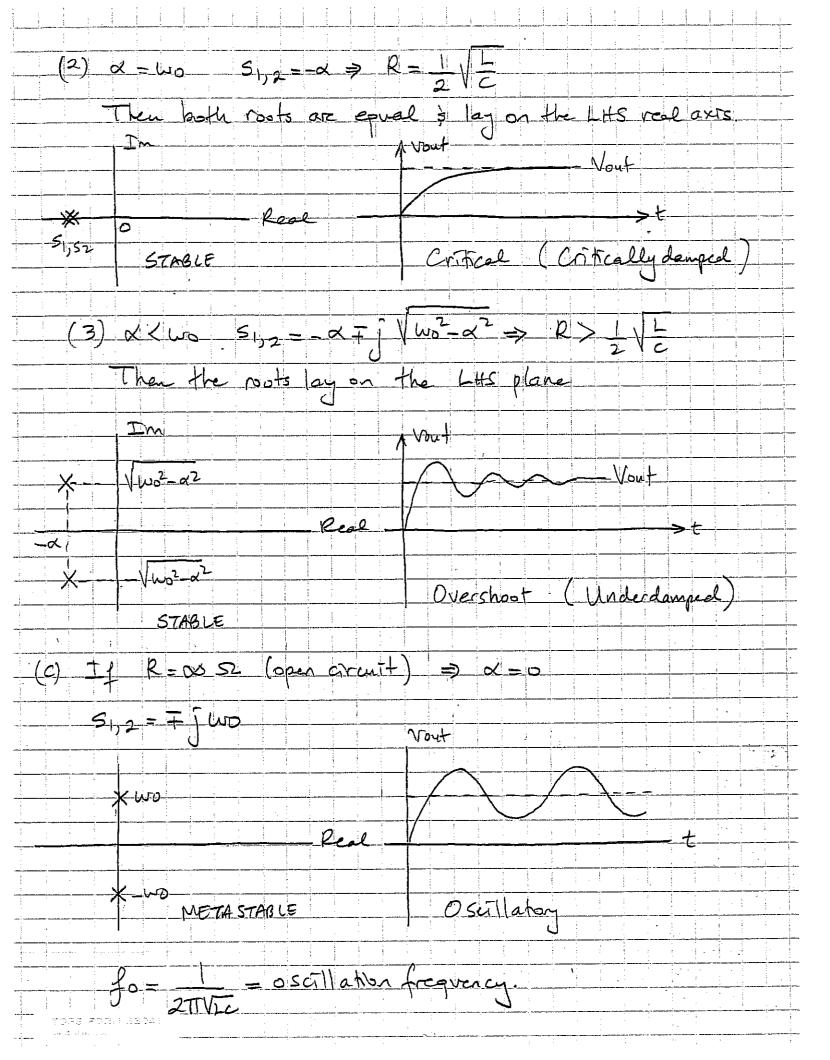












CmpE 110

Design the following logic function and size the transistors such that $T_R = 2 \ T_F$.

$$f = \overline{A}.B + C$$

NOTE:

Do NOT consider Elmore delay components.

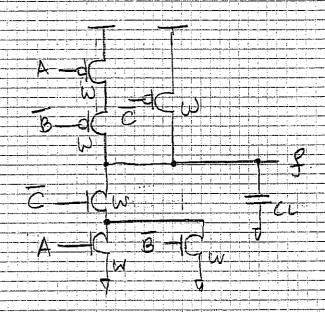
Do NOT use any inverters at the output.

Solutions

Since we are not allowed to use any involve at the output we need to find out I.

$$f = A.B+C$$

$$=(A+\overline{B}).\overline{C}$$



$$T_{F} = 2.2 C_{L} R_{neg} = 2.2 C_{L} (P_{r} + P_{n})$$

$$= 2.2 C_{L} (2 R_{n})$$

$$= 2.2 C_{L} R_{peq} = 2.2 C_{L} (R_{p} + R_{p})$$

$$= 2.2 C_{L} (2 P_{p})$$

$$= 2.2 C_{L} (2 P_{p})$$

$$2 T_{F} = T_{e} \Rightarrow 2 R_{n} = R_{p}$$

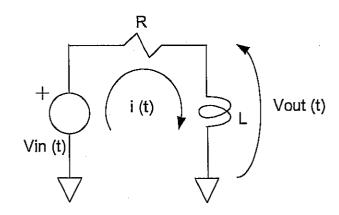
$$R_{n} = K R_{p} = K$$

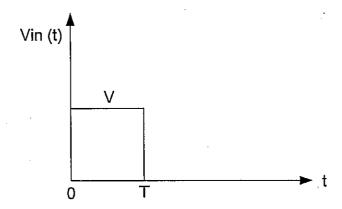
$$2 W_{n} = W_{p} = K$$

$$W_{p} = W_{p} = W_{p}$$

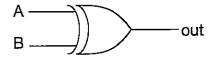
tre=wn=ut

1.

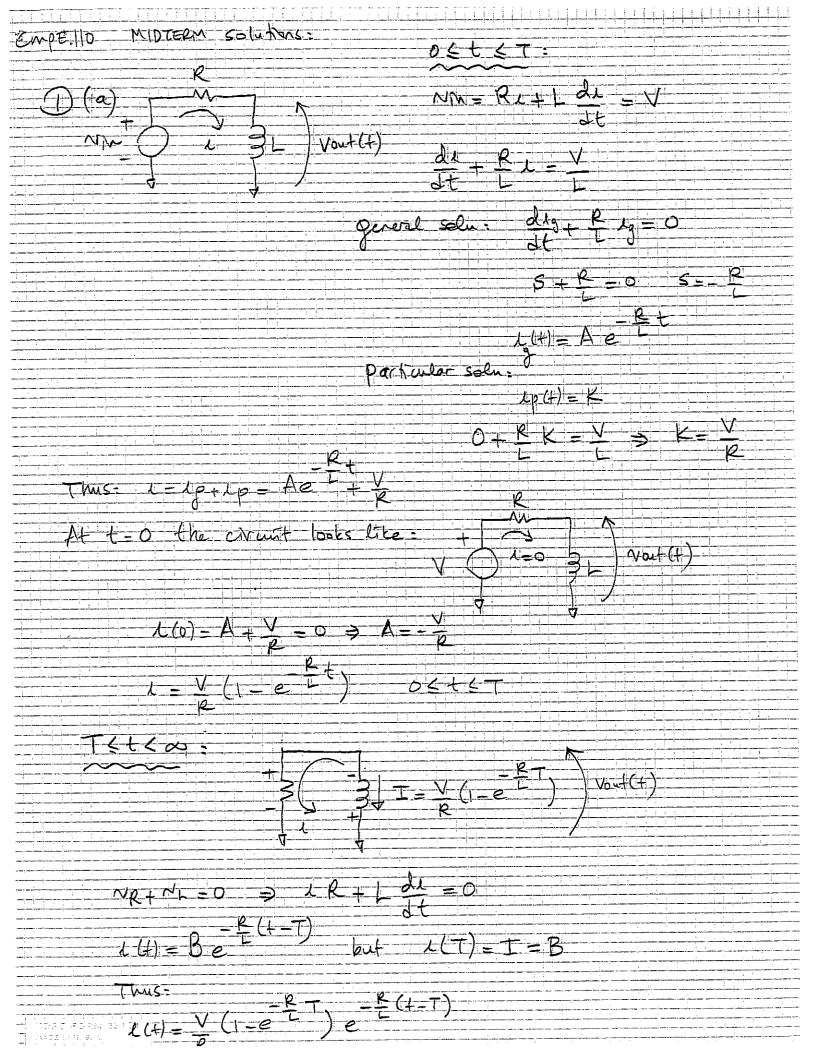




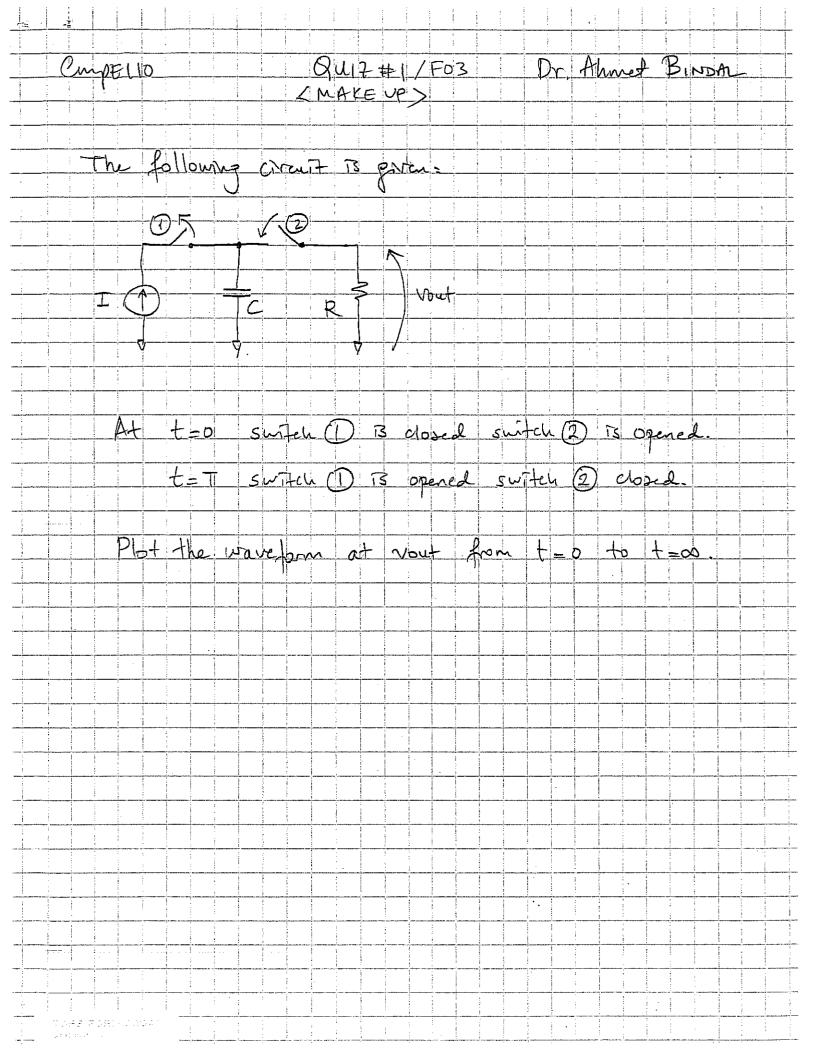
- (a) If Vin(t) is given above, find i(t) using time-domain analysis. Note that i(0) = 0 in the inductor.
- (b) Compute Vout(t) using time-domain analysis.

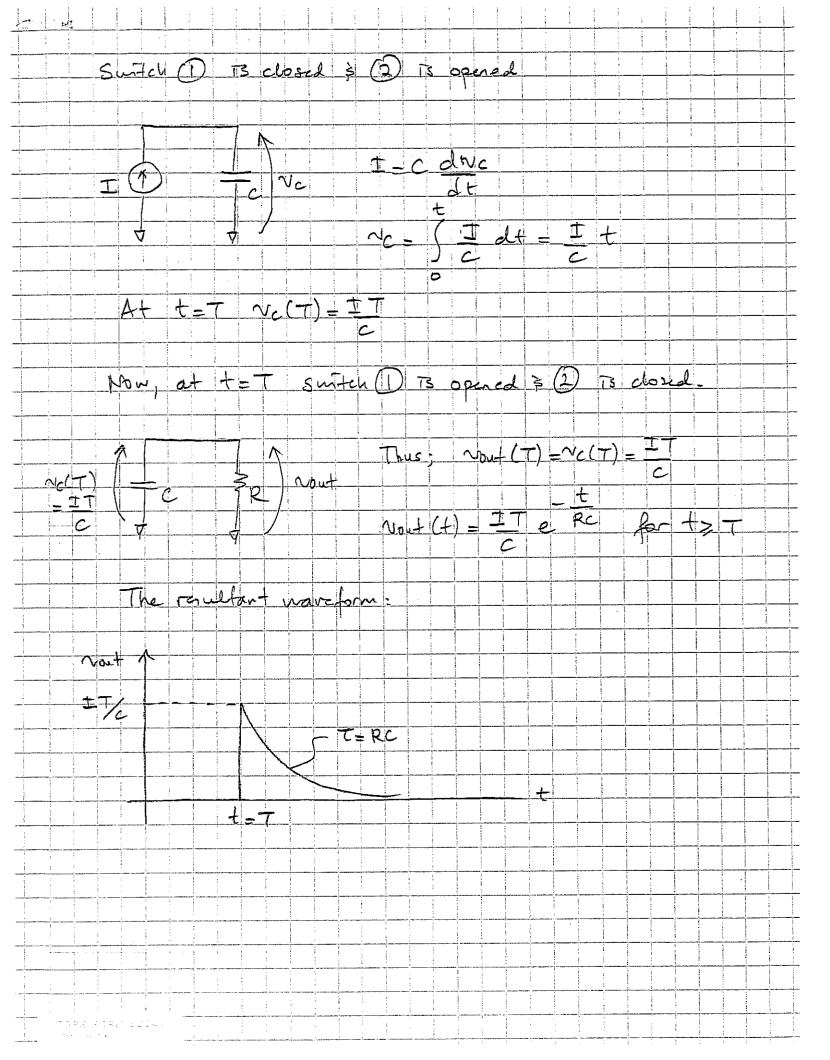


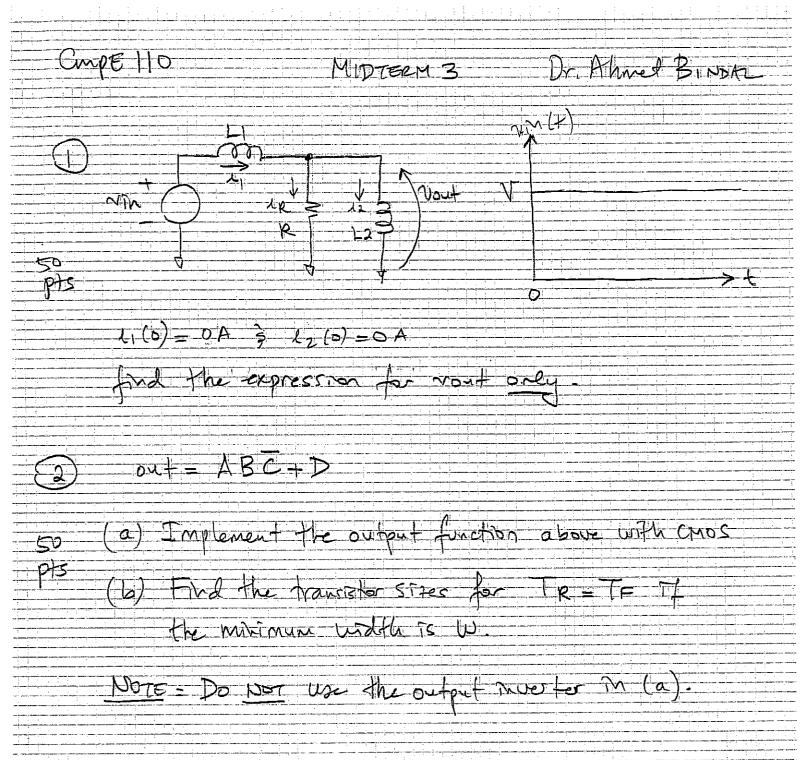
- (a) Write output function of this gate in terms of its inputs, A and B (Form a minterm function).
- (b) Implement the above gate with CMOS circuitry.



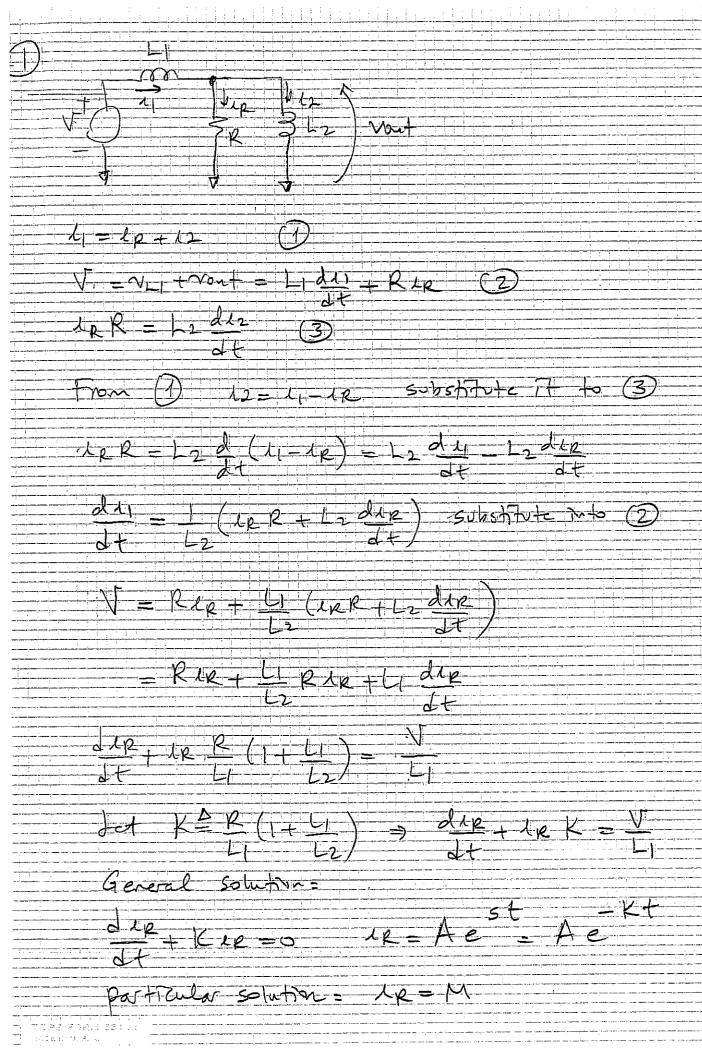
(b)
$$N_{OH} = 1$$
 $\frac{d\lambda}{dt} = 1$ $\frac{1}{2}$ \frac







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(a)

$$A = C + D = A + B + C + D$$

(a)

 $A = C + D = A + B + C + D$
 $A = C + D = A + B + C + D$

(b)

 $A = C + D = A + B + C + D$
 $A = C + D = A + B + C + D$

(b)

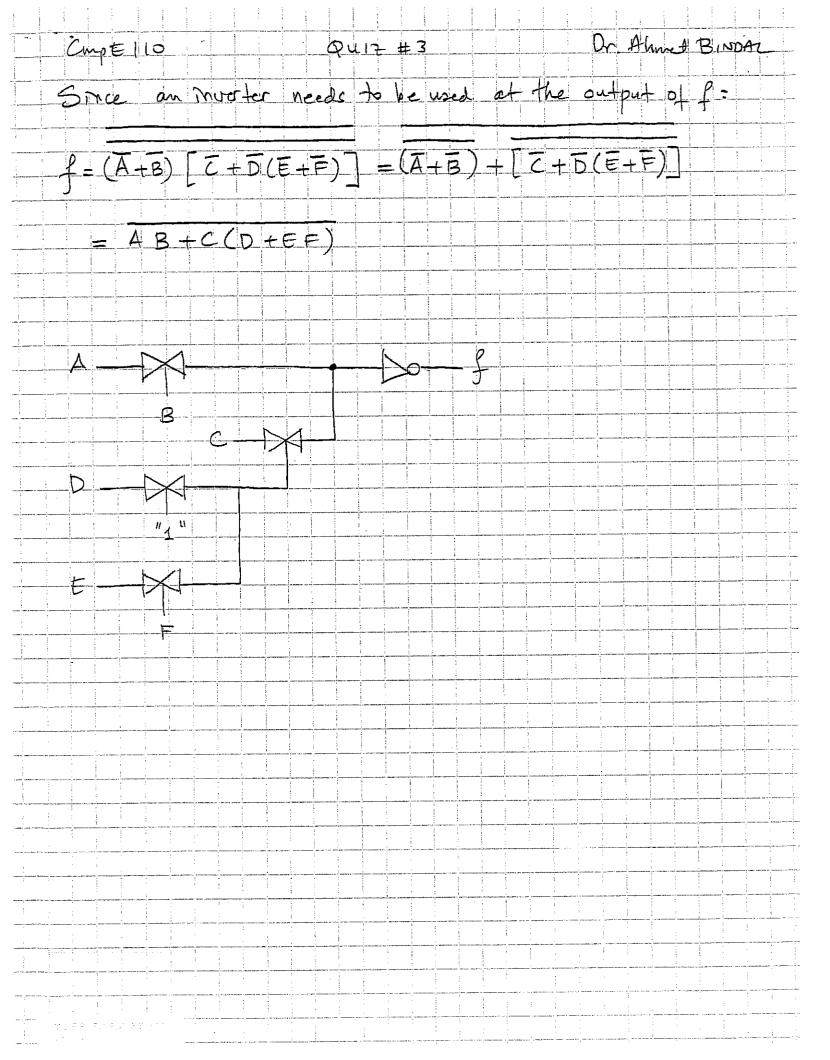
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 $A = C + D = A + C + D = A + C + D = A + C + D$
 $A = C + D = A + D = A + C + D$

The following function is given:

$$f = \overline{A} + \overline{B} [\overline{C} + \overline{D} (\overline{E} + \overline{F})]$$

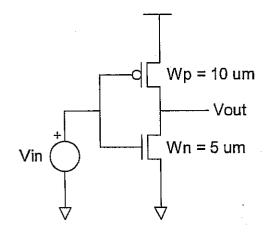
This circuit needs to drive a large fan-out composed of a large capacitor, therefore, an inverter needs to be added to its output.

Implement the function, f, with minimum number of elements using transmission gate logic.



An inverter below is given.

$$\begin{split} V_{DD} &= 3 \text{ V} \\ V_{TN} &= V_{TP} = 0.6 \text{ V} \\ \text{Mobility for electrons } (u_n) = 1200 \text{ cm}^2/\text{Vsec} \\ \text{Mobility for holes } (u_p) = 600 \text{ cm}^2/\text{Vsec} \\ C_{OX} &= 6.9 \text{ x } 10^{-7} \text{ F/cm}^2 \\ L &= 0.25 \text{ um} \end{split}$$

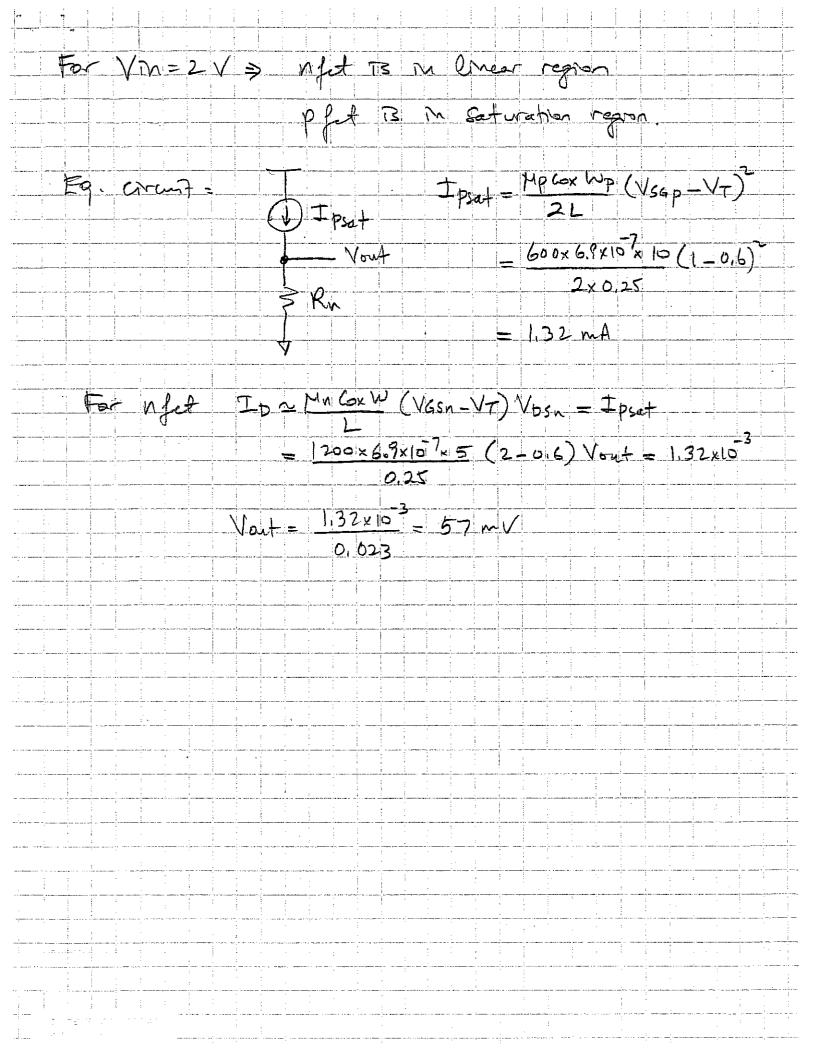


The current through a MOSFET is defined as:

$$I_{D} = \frac{\mu C_{OX} W}{L} \left[(V_{GS} - V_{T}) V_{DS} - \frac{V_{DS}^{2}}{2} \right]$$

- (a) Compute the static DC current when $Vin = 2 V (C_{OUT} = 0 F)$.
- (b) Compute the output voltage when Vin = 2 V.

HINT: Consider the equivalent circuits of nfet and pfet at this bias condition.

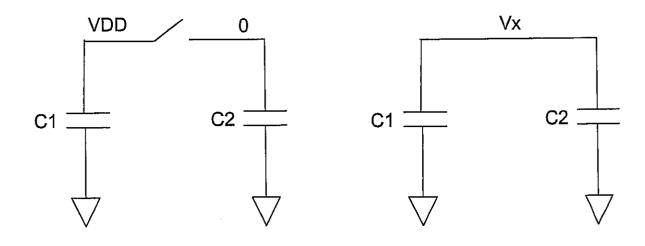


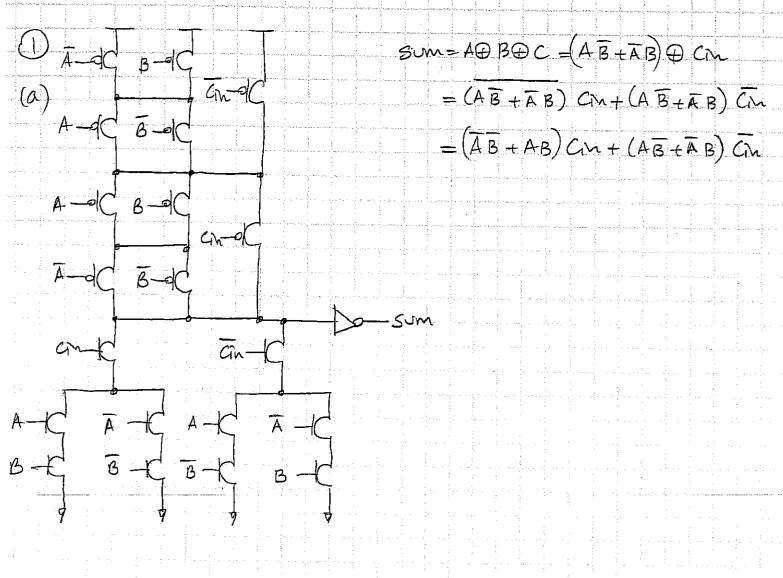
(1)
$$sum = A \oplus B \oplus Cin$$
$$Cout = AB + Cin(A + B)$$

- (a) Draw the schematic in CMOS implementing sum and Cout. Assume to use an output inverter due to high load capacitance, CL.
- (b) Draw the schematic in transmission gates implementing sum and Cout. Also use an output inverter due to high load capacitance, CL.
- (2) (a) Obtain only the pfet tree for the following function, $out = \overline{E} + \overline{D}(\overline{A} + \overline{BC})$
 - (b) Now construct the nfet tree separately from the pfet tree obtained in (a), yielding the same function, out.
 - (c) Now join the nfet and pfet trees and size them according to Rinv = 4 (inverter ratio) in units of W.

The minimum width must be W/2 in the schematic.

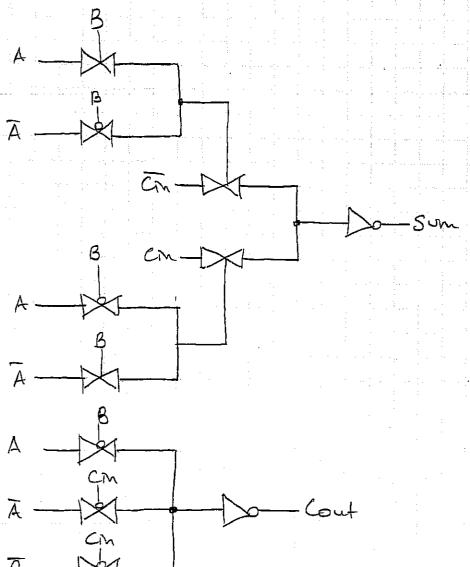
- (d) Find TR/TF (the ratio of rise time to fall time).
- (3) Find Vx after the switch closes.

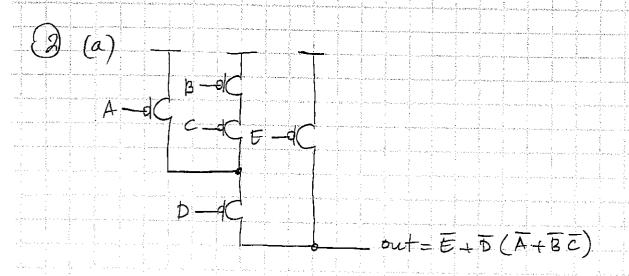




(b) Sum =
$$\overline{A} \oplus \overline{B} \oplus \overline{C} = (\overline{A} B + A \overline{B}) \oplus \overline{C} \cap$$

= $(\overline{A} B + A \overline{B}) \oplus \overline{C} \cap + (A B + \overline{A} \overline{B}) \oplus \overline{C} \cap$
= $(\overline{A} B + \overline{A} \overline{B}) + \overline{C} \cap (\overline{A} B + \overline{A} \overline{B}) + \overline{C} \cap (\overline{A} B + \overline{A} \overline{B}) \oplus \overline{C} \cap (\overline{A} B + \overline{A} B)$
= $\overline{C} \cap (\overline{A} B + \overline{A} \overline{B}) + \overline{C} \cap (\overline{A} B + \overline{A} B)$
= $\overline{C} \cap (\overline{A} + \overline{C} \cap \overline{C} + \overline{C}) \oplus \overline{C} \cap (\overline{A} + \overline{C}) \oplus \overline{C} \cap (\overline{A} + \overline{C}) \oplus \overline{A} \overline{B}$
= $\overline{C} \cap \overline{A} + \overline{C} \cap \overline{B} + \overline{A} \overline{B}$





(b) Since out =
$$\overline{E} + \overline{D}(\overline{A} + \overline{B}\overline{C})$$

out = $\overline{E} \left\{ D + [A(B+C)] \right\} = \overline{E}[D + A(B+C)]$

Thus, the refet tree:

$$B \rightarrow C$$

$$C \rightarrow C$$

$$D \rightarrow C$$

$$C \rightarrow C$$

(c)
$$B \rightarrow C | X = 4w$$
 $A \rightarrow C C \rightarrow C | X = 4w$
 $X = 2w$
 $X = 4w$
 $X = 4w$

(d)
$$T_R = 2.22 C_L \frac{k}{4w} \times 3$$

 $T_F = 2.22 C_L \frac{k}{2w} \times 3$
 $T_F = 2.22 C_L \frac{k}{2w} \times 3$

3)
$$V_{DD}$$
 0 V_{X} Qtotact = Qto

Implement the following function using CMOS.

$$out = (A + .\overline{B}C)(D + E)$$

- (a) Implement this function with an inverter at the output. Size the transistors such that the inverter ratio, Ri, is equal to 1. Use W as the minimum width.
- (b) Implement the same function without an output inverter. Size the transistors such that TR = 2 TF. Use W as the minimum NMOS transistor width (PMOS width can be smaller).

TR = 2.22 CL Rpeq

TF = 2.22 CL Rneq

CL is the output load capacitor Rpeq and Rneq are th equivalent resistors in the charge and discharge paths, respectively.

Ignore the intrinsic capacitances and the resulting Elmore's effect.

