CMPE 124 100+5 TEST 2 April 13, 2015
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**NOTE: All circuits must be presented according to the mixed logic notations. If you make any assumption make sure you explain it. Circuit design must obey all the electrical characteristics of the devices. Obey noise margin rules. You can always use 7404 unless it is stated otherwise. TTL Manual is not a notebook.**

1. Use **ONLY one** mux (74153) to design the following function and **test your design** using **Voltage table**. **Signal assignments are: C, Y, Z are active Low and W, F are active High**. For every extra gate 5 points will be deducted. 15

$F = [C(Y \oplus Z)]W$

$= [C(y\bar{z} + \bar{y}z)]W$

$= (C y\bar{z} + C\bar{y}z)W$

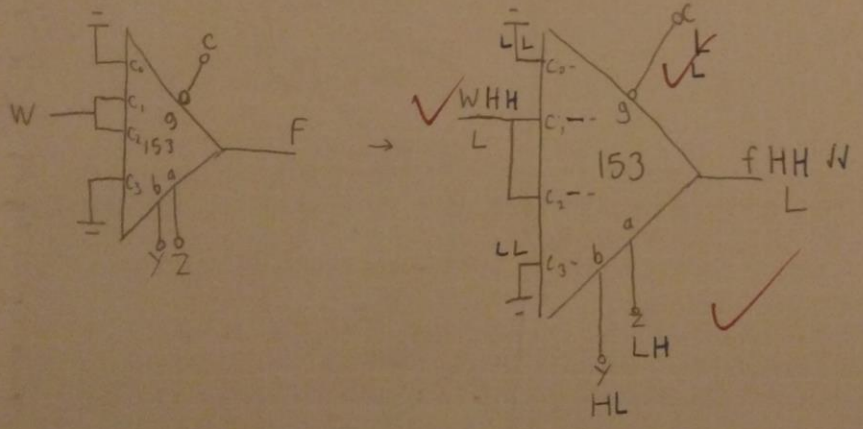
$F = [C(y\bar{z}) + C(\bar{y}z)]W$

C control →

| C | Y | Z | W | F |
|---|---|---|---|---|
| 0 | X | X | X | 0 |
| X | X | X | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 |

Truth → Voltage

| C-- | Y-- | Z-- | W++ | F++ | |
|---|---|---|---|---|---|
| H | x | x | x | L | 0 |
| X | X | X | L | L | 1 1 |
| L | H | H | H | L | 2 2 |
| L | H | L | H | H | 3 3 |
| L | L | H | H | H | 4 |
| L | L | L | H | L | 5 |



f. Complete the timing diagram.

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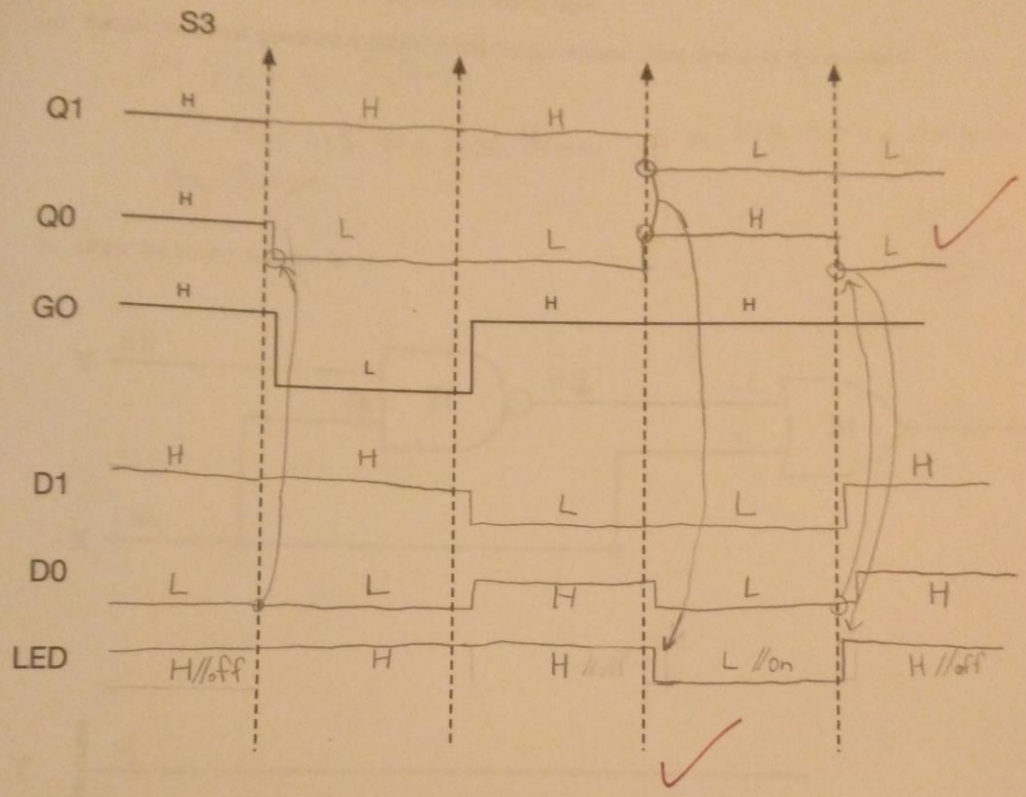

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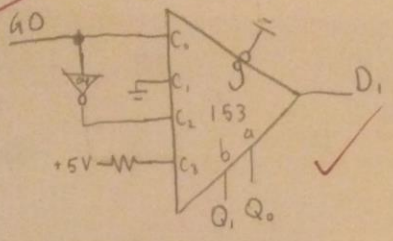
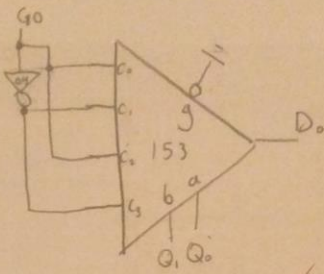
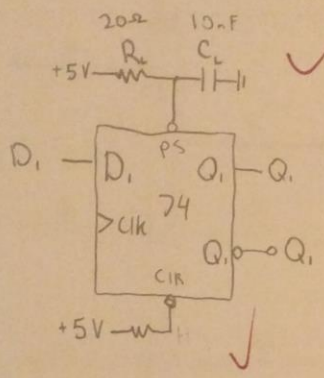
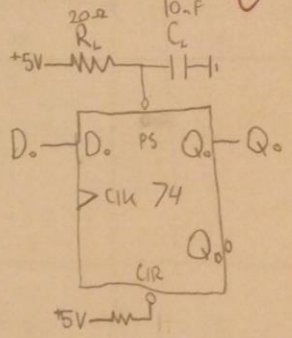
e. Show the complete circuit diagram so that state machine will start from S3. PS* and CLR* needs to be kept active for at least 30 ns if needs to be used.



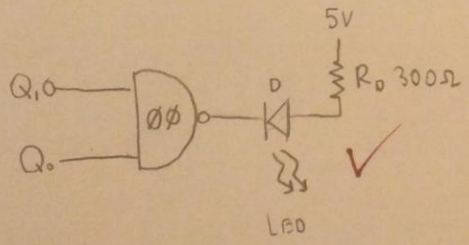




Assume
$V_D = 1.6V$
$I_D = 8mA$

$5V = V_{R_D} + V_D + V_{OL}$
$5V = I_{R_D} R_D + 1.6V + .4V$

We use $I_{R_D}$ as 10mA, it's lower than $I_{OL}$ (16mA) and higher than $I_D$.

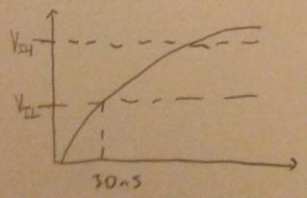
$3V = 10mA\, R_D$
$R_D = 300\Omega$




$C_L = 10nF$
$R_L = 20\Omega$

· $R_L$ $C_L$ values

Use 10nF as C
$R \cdot 10nF = 200ns$ $R = 20\Omega$




$V_{IL\,max} = .8V$

$V = V_{cc}(1 - e^{-t/\tau})$
$.8V = 5V(1 - e^{-30\times10^{-9}/RC})$
$.16 = 1 - e^{-30\times10^{-9}/RC}$

$\ln(.84) = \ln e^{-30\times10^{-9}/RC}$
$-.174 = -30\times10^{-9}/RC$
$RC = .0000002005$
$RC = 200ns$

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b. Show the Exitation Table (transition table)

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| PS S# | $Q_1$ | $Q_0$ | GO | NS S# | $D_1$ | $D_0$ | LED |
|---|---|---|---|---|---|---|---|
| $S_0$ | 0L | 0L | 1H | $S_1$ | 1H | 1H | 0H |
| $S_1$ | 0L | 1H | 1H | $S_0$ | 0L | 0L | 1L |
| $S_2$ | 1H | 0L | 1H | $S_1$ | 0L | 1H | 0H |
| $S_3$ | 1H | 1H | 1H | $S_2$ | 1H | 0L | 0H |
| $S_0$ | 0L | 0L | 0L | $S_0$ | 0L | 0L | 0H |
| $S_1$ | 0L | 1H | 0L | $S_1$ | 0L | 1H | 1L |
| $S_2$ | 1H | 0L | 0L | $S_2$ | 1H | 0L | 0H |
| $S_3$ | 1H | 1H | 0L | $S_3$ | 1H | 1H | 0H |

✓

SEE ME

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c. Derive the Flip Flop input equations

✓

$D_1 = GO(S_0+S_3) + \overline{GO}(S_2+S_3) = GOS_0 + GOS_3 + \overline{GO}S_2 + \overline{GO}S_3 = GOS_0 + \overline{GO}S_2 + S_3$ simple

$D_0 = GO(S_0+S_2) + \overline{GO}(S_1+S_3) = GOS_0 + GOS_2 + \overline{GO}S_1 + \overline{GO}S_3$

$= GO\overline{Q_1}\overline{Q_0} + \overline{GO}\overline{Q_1}Q_0 + GOQ_1\overline{Q_0} + \overline{GO}Q_1Q_0$

$= GO\overline{Q_0} + \overline{GO}Q_0$ simple ✓

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d. Derive the output equation for LED.

✓ $LED = S_1 = \overline{Q_1}Q_0$

0 3 2 1

2. Design a two-bit counter that counts the following sequence: 00-11-10-01. This counter should have an input **GO** to start and stop the counting **at any state**. It should generate an output **(LED)** when the count reaches state 01 (S1). When the power is turned on the state machine should start from state 3 (S3).

   Use D flip-flops 74LS74, Mux 74153 and necessary gates.

   a. Show the ASM chart

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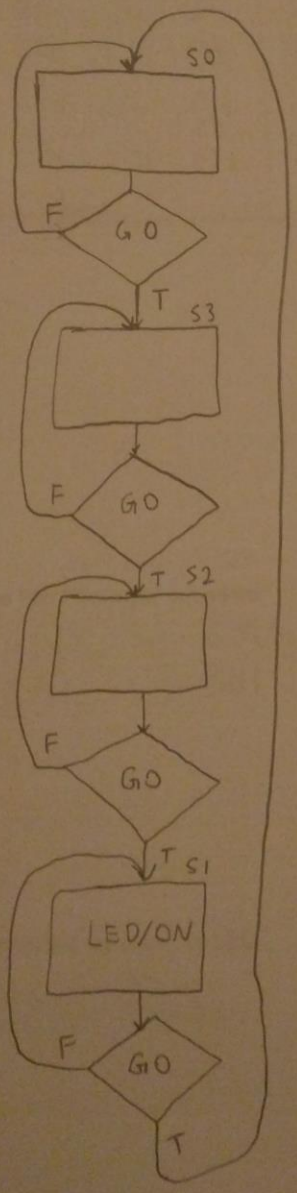

**EXTRA CREDIT:**

3. Below a digital circuit is given. All signals are active high.

   a) Would the circuit generate a glitch? Explain your answer. (Hint: first write the equation)

$F = \overline{Y}X + X = \overline{Y} + \overline{X} + X$

Yes there would be a glitch. Wherever you see $\overline{X}+X$ there is a glitch because of propagation delays for inputs.

   b) Draw the timing diagram for F.

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