/124 zemek TEST 2

Last Name

First Name		
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NOTE: All circuits must be presented according to the mixed logic notations. It you make any assumption make sure you explain it. Circuit design must obey all the electrical characteristics of the devices. Obey noise margin rules. You can always use 7404. TTL Manual is not a notebook.

Use a mux (74153) to design the following function. Signal assignments are: X, Y, F is active high and W active low.

 $F = (x \oplus y \oplus z)w$ 

Design a two-bit counter that counts the following sequence: 00-11-10-01. This counter should have an input x to start and stop the counting at any state. It should generate an output when 2. the count reaches state 01 (S1). When the power is turned on the state machine should start from state 11 (S3). Use D flip-flops 74LS74.

Show the state diagram

Show the ASM chart \_\_\_\_ /5

Show the transition table — 'TS

Drive the equations \_\_\_\_ /2

Show the circuit diagram - 8

Show the necessary circuits and calculations so that state machine will start from S3.

PS and CLR needs to be kept active for at least 30 ns if needs to be used. - 15

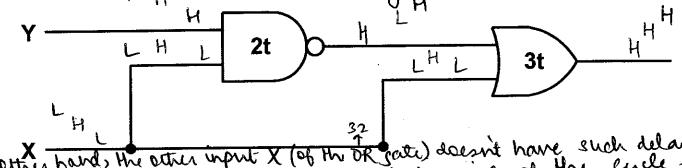
For two clock period show the timing diagram. 10

## **EXTRA CREDIT:**

- 3. Below a digital circuit is given. All signals are active high.
  - a) Would the circuit generate a glitch? Explain your answer. (Hint: first write the equation)

 $\frac{|F=(xy)+x|}{=\overline{y}+\overline{x}+x}=\overline{y}+1=1\Rightarrow \overline{|F=1|}$ 

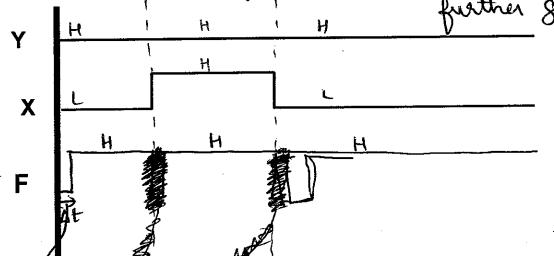
Yes, the consuit will have a flitch and that is because of the propagation delays incide the NAND and Oligates and because b) b) Draw the timing diagram for F. of the mappy unsymmetrical number of gates. The upper (xy) of the or gate is coming from a upper gate which the course an extra delay.



on the other hard, the other input X (of the DR gate) doesn't have such delay.

Thus, there will be a flitch at the beginning of the cycle.

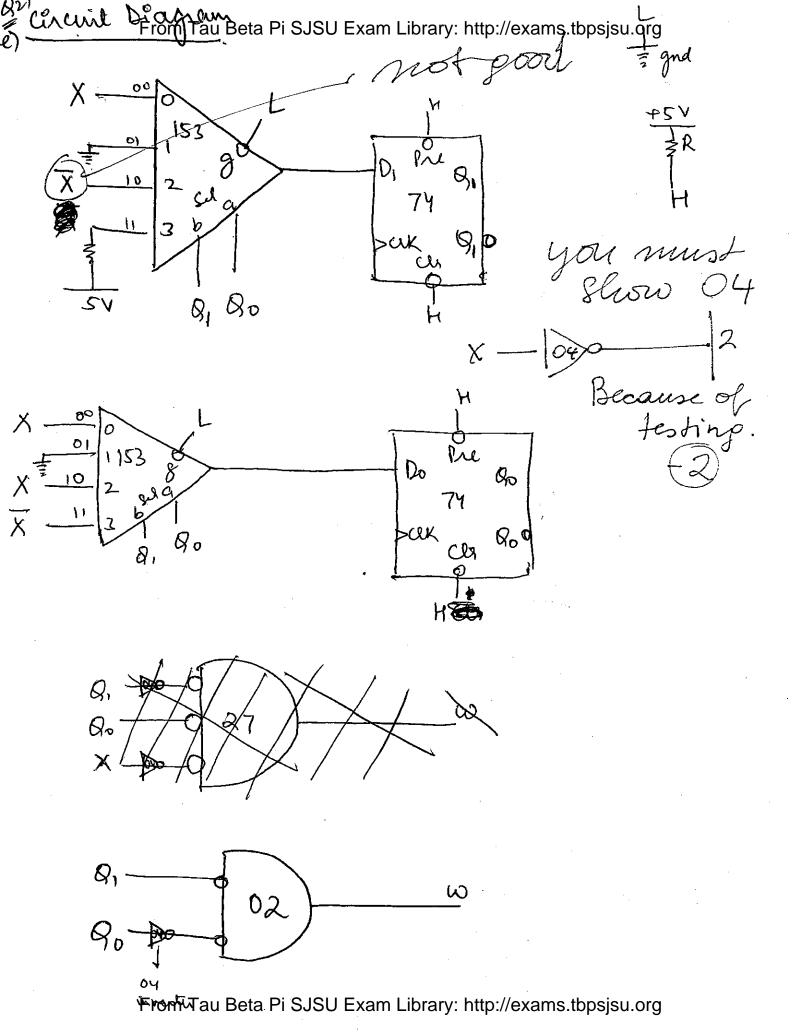
But, then the be value of the function will be camp high for all values of X and Y and hence, will have no further slitch.

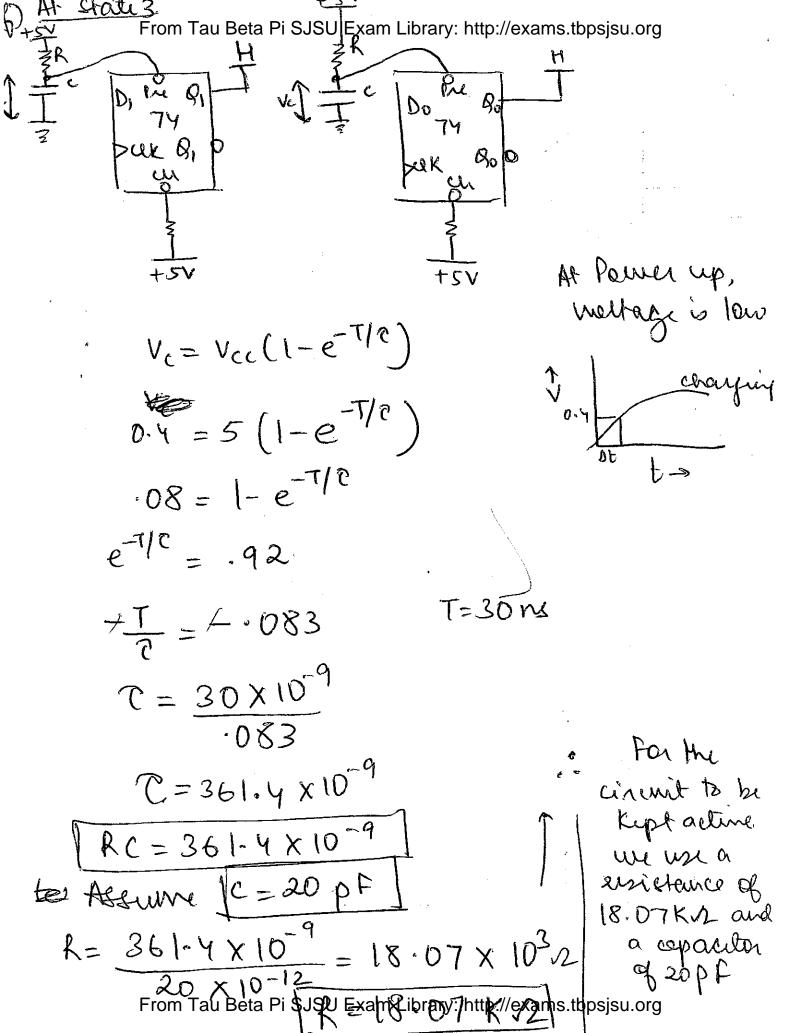


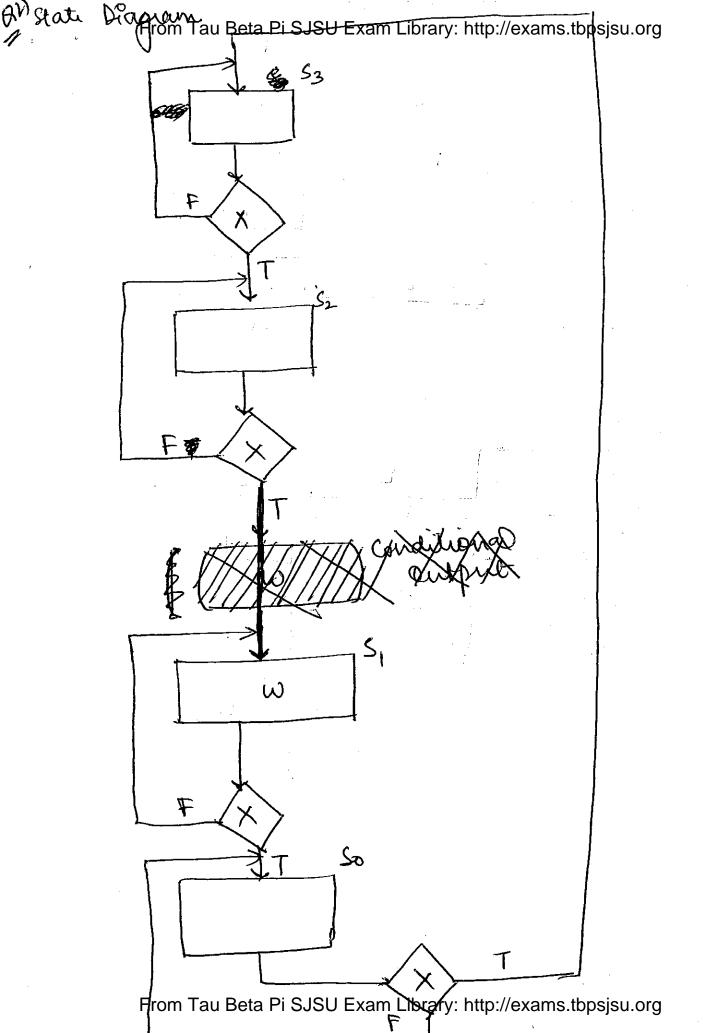
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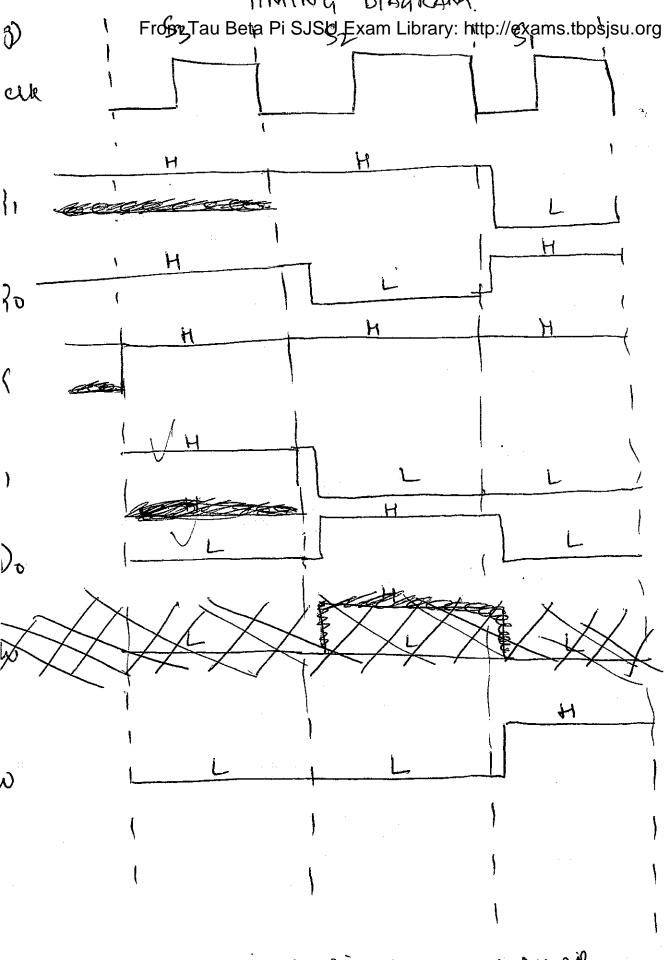
From Tat Beta Pi SJSU Exam Library: http://exams.tbpsjsu.org

Assumeronx Tata Beta PitSJ& & Examplibrary: http://exams.tbpsjsu.org let w be the output at state 01 and it is also the positive assigned 9, Jactive high Next Hate hisur seate w (unconditional g. 0  $\circ$ 53 O O  $\bigcirc$ Si Equations D1= Q1 Q0X + Q1 Q0X + Q1 Q0X + Q1 Q0X = S0X+ S3 X + S3X + S2 X = 0,00 X + 9,00 + 9,00 X Do= B, BoX+B, BoX+B, BoX Tau Beta Pi SJSH Exam Library: http://exams.topsjsu.org









Assuring X to be high for first three clock periods

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GI) 
$$F = (x \overline{y}) \overline{y} = \overline{y}$$

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