			From Tau Beta Pi SJSU Exam Library: http://exams.tbpsjsu.org
1			Glife
-		-	TEST 2 85 + 20 + State diagr 21, 2011
CMPE 124 Dr. Ozemek			
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Las	Last Name _		First Name
exp	lain	it. Circ	cuits must be presented according to the mixed logic notations. If you make any assumption make sure you cuit design must obey all the electrical characteristics of the devices. Obey noise margin rules. You can always . Manual is not a notebook.
151.		Use a mux (74153) to design the following function. Signal assignments are: X, Y, F is active high and W active low.	
		F =	$(x \oplus y \oplus z)w$
2.		have the	ign a two-bit counter that counts the following sequence: 00-11-10-01. This counter should be an input x to start and stop the counting at any state. It should generate an output when count reaches state 01 (S1). When the power is turned on the state machine should start a state 11 (S3). Use D flip-flops 74LS74.
		a.	Show the state diagram
	D	b.	Show the ASM chart (-5)
	15		Show the transition table
	15	d.	Drive the equations
	10		Show the circuit diagram
	10	f.	Show the necessary circuits and calculations so that state machine will start from S3. PS and CLR needs to be kept active for at least 30 ns if needs to be used.

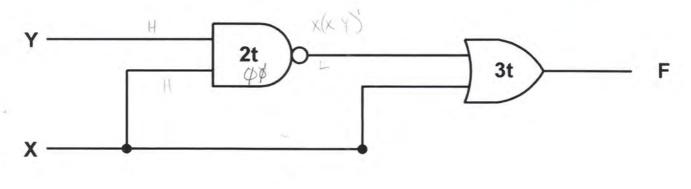
For two clock period show the timing diagram.

10 g.

A CREDIT:

- 3. Below a digital circuit is given. All signals are active high.
 - a) Would the circuit generate a glitch? Explain your answer. (Hint: first write the equation)

Yes, because the equation is F = (xy)+x=x+y'+x; which should bet \$1, but since the X & y have to experience and elay through the DD, whenever X switches from high to low, given yis this during that time (xy) will remain at L for 2t, giving an output of Low, where b) Draw the timing diagram for F. if should be High



2t of Low Signal 3t of

