

PROBLEMS

4.1 Construct a logic truth table for the circuit in Figure P4.1.

4.2 Construct a logic truth table for the circuit in Figure P4.2.

4.3 Construct a logic truth table for the circuit in Figure P4.3.

4.4 Construct a logic truth table for the circuit in Figure P4.4.

Refer to Figure 4.17 for Problems 4.5 to 4.8.

4.5 Show that $g = x'y$ when the 00 assignments are x (—), y (++) , g (—).

4.6 Show that $g = x + y'$ when the 00 assignments are x (—), y (++) , g (++) .

4.7 Show that $g = xy'$ when the 00 assignments are x (++) , y (—) , g (—).

FIGURE P4.1

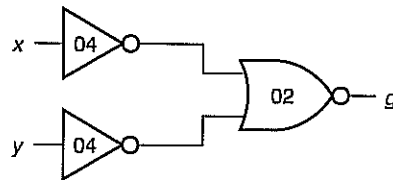


FIGURE P4.2

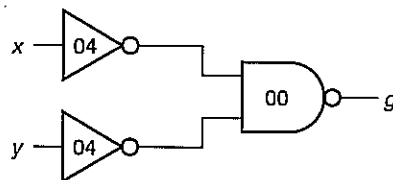


FIGURE P4.3

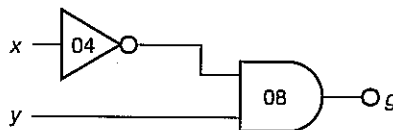
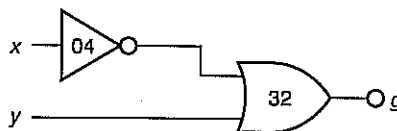


FIGURE P4.4



4.8 Show that $g = x' + y$ when the 00 assignments are $x (+ +)$, $y (- -)$, $g (+ +)$.

Refer to Figure 4.21 for Problems 4.9 to 4.12.

4.9 Show that $g = x' + y$ when the 02 assignments are $x (- -)$, $y (+ +)$, $g (- -)$.

4.10 Show that $g = xy'$ when the 02 assignments are $x (- -)$, $y (+ +)$, $g (+ +)$.

4.11 Show that $g = x + y'$ when the 02 assignments are $x (+ +)$, $y (- -)$, $g (- -)$.

4.12 Show that $g = x'y$ when the 02 assignments are $x (+ +)$, $y (- -)$, $g (+ +)$.

4.13 Use algebra to prove $g_0 = g_2$ (see Figure 4.23).

4.14 Use algebra to prove $g_1 = g_2$ (see Figure 4.23).

4.15 Use algebra to prove $g_4 = g_5$ (see Figure 4.24).

4.16 Use algebra to prove $g_6 = g_7$ (see Figure 4.24).

4.17 Prove Theorems X1 and X1D. Use axioms and theorems in Table 3.1.

4.18 Prove Theorem X6. Use axioms and theorems in Table 3.1.

4.19 Prove Theorem X8. Use axioms and theorems in Table 3.1.

4.20 Prove Theorem X11. Use axioms and theorems in Table 3.1.

4.21 Mixed-Logic and DeMorgan's Theorems

Using all possible product combinations of two variables and their complements, eight functions are generated as follows. DeMorgan's theorems generate the eight complementary functions. Draw the circuits for each function pair.

(a) $z = ba = (b' + a')'$

(b) $z = ba' = (b' + a)'$

(c) $z = b'a = (b + a')'$

(d) $z = b'a' = (b + a)'$

- (e) $z = (ba)' = b' + a'$
 (f) $z = (ba')' = b' + a$
 (g) $z = (b'a)' = b + a'$
 (h) $z = (b'a')' = b + a$

4.22 Use mixed-logic circuit analysis to find g (for the circuits in the listed figures) as follows:

Use algebra to find an expression for g' (*not* g).

Write g' to the K-map for g (not g').

Read g from the K-map.

- (a) Figure P4.5
 (b) Figure P4.6
 (c) Figure P4.7
 (d) Figure P4.8
 (e) Figure P4.9
 (f) Figure P4.10
 (g) Figure P4.11

FIGURE P4.5

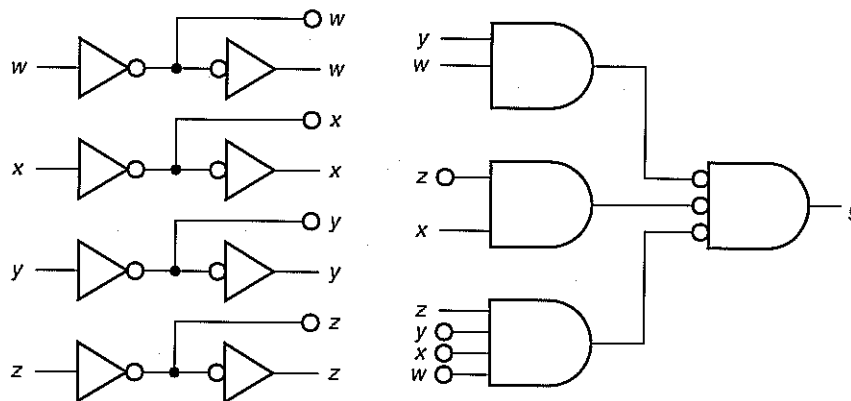


FIGURE P4.6

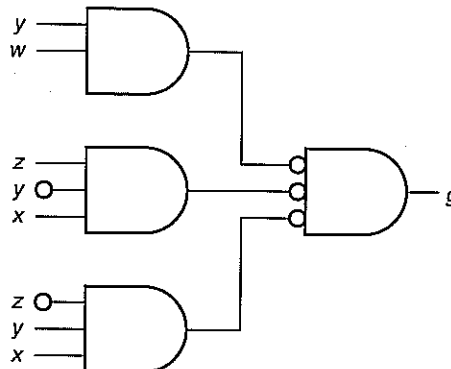


FIGURE P4.7

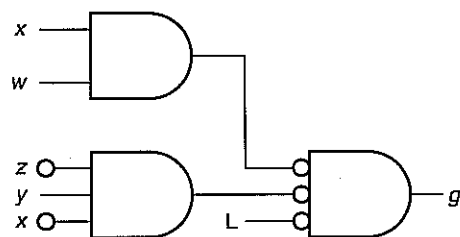


FIGURE P4.8

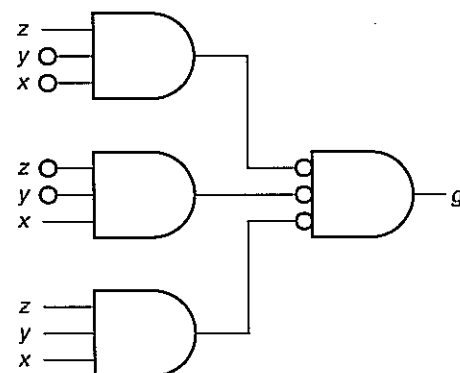


FIGURE P4.9

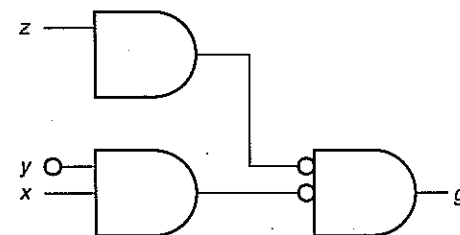


FIGURE P4.10

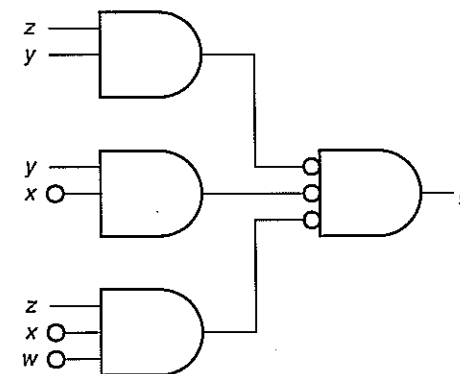
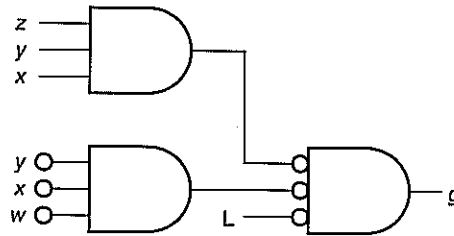


FIGURE P4.11



4.23 Assume all variables are active high. Draw a mixed-logic circuit for the following equations. Do not use 08 or 32 type gates. Do not modify the equations.

- (a) $f = n_3'[n_1 + (n_2 \text{ XOR } n_0)'] + n_3 n_2 n_1'$
- (b) $f = n_3' n_2' + n_2[n_1' n_0' + n_0(n_3 \text{ XOR } n_1)]$
- (c) $f = n_3'(n_1' + n_0) + n_2(n_1' + n_3)$
- (d) $f = (n_3 \text{ XOR } n_0) + n_3'[n_2'(n_1 + n_0') + n_1 n_0']$
- (e) $f = n_0'(n_3 \text{ XOR } n_2 n_1')$
- (f) $f = n_2(n_1' + n_3' n_0') + n_3' n_1' n_0'$
- (g) $f = n_2 n_1' + n_3' n_1(n_0' + n_2')$

4.24 Assume all variables are active high. Draw a mixed-logic circuit for the following equations. Do not use 08 or 32 type gates. Use NAND NAND logic.

- (a) $f = n_3'[n_1 + (n_2 \text{ XOR } n_0)'] + n_3 n_2 n_1'$
- (b) $f = n_3' n_2' + n_2[n_1' n_0' + n_0(n_3 \text{ XOR } n_1)]$
- (c) $f = n_3'(n_1' + n_0) + n_2(n_1' + n_3)$
- (d) $f = (n_3 \text{ XOR } n_0) + n_3'[n_2'(n_1 + n_0') + n_1 n_0']$

4.25 Assume all variables are active high. Draw a mixed-logic circuit for the following equations. Do not use 08 or 32 type gates. Use NOR NOR logic.

- (e) $f = n_0'(n_3 \text{ XOR } n_2 n_1')$
- (f) $f = n_2(n_1' + n_3' n_0') + n_3' n_1' n_0'$
- (g) $f = n_2 n_1' + n_3' n_1(n_0' + n_2')$

5

COMBINATIONAL BUILDING BLOCKS

5.1 Timing

- 5.1.1 Propagation Delay
- 5.1.2 Timing Diagrams
- 5.1.3 Hazards

5.2 Multiplexing

- 5.2.1 Definition and Implementation
- 5.2.2 Devices with Three-State Outputs
- 5.2.3 Function Generators
- 5.2.4 Conversion from Parallel to Serial
- 5.2.5 Data Routing

5.3 Decoding

- 5.3.1 Definition and Implementation
- 5.3.2 Decoders as Function Generators
- 5.3.3 Decoders as Demultiplexers

5.4 Priority Encoding

5.5 Comparing

5.6 Generating and Checking Parity

5.7 Adding and Carrying

- 5.7.1 Adding
- 5.7.2 Carrying
- 5.7.3 283 Four-Bit Adder
- 5.7.4 Conversion from BCD to Binary

5.8 Arithmetic-Logic Unit (ALU)

- 5.8.1 Universal-Logic Circuit (ULC)
- 5.8.2 The 74LS181 Four-Bit ALU
- 5.8.3 The 74LS182 Sixteen-Bit Look-Ahead Carry