San Jose State University
Department of Computer Engineering

CMPE 125 Spring 2017

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Lab 7 Report

System-level Design (1)

Date ____4/22/17_____

by

Name ____Anahit Sarao_____ SID __008435583_____

Name ____Maxwell Cheshier_____ SID __009193717___

Lab Record

Tasks	Designed by (print name)	Verified by (print name)	*Completion Status
1	Both	Ryan	A
2	Maxwell	Ryan	A
3	Anahit	Ryan	A

Task	Performed by (print name)	Validated by (print name)	*Completion Status
4	**N/A**	**Ryan**	**X**

*** Enter the following:**
A – if the task was successfully completed
B – if the task was partially completed
X – if the task was failed or not performed
If you entered B or X, detailed description about the incompletion or failure must be given in the report.