CmpE 124 TEST 3 95 May 2, 2011
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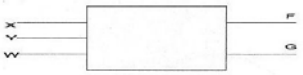
Last Name_____ First Name_____

NOTE: All circuits must be presented according to the mixed logic notations. If you make any assumption make sure you explain it. Circuit design must obey all the electrical characteristics of the devices. Obey noise margin rules. You can always use 7404. TTL Manual is not a notebook.

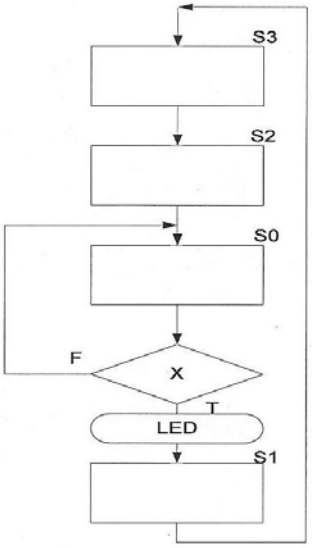
1- Design the following multiple output logic function using only **one** 74LS138 (decoder) and 74LS20 NAND gates (you can always use 04 if needed).

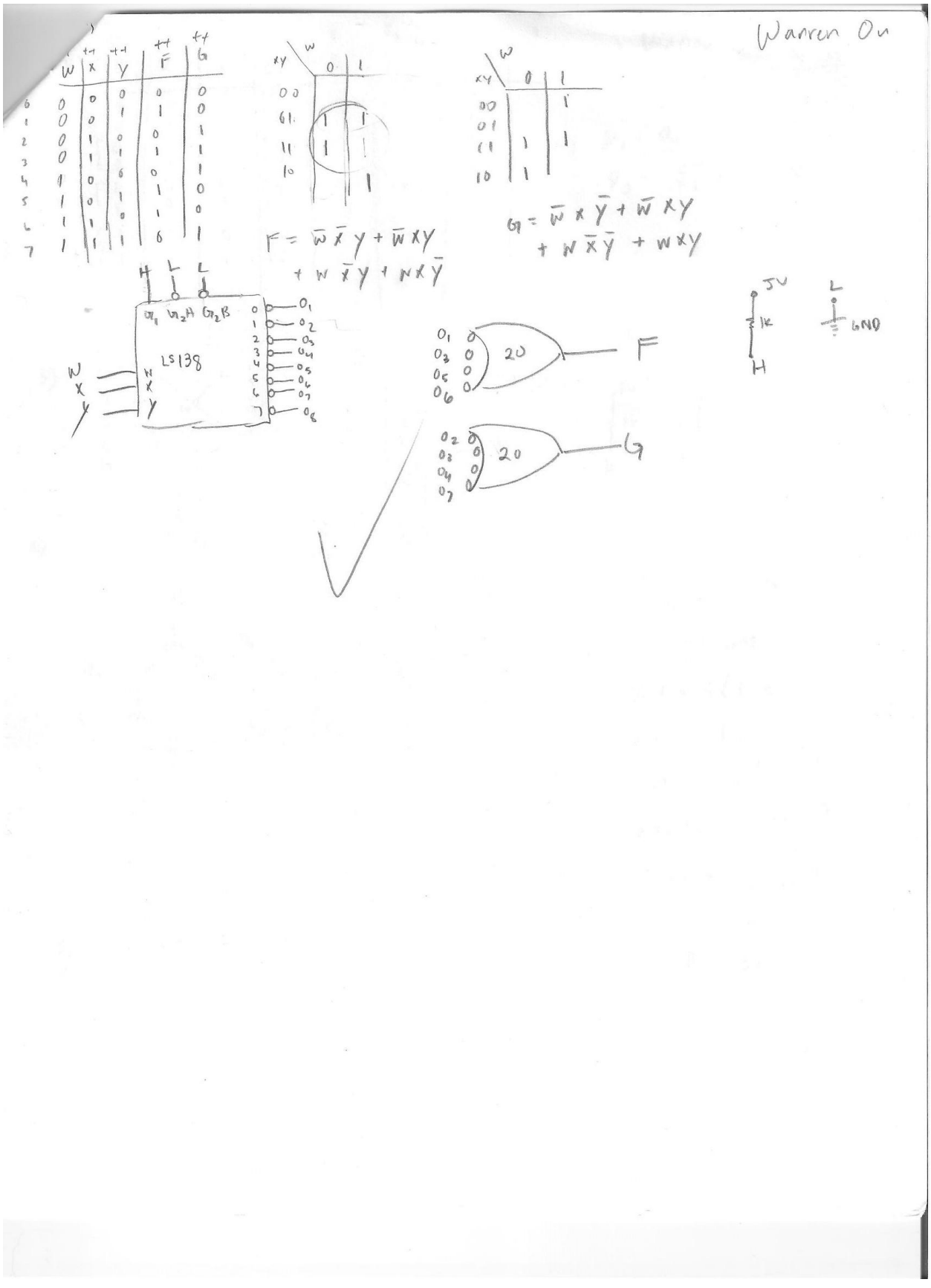
$$F = \sum_{W,X,Y}(1,3,5,6)$$
$$G = \sum_{W,X,Y}(2,3,4,7)$$



2- Design the state machine given in Figure 1. Use D flip-flops 74LS74 and Multiplexers (74153) for D inputs and any necessary gate.

a) Construct the state transition table.
b) Derive the Flip Flop input equations.
c) Derive the output equation.
d) The SM should start from state 1 after power up; calculate R and C for 30 ns.
e) Show the complete circuit diagram.
f) The output should turn a LED when it is True, design the interface circuit (V_d=1.6V I_d=10 ma)
g) Plot the actual timing diagram for 3 clock cycles.





a)

	Q_1	Q_0	x	St	P_1 Q_1^+	P_0 Q_0^+	LED
S_0	0	0	0	S0	0	0	0
	0	0	1	S1	0	1	1
S_1	0	1	0	S3	1	1	0
	0	1	1	S3	1	1	0
S_2	1	0	0	S0	0	0	0
	1	0	1	S0	0	0	0
S_3	1	1	0	S2	1	0	0
	1	1	1	S2	1	0	0

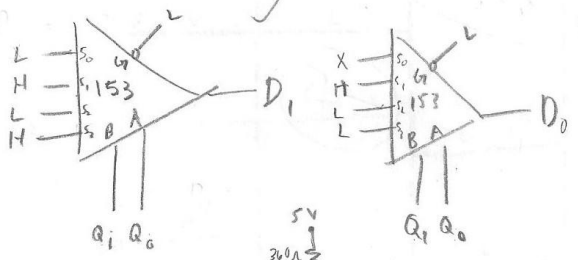
Karnaugh Map

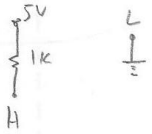
	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	0	0

c) $D_1 = Q_1$

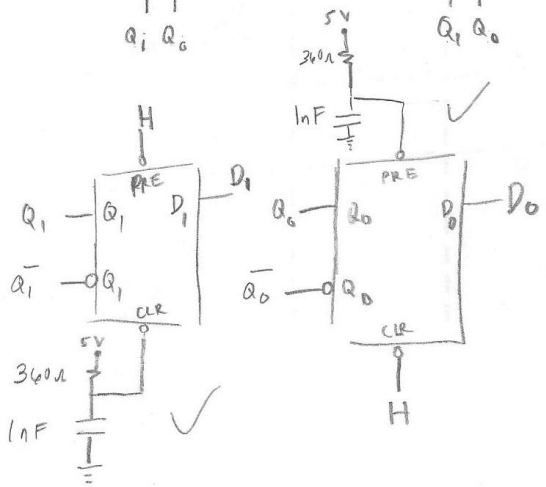
$D_0 = \overline{Q_1}\, x + \overline{Q}\, Q_0$

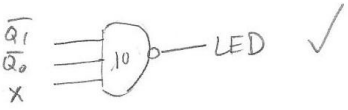
b)





e)





f) $V_c = V_{cc}(1 - e^{-t/RC})$

$t = 30ns$

$0.4V = 5(1 - e^{-30\times10^{-9}/RC})$

$0.08 = 1 - e^{-30\times10^{-9}/RC}$

$0.92 = e^{-30\times10^{-9}/RC}$

$-0.0833 = \frac{-30\times10^{-9}}{RC}$

$RC \approx 3.6\times10^{-7}$

$C = 1nF$

$R = 360\Omega$