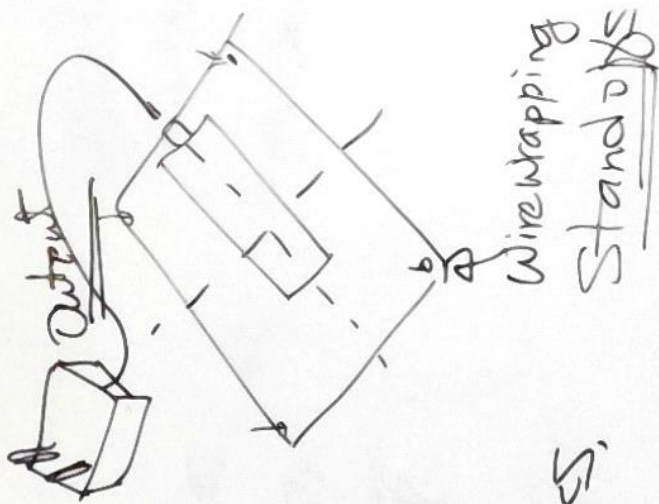# CMPE127 MicroProcessor Systems.
Feb 6th, 2017 ITL.

Quiz: Draw System Block Diagram
Which Shows (1) CPU Core and
JTag Unit + (2) Memory Controller Blocks,
(3) Peripheral Controllers.

Today's Topics: 1° Layout Design Lab
2° CPU Architecture (memory map) → IDE/Lab1

Homework: NXP website → As Developer
By Next Monday. Xpresso

Example: Layout Design.

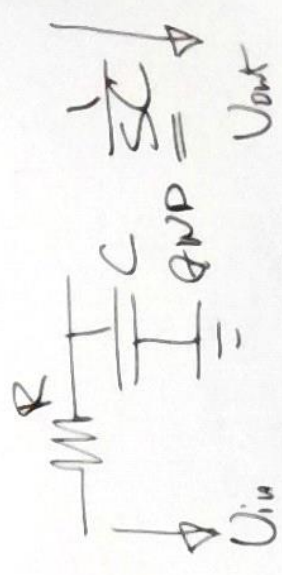
PWR CKT Design.
Table 1 PWR CKT

$$I_c = \frac{V}{R}$$

$$I_{GND} = \frac{V}{R}$$

$$V_{out}(S) = \frac{V_{in}}{R + SC}$$

$$= \frac{V_{in}}{1 + SCR}$$

$$\tau = \text{Time Constant}$$

$$V_{cd}\left(1 - e^{-t/\tau}\right) \quad \text{Charging}$$

$$V_{cc}\, e^{-t/\tau}$$

U1	Wall mount PWR Adaptor 7.5 VDC	1500~2000 mA

WireWrapping
StandOFF

HS.C.
Central Expwy + Corin
SW1 (South West Corner)
J1

Input
Output

Fig. 18. Note: Two Caps Needed to form L.P.F. To Remove

7.5VDC
GND
LM7805
78XX
5.0 VDC

SMD — Surface Mount Device