PROBLEMS

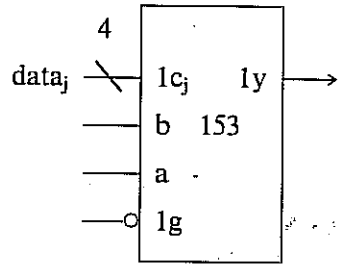
5.1 *Static hazard:* Show by replicating Figure 5.2a that the static hazard in $g_0 = (x + z)(x' + y')$ is eliminated when the consensus term $(y' + z)$ is added as a factor to g_0. Show by using a K map that g_0 is not changed by adding $(y' + z)$ to the expression.

5.2 *Static hazard:* Show by replicating Figure 5.2b that the static hazard in $g_1 = x'z + xy'$ is eliminated when the consensus term zy' is added to g_1. Show by using a K map that g_1 is not changed by adding zy' to the expression.

5.3 *Dynamic hazard:* Show by replicating Figure 5.3 that the dynamic hazard is eliminated by adding the consensus term to $(xz + yz')$.

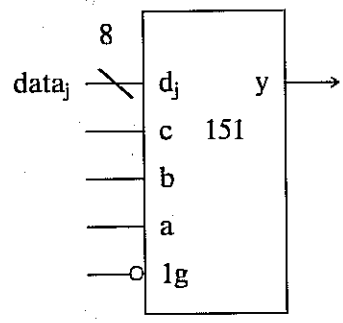
5.4 The 74LS153 schematic is found in any TTL data book. Assume select inputs A (pin 14) and B (pin 2) are at the L level. Assume that data input 1C0 (pin 6) is at the L level, and that 1C1 (pin 5) is at the H level. Let input A switch from L to H. Make a timing diagram showing the ideal digital waveforms, including propagation delays, at the outputs of the four gates in the signal path from A (pin 14) to 1Y (pin 7). Refer to Figure 5.2.

5.5 Use one 4 × 1 mux (153) and supplementary gates to synthesize the following functions.



(a) $f = (x \text{ xor } y \text{ xor } z)w$
(b) $f = [xy + z(x \text{ xor } y)]w$
(c) $f = [xy + z(x + y)]w$
(d) $f = x' + y'z$
(e) $f = x' + z + y'$

5.6 Use one 8 × 1 mux (151) and supplementary gates to synthesize the following functions.



(a) $f = x$ xor y xor zw
(b) $f = xy + z(x \text{ xor } wy)$
(c) $f = xy + z(x + yw)$
(d) $f = wx' + y'z$
(e) $f = wx' + wz + xy' + w'yz'$

5.7 Use multiplexers and supplementary gates to design Gray-code-to-binary converters defined by the following truth table.

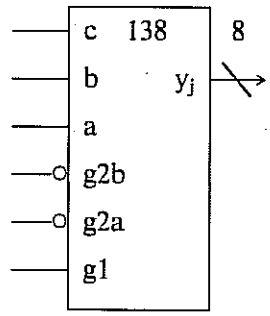
(a) Use four 151 chips plus gates.
(b) Use four 153 chips plus gates.
(c) Use two 151 chips plus gates.
(d) Use two 153 chips plus gates.

INPUTS—GRAY				OUTPUTS—BINARY			
w	x	y	z	g_3	g_2	g_1	g_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1

INPUTS—GRAY				OUTPUTS—BINARY			
w	x	y	z	g_3	g_2	g_1	g_0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

5.8 The 74LS139 schematic is found in any TTL data book. Assume select inputs 1A (pin 2) and 1B (pin 3) are at the L level. Assume that enable input 1G (pin 1) is at the L level. Let input 1A switch from L to H. Make a timing diagram showing the ideal digital waveforms, including propagation delays, at the outputs of the three gates in the signal path from 1A (pin 2) to 1Y1 (pin 5). Refer to Figure 5.2.

5.9 Use a 3 × 8 decoder (138) and supplementary gates to synthesize the following functions.



(a) $f = (x \text{ xor } y \text{ xor } z)w$
(b) $f = [xy + z(x \text{ xor } y)]w$
(c) $f = [xy + z(x + y)]w$
(d) $f = x' + y'z$
(e) $f = x' + z + y'$

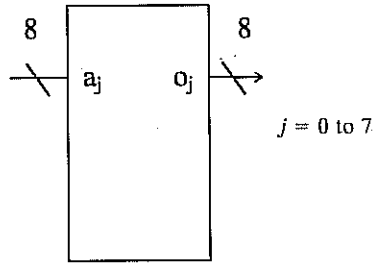
5.10 Use two 3 × 8 decoders (138) and supplementary gates to synthesize the following functions.

(a) $f = x \text{ xor } y \text{ xor } zw$
(b) $f = xy + z(x \text{ xor } wy)$
(c) $f = xy + z(x + yw)$
(d) $f = wx' + y'z$
(e) $f = xw' + wz + wy' + w'yz'$

5.11 Use decoders and supplementary gates to design Gray-code-to-binary converters defined by the truth table in Problem 5.7.

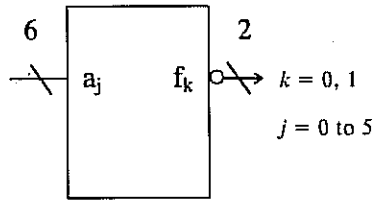
(a) Use four 138 chips plus gates.
(b) Use four 139 chips plus gates.

5.12 Use a 3 × 8 decoder (138) and supplementary gates to decode an eight-bit address a_j (j = 0 to 7) by producing asserted low output lines o_j for hex addresses C7, CF, D7, DF, E7, EF, F7, and FF. Write the equation for the E7 output.

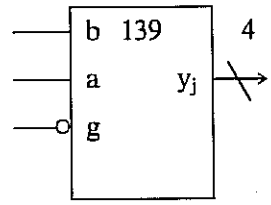


5.13 Use two 3 × 8 decoders (138) and *no* supplementary gates to synthesize f_0 and f_1.

$$f_0 = a_5'a_4'a_3'a_2'a_1a_0'$$
$$f_1 = a_5'a_4'a_3a_2'a_1a_0$$



5.14 Use one or two 2 × 4 decoders (139) and supplementary gates to synthesize the following functions.

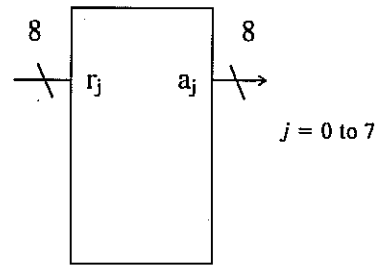


(a) $f = x$ xor y xor z
(b) $f = xy + z(x \text{ xor } y)$
(c) $f = xy + z(x + y)$
(d) $f = x' + y'z$
(e) $f = (y + z)(x' + y')$

5.15 The 74LS148 schematic is found in any TTL data book. Assume all inputs are at the H level except input EI, which is at the L level. Let input_6 (pin 3) switch from H to L. Make a timing diagram showing the ideal digital waveforms, including propagation delays, at the outputs of the gates in the signal paths from input_6 (pin 3) to A1 (pin 7). Refer to Figure 5.2.

5.16 Use a priority encoder (148) and supplementary gates to synthesize the following truth table.

In	Address out
r_0	C7
r_1	CF
r_2	D7
r_3	DF
r_4	E7
r_5	EF
r_6	F7
r_7	FF

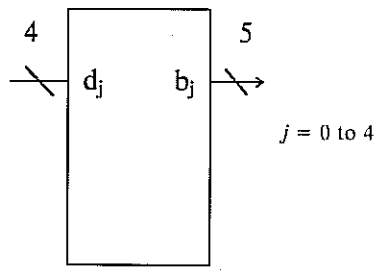


5.17 Synthesize a less-than function for four-bit signed numbers.

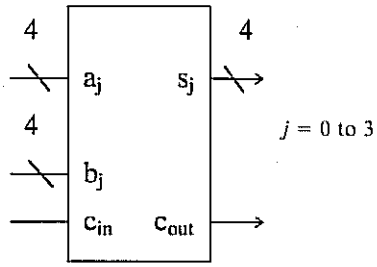
5.18 Can glue logic plus an 85 be used for signed number comparisons? Explain why not, or design a circuit to do so.

5.19 The 74LS283 schematic is found in any TTL data book. Assume all inputs are at the L level. Let A3 (pin 14) switch from L to H. Make a timing diagram showing the ideal digital waveforms, including propagation delays, at the outputs of all the gates in the signal path from A3 (pin 14) to Σ3 (pin 13). Refer to Figure 5.2.

5.20 Convert binary 0000 to 1111 (d_j) into BCD 00 to 15 (b_j). Use a 157 mux, a 283 adder, and supplementary gates for this highly specialized code converter.



5.21 Synthesize a one-digit BCD adder $s = a$ BCD_add b. Use 283 adders and supplementary gates.



5.22 Use the adder equations for sum_j, and carry out c_j for $j = 0, 1, 2, 3$ to sum $c_{in} = 0$, $a = 1011$, and $b = 0101$. Build a table of values with columns for b_j, a_j, c_j, and sum_j, in that order.

5.23 Use algebra to demonstrate that

$$p_j g_j' \text{ xor } c_{i,j} = b_j \text{ xor } a_j \text{ xor } c_{i,j} = \text{sum}_j$$

For $c_{in} = 1$, $a = 1011$, and $b = 0101$, build a table of values with columns for b_j, a_j, p_j, g_j, $p_j g_j'$, c_j, and sum_j, in that order.

5.24 Use the ULC z equation to demonstrate that

$$z_6 = b' \text{ xor } a = b \text{ xor } a'$$

5.25 For $c_{in} = 1$, $a = 1011$, and $b = 0101$, calculate a minus b using 181 s_j code 6. Build a table of values with columns for b_j, a_j, z_{6j}, c_j, and f_j, in that order.