CMPE 140 Lab #7 Assignment

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Enhanced Single-cycle MIPS Processor

Description:

In this lab you will extend the initial design of the single-cycle MIPS processor (from Lab #5 and #6) to support more MIPS instructions. You are required to enhance the single-cycle MIPS processor's functionality by extending its instruction set (`add, sub, and, or, slt, lw, sw, beq, j, addi`) to cover the following additional instructions: `MULTU, MFHI, MFLO, JR, JAL.`

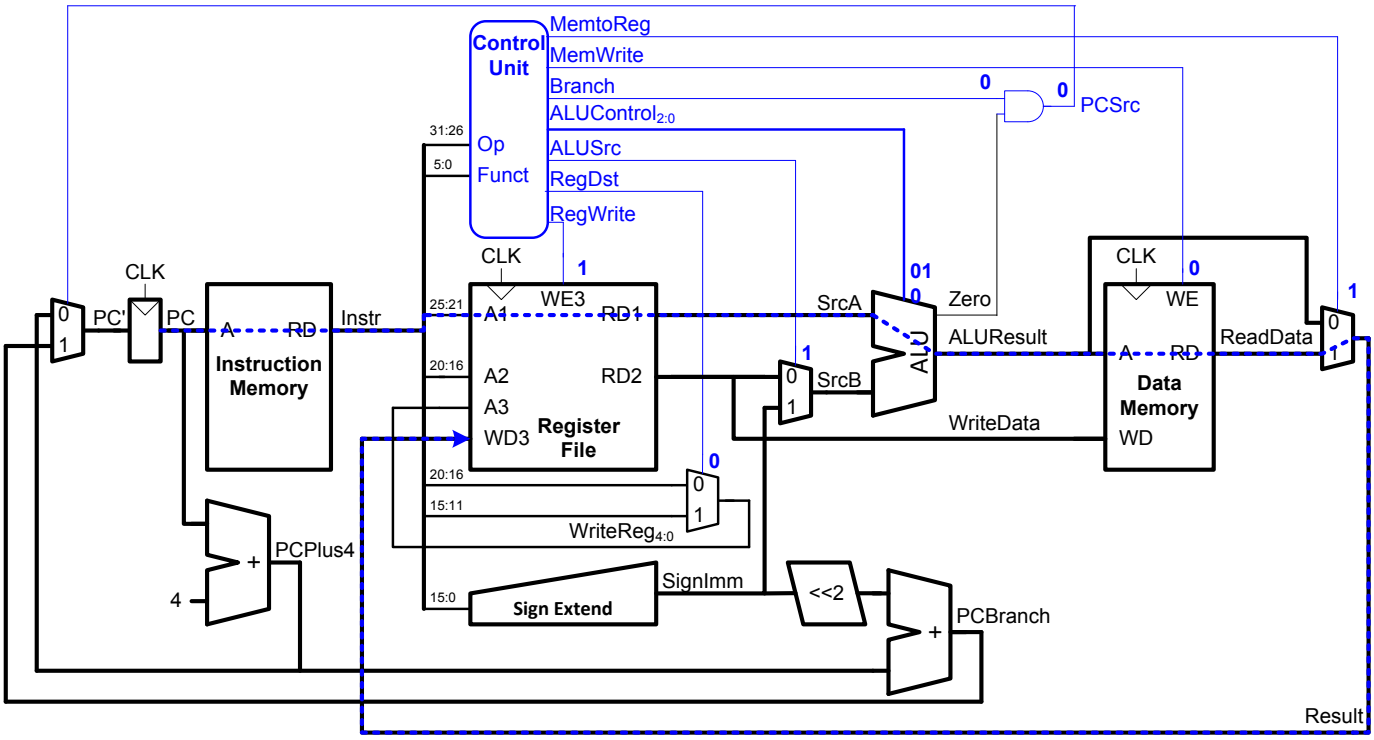
Your design must be tested via both functional verification and FPGA validation. Schematics of the initial MIPS design and the test program for your extended design are given in Attachment 1 and Attachment 2 respectively. As a reminder, machine code of a test programs should be stored in the memory file named *memfile.dat*, which should be placed in your project directory. This file should contain one 32-bit piece of machine code (in hex) per line (unused memory space should be filled with zero's), and you will have to re-synthesize and implement the entire design any time changes are made to the machine code in order to properly program the FPGA on the Nexys4 board.

You should document your work professionally. In addition to descriptions and discussions, your report should include schematics (generated by professional drawing tools such as Microsoft Visio) for the enhanced processor micro architecture, tables for the control unit decoders, the simulation log, testbench waveforms, and commented source code. Signal naming must adhere with the list given in Assignment 5. **Any microarchitecture changes (modification and/or extension) to the initial design (figure and source code) must be in a different color and clearly noted.**

This is a three week long lab. This extended time is to allow for proper development of the extended MIPS processor. In order to ensure that students are staying on track with the lab there will be checkpoints for each lab session. Please see the following schedule of due dates to see what is due for each week:

Week	Due to be Checked by TA
Week #1 (week of 10/23)	1. Initial draft (hand drawn ok) of extended datapath and control unit schematic
Week #2 (week of 10/30)	1. Official draft (generated by Microsoft Visio or other professional drawing tool) of extended MIPS microarchitecture (datapath & control) 2. Control unit truth table (Microsoft Excel only)
Week #3 (week of 11/6)	1. Completed extended MIPS processor design 2. Test bench simulation 3. Demo of MIPS processor on Nexys4 FPGA.

Attachment 1: Initial Design of the Single-cycle MIPS (w/o jump)



Attachment 2: Test Program I

Test code for extended design. Use the MIPS assembler/simulator to test it first!

```
.data
.globl main
.text
main:
     # addi $sp, $0, 48         not for SPIM
       addi $a0, $0, 4      # set arg
       jal factorial        # compute the factorial
       add $s0, $v0, $0     # move result into $s0
       j end
factorial:
       addi $sp, $sp, -8    # make room on stack
       sw $a0, 4($sp)       # store $a0
       sw $ra, 0($sp)       # store $ra
       addi $t0, $0, 2      # $t0 = 2
       slt $t0, $a0, $t0    # a <= 1 ?
       beq $t0, $0, else    # no - goto else
       addi $v0, $0, 1      # yes - return 1
       addi $sp, $sp, 8     # restore $sp
       jr $ra               # return
else:
       addi $a0, $a0, -1    # n = n - 1
       jal factorial        # recursive call
       lw $ra, 0($sp)       # restore $ra
       lw $a0, 4($sp)       # restore $a0
       addi $sp, $sp, 8     # restore $sp
       multu $a0, $v0       # n * factorial(n-1)
       mflo $v0             # mv result into $v0
       jr $ra
end:
```