San Jose State University
Department of Computer Engineering

CMPE 125 Spring 2017

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Lab 8 Report

System-level Design (2)

Date _____5/13/17_____

by

Name _____Anahit Sarao___ SID ___008435583_____

Name _____Maxwell Cheshier__ SID __009193717_____

Lab Record

Tasks	Designed by (print name)	Verified by (print name)	*Completion Status
1	**Anahit & Maxwell**	Ryan	A
2	Maxwell	Charles	A
3	Anahit	Charles	A

Task	Performed by (print name)	Validated by (print name)	*Completion Status
4	**Anahit & Maxwell**	Ryan	A

*** Enter the following:**
A – if the task was successfully completed
B – if the task was partially completed
X – if the task was failed or not performed
If you entered B or X, detailed description about the incompletion or failure must be given in the report.