CMPE 140 Laboratory Assignment 8

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Pipelined MIPS Processor, I/O, and Interfacing

Purpose

Convert the fifteen-instruction 32-bit single-cycle MIPS processor into a five-stage, pipelined design. Interface the processor with a factorial accelerator and a general-purpose I/O unit using memory-mapped interface registers.

Description

In this assignment, you are required to complete the design, functional verification, and FPGA implementation of a pipelined MIPS processor. You are further required to complete the design, functional verification, and FPGA implementation of a small system-on-chip (SoC) system which includes the pipelined MIPS processor, a factorial accelerator (you have completed in Lab 1), and a simple general-purpose IO (GPIO) unit, all connected via direct interface to the MIPS local bus, using memory-mapped interface registers.

Based on the enhanced single-cycle MIPS processor (which supports the additional instructions `multu, mfhi, mflo, jr, jal`) you successfully accomplished in lab 7, use the test program (factorial calculation via nested procedure calls) included in the assignment to test the pipelined MIPS processor. Extra credit will be given if your design is enhanced to have control and data hazard handling capabilities.

For the SoC design, requirements include:

1) The factorial accelerator should be able to handle 4-bit input data (n).
2) You should use the simple GPIO for FPGA validation. Specifically, the MIPS should read input (n) from on-board switch via GPIO, and display the result (n!) on on-board 7-segment LEDs, also via GPIO.
3) Your report should include an analytical performance comparison between the software-only and hardware-accelerated execution of the factorial function.

All the information you need (background, methodologies, technical details such as memory space allocation) are discussed in class and available from class Canvas site (Lecture Slices 14: I/O and Interface).

For this assignment, you are also expected to predict the expected performance of factorial computations between the single-cycle MIPS, pipelined MIPS, and SoC designs. Analysis of each design should be graphed, showing the relationship between runtime (in cycles) and the factorial input parameter.

As always, you should document your work professionally. In addition to descriptions and discussions, your report should include schematics (generated by Visio) of the pipelined MIPS micro architecture, including the pipelined datapath, the pipelined

control unit, and each of the memory modules. Your report should also include schematics of the SoC top-level, factorial module, and GPIO module. If your design contains hazard handling capabilities, the logic equations used for each function must be included. All source code must be attached and commented.

This is a four week laboratory assignment. In order to ensure that students are staying on track with the lab, there will be checkpoints for each lab session. Please see the following schedule of due dates to see what is due for each week:

Week	Due to be Checked by TA
Week #1 (week of 11/13)	1. Draft of pipelined MIPS microarchitecture schematic (digital copy only) 2. Draft of SoC interface schematic (digital copy only)
Week #2 (week of 11/20)	1. Tables for MIPS control unit (Microsoft Excel only) and memory maps for SoC interface 2. Performance analysis of hardware accelerated *n*! 3. Unit-level (with interface wrappers) simulation waveforms
Week #3 (week of 11/27)	1. Completed interface design for the SoC with the single-cycle MIPS processor (from Lab 7), the factorial unit (from Lab 1) and the simple GPIO 2. Demo of the integrated SoC on Nexys4 FPGA.
Week #4 (week of 12/4)	1. Completed integration of the SoC using a pipelined MIPS processor 2. Demo of this upgraded SoC on Nexys4 FPGA.