

San Jose State University
Department of Computer Engineering

CMPE 140 Lab Report

Lab 5 Report

Title Processor Design (1): Design Code Review and Functional Verification

Semester Fall 2018

Date 10/9/18

by

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Lab Checkup Record

Week	Performed By (signature)	Checked By (signature)	Tasks Successfully Completed*	Tasks Partially Completed*	Tasks Failed or Not Performed*
1					

*** Detailed descriptions must be given in the report.**