Write and Read to AT45

Algorithm for Write data to buffer

1. Select (CS =0)
2. Command (0x84 for Buffer 1, 0x87 for Buffer 2)
3. Three bytes address
4. Data (1-256 bytes)
5. Deselect (CS=1)

Algorithm write buffer to flash

1. Select (CS =0)
2. Command (0x83 for Buffer 1, 0x86 for Buffer2)
3. Three bytes address
4. Deselect (CS=1)

Algorithm for read buffer

1. Select (CS =0)
2. Command (0xd4 for Buffer 1, 0xd6 for Buffer 2)
3. Three bytes address
4. don't care bits (1 byte)
5. Data (1-256 bytes)
6. Deselect (CS=1)

Algorithm for read flash to buffer

1. Select (CS =0)
2. Command (0x53 for Buffer 1, 0x55 Buffer 2)
3. Three bytes address
4. Deselect (CS=1)

SPI Protocol from Coding Perspective

```
#define SPI_DELAY 1000
int main (void)
{ int i;
InitSSP1();
        for ( i = 0; i < 10000; i++ );
        printf("Device ID\n");
        LPC_GPIO0->FIOCLR = (1<<6);
        printf("\n 0\t %x",SSP1exchangeByte(0x9f));
        printf("\n 1\t %x",SSP1exchangeByte(0x9f));
        printf("\n 2\t %x",SSP1exchangeByte(0x00));
        printf("\n 3\t %x",SSP1exchangeByte(0x00));
        LPC_GPIO2->FIOSET = (1<<6);
        for ( i = 0; i < 10000; i++ );
        printf("\n*********************************\n");
        //***Write to buffer1
        initSSP1();
        printf("\nWriting to Buffer 1\n");
        LPC_GPIO0->FIOCLR = (1<<6);
        SSP1exchangeByte(0x84); //Send 3 Bytes = 16 don't care bits + 8 (1st Byte of buffer) bits
        SSP1exchangeByte(0x00);
        SSP1exchangeByte(0x00);
        SSP1exchangeByte(0x00);
```

1

This register controls the state of output pins. Writing 1s produces low

Table 102. GPIO register, pp 131

2

SPI Pins

VB (battery supply)		VBAT	J2-3
RESET_N		TARGET_RESET	J2-4
P0.9	MOSI1	P0.9	J2-5
P0.8	MISO1	P0.8	J2-6
P0.7	SCK1	P0.7	J2-7
P0.6	SSEL1	P0.6	J2-8

Source: From SCH revis

1

LPC_GPIO0->FIOCLR = (1<<6);

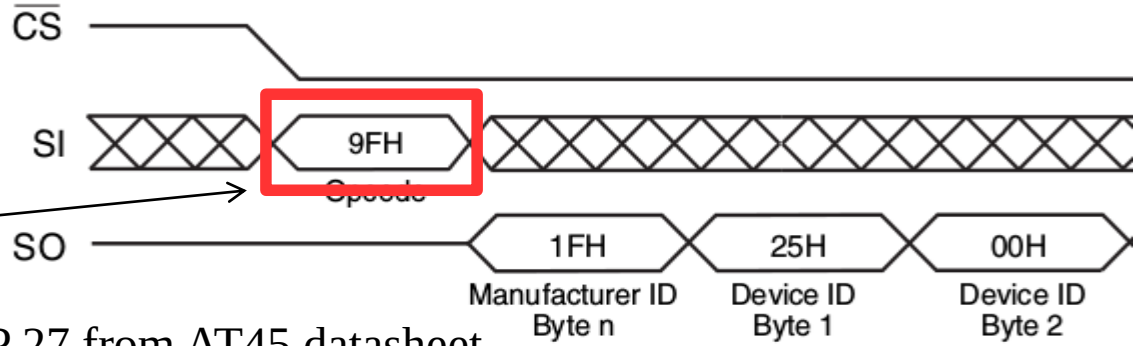
Writing 1 to P0.6 which is SSEL1 produces low, if SSP1 controller is enabled by active low then this will e

2

SSP1exchangeByte(0x9f)

A module to write a byte to SSP1

Opcode 0x9f for manufacturer, device I



PP 27 from AT45 datasheet

Write and Read to SSP Port

SSP reference from CPU data sheet, Chapt

```
uint8_t SSP1exchangeByte(uint8_t out){
    LPC_SSP1->DR = out;
    while(LPC_SSP1->SR & (1<<4));
    return LPC_SSP1->DR;
}
```

Table 370. SSP special purpose register m

DR	Data Register. Writes fill the transmit FIFO, and reads empty the receive FIFO.	R/W	0

18.6.3 SSPn Data Register

SR	Status Register	Read only	O

Write to DR: software can write data to be sent in a future frame to DR when TNF bit = 1 in SR

Read from DR: software can read data from DR register when RNE = 1 of SR, Status register, in

SR Register of the SSP Port

18.6.4 SSPn Status Register (SSP0SR - 0x4008 800C, SSP1SR - 0x4003 000C) Pp 433

SR	Status Register	Read only O

Table 374: SSPn Status Register (SSP0SR - address 0x4008 800C, SSP1SR - 0x4003 000C) bit descripti

Bit	Symbol
0	TFE
1	TNF
2	RNE
3	RFF
4	BSY
31:5	-

```
while(LPC_SSP1->SR & (1<<4));
return LPC_SSP1->DR;
```

"Transmit FIF0 Not Full. This bit is 0 if the Tx FIF0 is full, 1 if not." fron

"Receive FIF0 Not Empty. This bit is 0 if the Receive FIF0 is empty, 1 i

Busy. This bit is 0 if the SSPn controller is idle, or 1 if it is currently sen