CMPE 125 Lab 5 Assignments

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Parallel Unsigned Integer Multiplier

Purpose:

1) To be familiar with designing function units using both combinational and sequential building blocks
2) To be familiar with the concept and technique of pipelining
3) To be familiar with the design/verification/validation flow and EDA tool used

Preparation:

Study Lecture Slides 6 and the relevant materials available on the class Canvas site.

Tasks:

Given the following building blocks:

- Parameterized D registers as shown on Page 6 of Lecture Slides 6
- AND units as shown on Page 14 of Lecture Slides 6
- Carry-look-ahead adders accomplished in Assignment 4

1. Design a 4-bit *combinational* unsigned integer multiplier based on the parallel architecture shown on Page 15 of Lecture Slides 6, and write a self-checking Verilog testbench to functionally verify your design. Note:

   a) You can use two slices of 4-bit carry-look-ahead adders to make an 8-bit adder.
   b) For functional verification, you can use an "inferred" (by using the Verilog multiplication operator *) 4-bit integer multiplier as the reference model.

2. Based on Task 1, design a *two-stage pipelined* integer multiplier by attaching input/output registers, and inserting stage registers, as shown on Page 16 of Lecture Slides 6. To test your design, you must perform both functional verification (software simulation) and hardware validation (FPGA prototyping using the Nexys4 DDR board). Note:

   For hardware validation, you should use a manual-driven clock and to do so, a debouncer must be used. Verilog source code for the debouncer can be found in the file "debounce2.v" on the class Canvas site.

Contents of Report:

1) Cover page.
2) A list of successfully accomplished tasks.
3) Your test plan (i.e., how to verify the design)
4) Commented source code (design and verification)
5) Captured verification results (waveforms/simulation log files)
6) Validation (hardware prototyping) setup and source codes

7) Descriptions and analysis on your observations
8) Detailed descriptions of the task(s) that you cannot, or did not accomplish, including reason(s) and/or your analysis.

Report checklist

Follow the "CMPE 125 Lab Report Guidelines" document on Canvas.

Your report should include these sections:

- Cover page *(with name, SID, and the Lab Record filled out with your name, TA's name, and lab demo score)*

- Introduction *(1 paragraph)*

- Design methodology *(1 paragraph for each module: combinational multiplier, pipelined multiplier)*
    - Block diagrams:
        - Parameterized D register
        - AND module
        - 8-bit adder (containing two 4-bit CLA adders)
        - Combinatorial unsigned integer multiplier
        - Two-stage pipelined integer multiplier

- Test plan for simulation *(1 paragraph for each module: combinational multiplier, pipelined multiplier)*
    - **No waveforms** as we are using self-checking test benches.
    - Console output from simulator (as a picture), one for <u>each</u> module.

- Test plan for FPGA board *(1 paragraph)*
    - Include photograph of FPGA board showing results with a caption that clearly labels the state of the switches and LEDs.

- Conclusion *(1 paragraph)*
    - In addition if you could not complete any part of the lab explain clearly what went wrong and how you could have remedied the problem.

- Appendix
    - Any tables or other diagrams go here that don't fit in the other sections.

- Source code
    - Use a fixed-width font such as `Courier New` for the source code.
    - Clearly label the file name of each source file you include.
    - Include **all** source code you used in the project, including constraints.