[[1]](#footnote-1)

CmpE 124 Lab 7: Multiplier Design

Anahit Sarao, 008435583, CmpE 124 Fall 2015, Lab Section 2

*Abstract*—This labs purpose was to create a binary multiplier by using logic gates and Boolean Equations. The multiplier design involved two full adders which are used to multiply binary numbers.

# INTRODUCTION

In this lab a 3-bit binary multiplier was designed using two full adders and a clock. By finding the equation for the multiplier a simple circuit design was constructed. Using two 4-bit full adders the extra bit is used for the carry. The design and testing was done in logicworks software.

# Design methodology

## Parts List

* Logicworks

## Truth Tables

Full Adder Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Cin | A | B | Sum | Cout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |

Full Adder Voltage Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Cin ++ | A ++ | B ++ | Sum ++ | Cout ++ |
| L | L | L | L | L |
| L | L | T | T | L |
| L | T | L | T | L |
| L | T | T | L | T |
| T | L | L | L | L |
| T | L | T | T | T |
| T | T | L | T | T |
| T | T | T | L | T |

## Karnaugh Maps

N/A

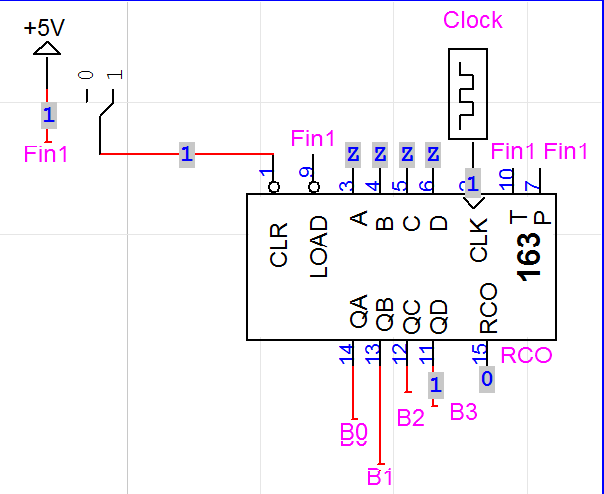
## Original and Derived Equations

For C= aj \* bj

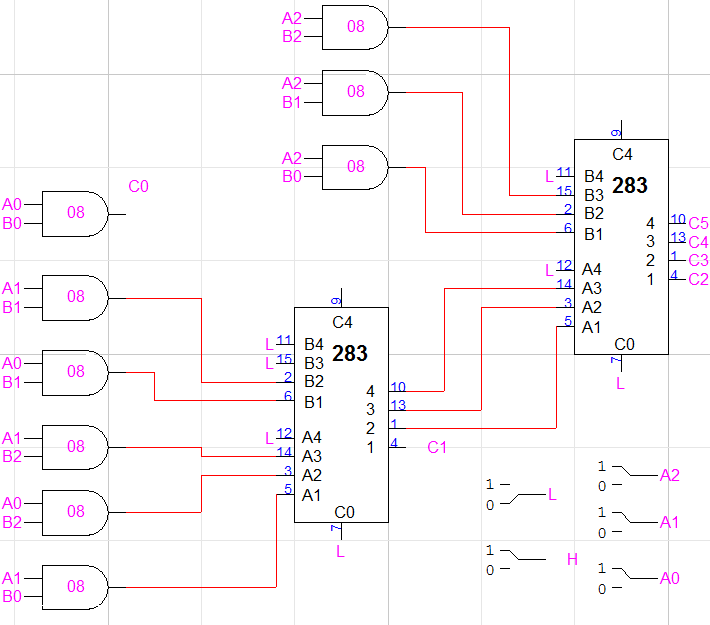
1. C0= a0b0
2. C1= a1b0 + a0b1
3. C2= a2b0+ a1b1+ a0b2
4. C3= a2b1+ a1b2
5. C4= a2b2
6. C5=0 or 1 (Carry bit)

## Schematics

Schematic 1: Clock



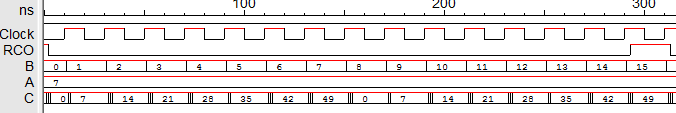
Schematic 2: Multiplier



# testing procedures

1. Multiply 111\*111 on paper. For each bit construct an equation.
2. Using the equations design a circuit.
3. Looking at waveforms the output of the second adder must be the product of Aj \*Bj

Waveform 1: Multiplier Simulation



# testing results

From waveform 1 A is a constant 7 also 111 in binary. While B is the clock which counts from 0-15. C is the product of A and B, from clock counts 0-7 the product are correct. After clock count 7 the products are not correct as there is not enough bits to compute the product. The circuit shown in schematic 2 generates six outputs. It simply preforms AND operation on the inputs and adds the output to the adder to give the product. This proves the functionality and correctness of the circuit and waveforms.

# Conclusion

In this lab a 3-bit binary multiplier was designed and simulated. The purpose of the multiplier is to multiply two 3-bit binary numbers and acquire the product. By using two full adders the equations were verified logicwork waveforms. There is no multiple operation within chipsets so when two binary numbers needs multiplication the chip uses addition operation to create the product.

# appendices and references

N/A

1. Anahit Sarao, [indianvip60@gmail.com](mailto:indianvip60@gmail.com) [↑](#footnote-ref-1)