***Introduction***

***Design Methodology***

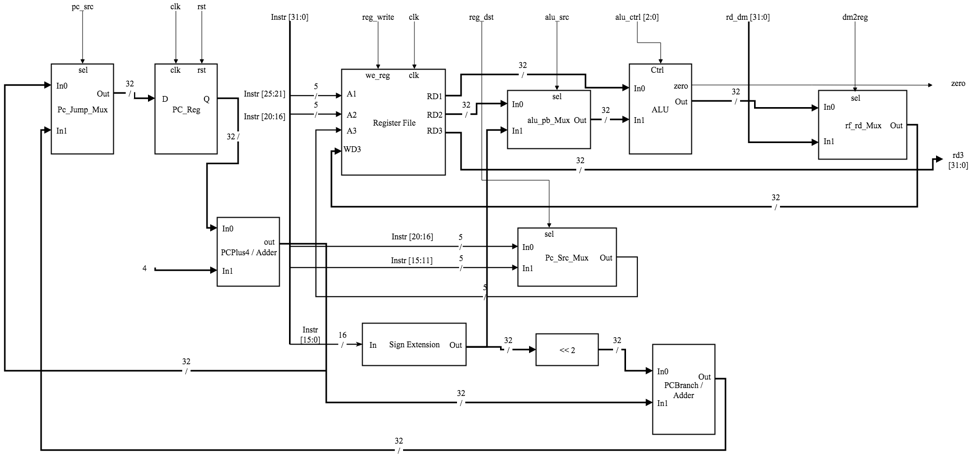


Figure 1. Data Path Diagram

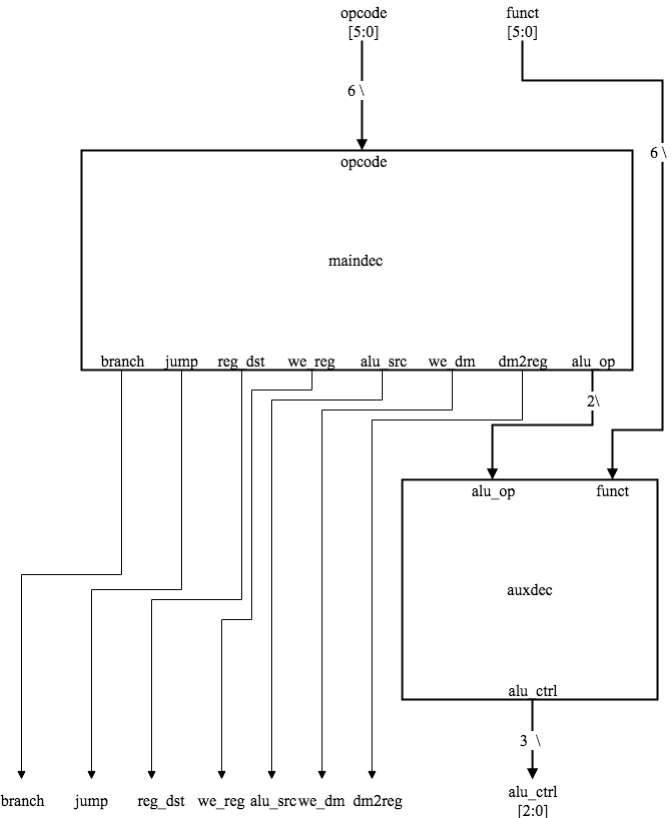


Figure 2. Control Unit Diagram

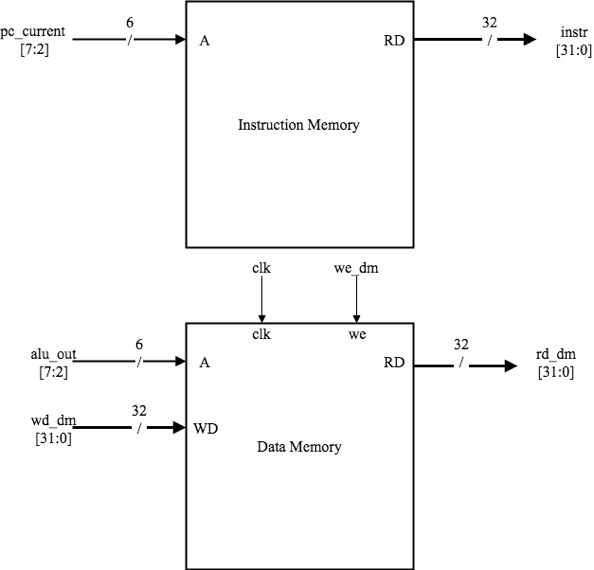


Figure 3. Instruction Memory and Data Memory Diagram

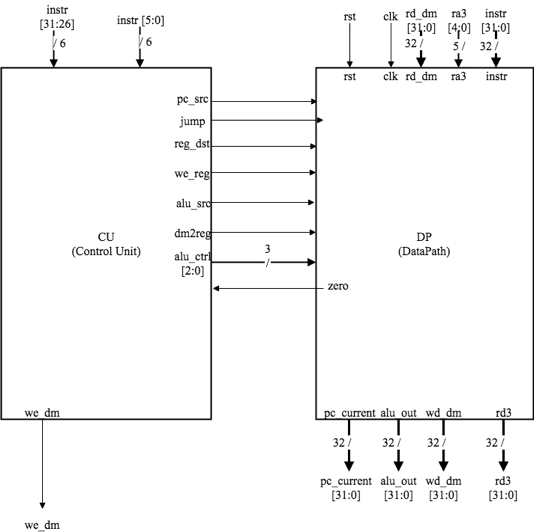


Figure 4. Control Unit and Data Path Diagram

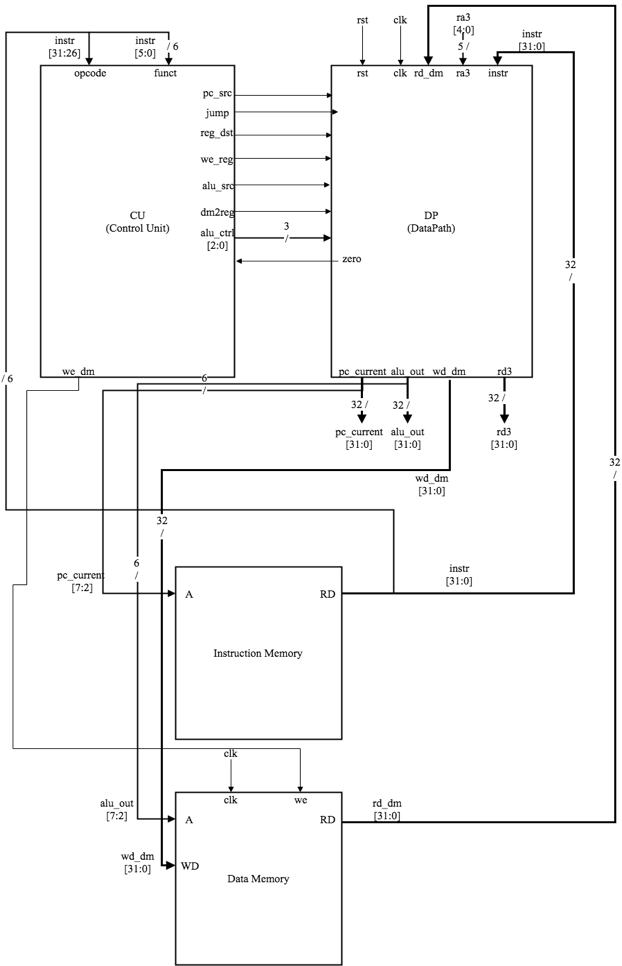


Figure 5. Complete Processor Diagram

***Simulation Test Plan***

***FPGA Test Plan***

***Conclusion***

***Appendix***

***Source Code***