1. (a) Design a 1-bit 2-to-1 multiplexer using Verilog primitives.

(b) Design a 2-bit 4-to-1 multiplexer using 1-bit 2-to-1 multiplexers and primitives.

|  |  |
| --- | --- |
| Mux2to1 |  |
| Testfixture |  |
| wave |  |
| Run |  |

|  |  |
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| Mux2to1 |  |
| Mux4to1 |  |
| Testfixture |  |
| wave |  |
| Run |  |

2. (a) Design a Full Adder using Verilog primitives.

(b) Design a 4-bit Adder using full adder and primitives.

|  |  |
| --- | --- |
| FullAdder |  |
| Testfixture |  |
| wave |  |
| Run |  |

|  |  |
| --- | --- |
| FullAdder |  |
| 4bit-adder |  |
| Testfixture |  |
| wave |  |
| Run | ellipsis |