1. Design a pipelined addition-multiplication circuit as shown in Figure 1.

|  |  |
| --- | --- |
| Mux4to1 |  |
| Testfixture |  |
| wave |  |
| Run |  |

2. Design a simplified pipelined MIPSR2000 datapath as shown in Figure 2.

|  |  |
| --- | --- |
| ALU |  |
| Testfixture |  |
| Run |  |

