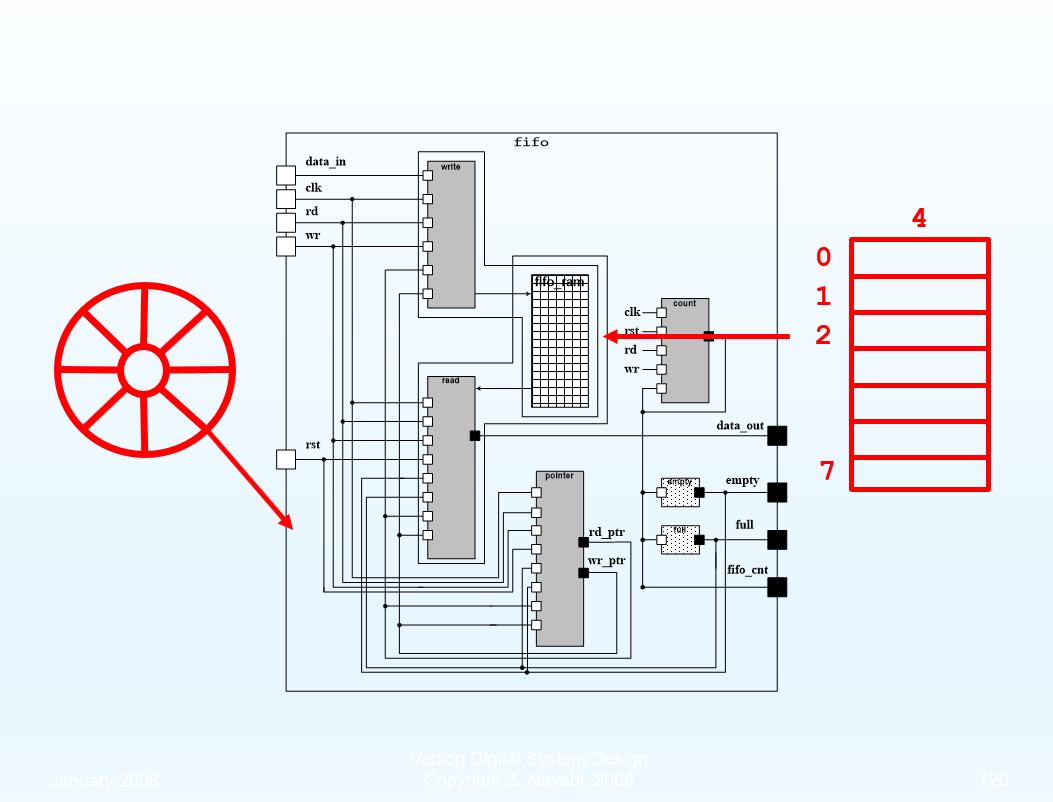
1. Design a FIFO (8 entries x 4bit). The FIFO has the following inputs: Data\_in (4-bit), read, write, clk, rst, and the following outputs: Data\_out, empty, full, count.

|  |  |
| --- | --- |
| FIFO |  |
| Testfixture |  |
| wave |  |
| Run |  |



3. Design a string 010/001 detector using (a) Moore FSM (b) Mealy FSM

|  |  |
| --- | --- |
| Moore |  |
| wave | 001  001 |
| Run | moore的輸出只跟目前狀態有關，所以只需要在posedge確認 |

|  |  |
| --- | --- |
| Mealy |  |
| wave |  |
| Run | mealy是跟當前狀態和輸入有關，所以X有變就要判斷Z  010  010 |