

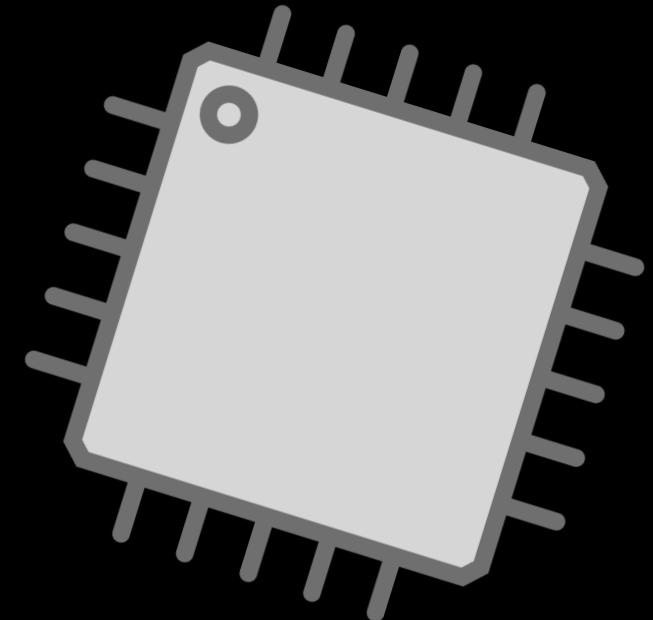
Cadence  
Full-Custom IC Design

# One Chip Design

SHIN HONGMIN

# INDEX

- Program & Tool
- Digital Circuits & Analog Circuits  
(Schematic / Simulation / Layout)
- Team Project
- One Chip  
(Schematic / Simulation / Layout)



# Program & Tool

- Cadence Virtuoso Schematic Editor / Layout Editor
- Cadence Virtuoso Spectre / ADE
- Assura(DRC & LVS)
- GPKD090

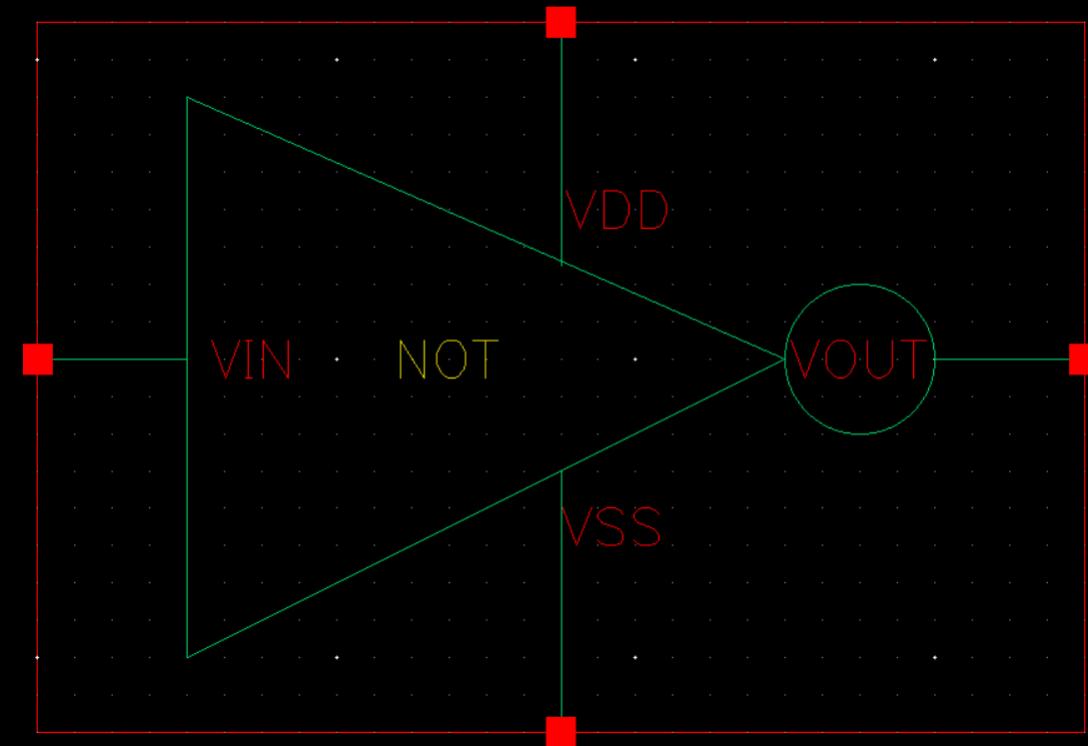
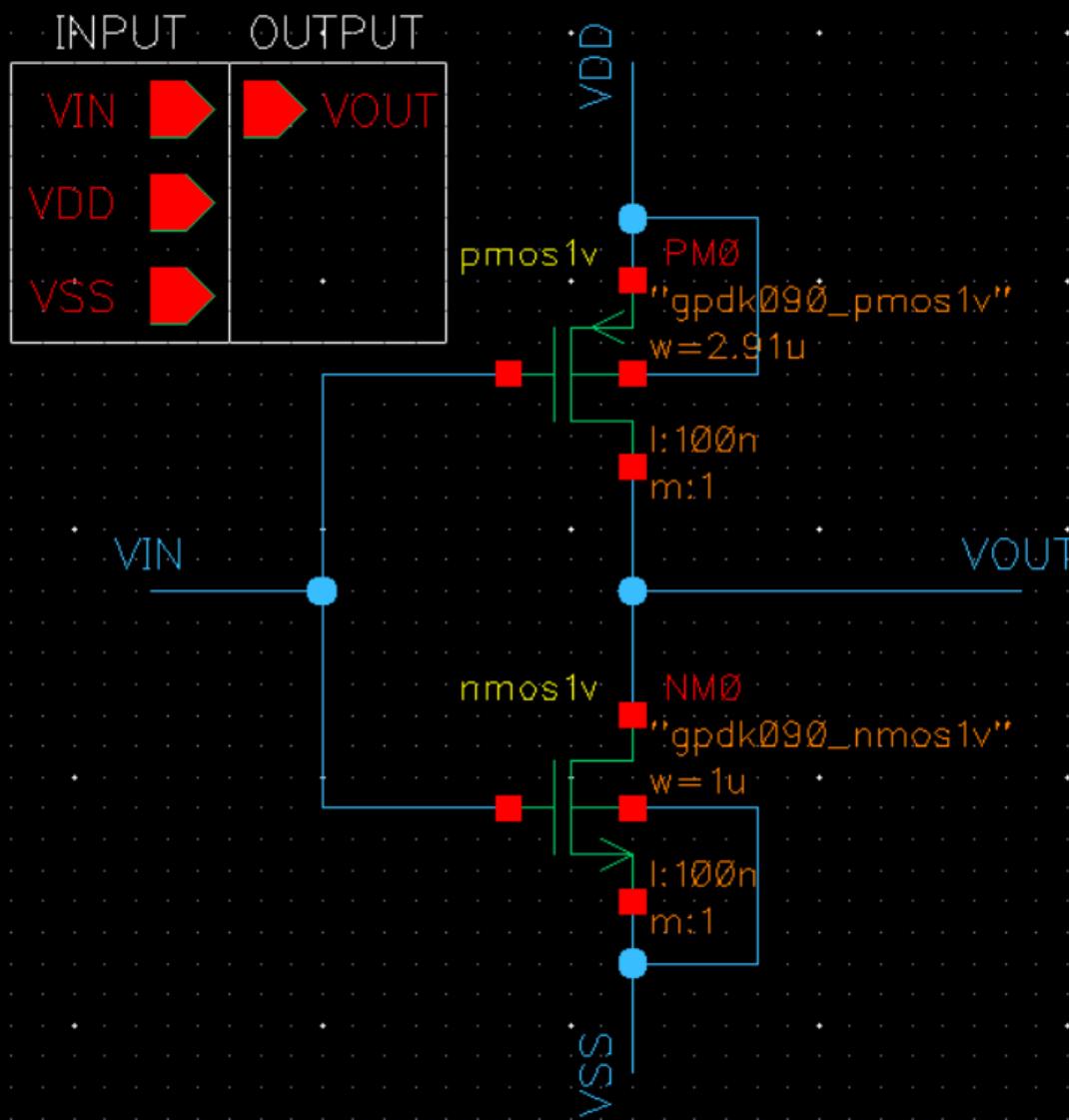
# Digital Circuits & Analog Circuits

- Digital Logic Gates
  - NOT / SWITCH
  - 2NAND / 3NAND / 4NAND
  - 2NOR / 3NAR / 4NOR
- Digital Circuits
  - 2x1 MUX / 4x1 MUX / 8x1 MUX / 16x1 MUX (Difference Logic & Switch)
  - HALF\_ADDER / FULL\_ADDER / 4BIT\_ADDER / 4BIT SUBTRACTOR
- Analog Circuits
  - Common Source Amp / Differential Amp (Single-ended Output)

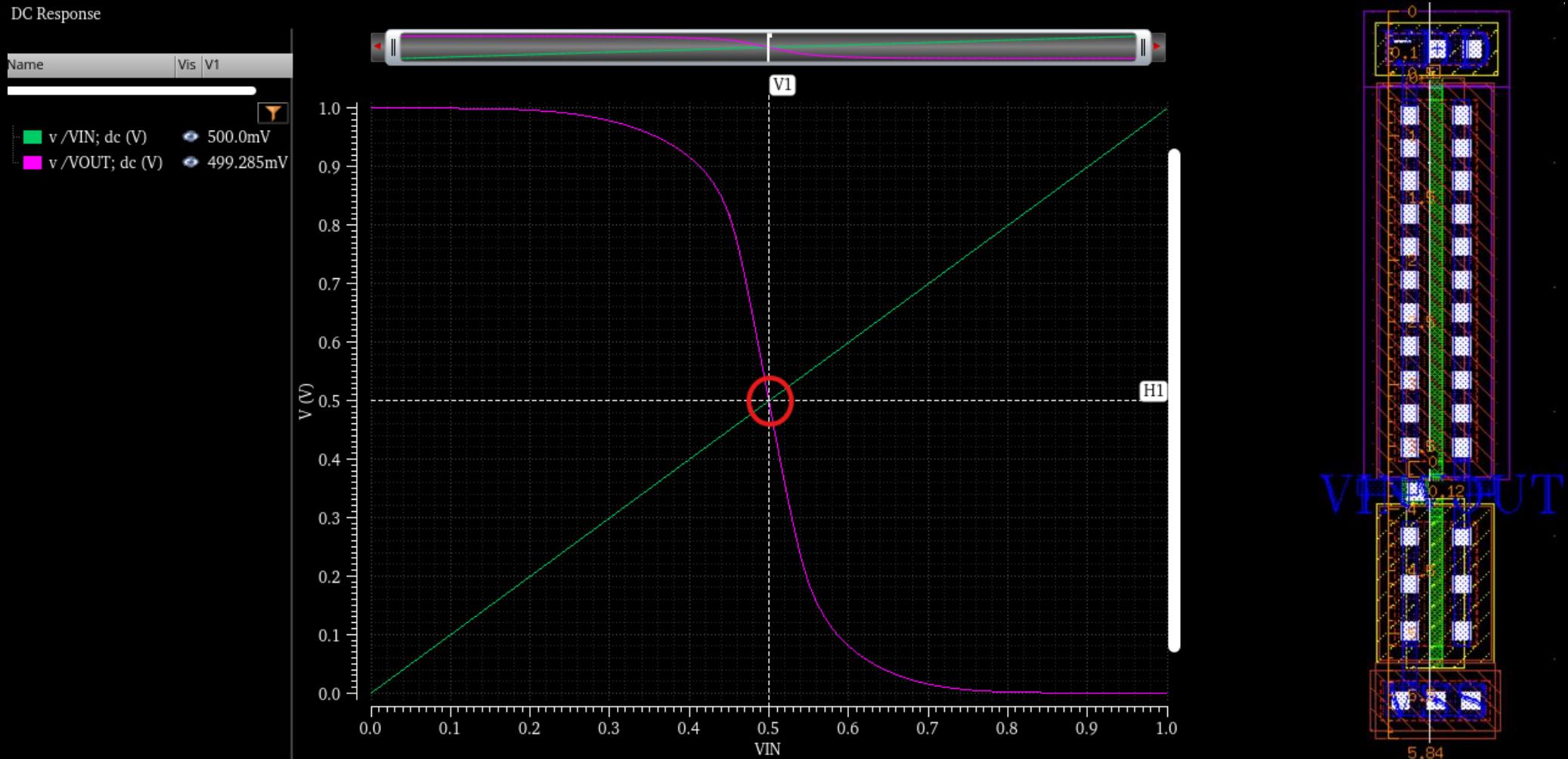
# Digital Logic Gate

- NOT / SWITCH / 2XOR
- 2NAND / 3NAND / 4NAND
- 2NOR / 3NOR / 4NOR

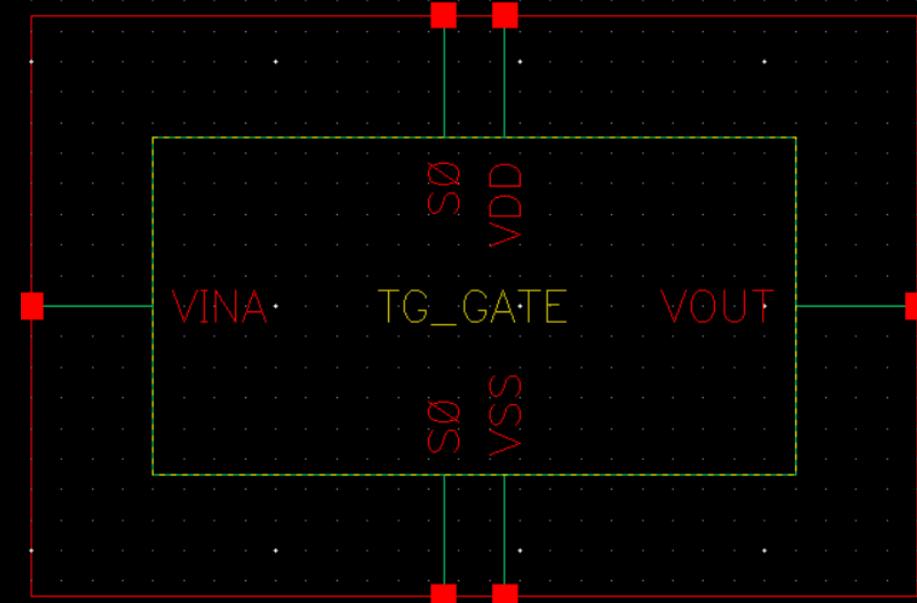
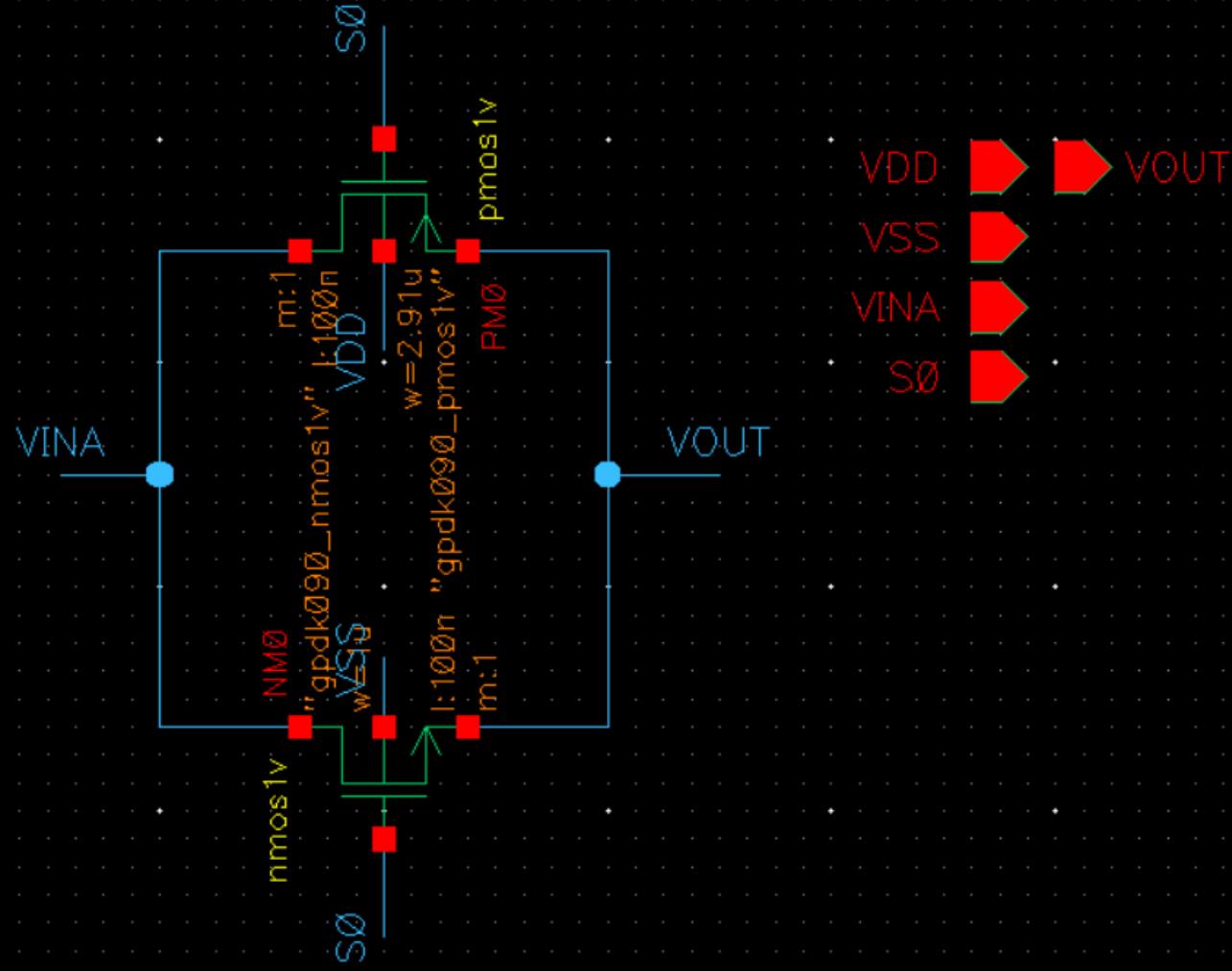
# NOT – Schematic & Symbol



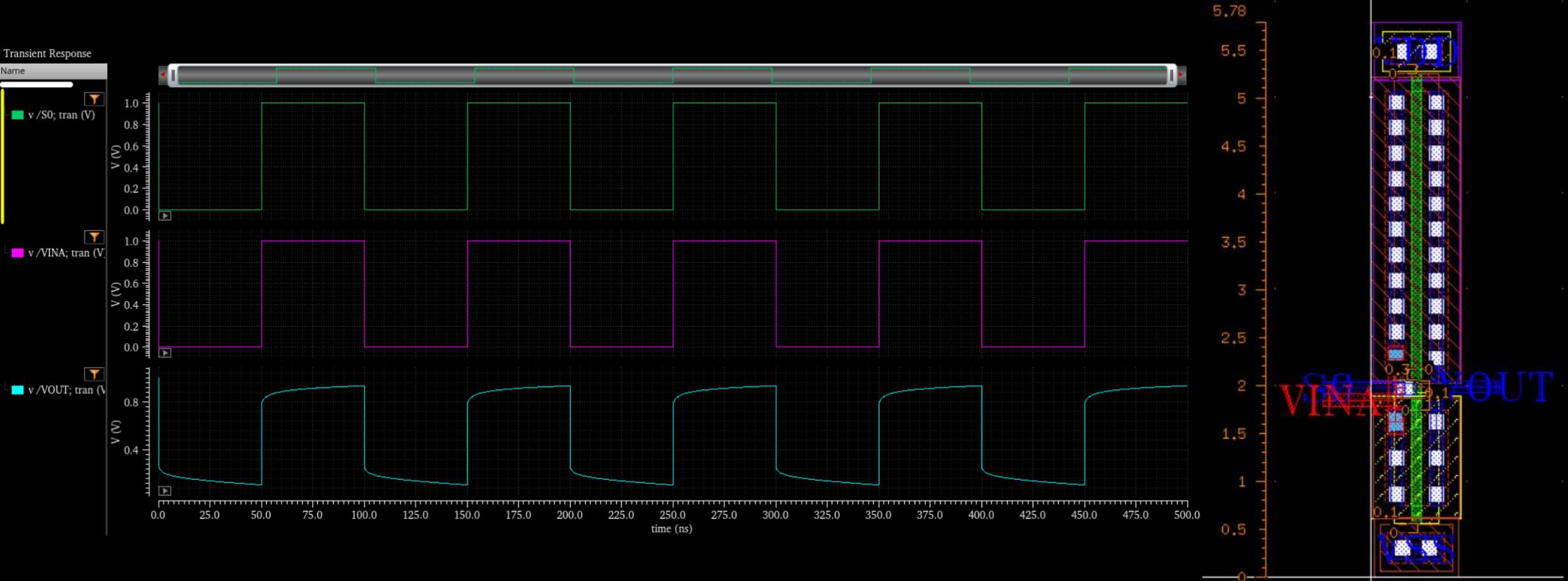
# NOT - Simulation & Layout



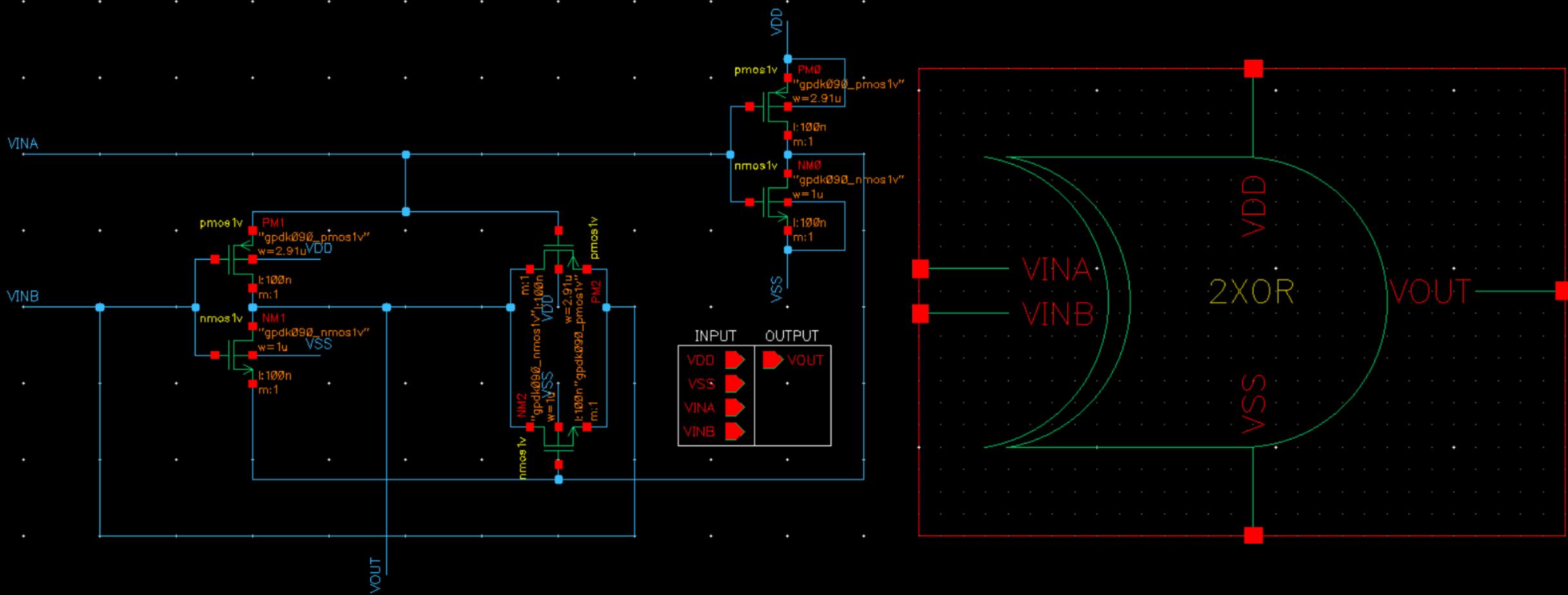
# Switch - Schematic & Symbol



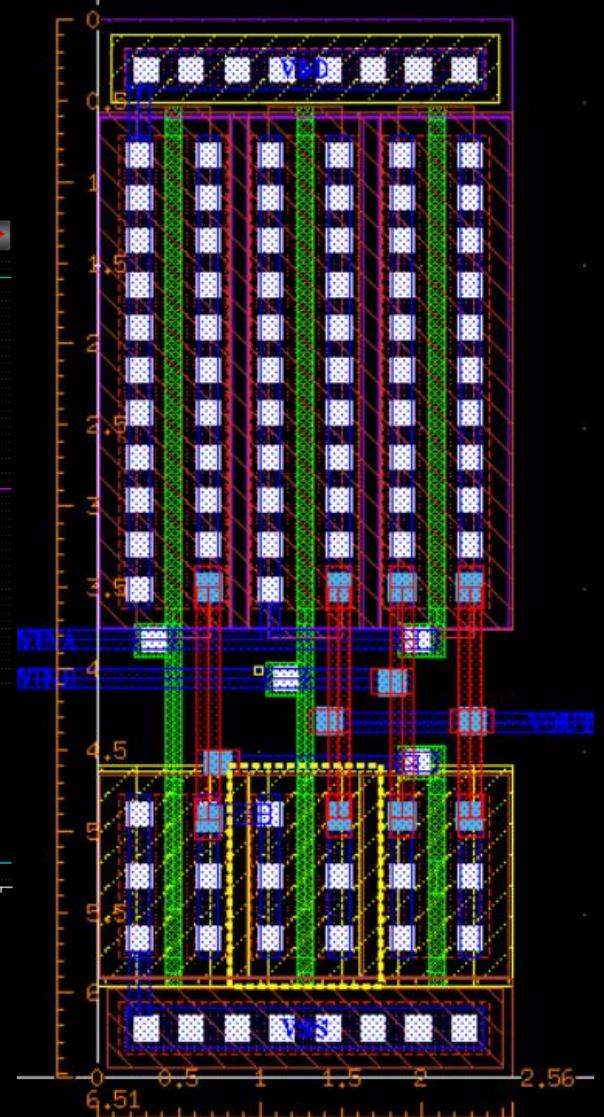
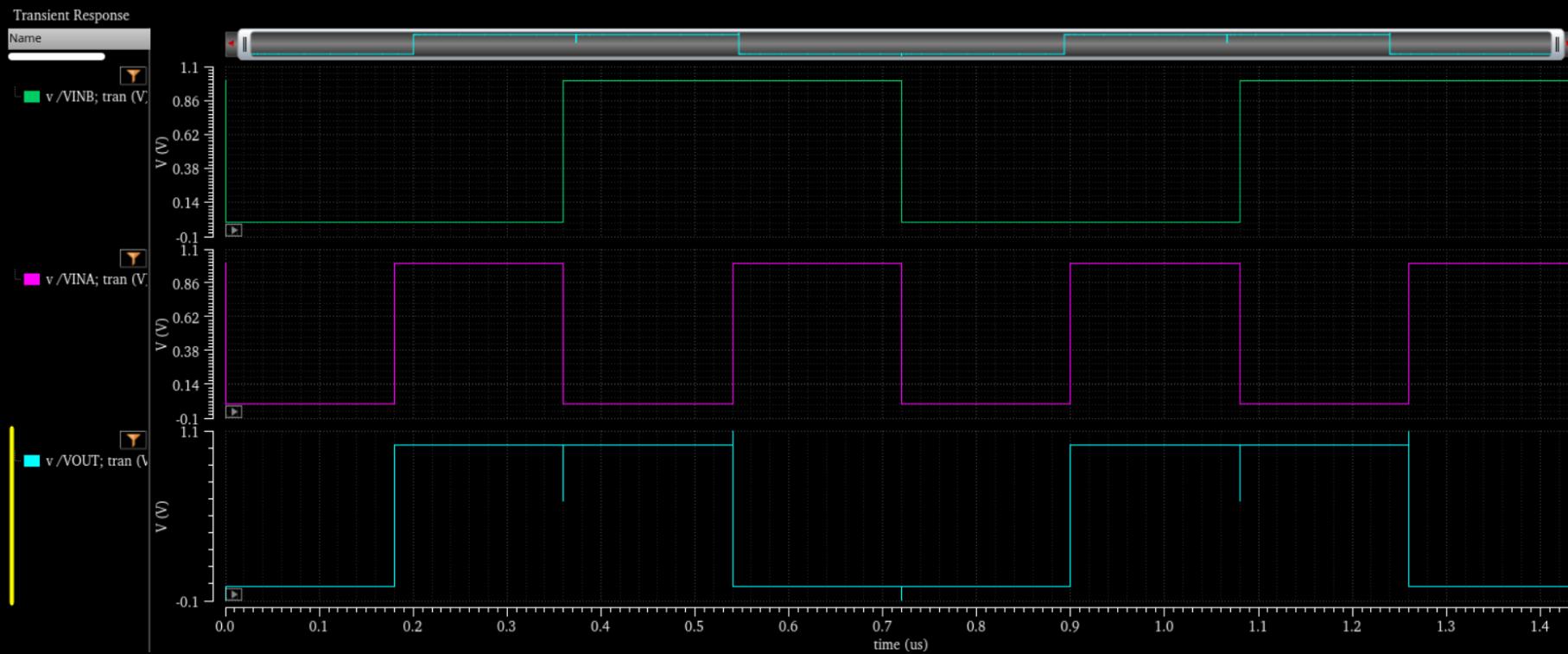
# Switch – Simulation & Layout



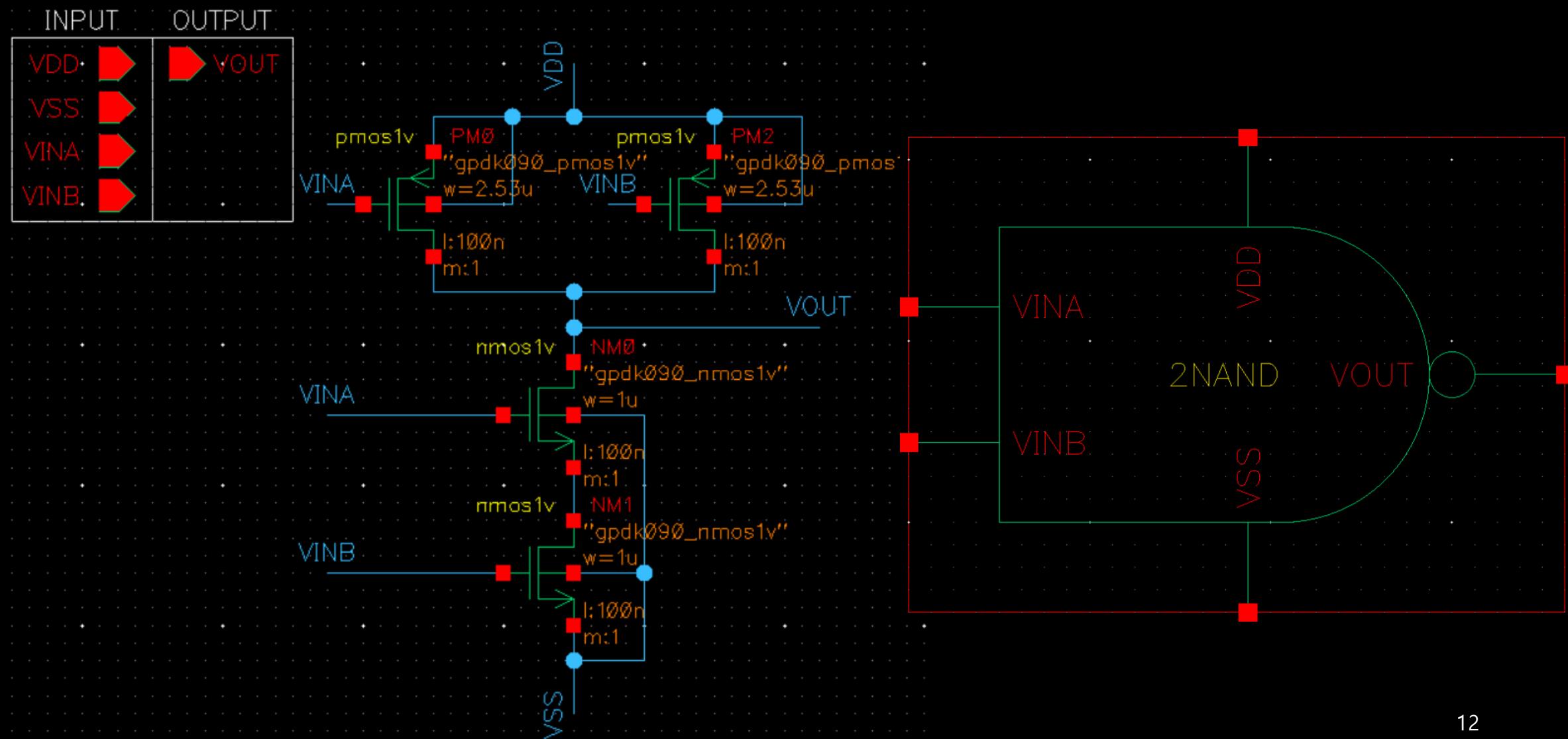
# 2XOR - Schematic & Symbol



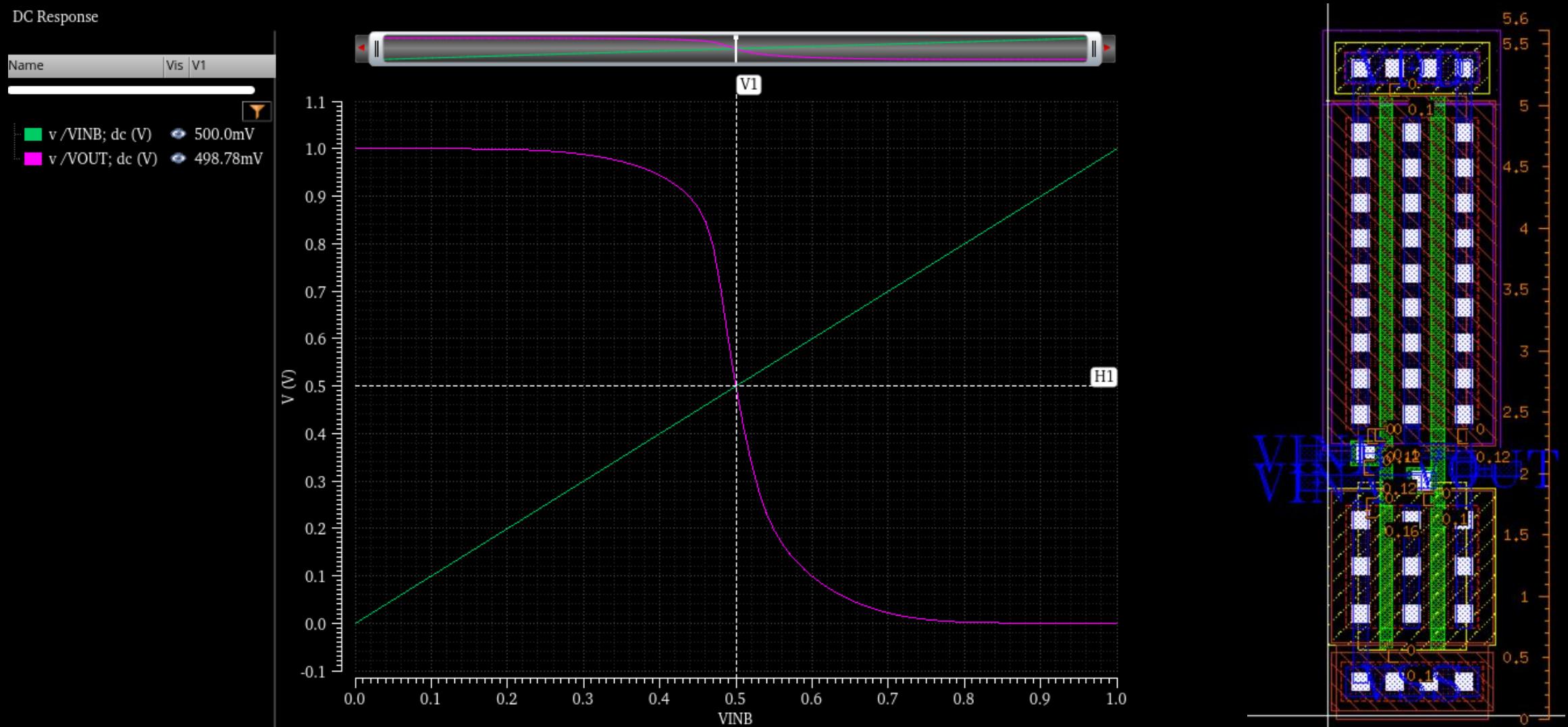
# 2XOR - Simulation & Layout



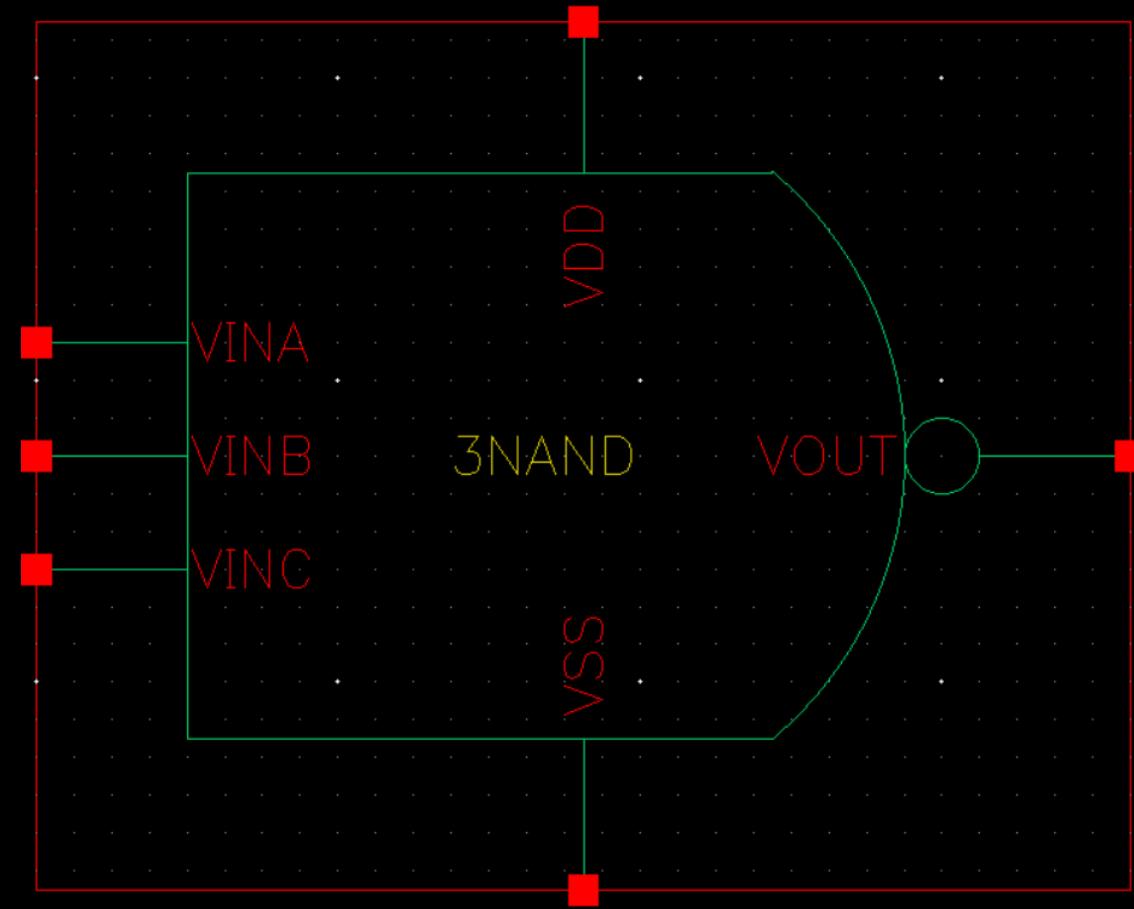
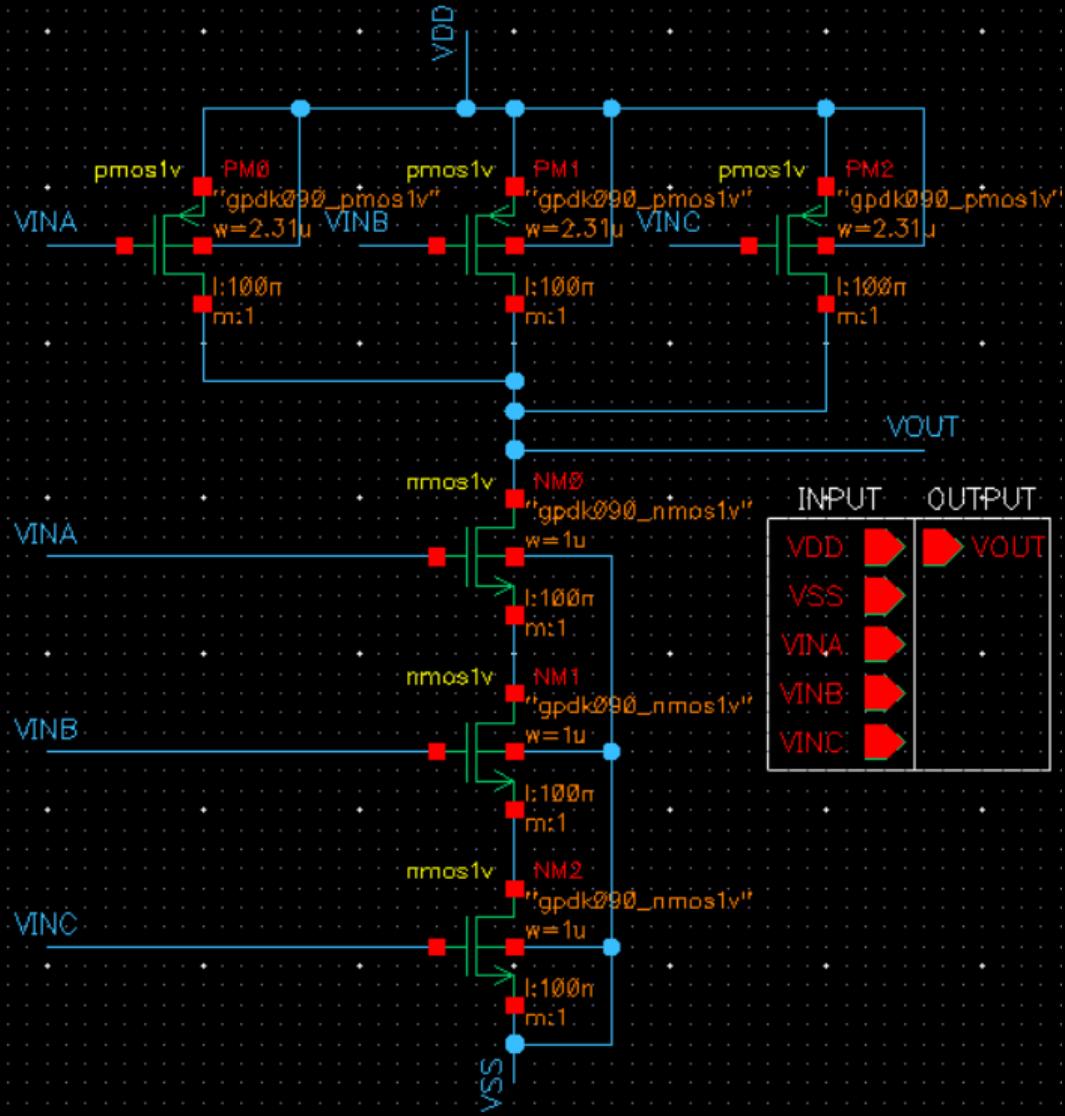
# 2NAND - Schematic & Symbol



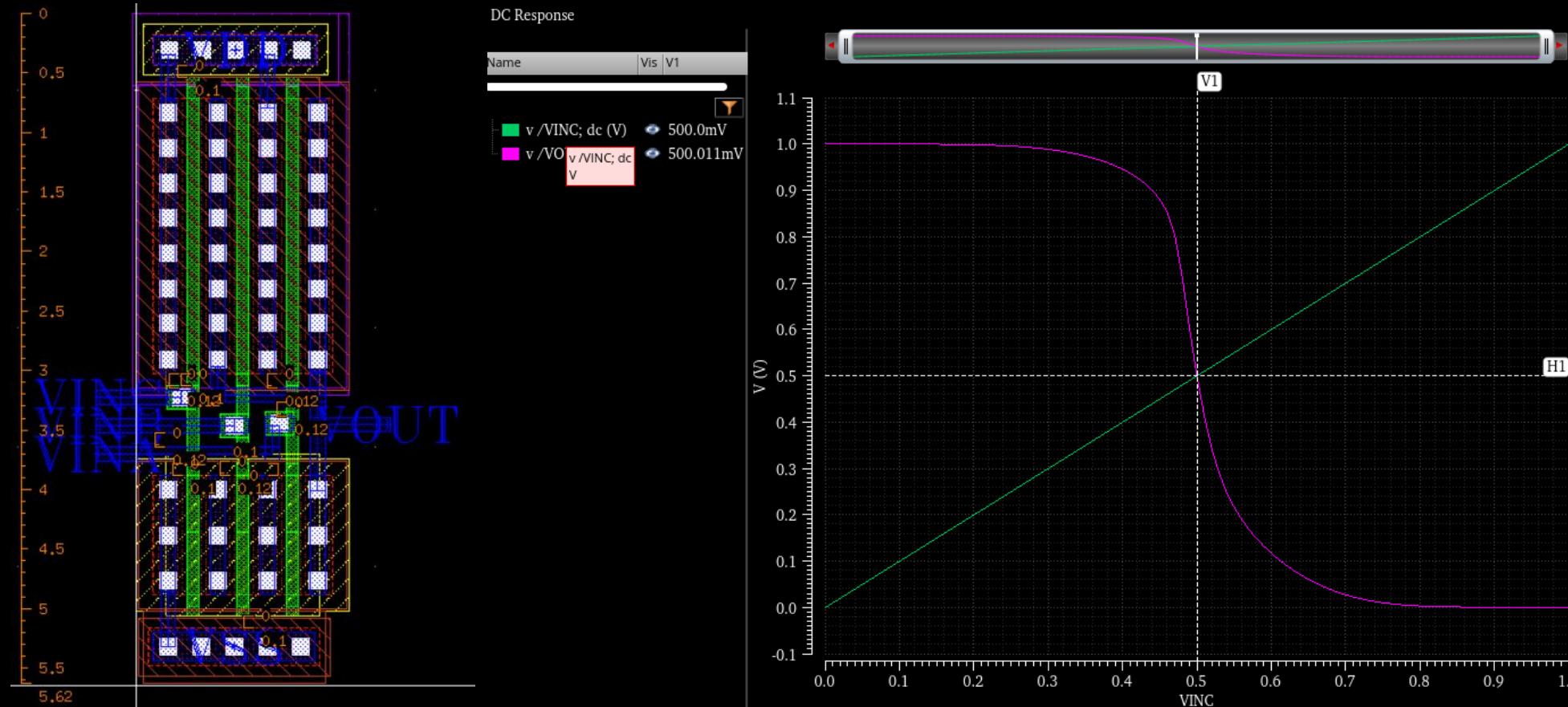
# 2NAND - Simulation & Layout



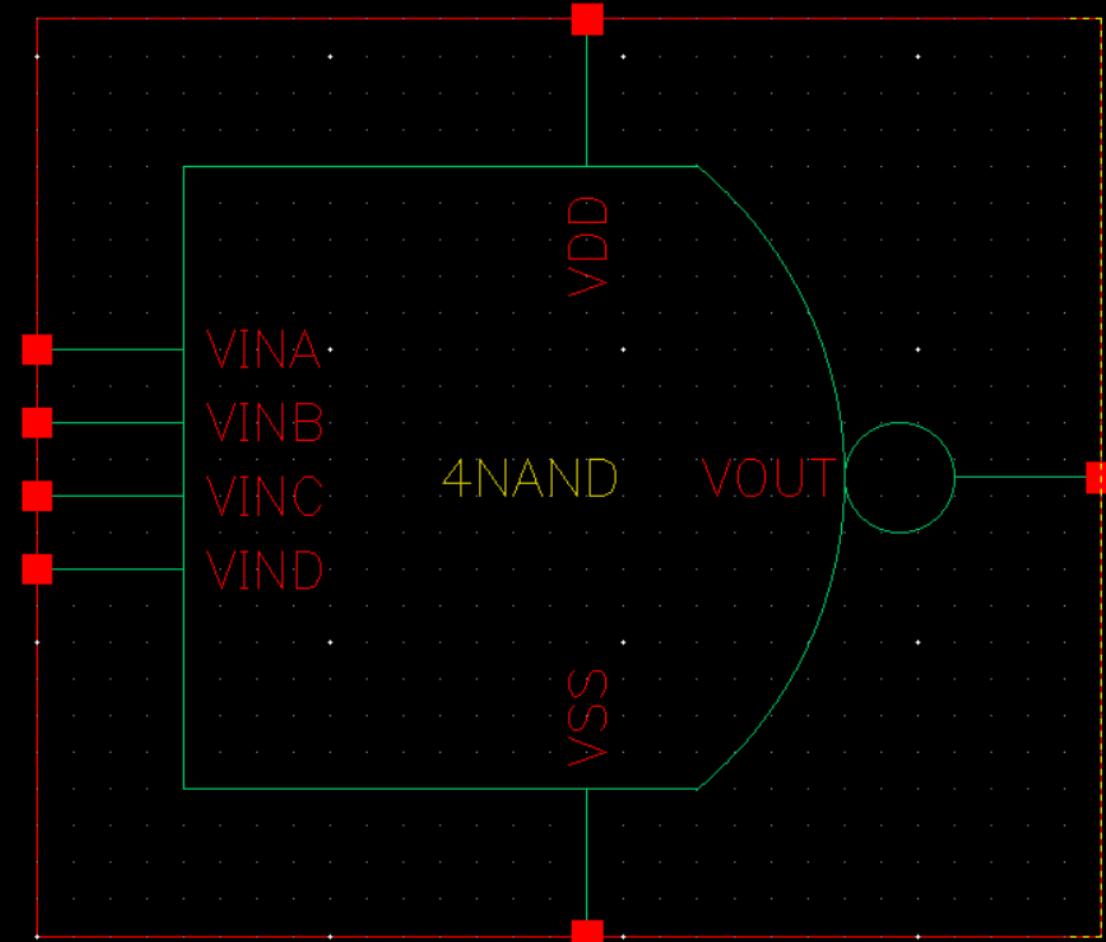
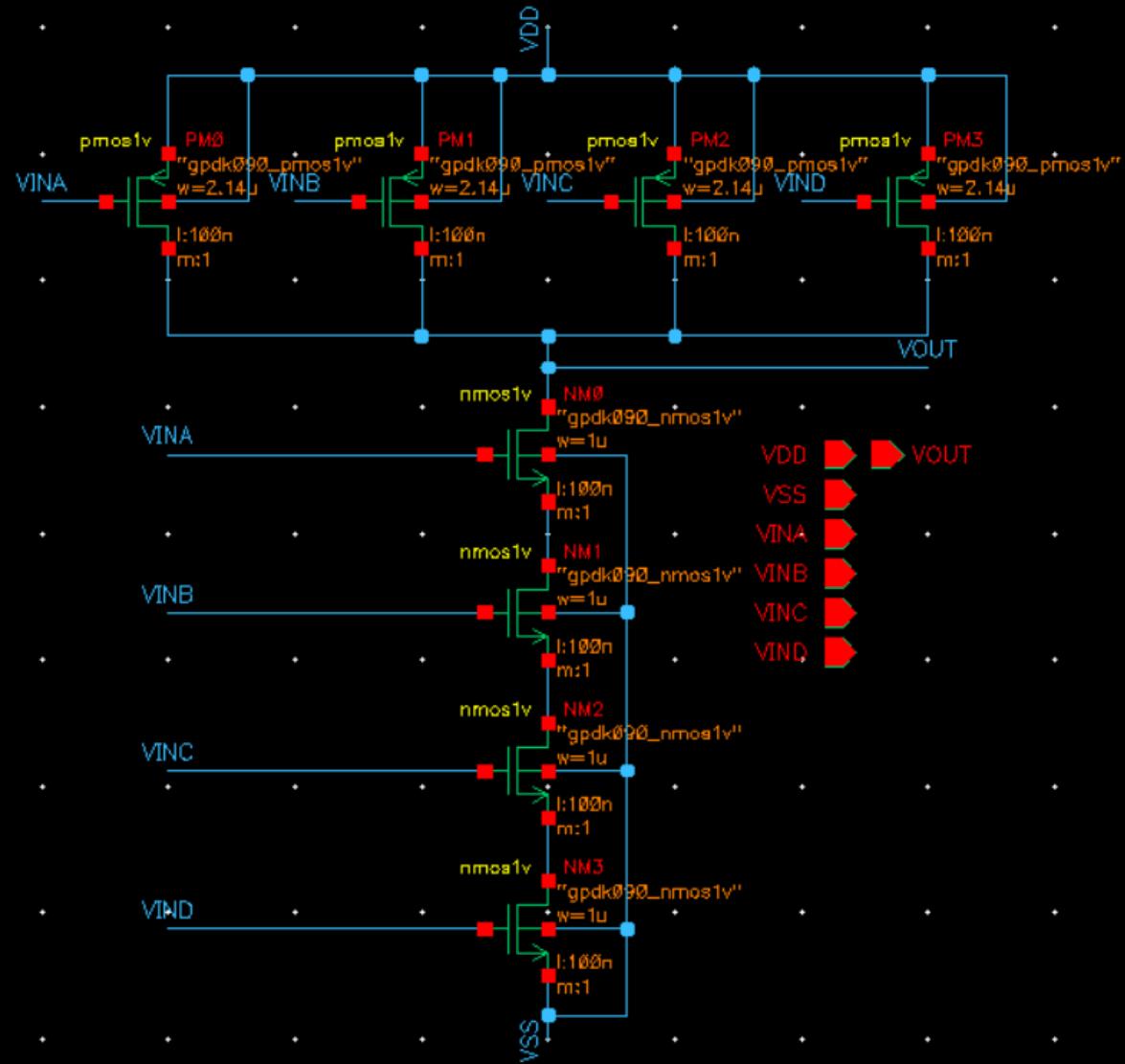
# 3NAND – Schematic & Symbol



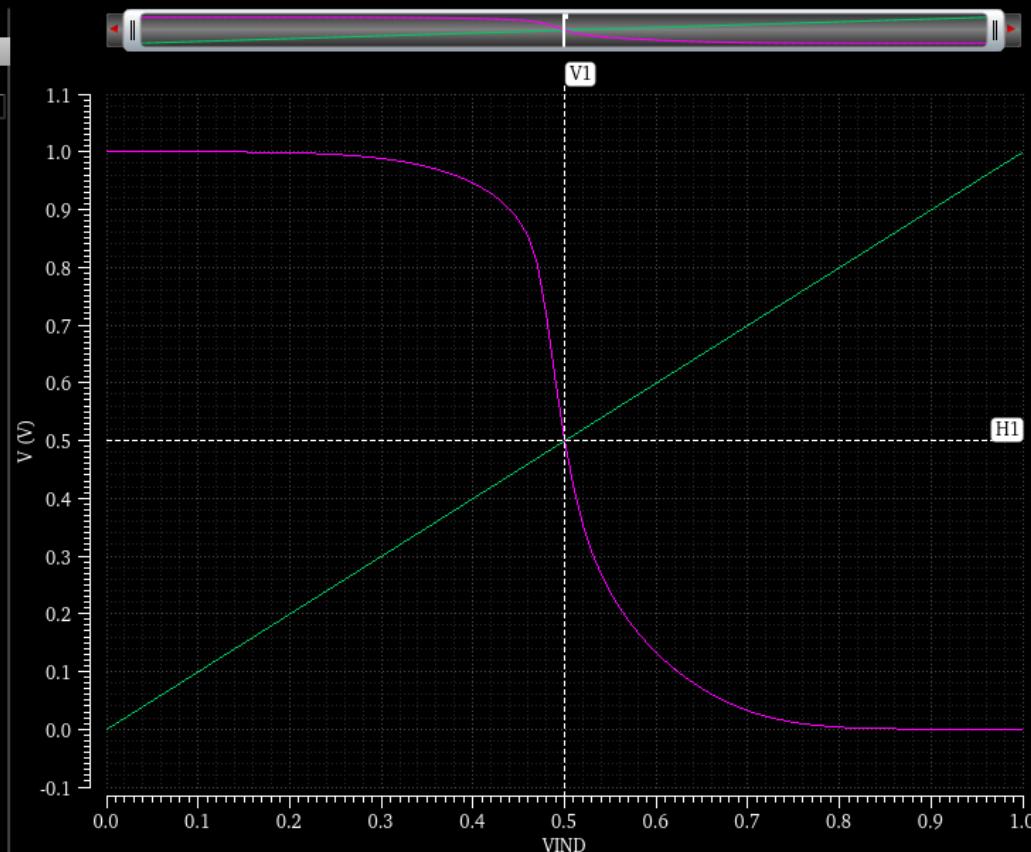
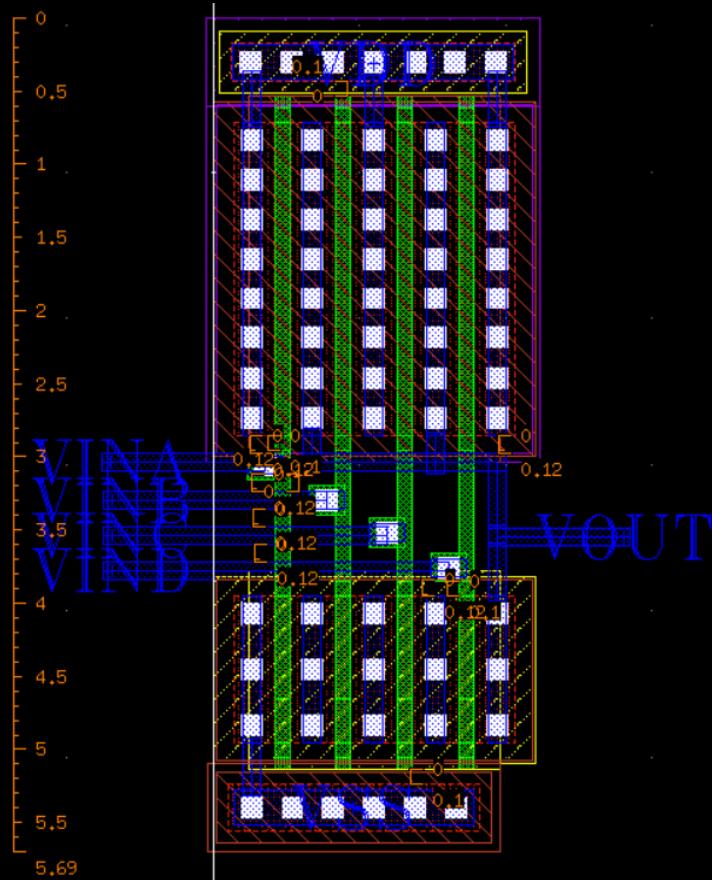
# 3NAND - Layout & Simulation



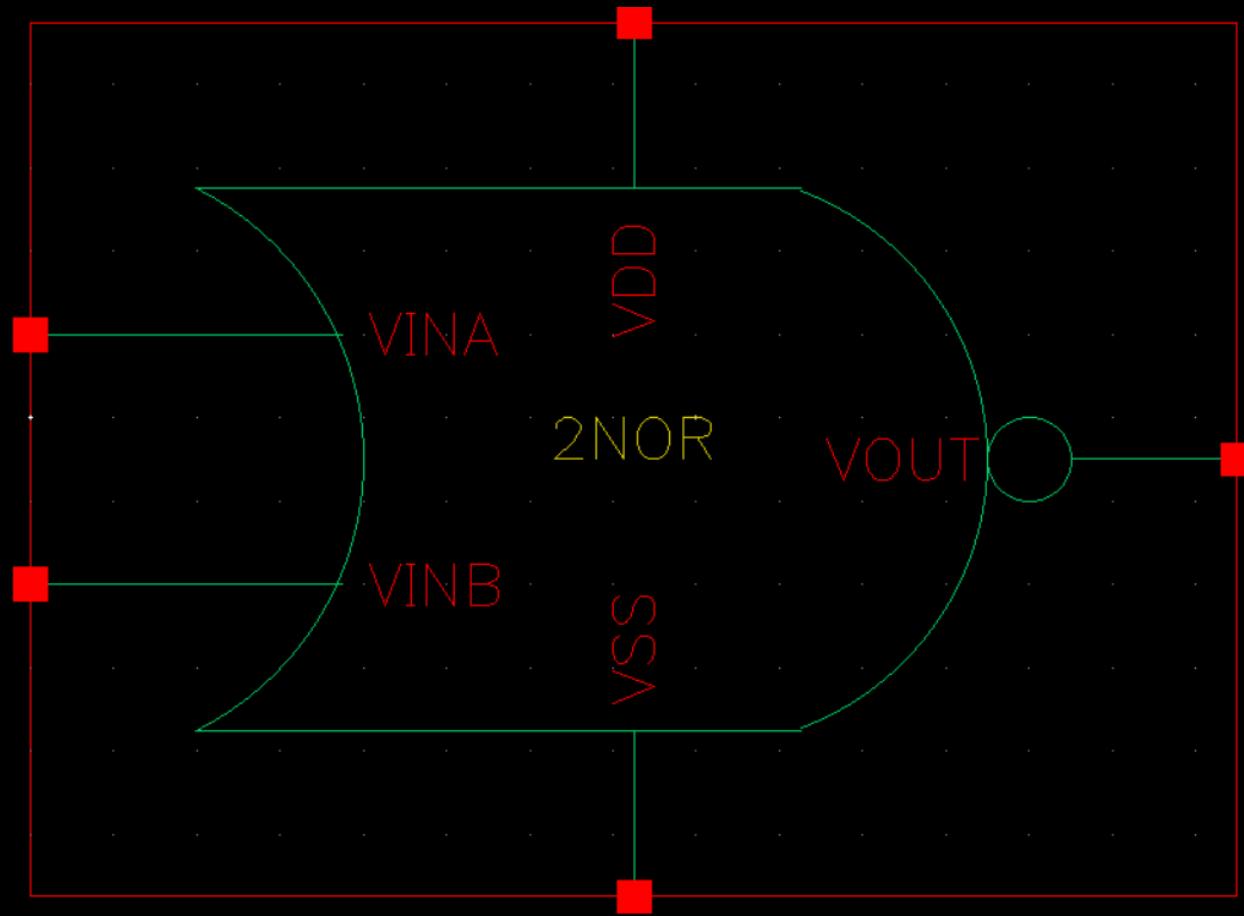
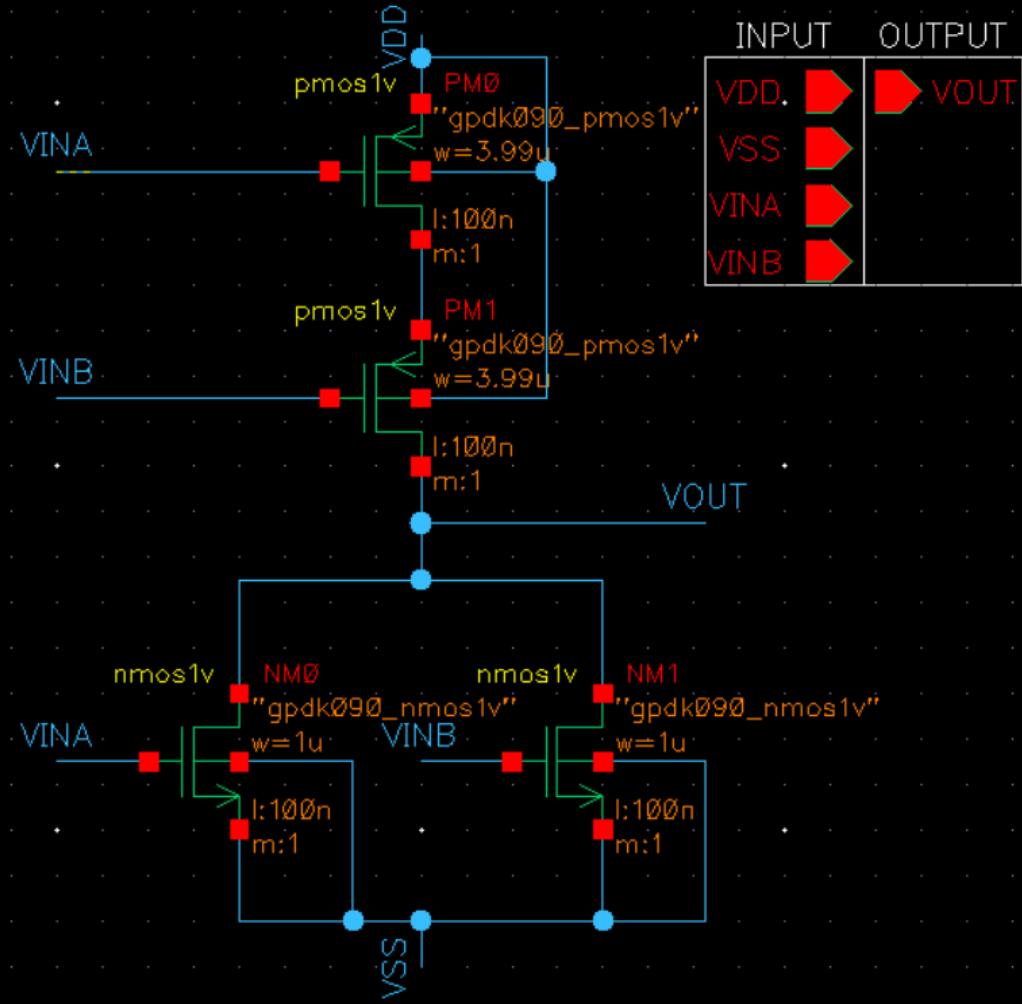
# 4NAND – Schematic & Symbol



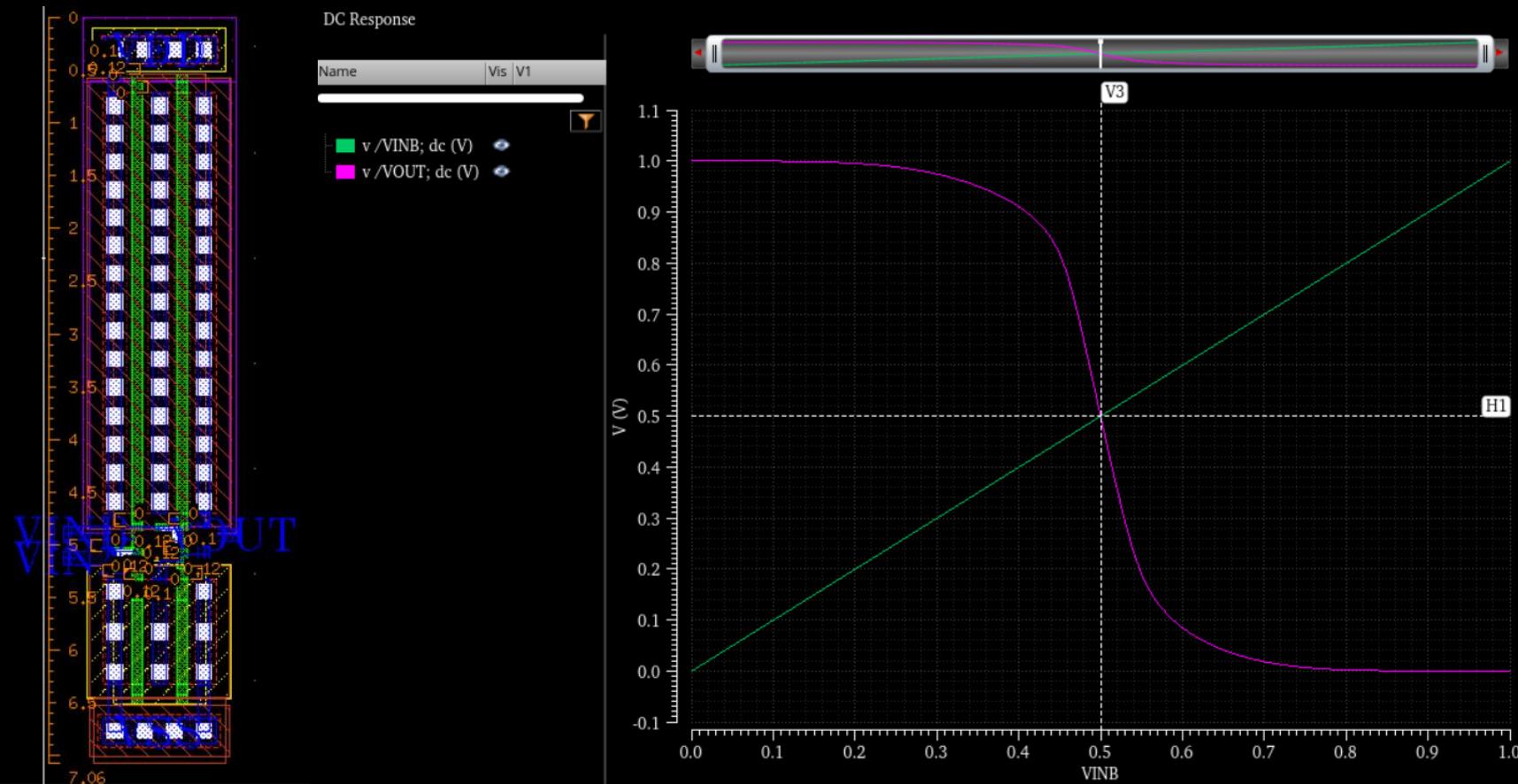
# 4NAND - Layout & Simulation



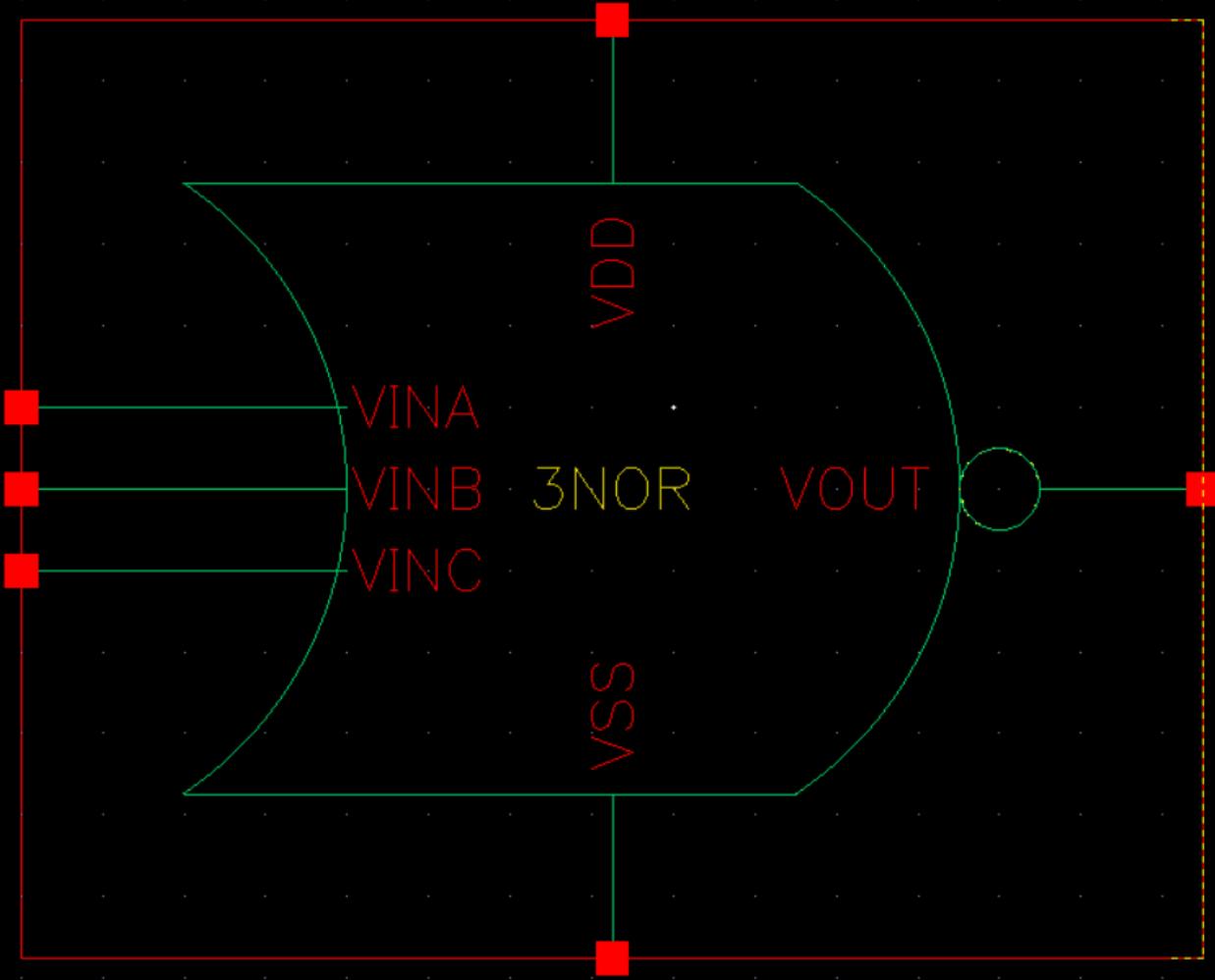
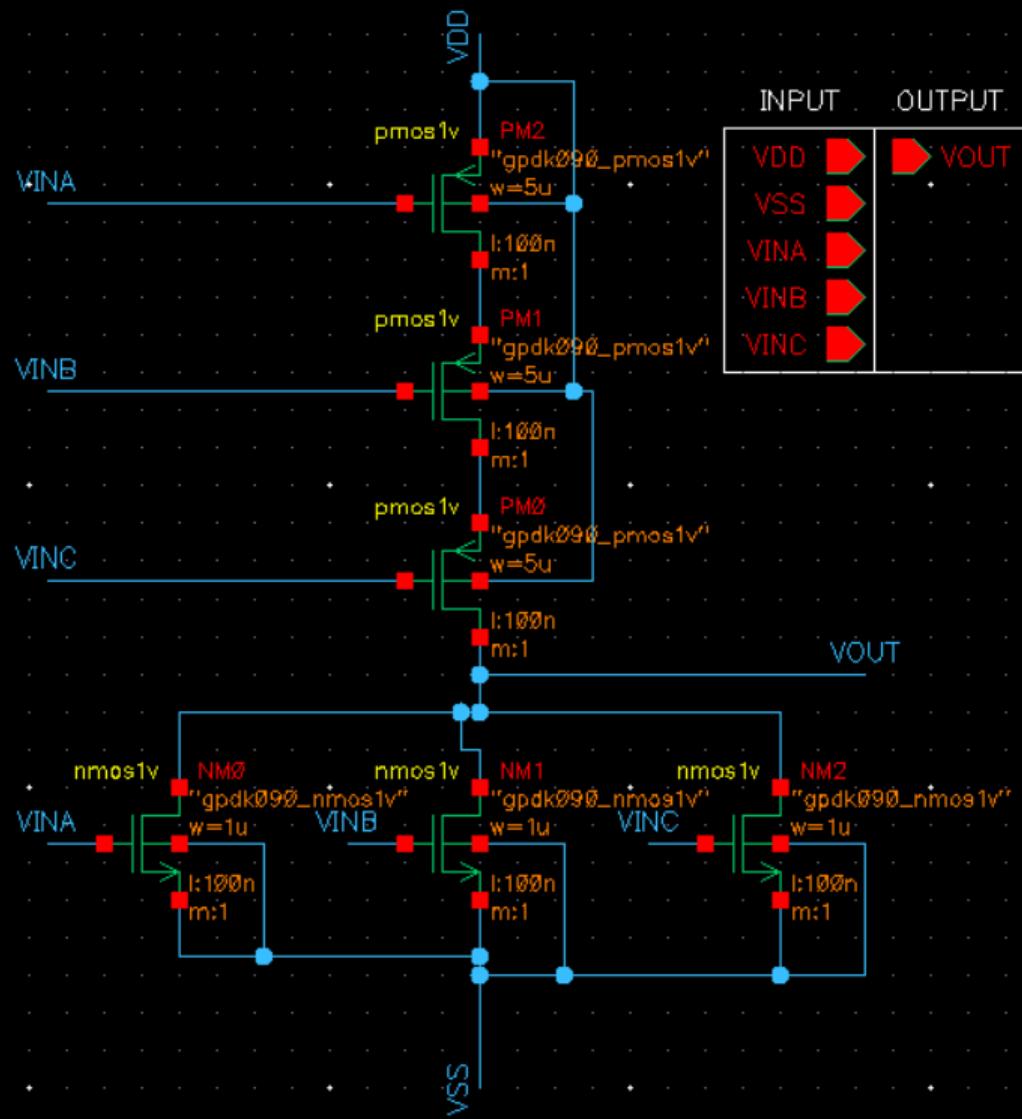
# 2NOR - Schematic & Symbol



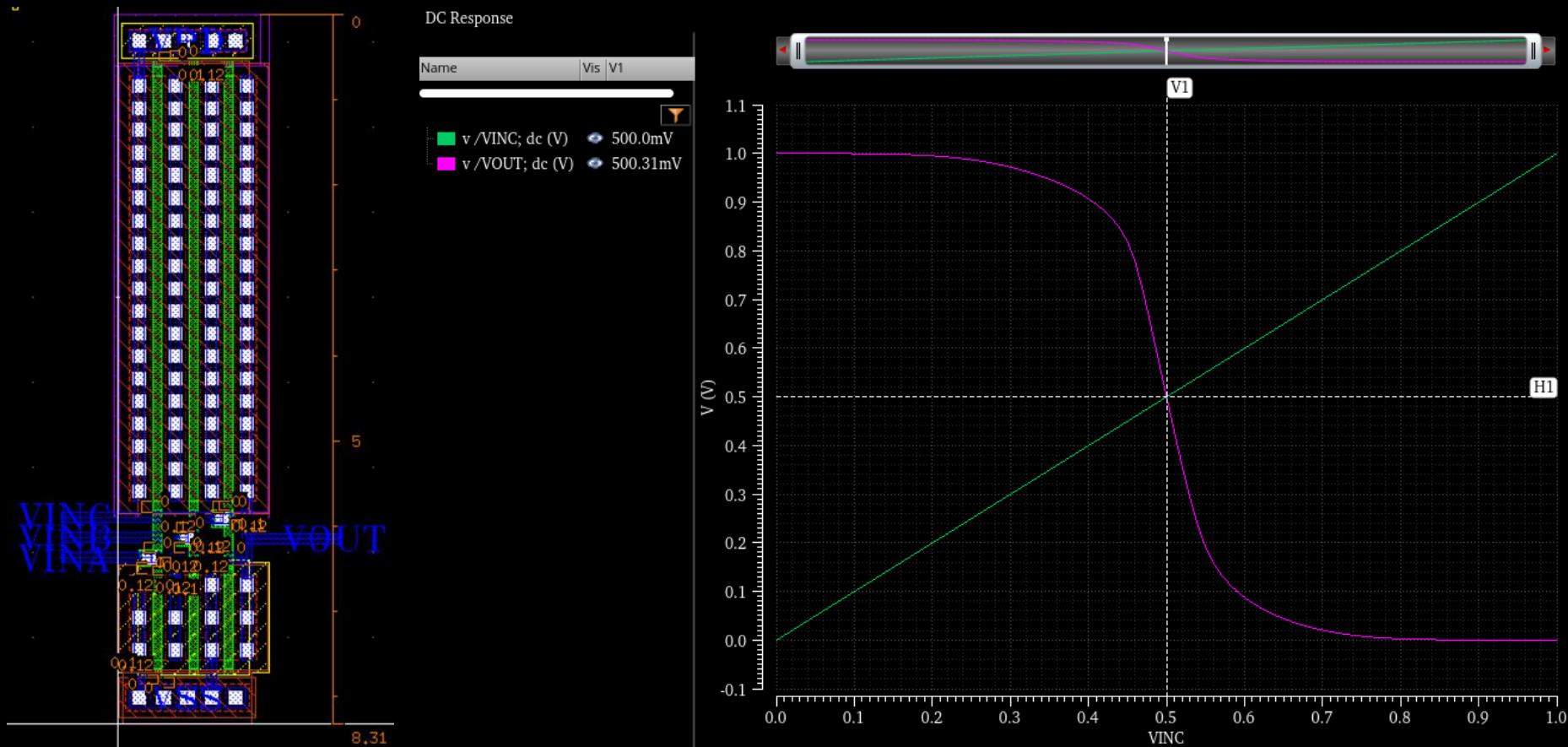
# 2NOR - Layout & Simulation



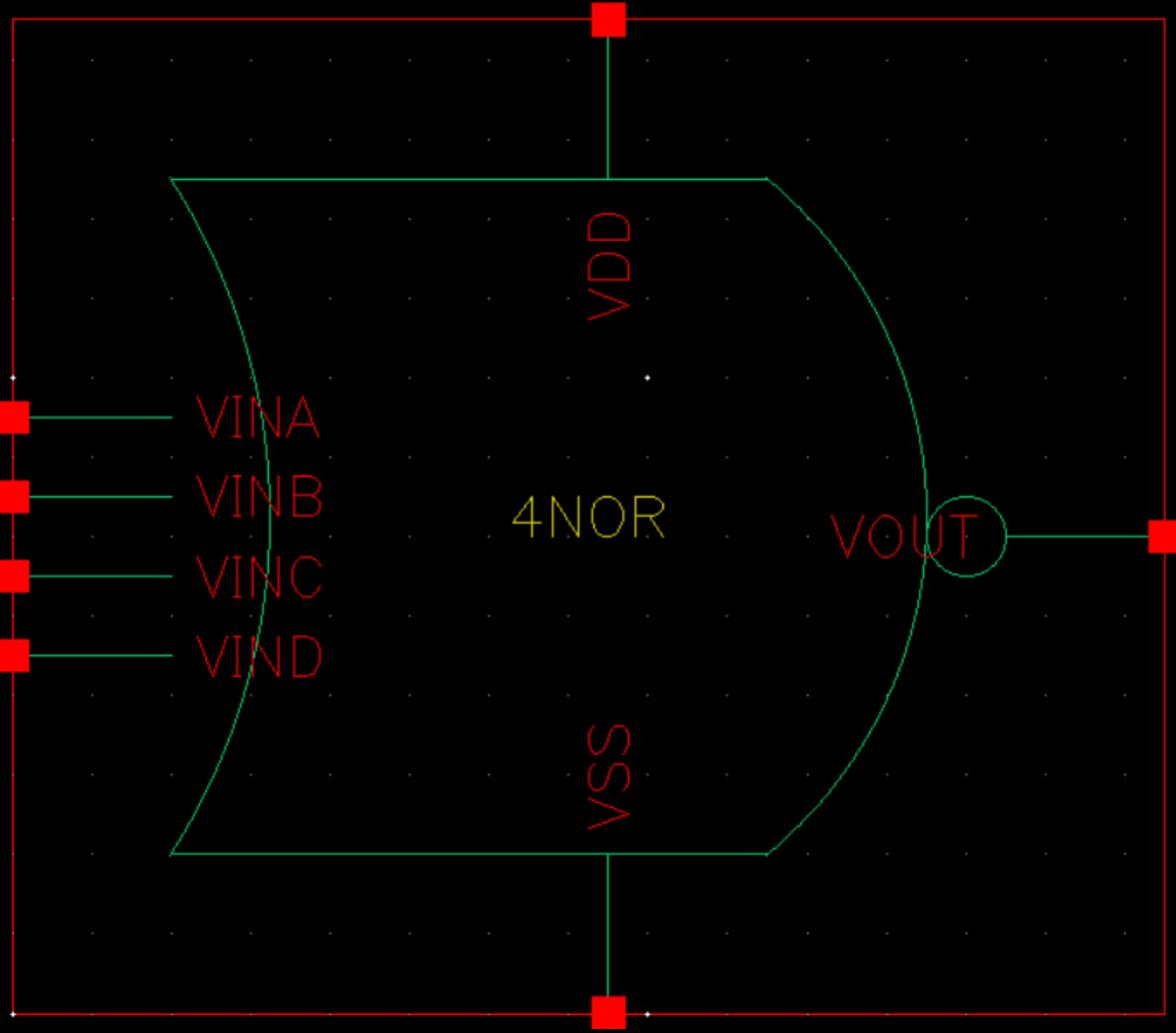
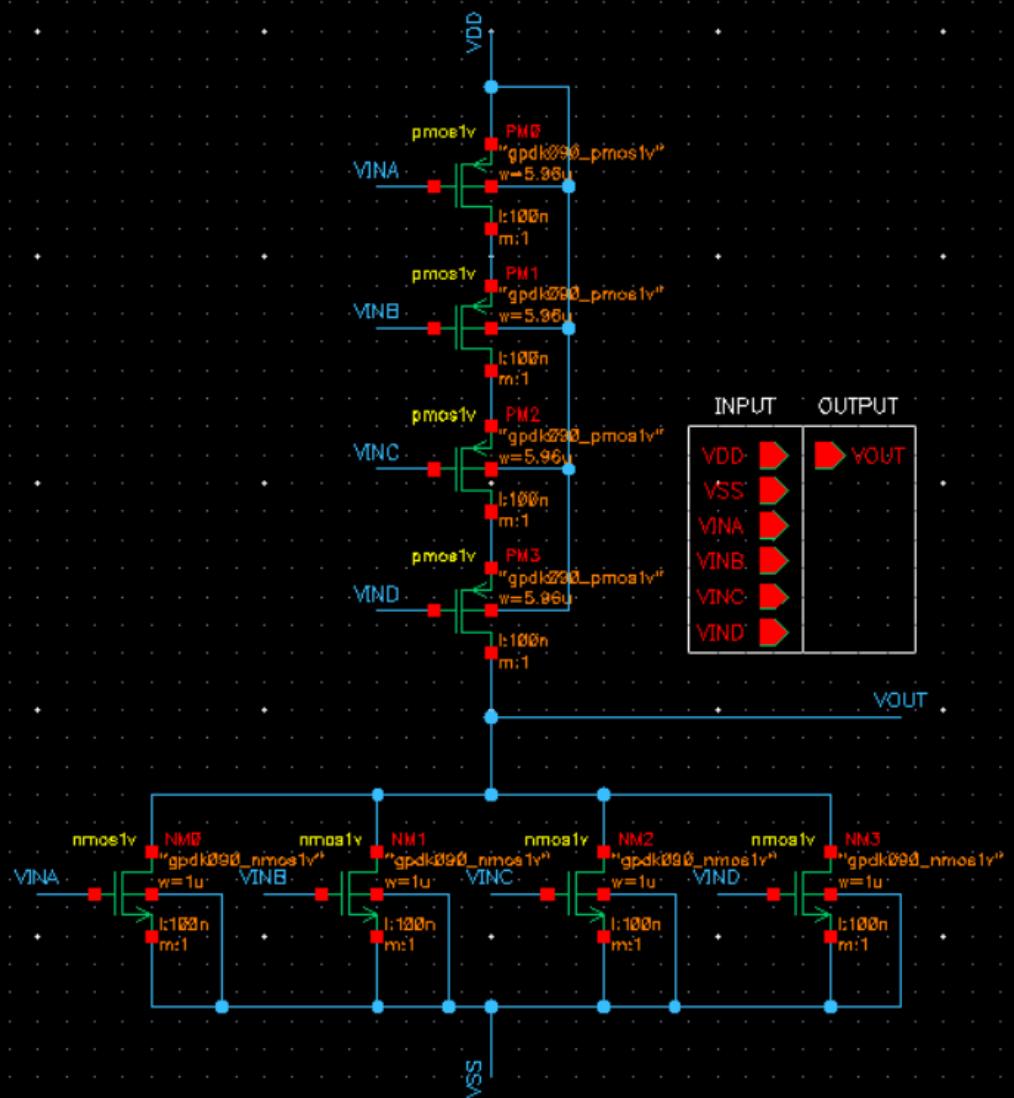
# 3NOR – Schematic & Symbol



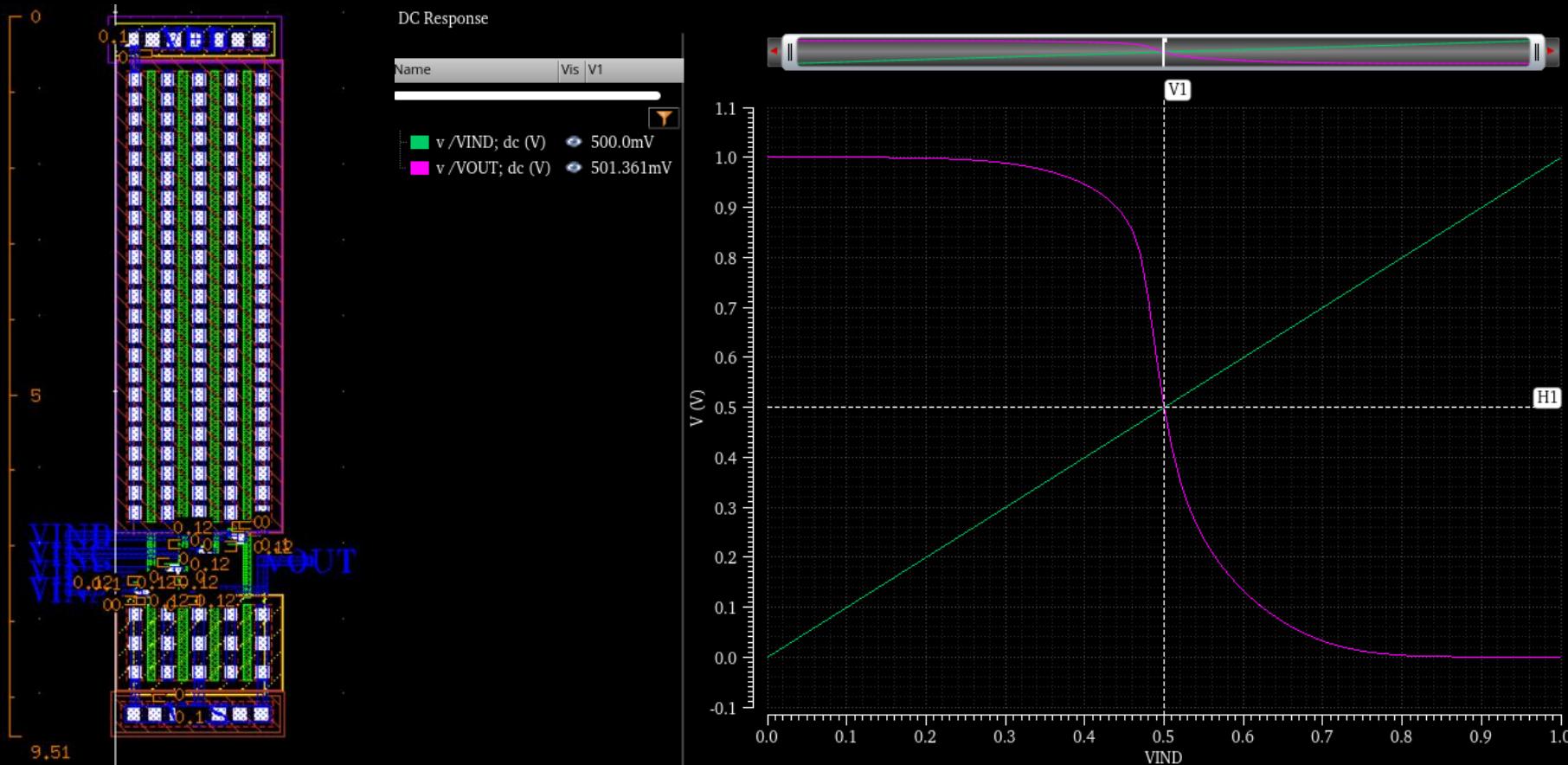
# 3NOR - Layout & Simulation



# 4NOR - Schematic & Symbol



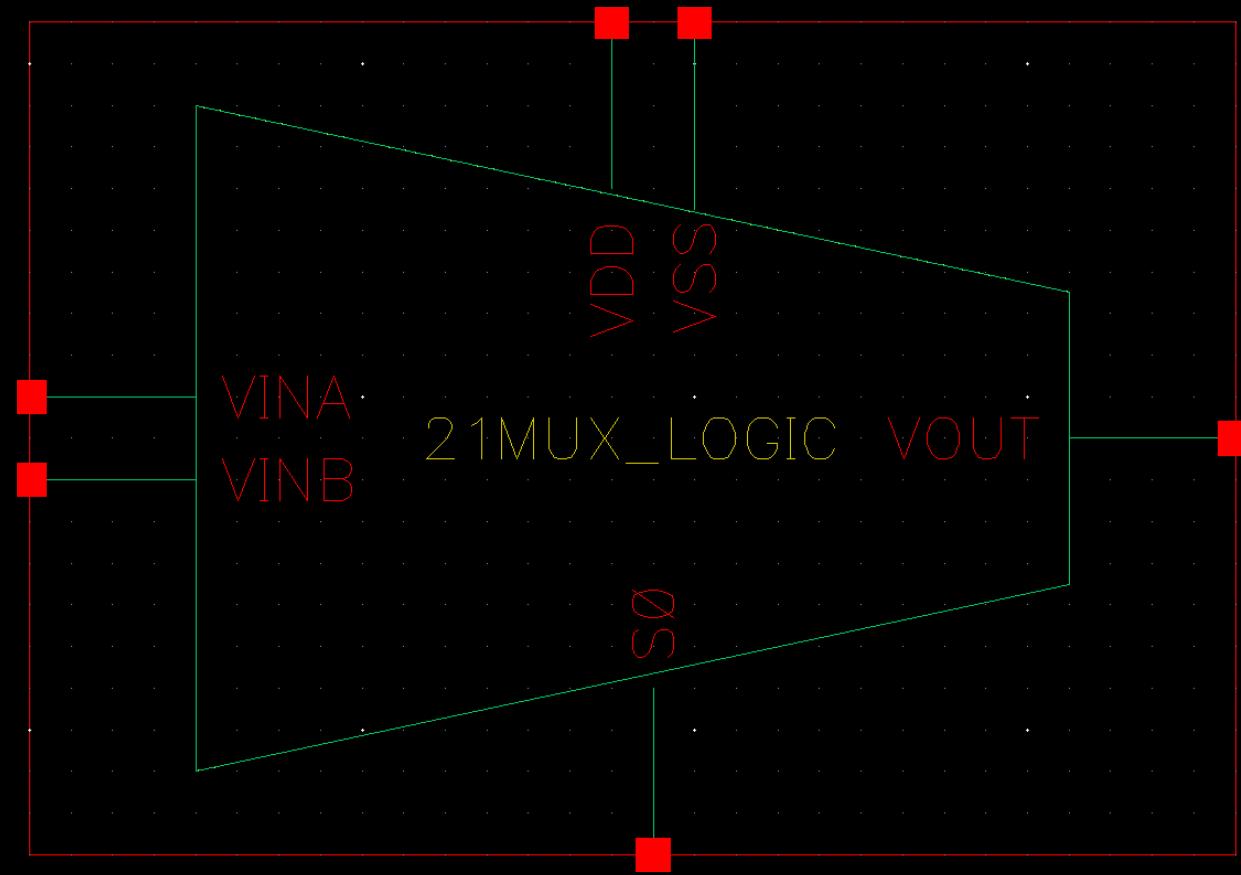
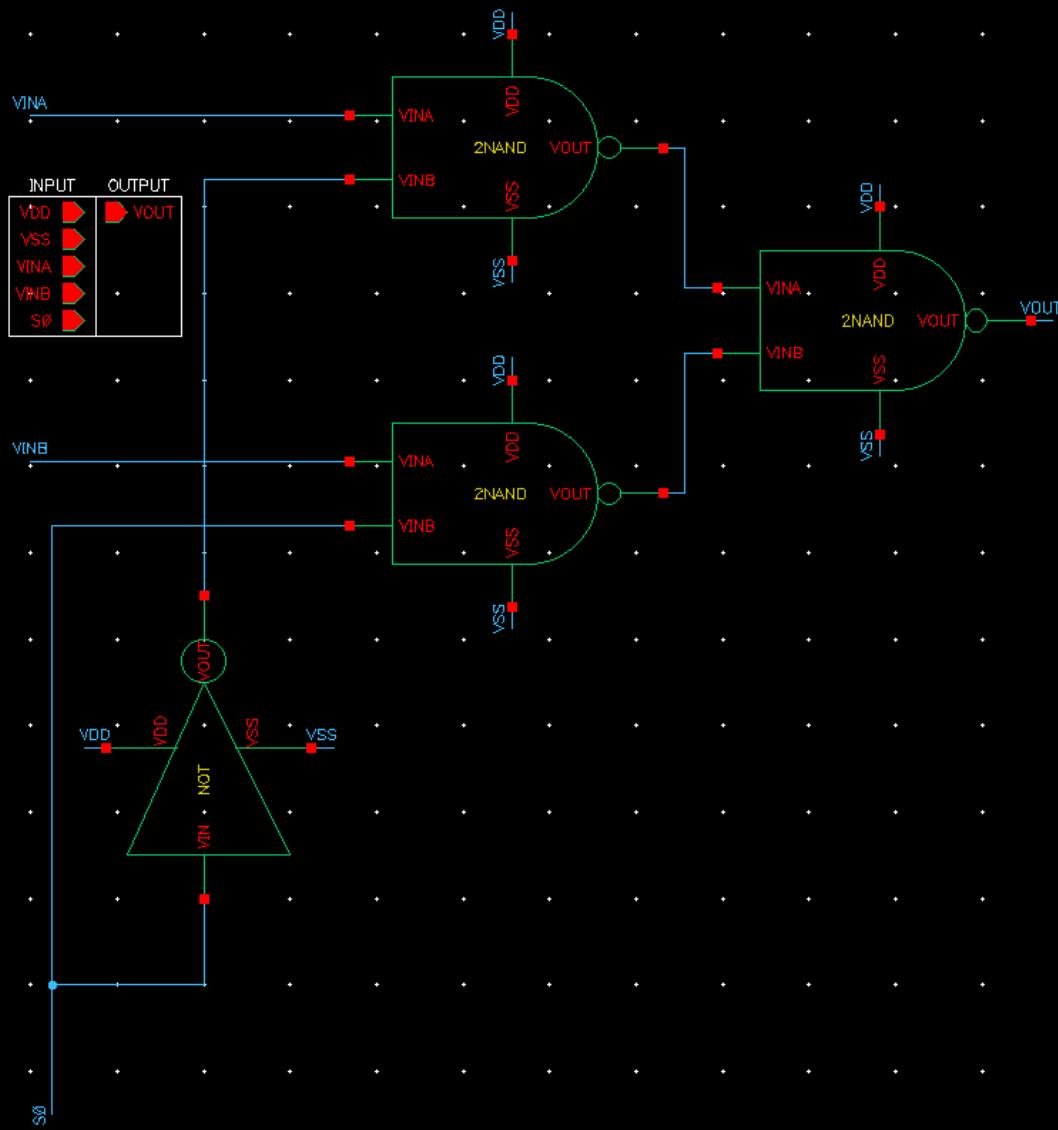
# 4NOR - Layout & Simulation



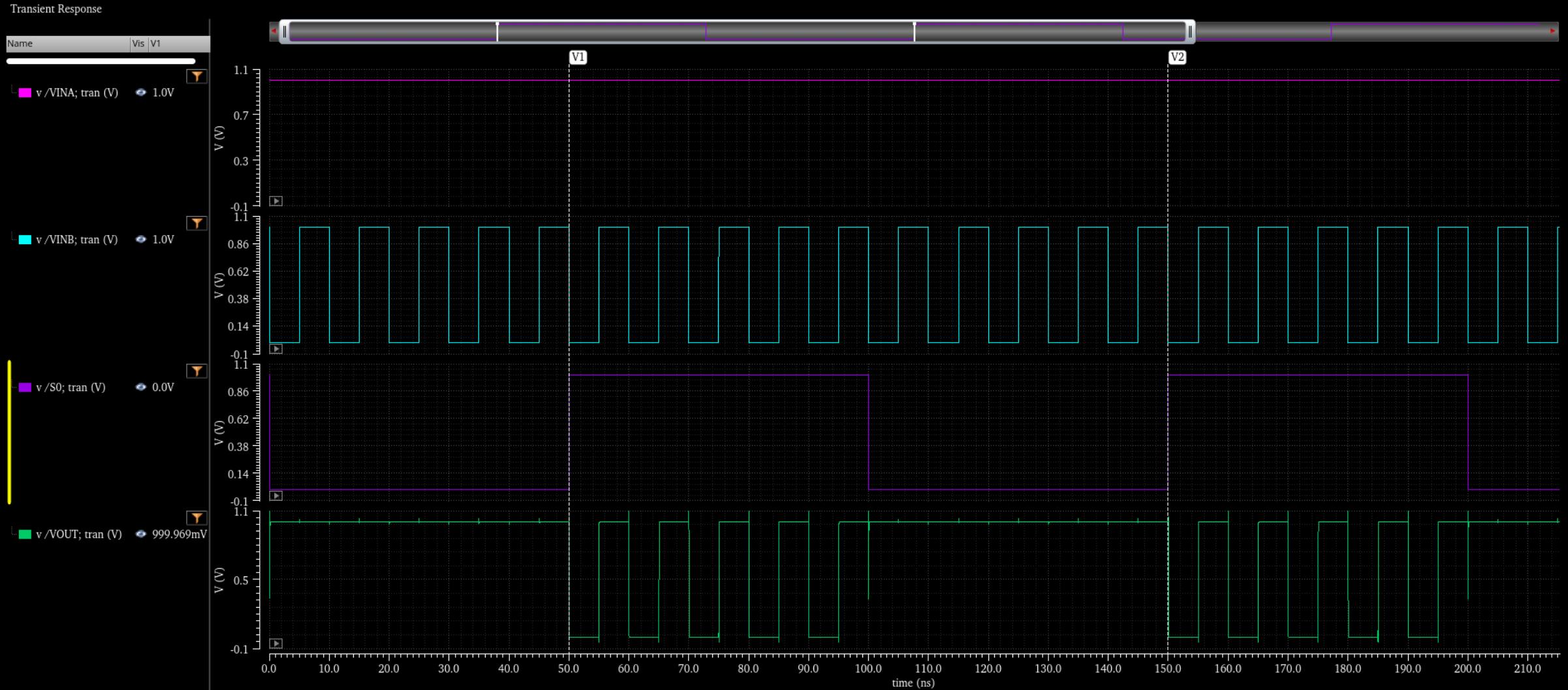
# Digital Circuits

- 2x1 MUX / 4x1 MUX / 8x1 MUX / 16x1 MUX  
(Difference Logic & Switch)
- HALF\_ADDER / FULL\_ADDER / 4BIT\_ADDER

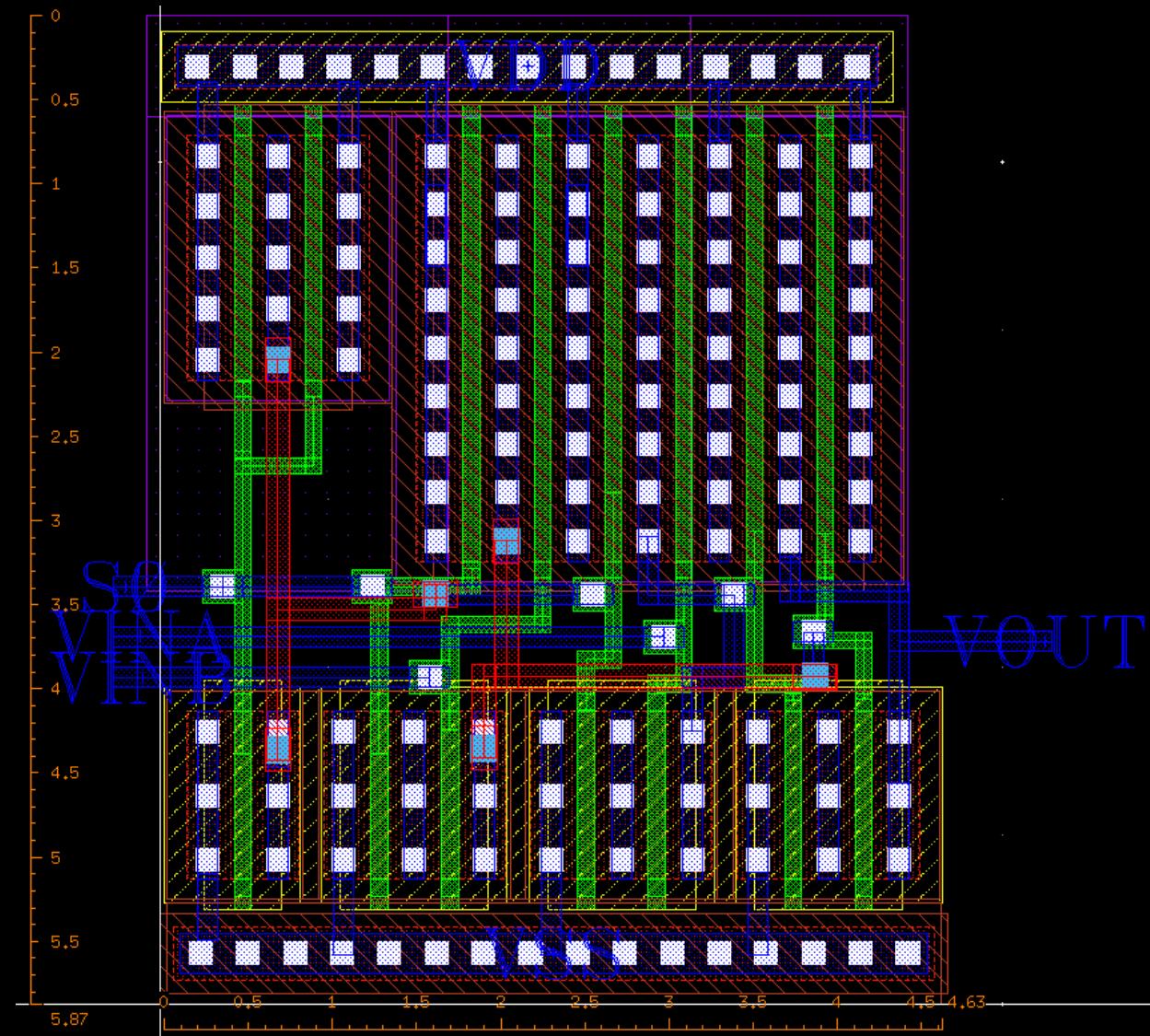
# 2x1 MUX Logic – Schematic & Symbol



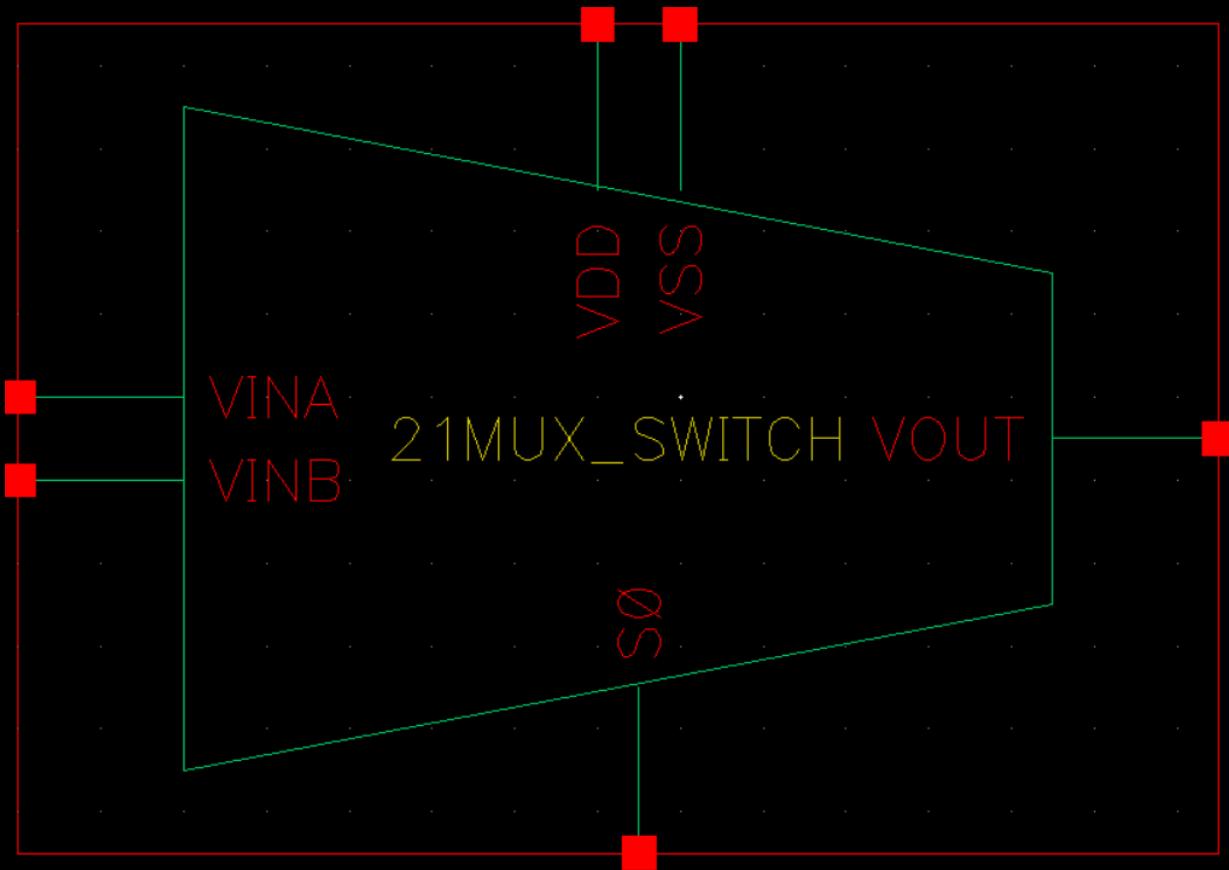
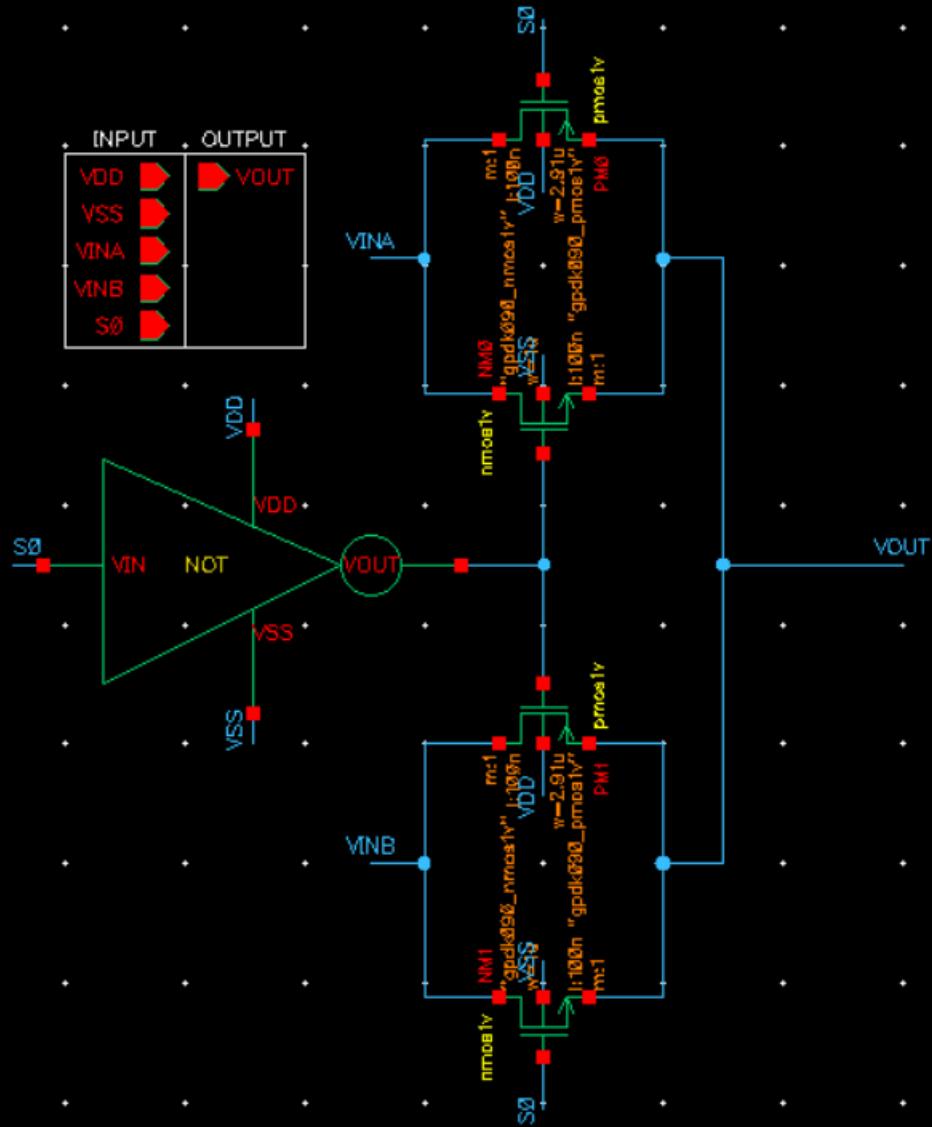
# 2x1 MUX Logic - Simulation



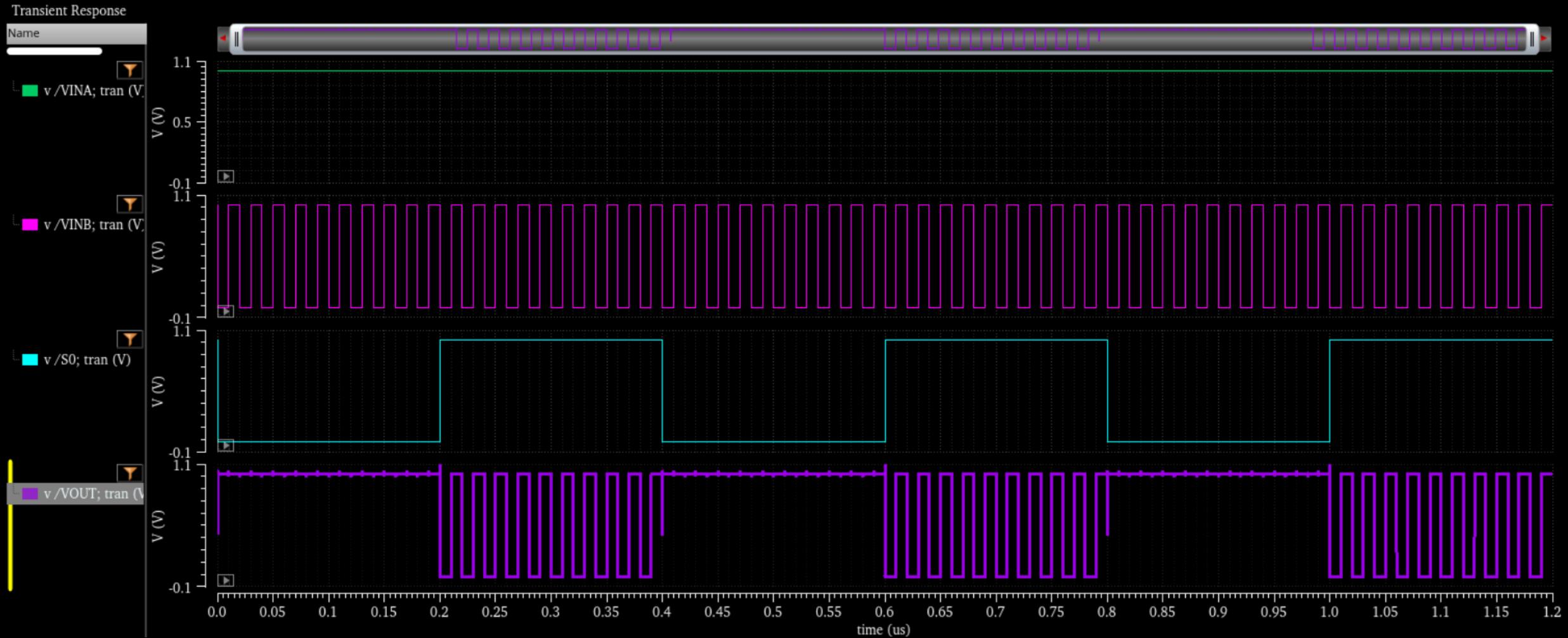
# 2x1 MUX Logic - Layout



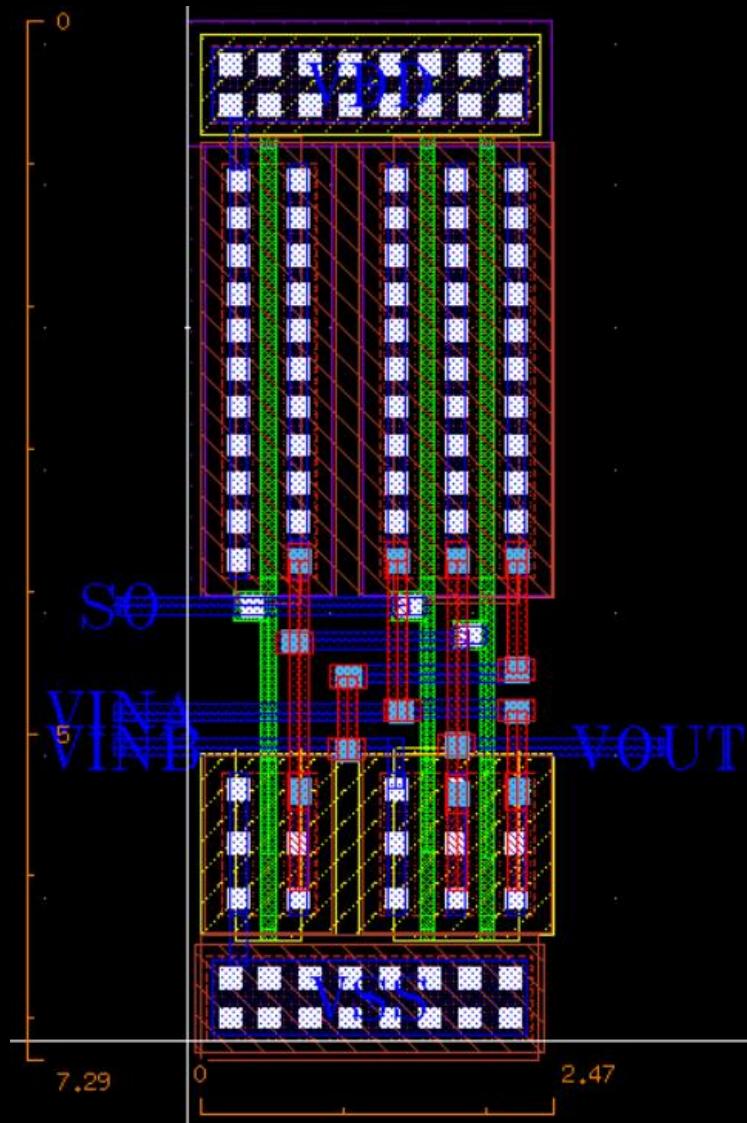
# 2x1 MUX Switch - Schematic & Symbol



# 2x1 MUX Switch - Simulation

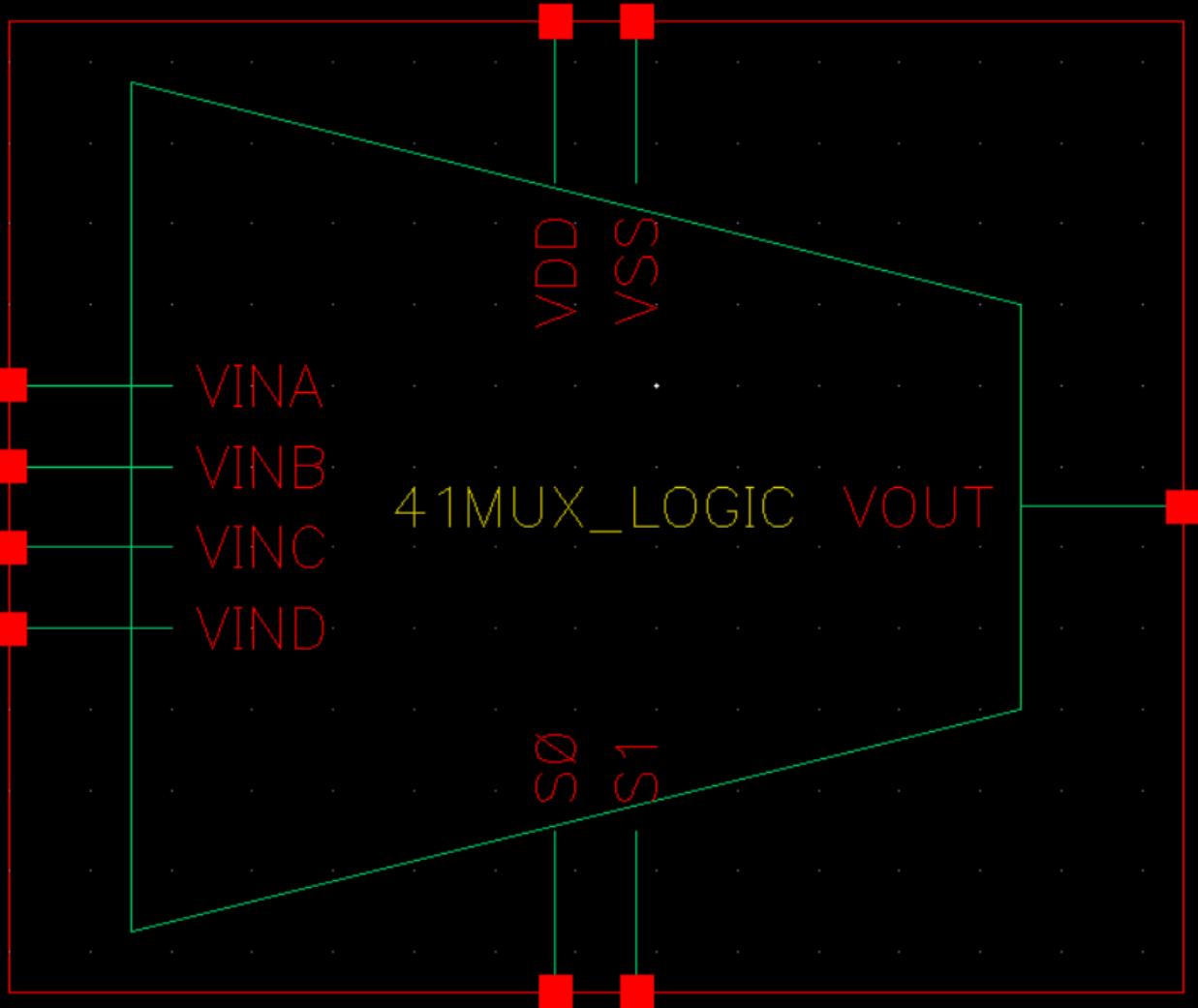
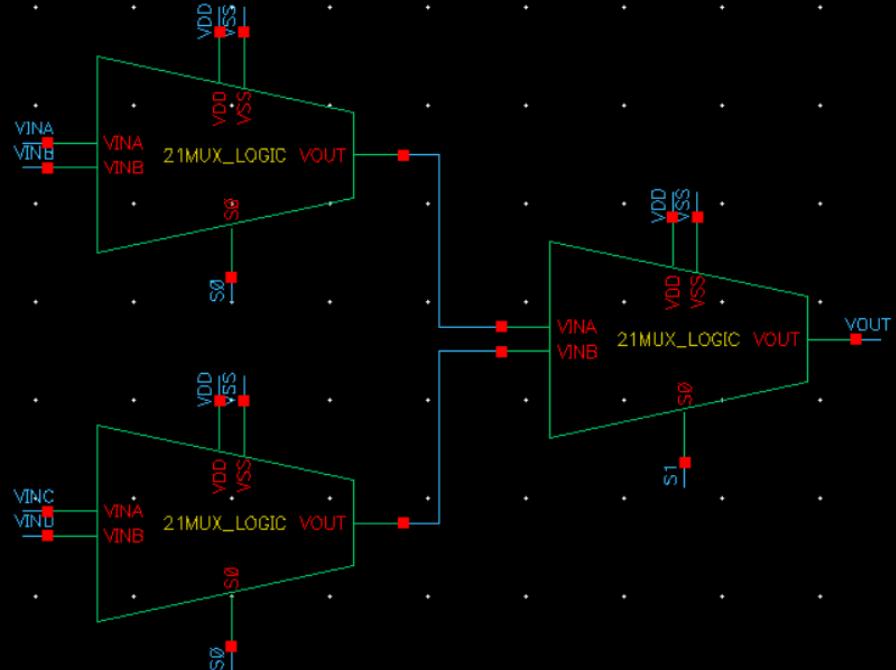


# 2x1 MUX Switch - Layout

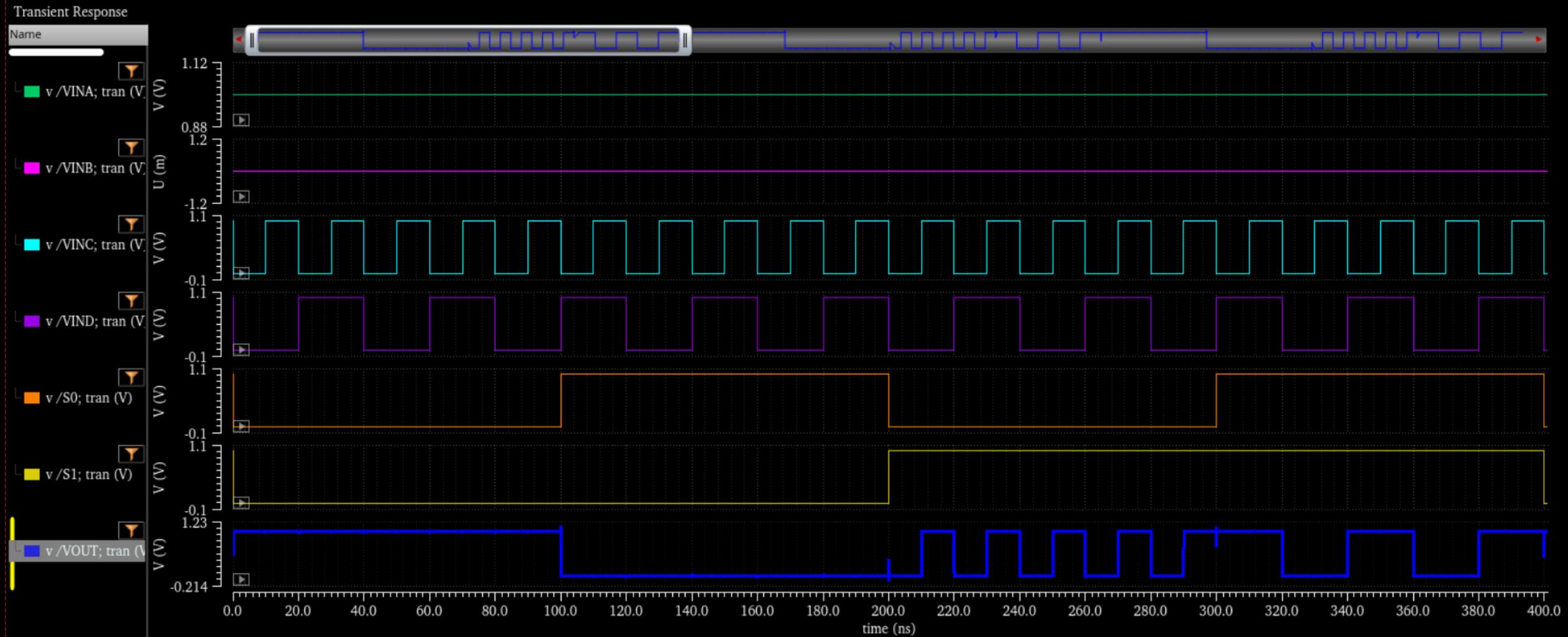


# 4x1 MUX LOGIC - Schematic & Symbol

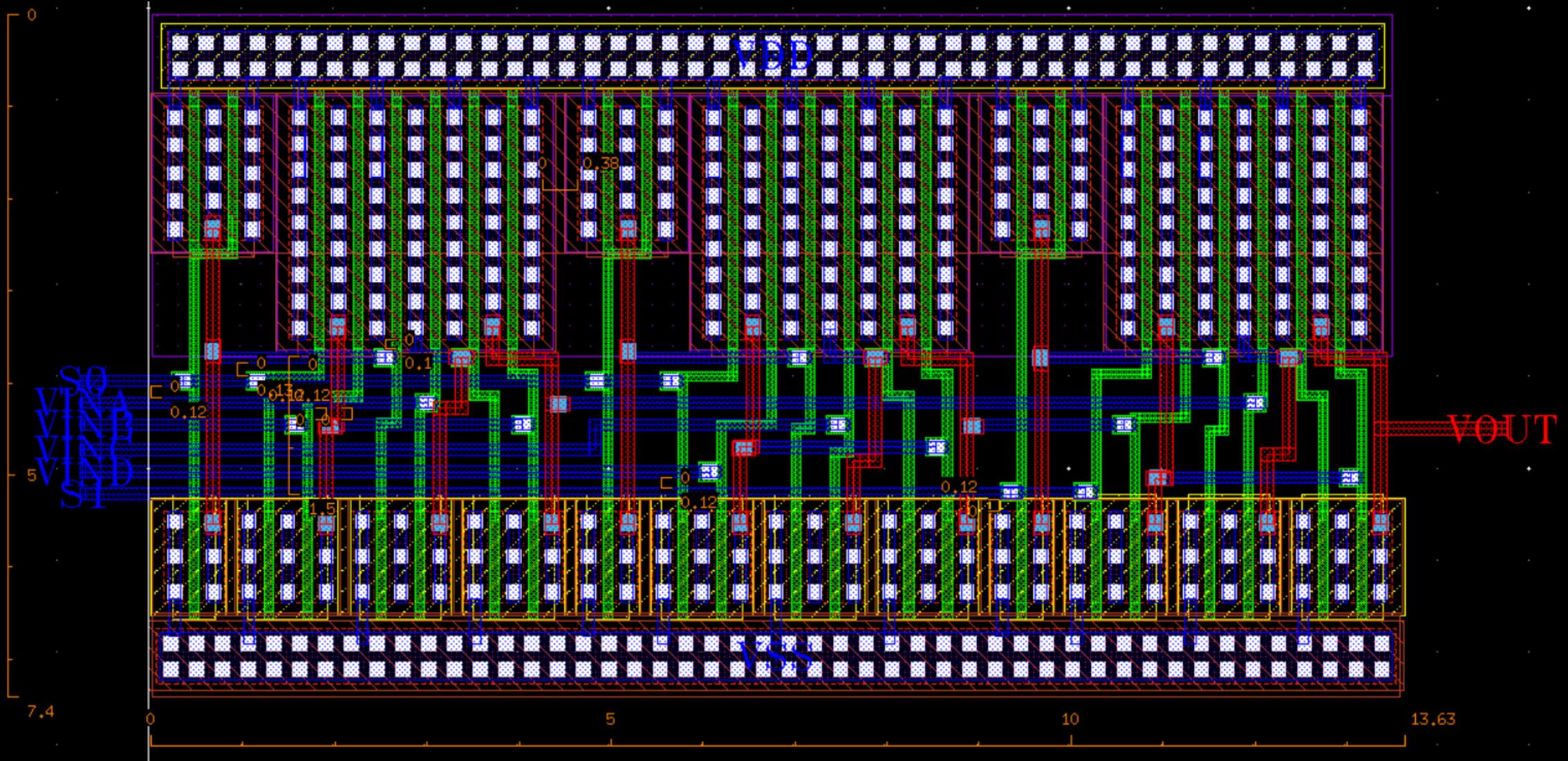
INPUT	OUTPUT
VDD	VOUT
VSS	
VINA	
VINB	
VINC	
VIND	
S0	
S1	



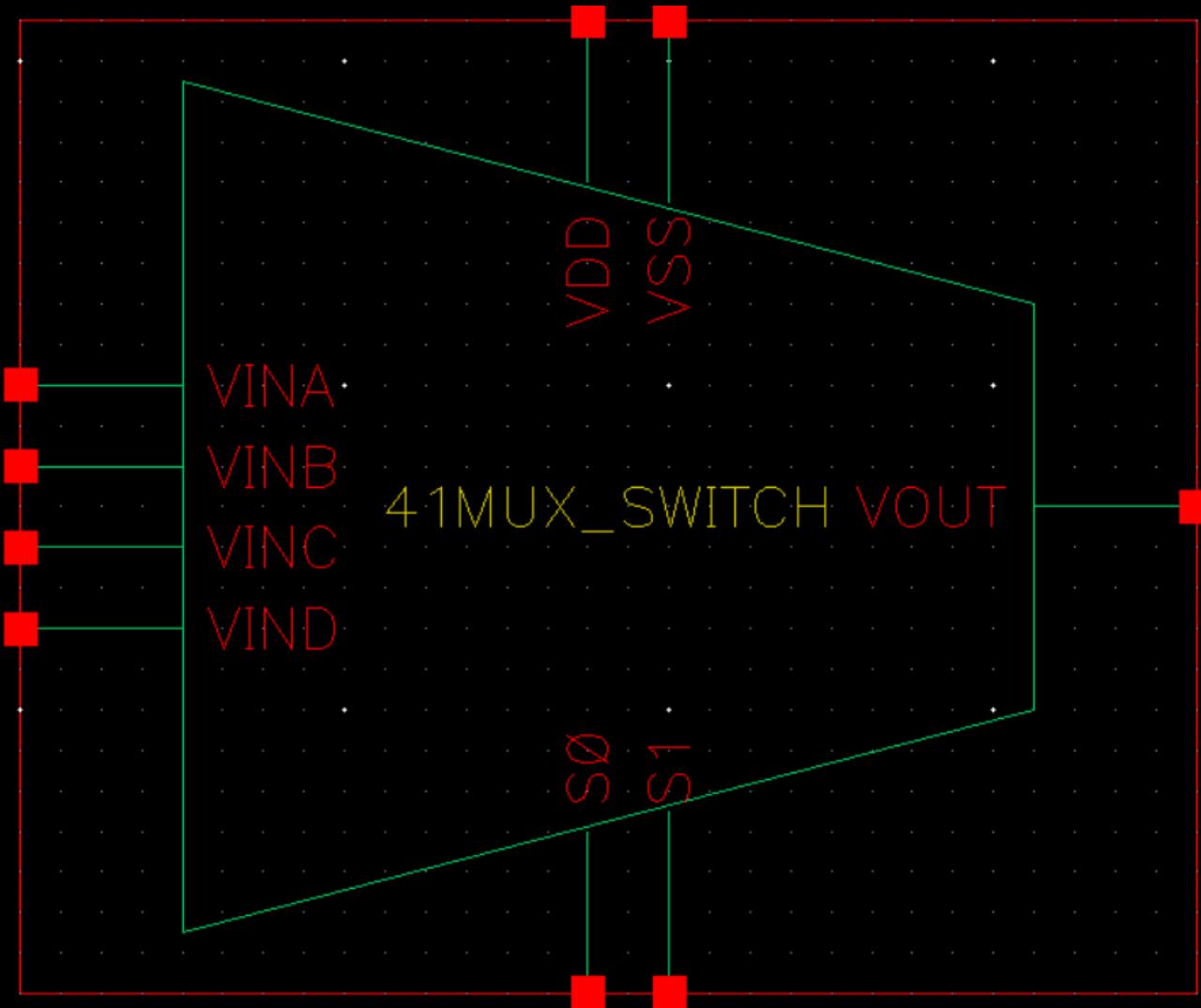
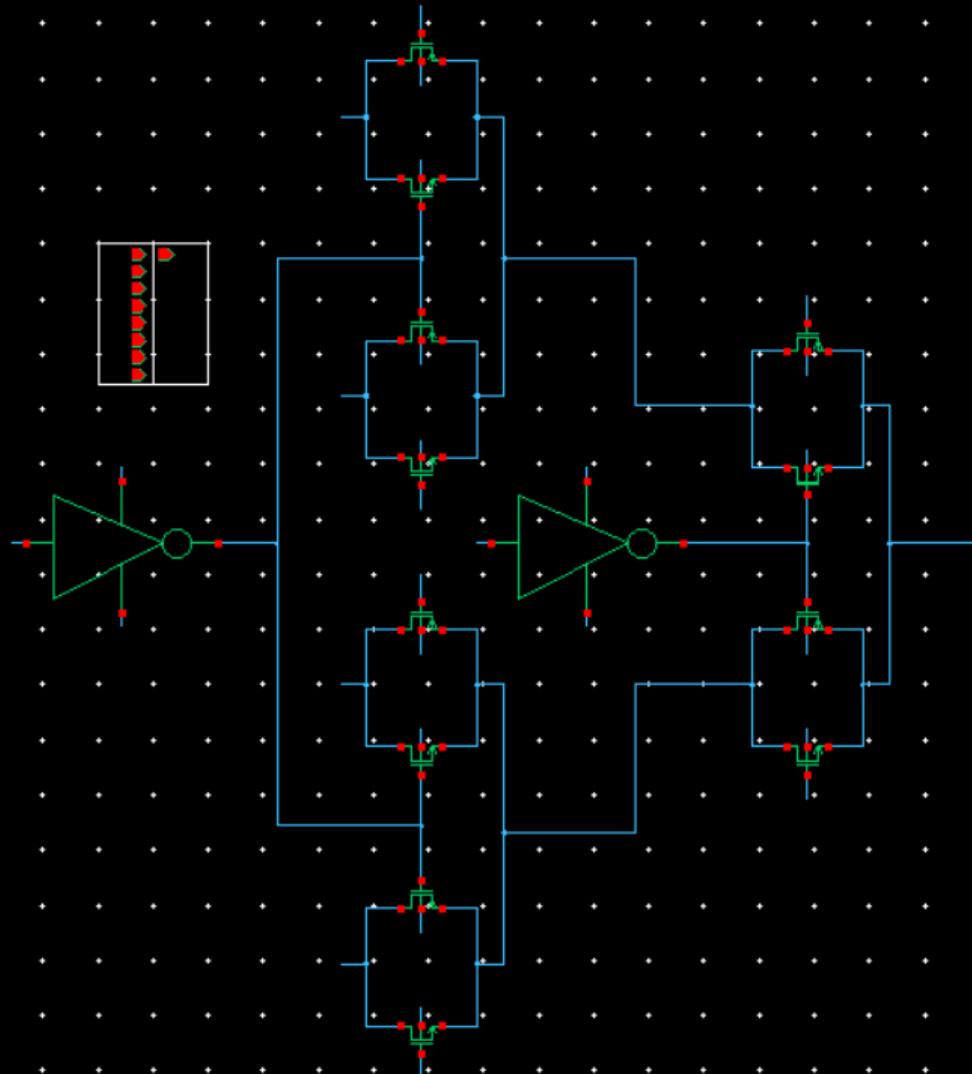
# 4x1 MUX LOGIC - Simulation



# 4x1 MUX LOGIC - Layout



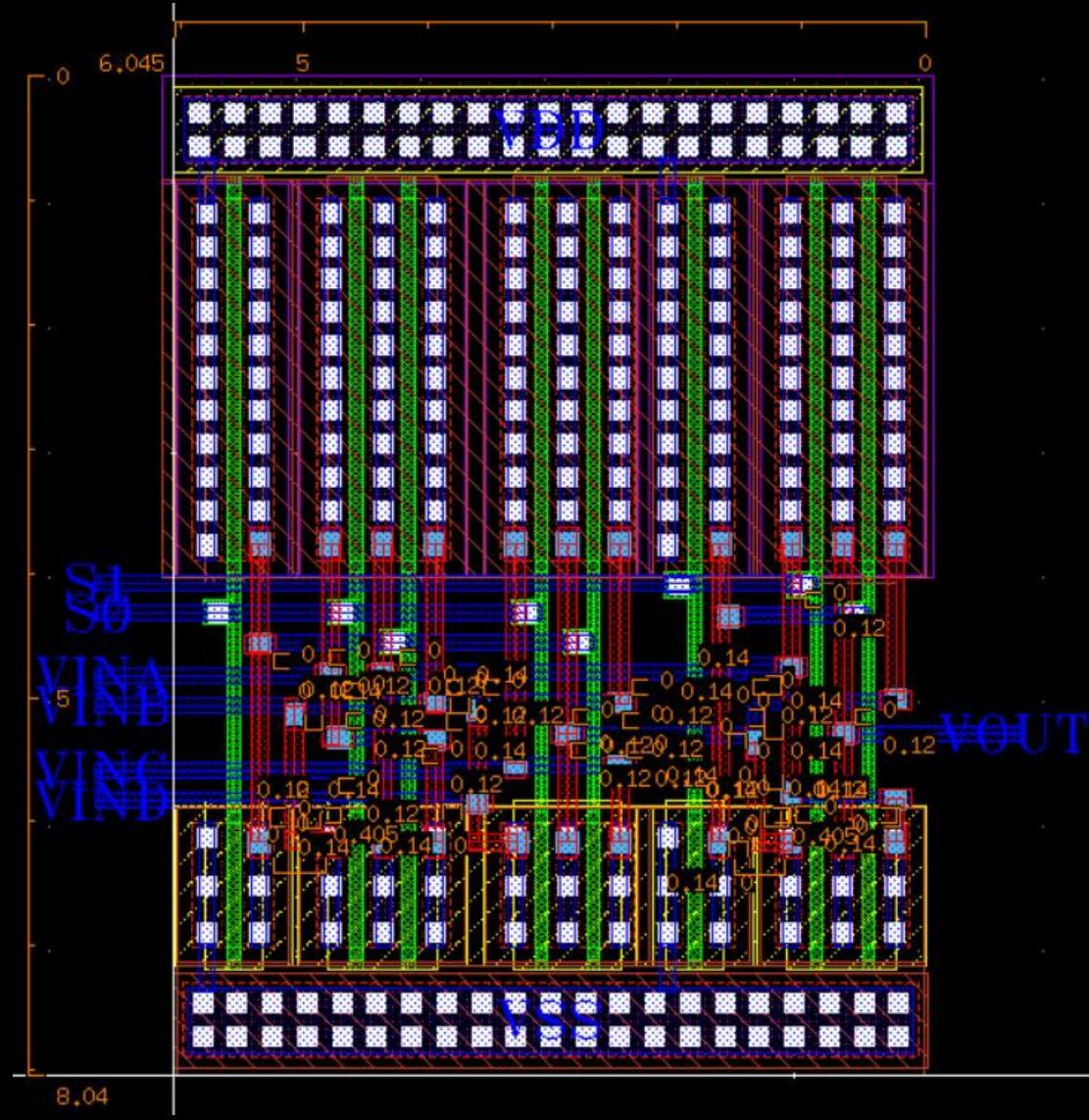
# 4x1 MUX SWITCH - Schematic & Symbol



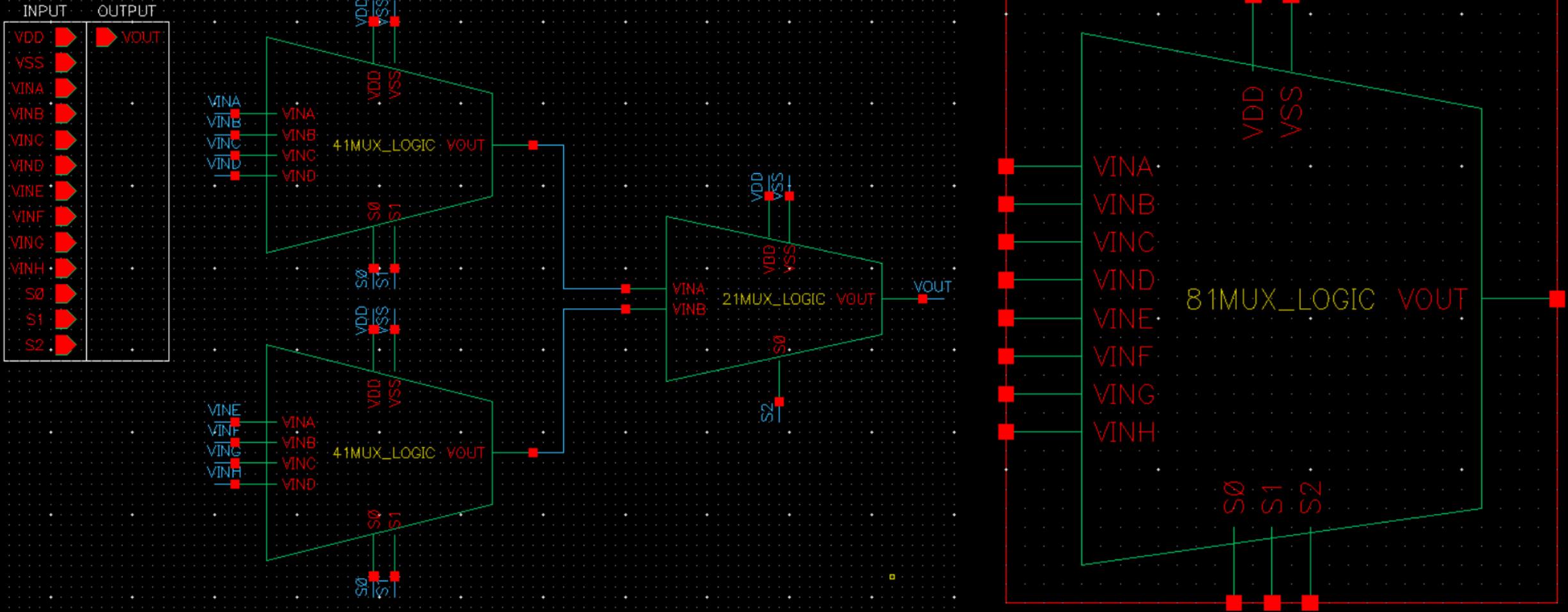
# 4x1 MUX SWITCH - Simulation



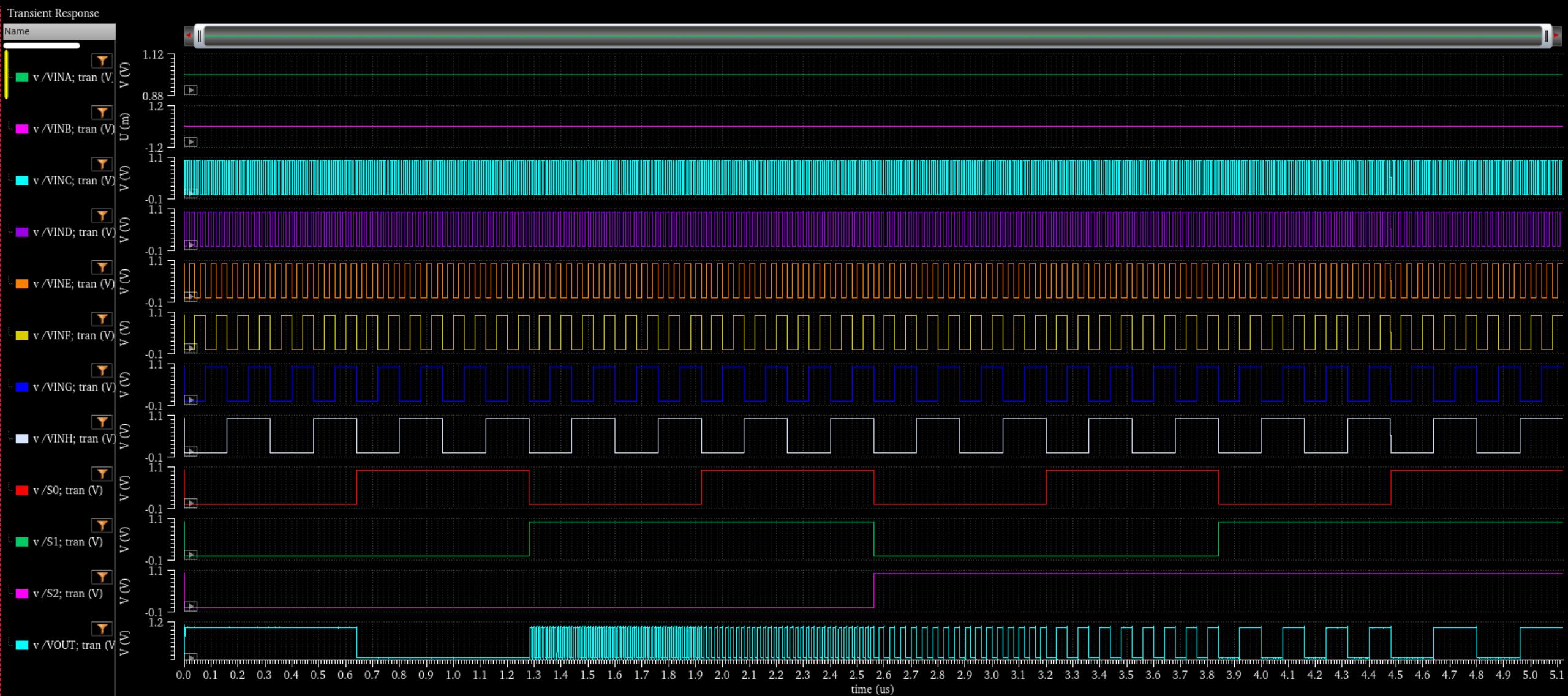
# 4x1 MUX SWITCH - Layout



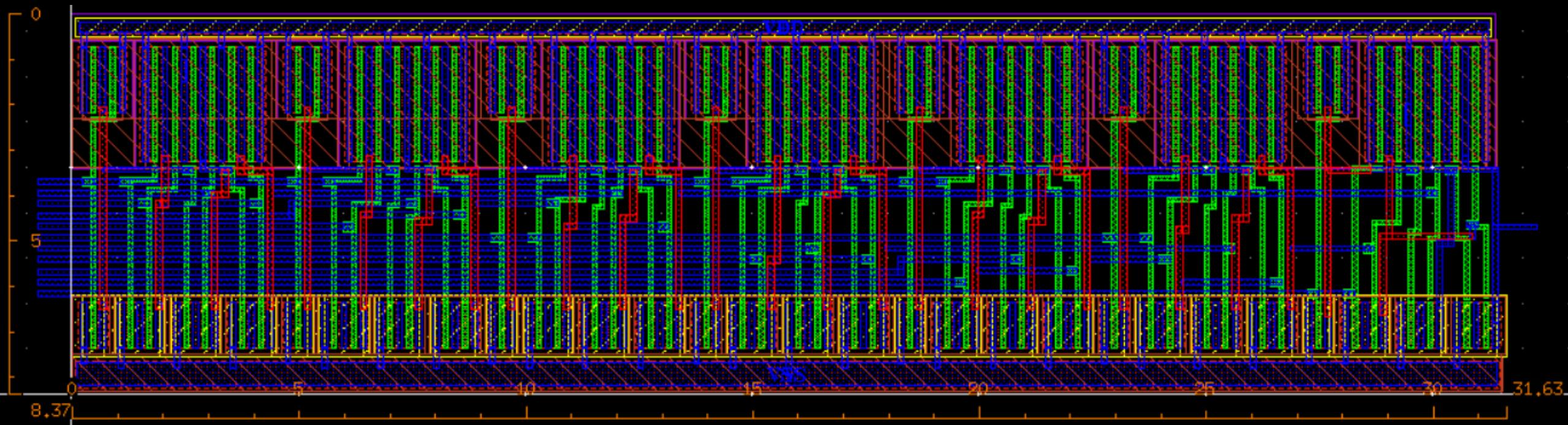
# 8x1 MUX LOGIC - Schematic & Symbol



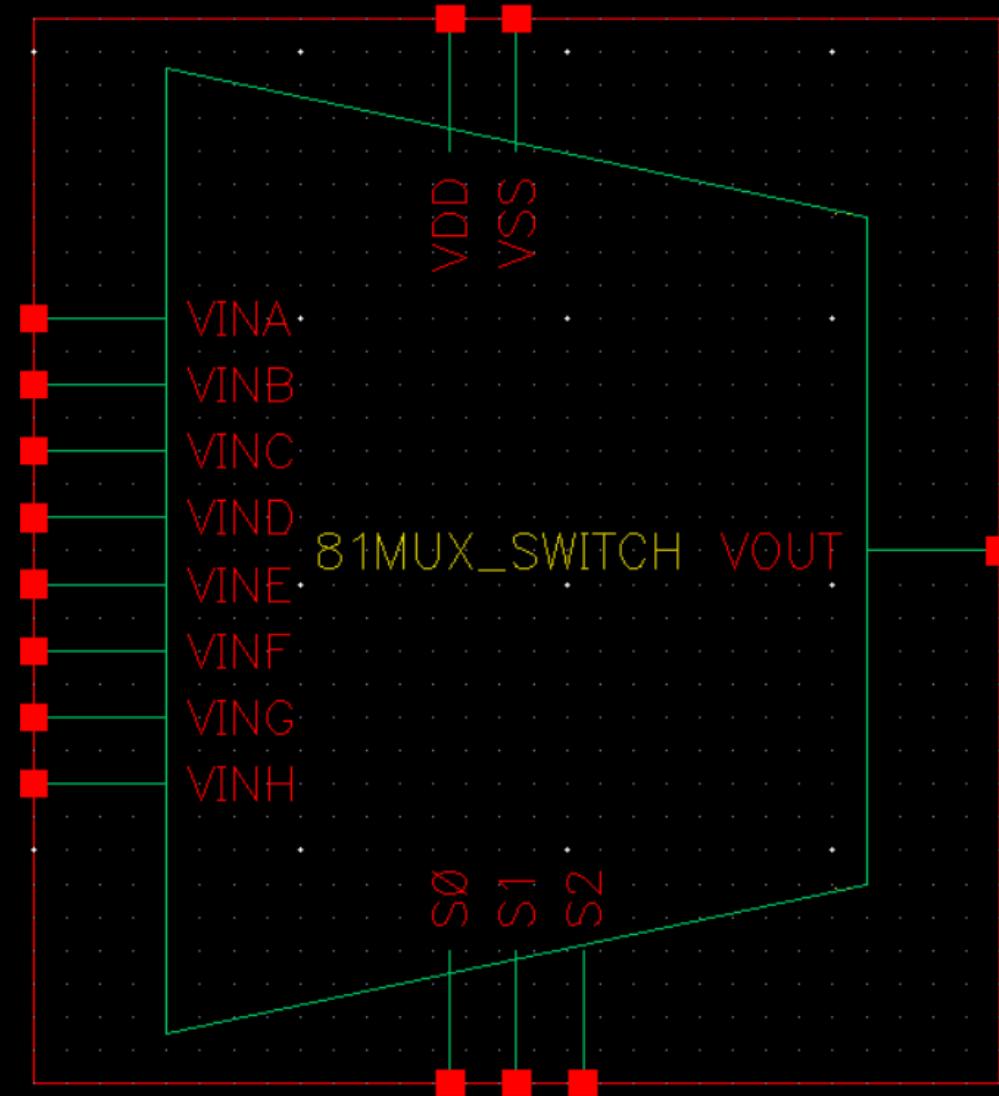
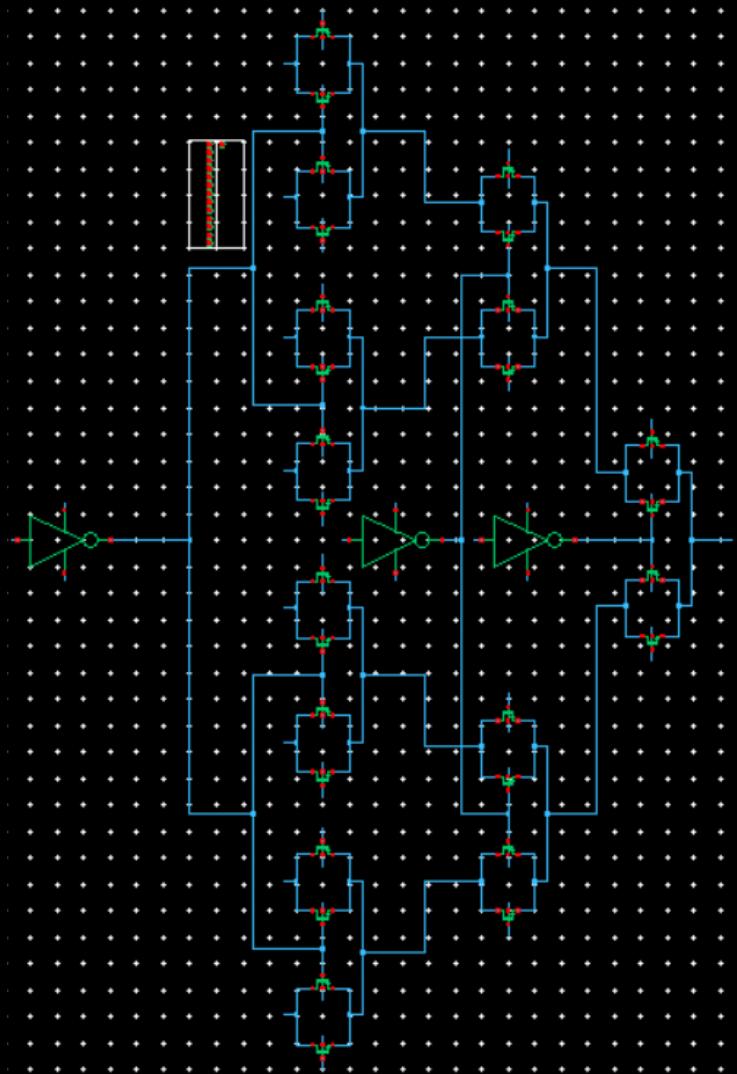
# 8x1 MUX LOGIC - Simulation



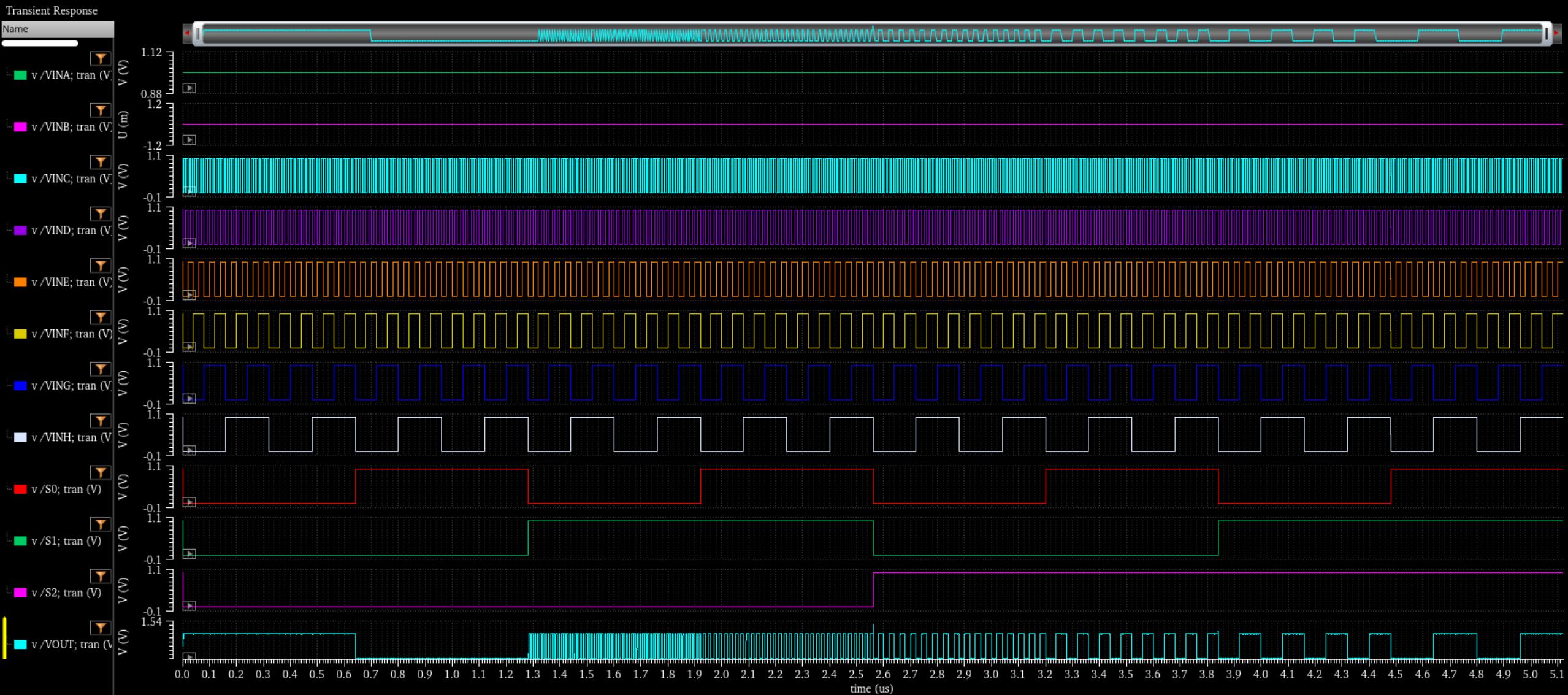
# 8x1 MUX LOGIC - Layout



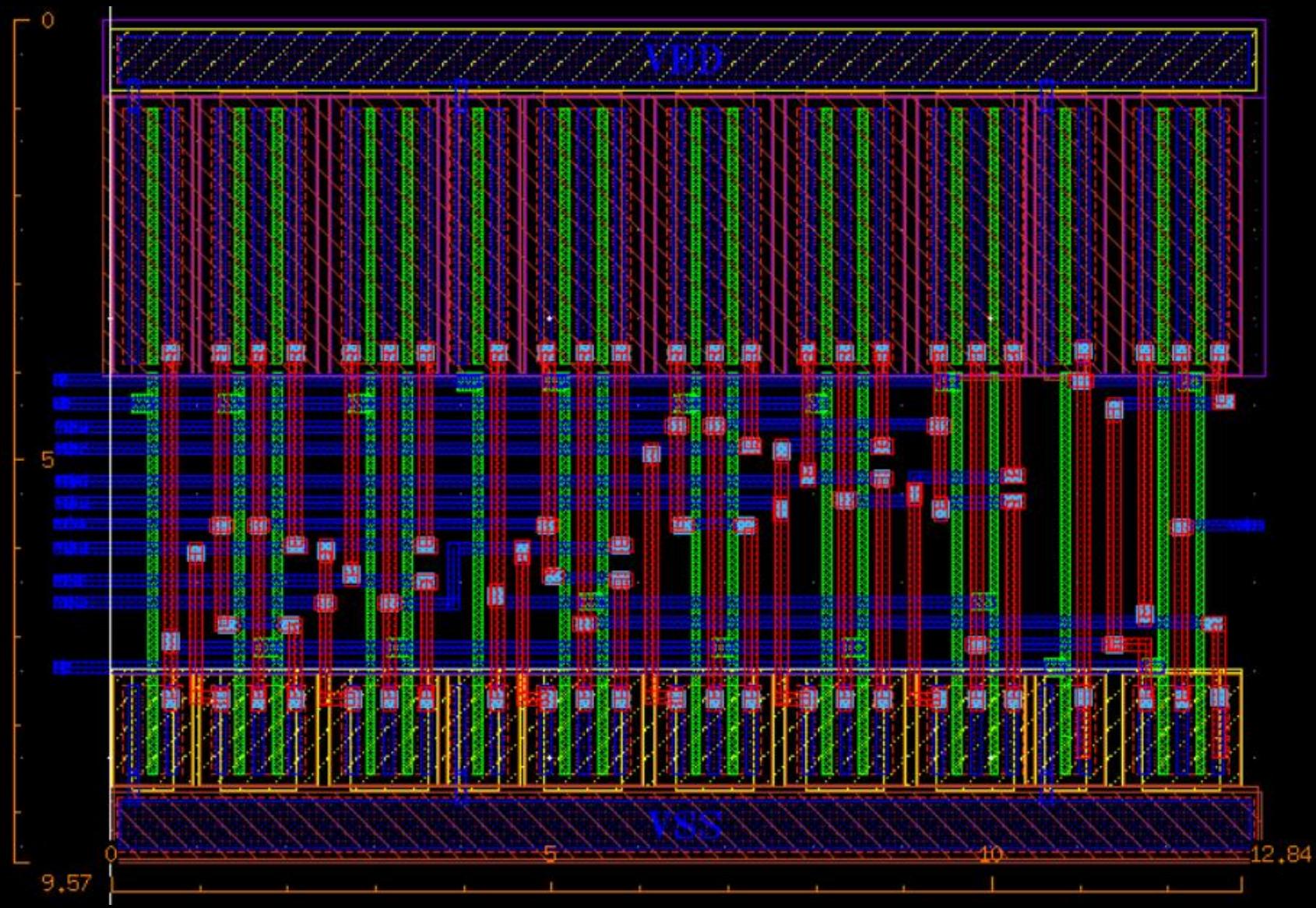
# 8x1 MUX SWITCH - Schematic & Symbol



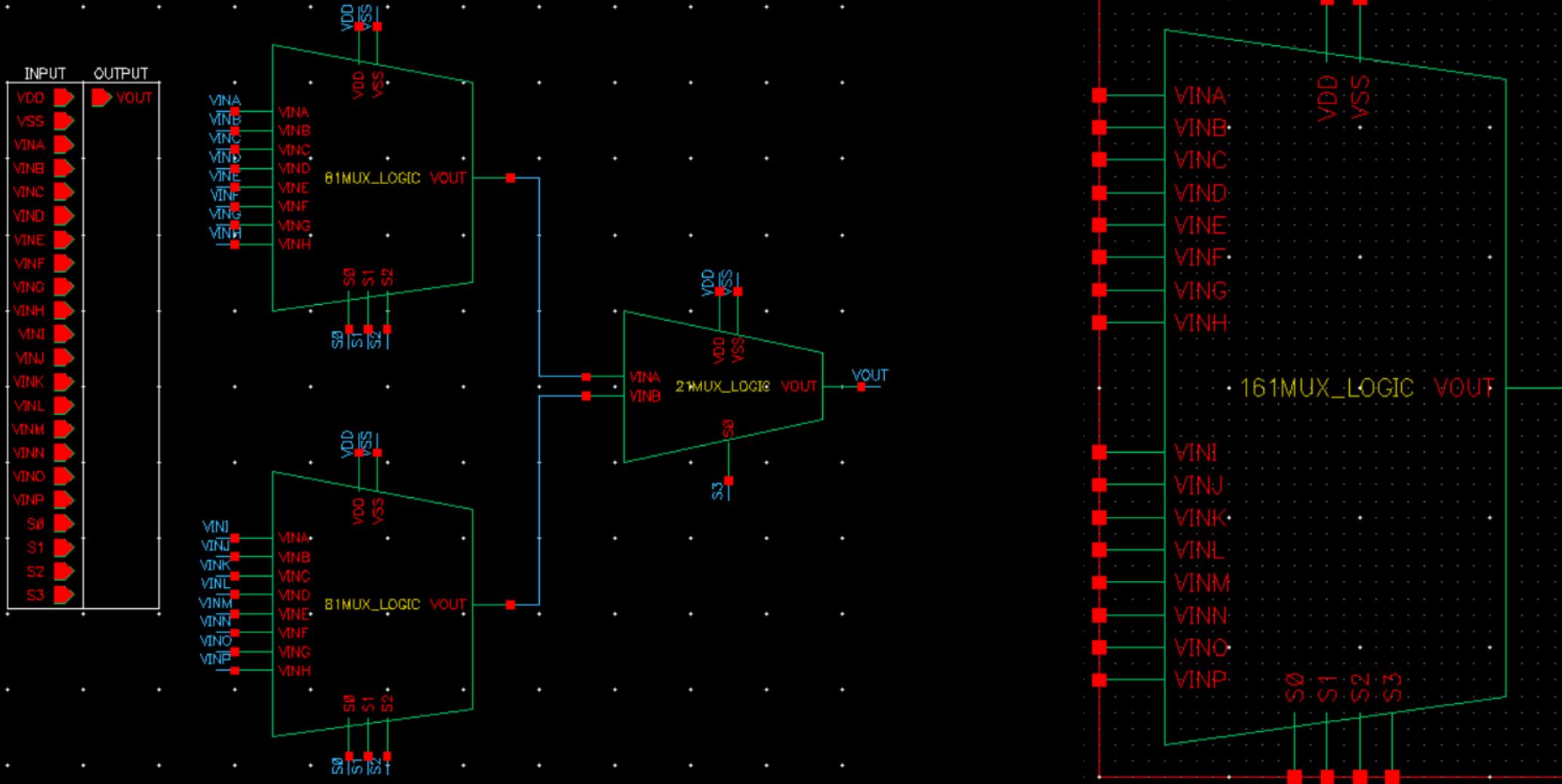
# 8x1 MUX SWITCH - Simulation



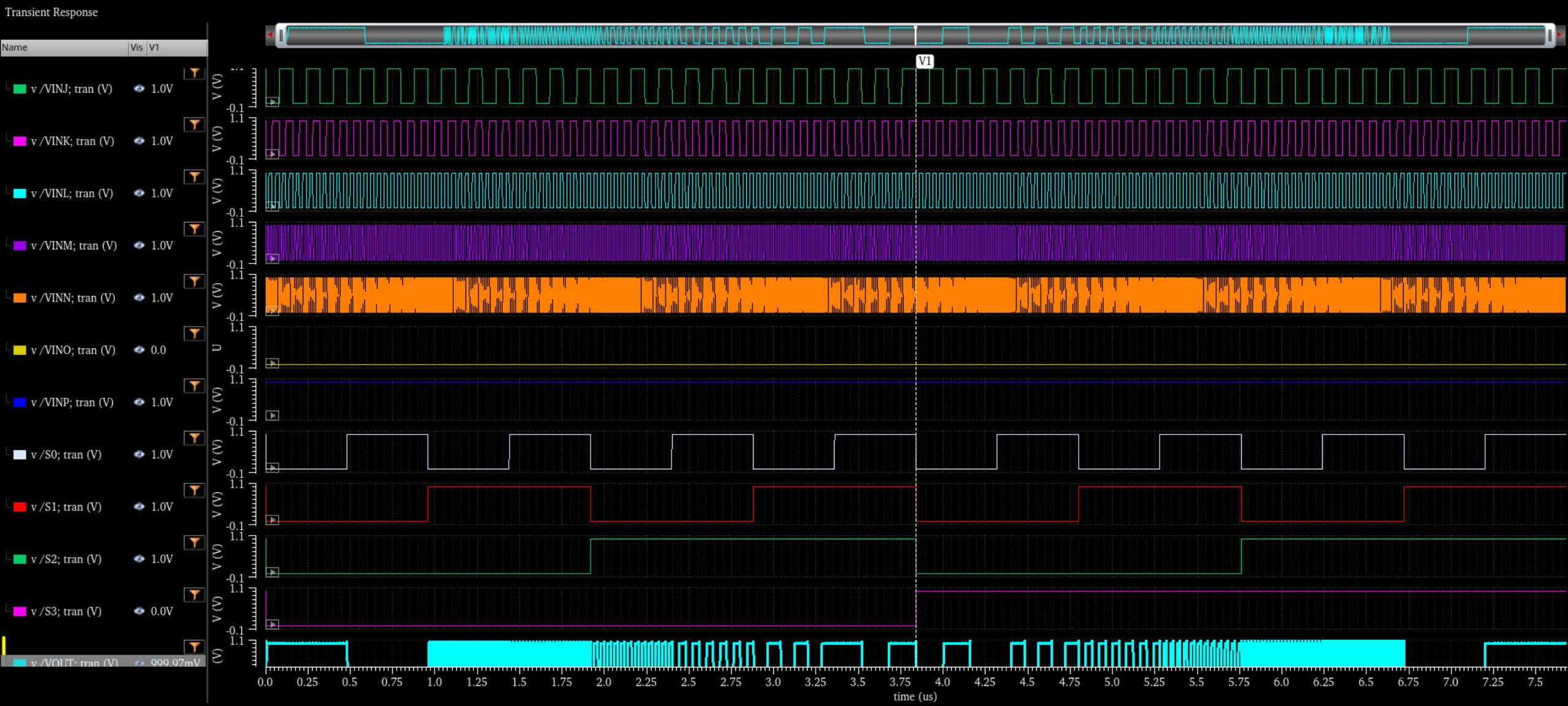
# 8x1 MUX SWITCH - Layout



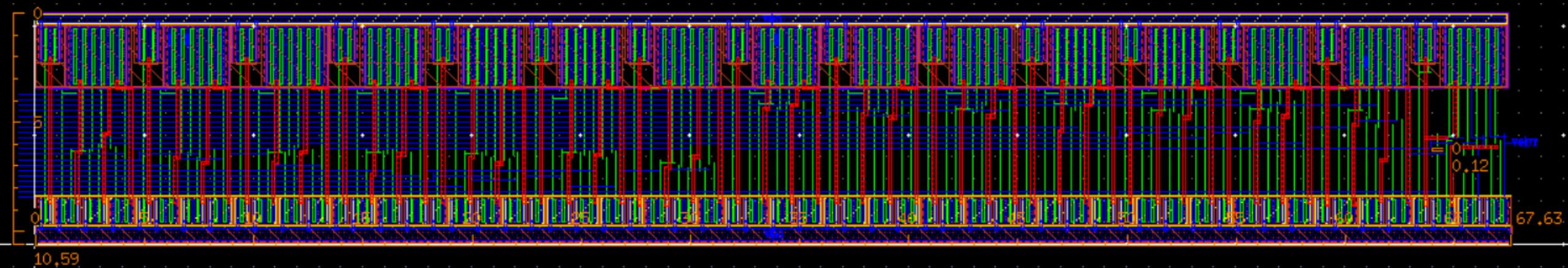
# 16x1 MUX LOGIC - Schematic & Symbol



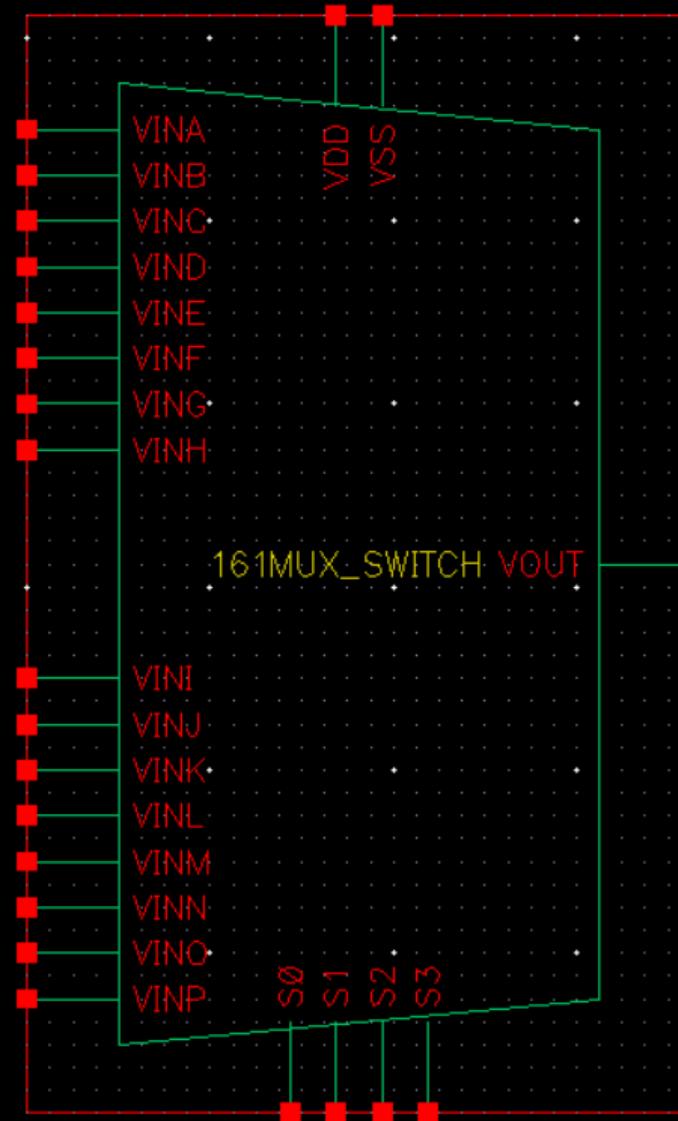
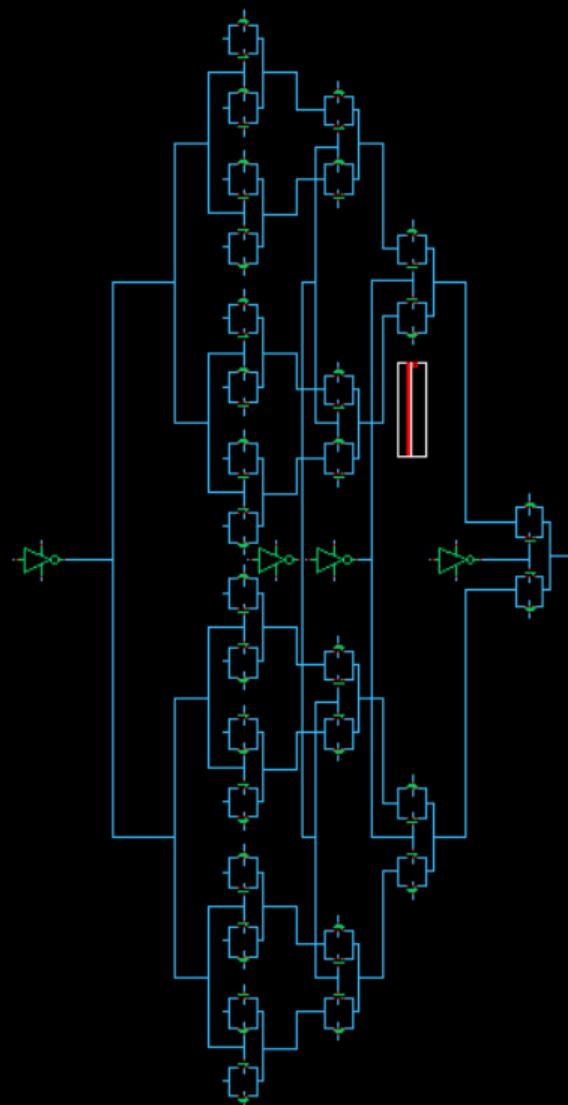
# 16x1 MUX LOGIC - Simulation



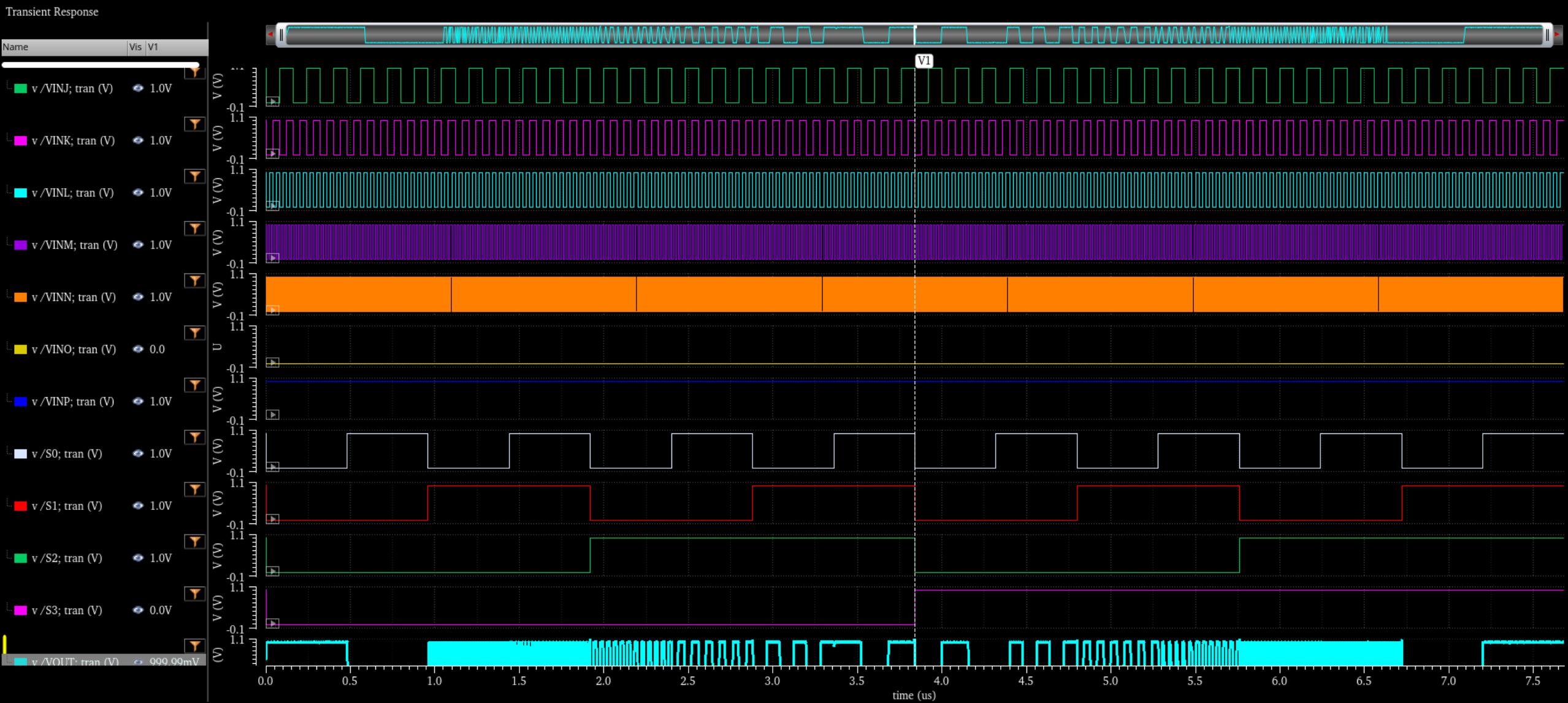
# 16x1 MUX LOGIC - Layout



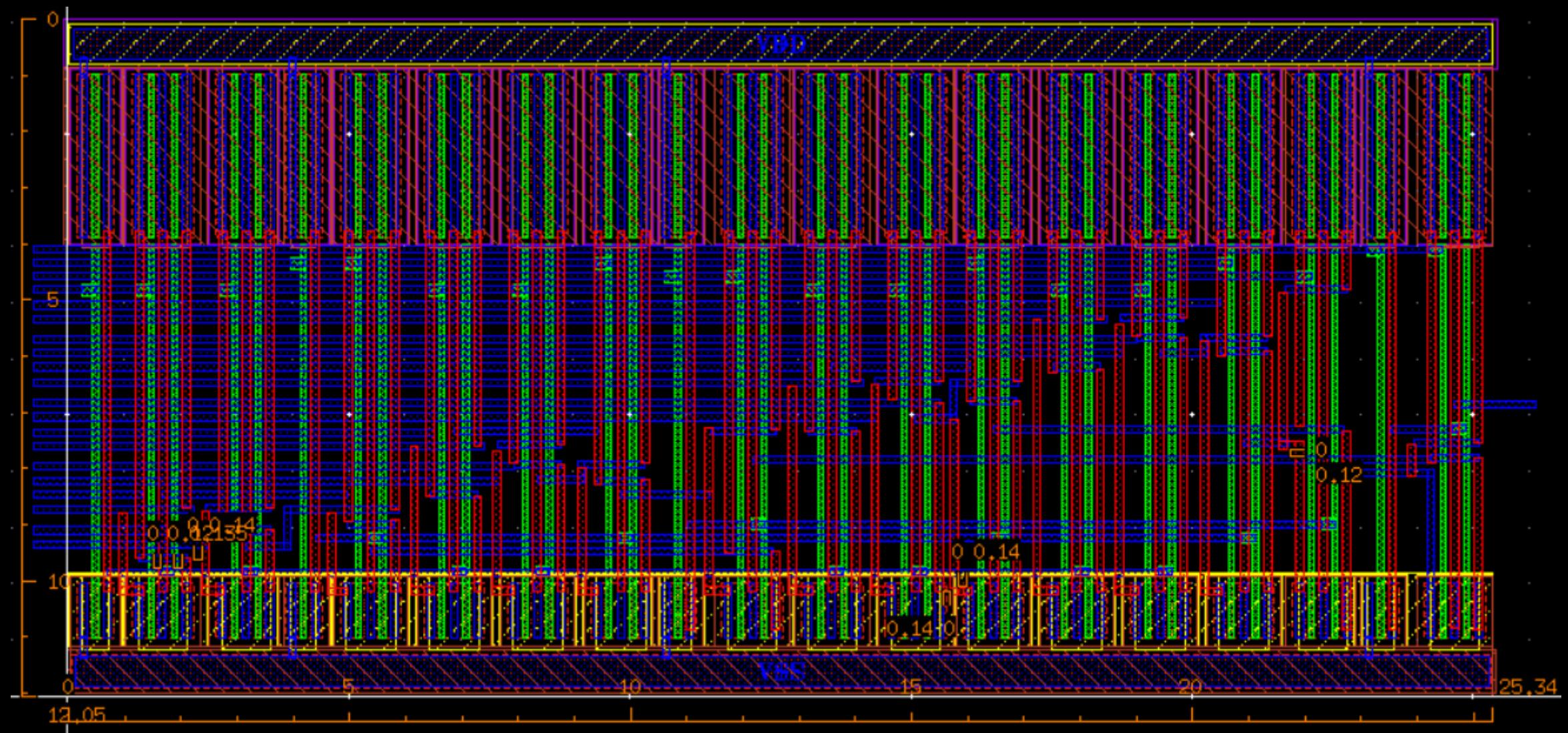
# 16x1 MUX SWITCH - Schematic & Symbol



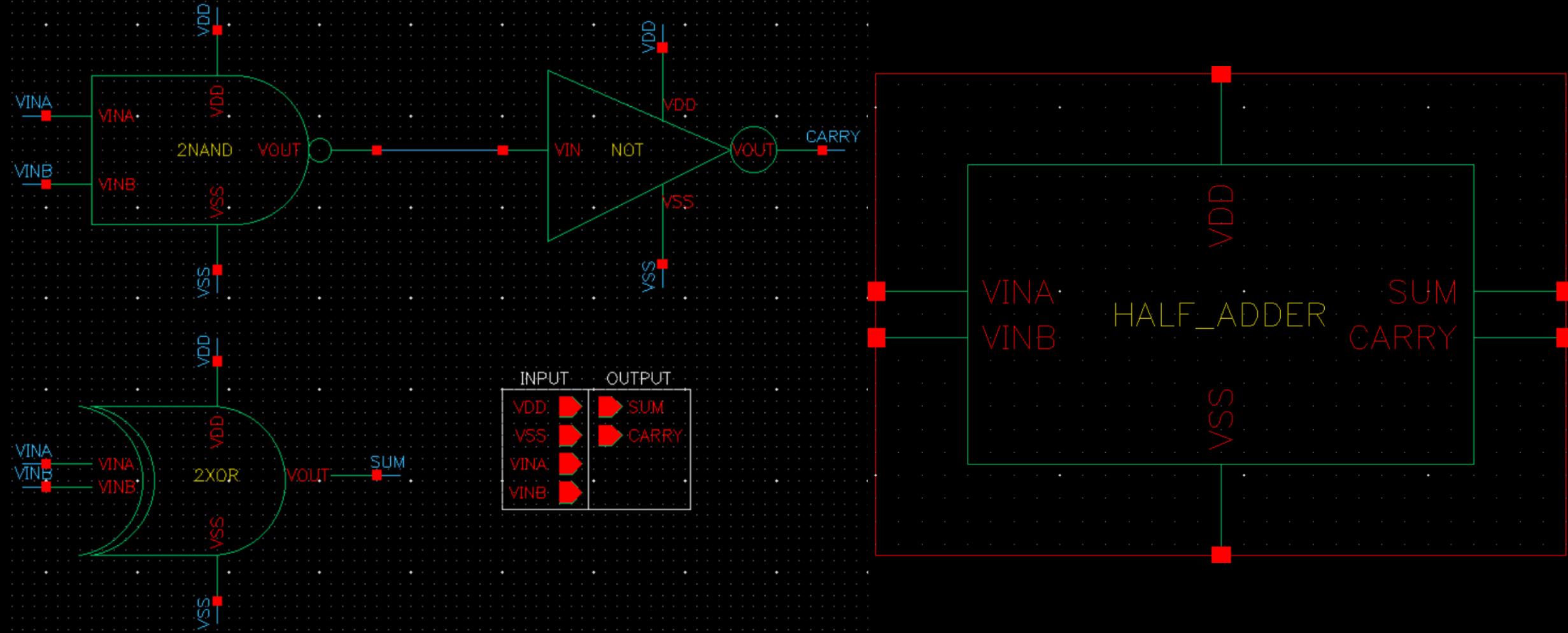
# 16x1 MUX SWITCH - Simulation



# 16x1 MUX SWITCH - Layout



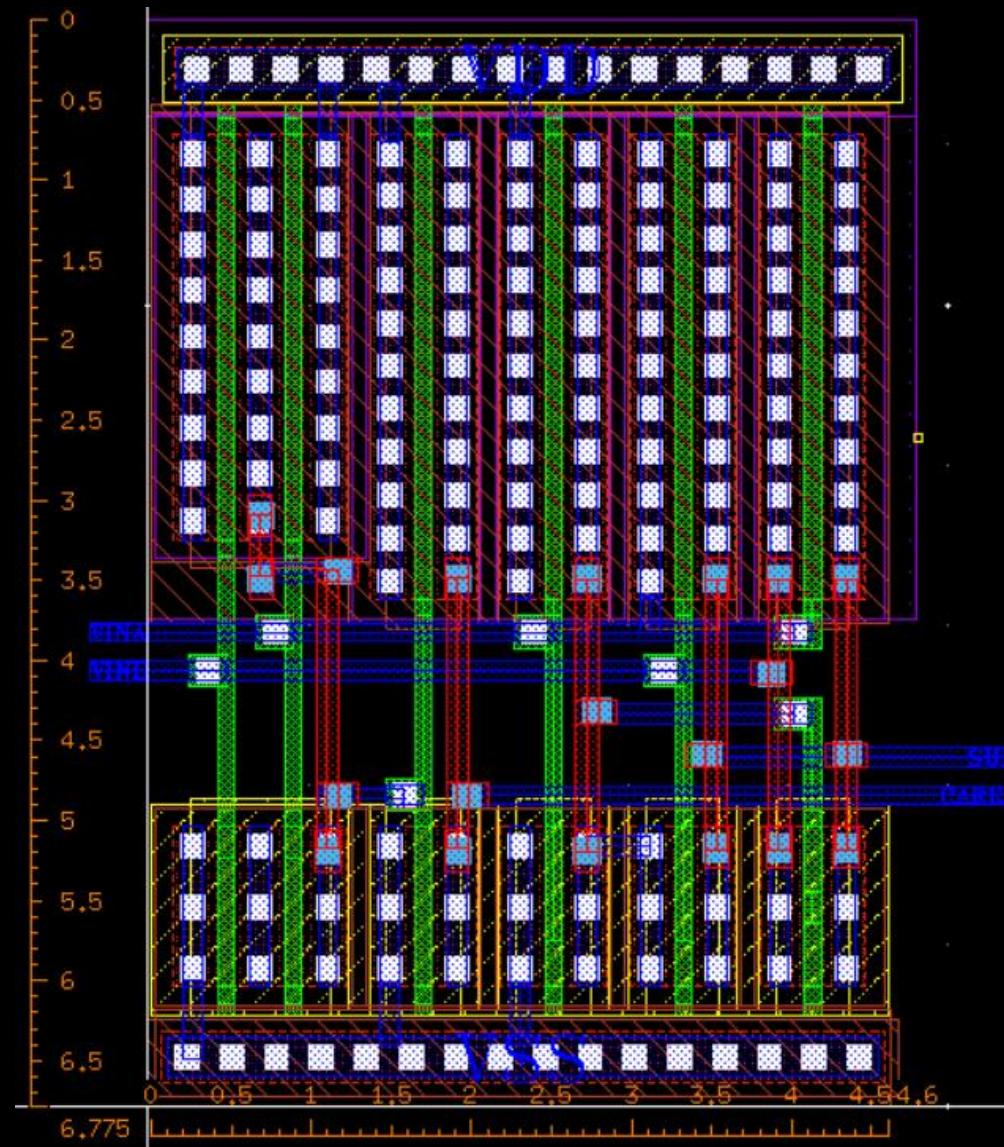
# HALF ADDER - Schematic & Symbol



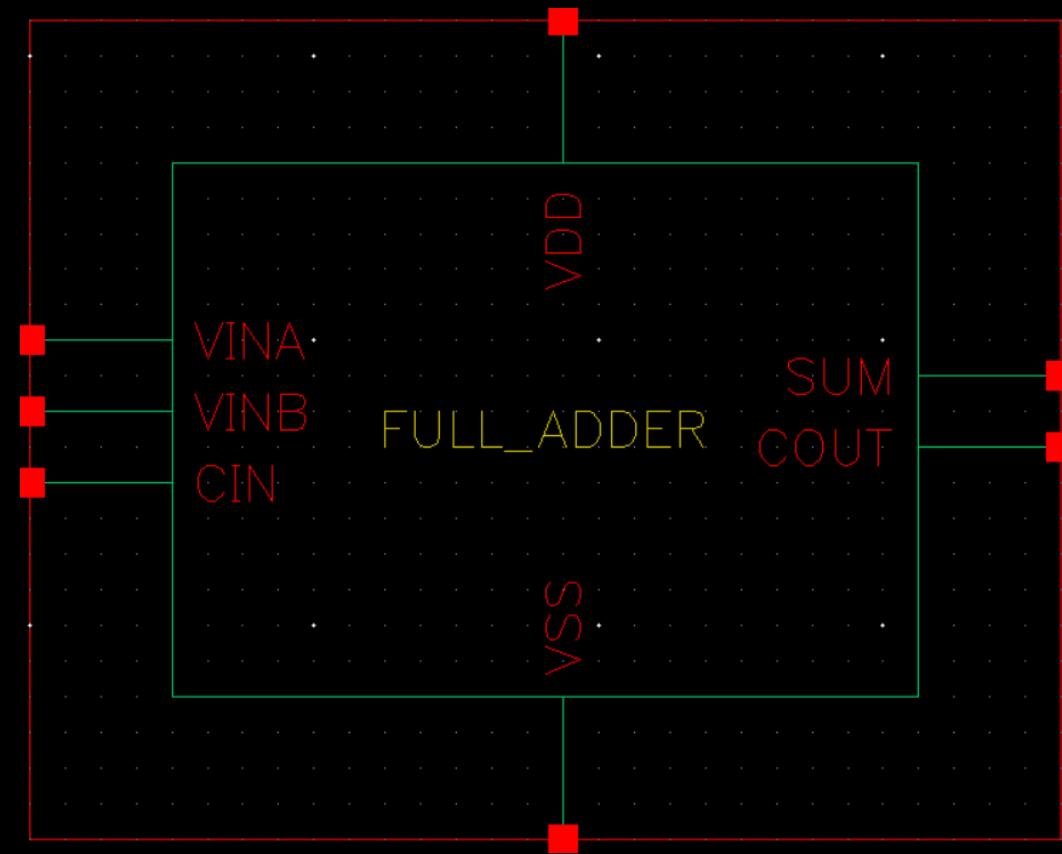
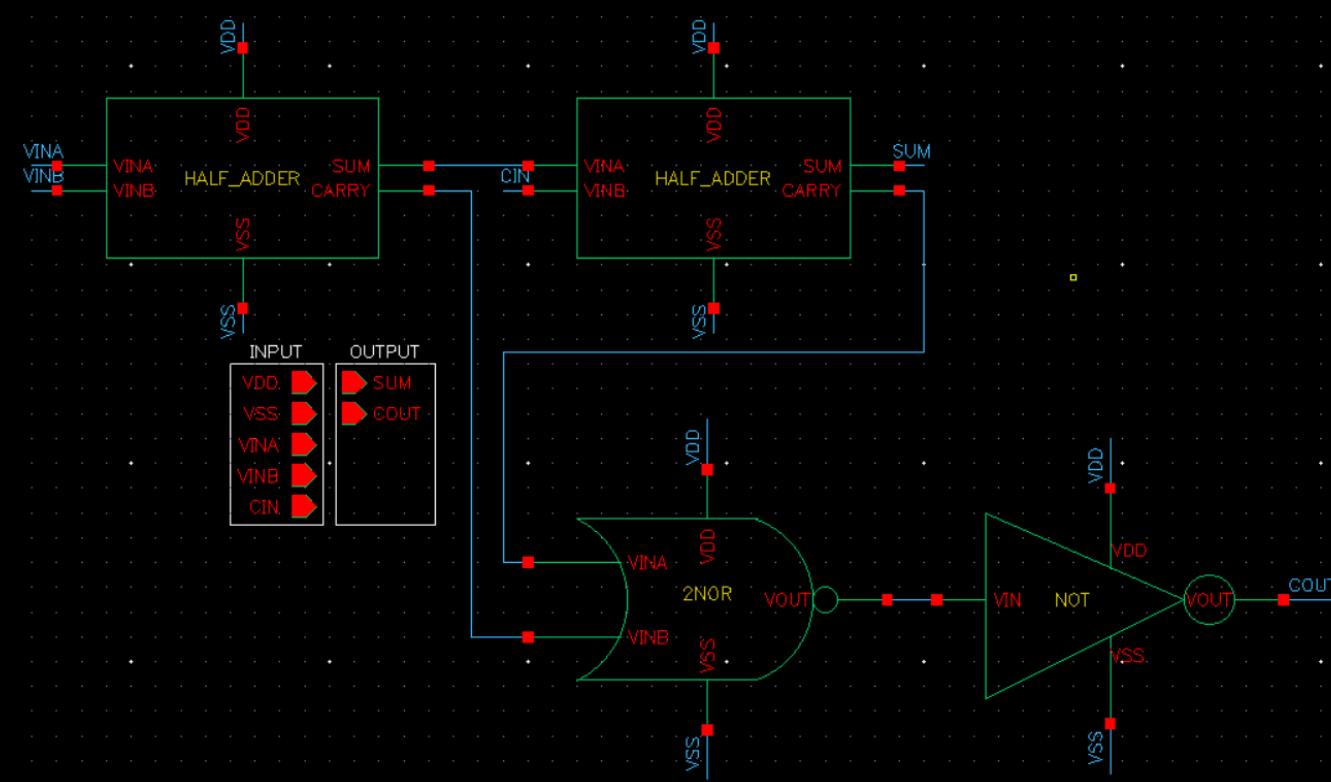
# HALF ADDER - Simulation



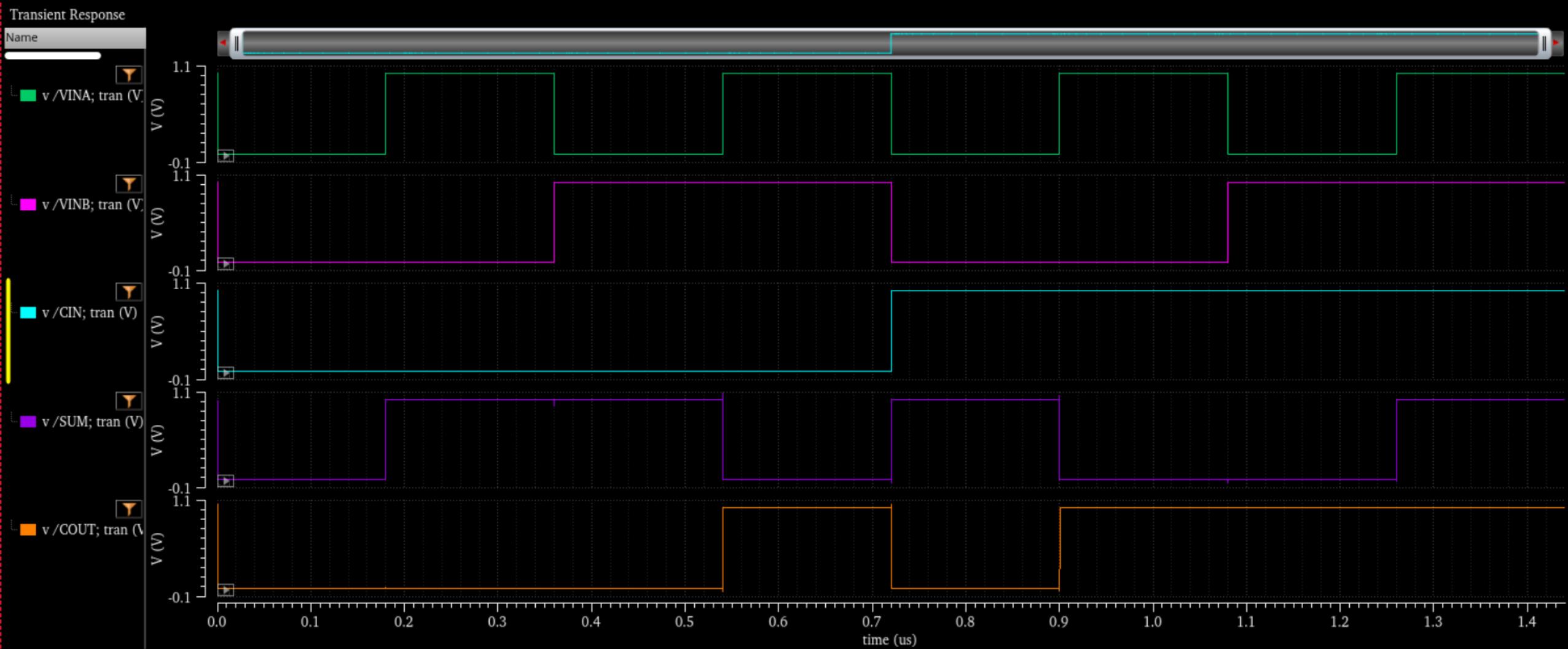
# HALF ADDER - Layout



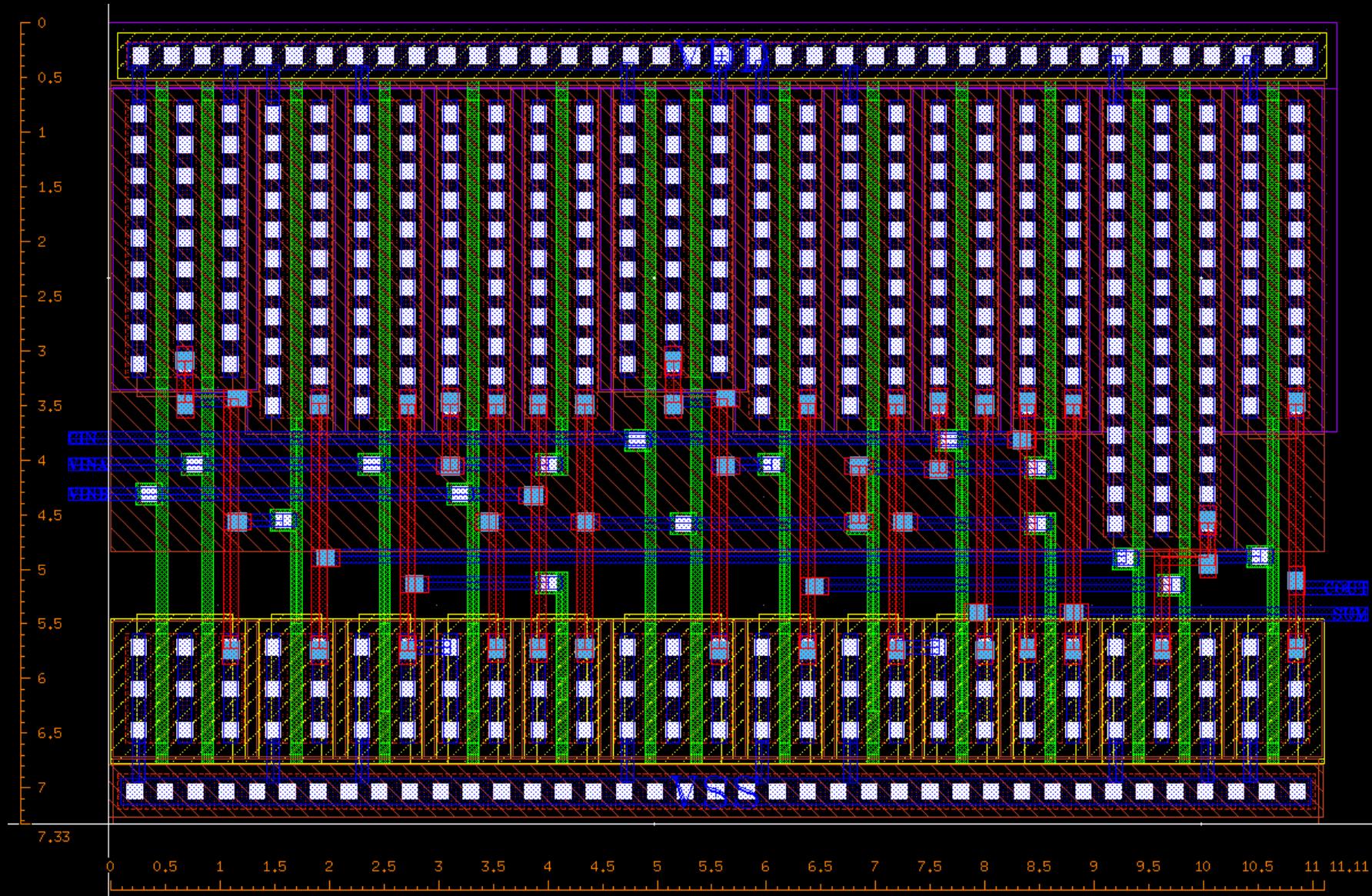
# FULL ADDER - Schematic & Symbol



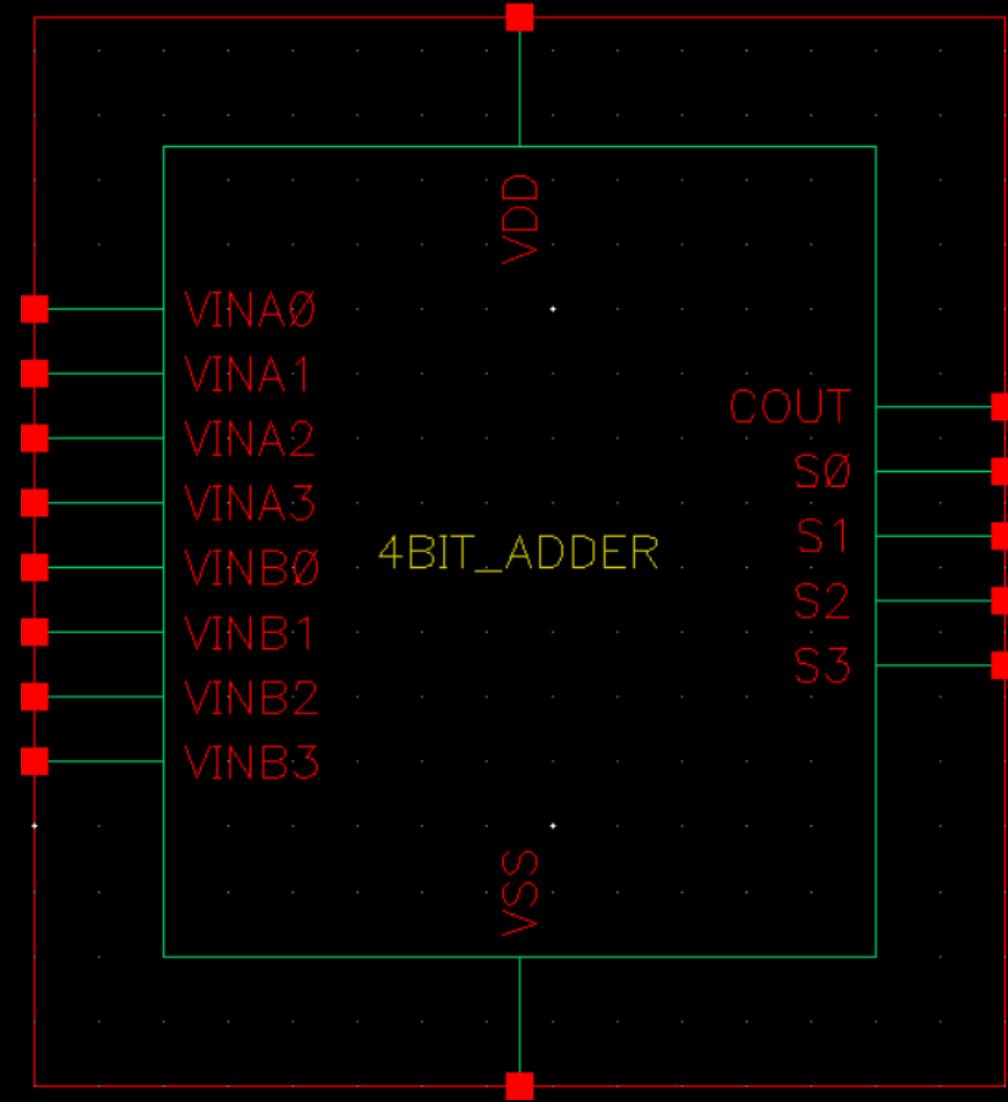
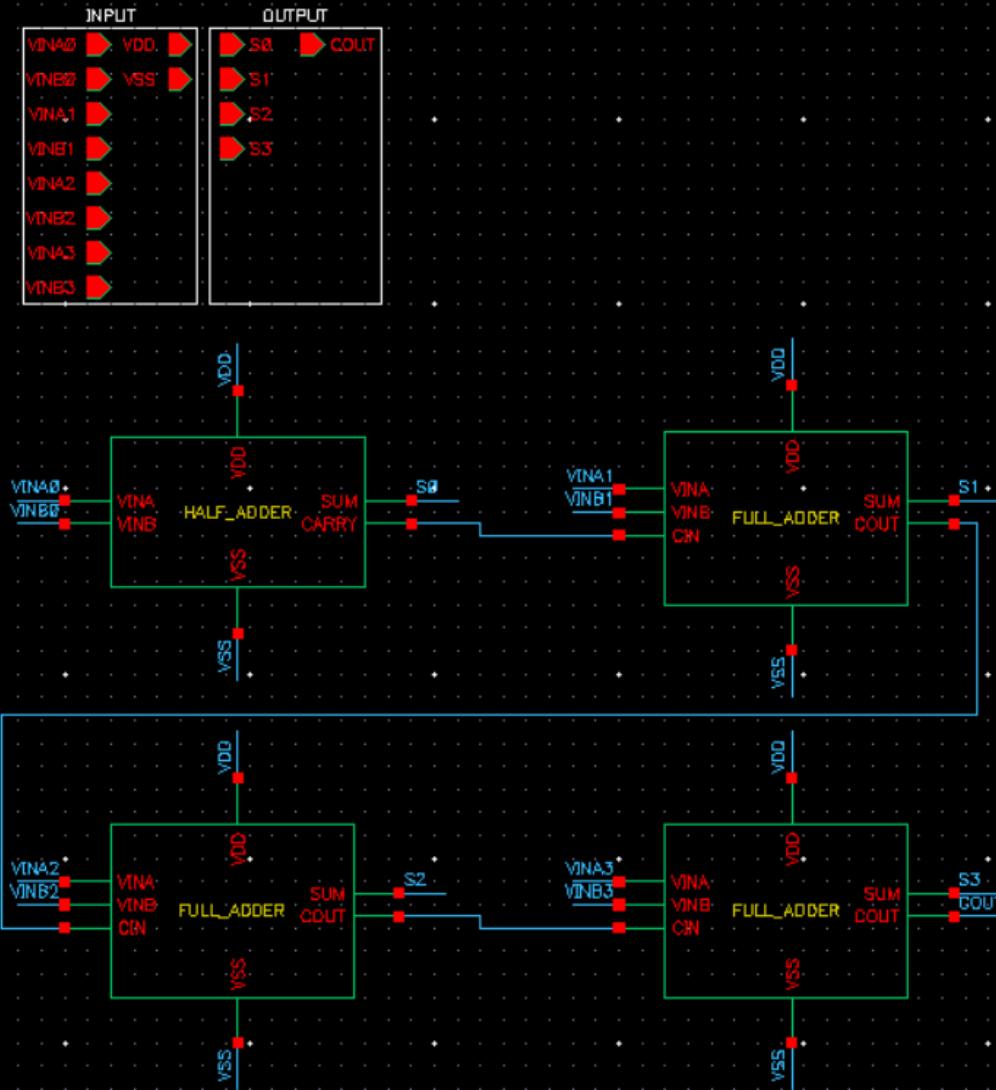
# FULL ADDER - Simulation



# FULL ADDER - Layout

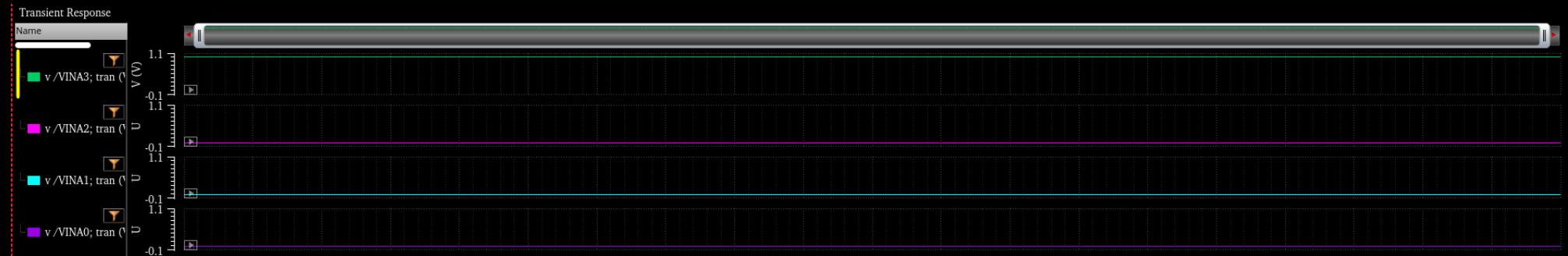


# 4BIT ADDER - Schematic & Symbol

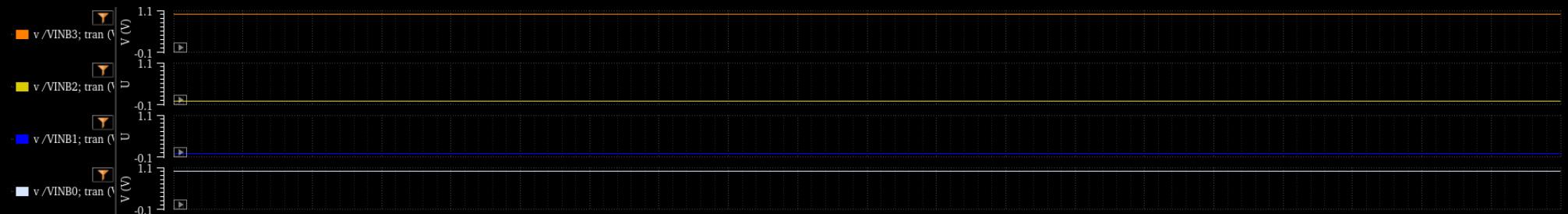


# 4BIT ADDER - Simulation

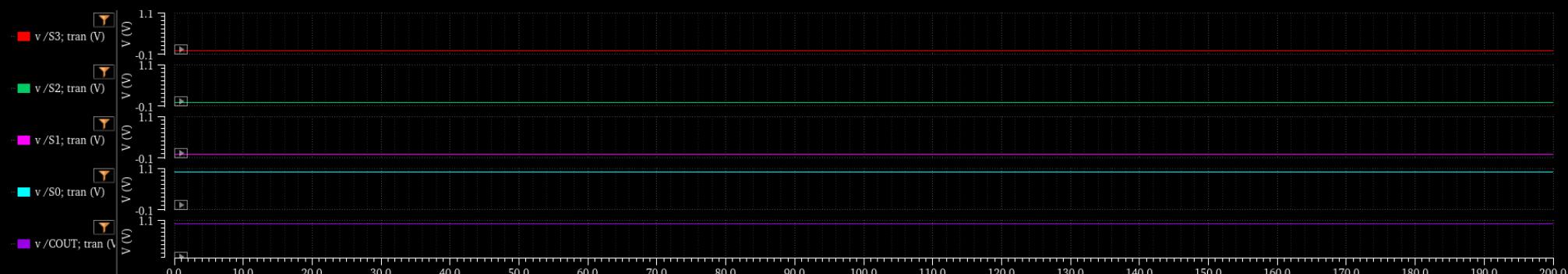
First bits  
1000<sub>b</sub> = 8



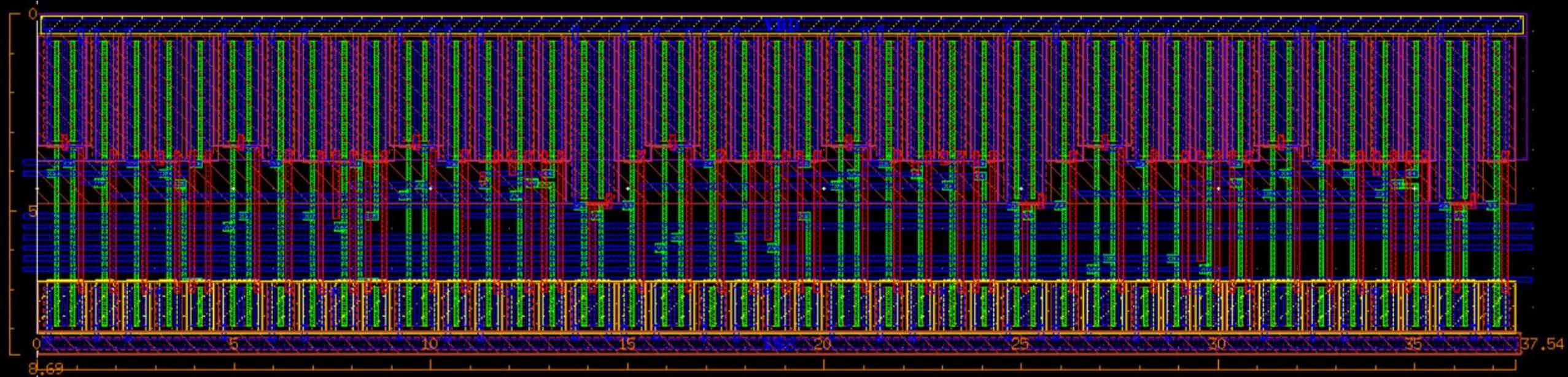
Second bits  
1001<sub>b</sub> = 9



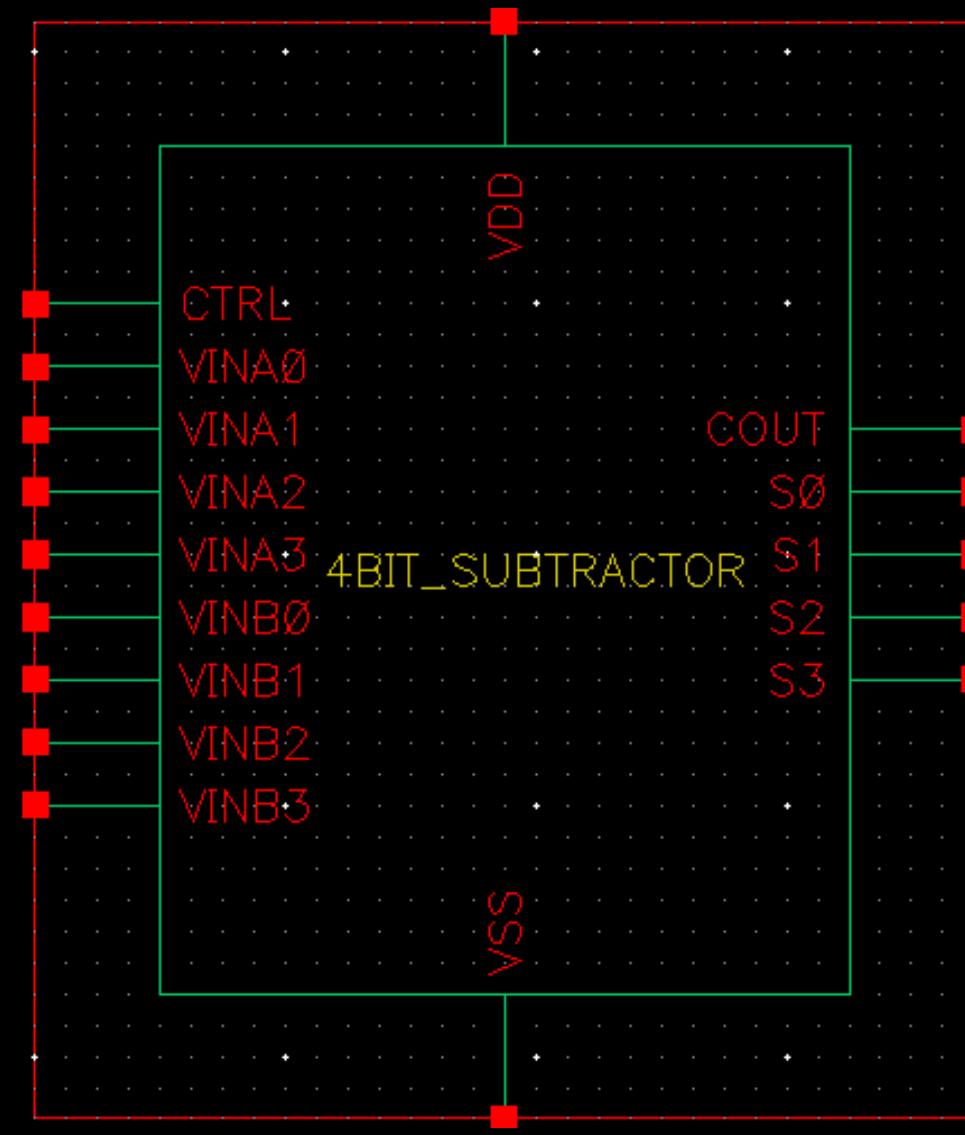
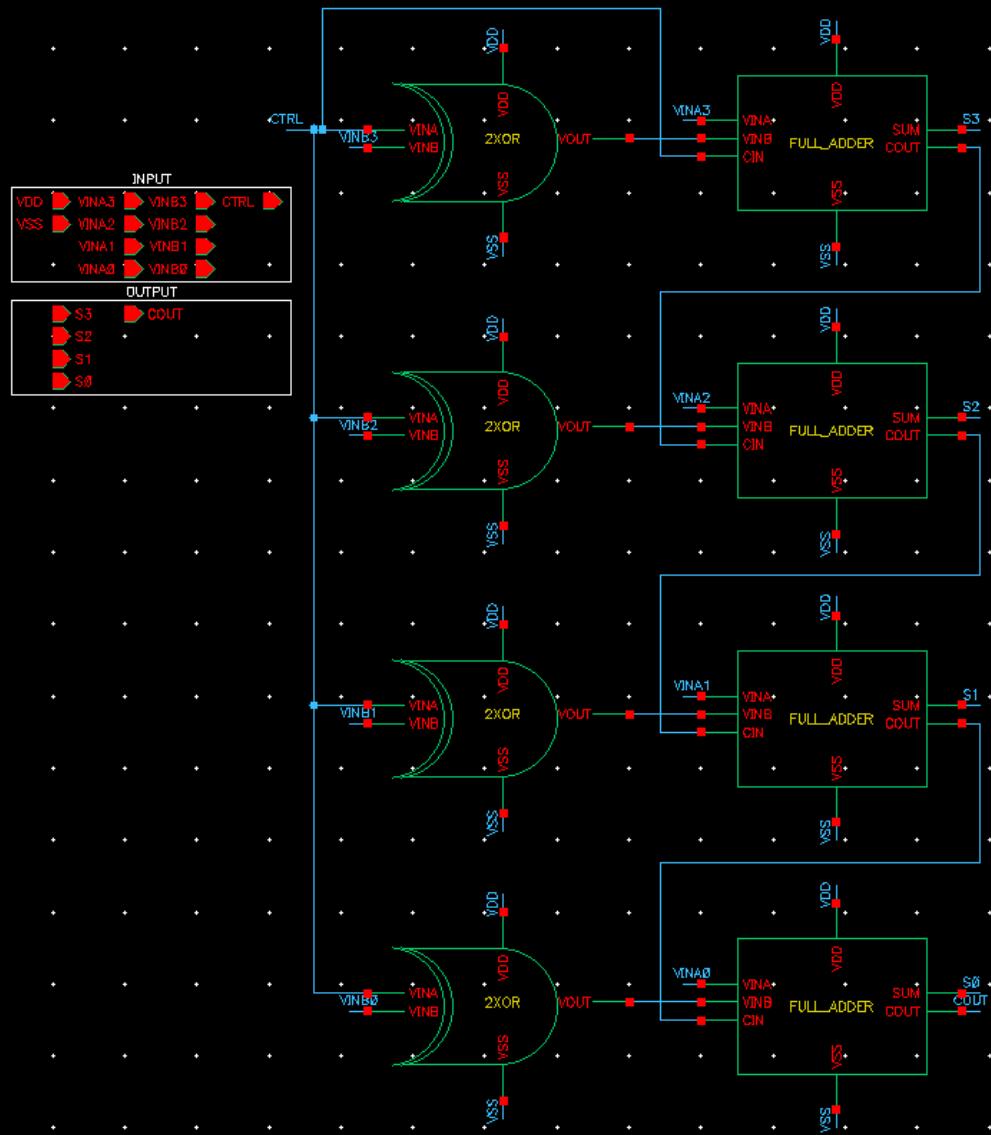
Final bits  
0001<sub>b</sub> = 1  
Carry = 1



# 4BIT ADDER - Layout



# 4BIT SUBTRACTOR - Schematic & Symbol

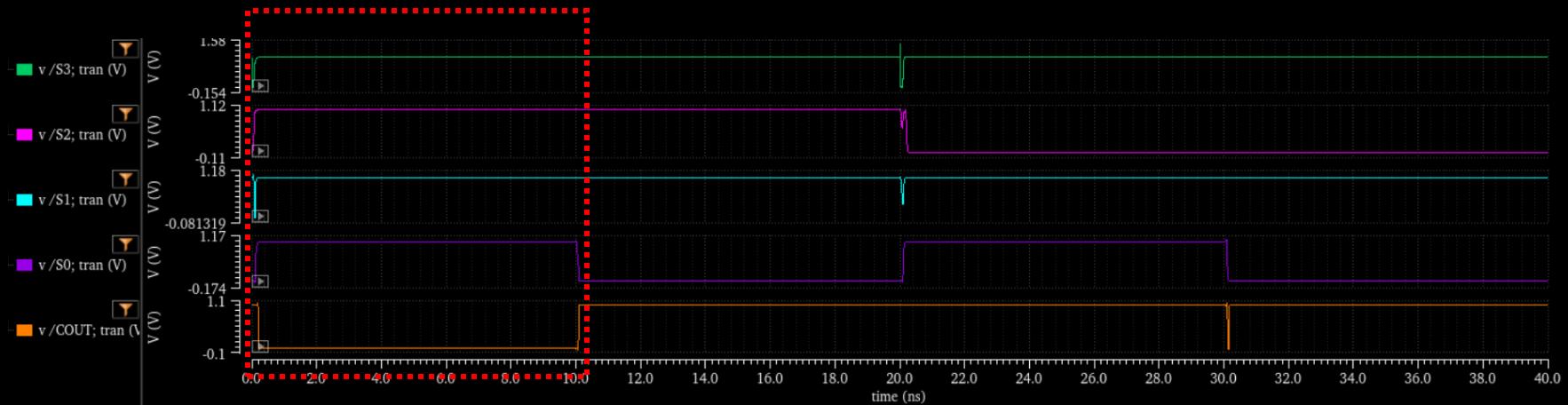


# 4BIT SUBTRACTOR - Simulation

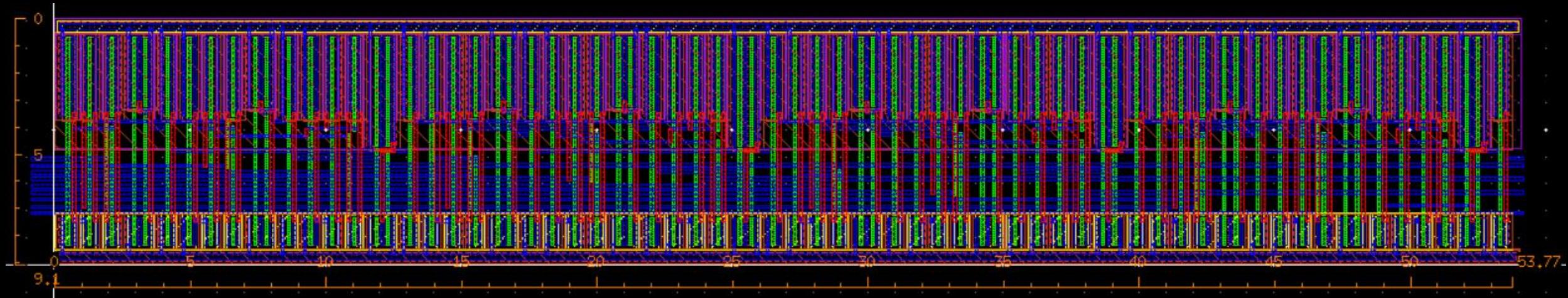
First bits  
 $0111_b = 7$



Second bits  
 $100xb = 8\sim 9$



# 4BIT SUBTRACTOR - Layout

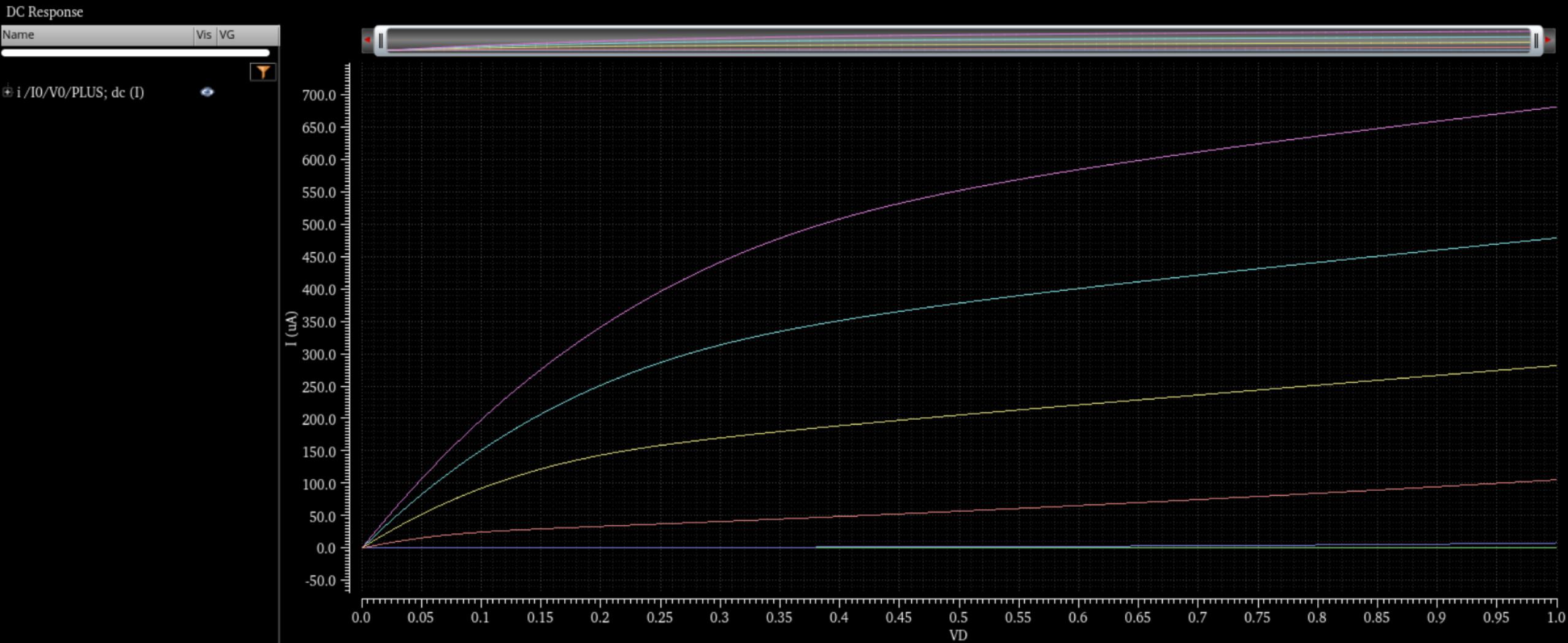


# Analog Circuits

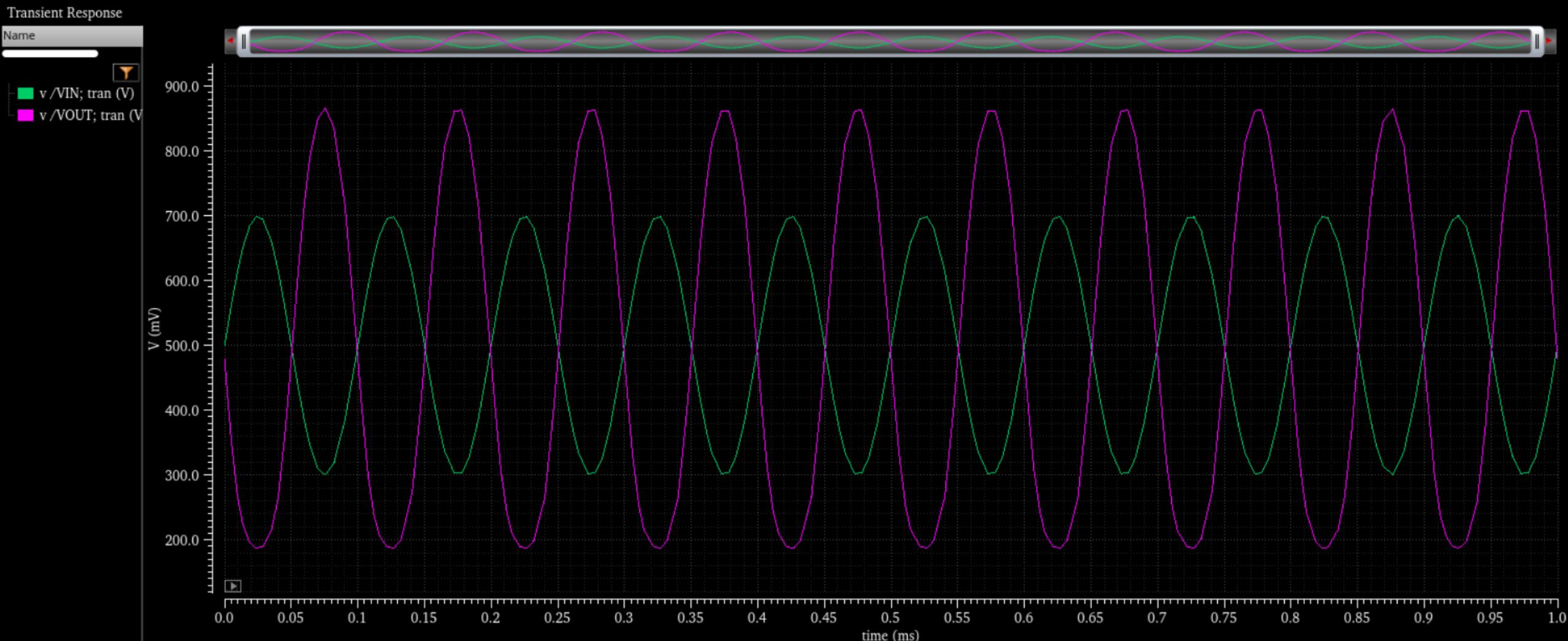
- Common Source AMP
- Differential AMP

# Common Source AMP - Schematics

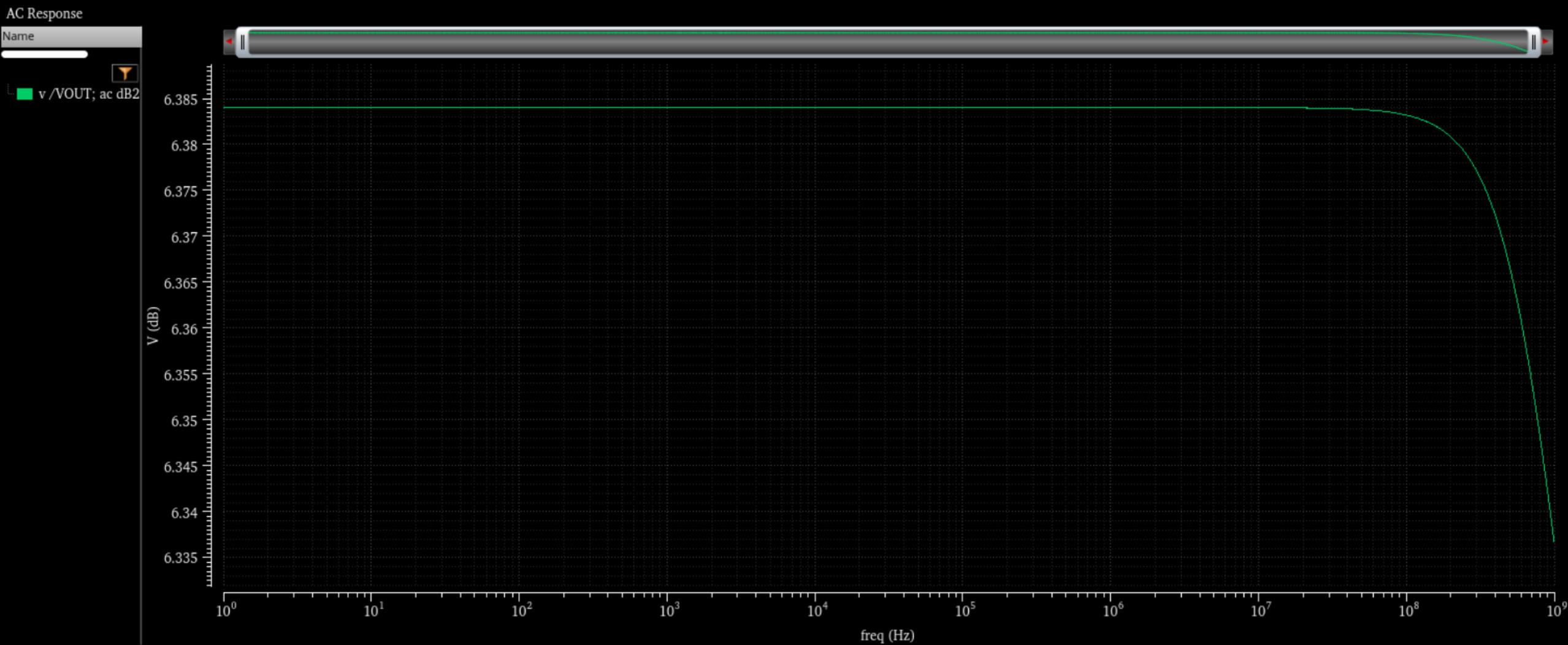
# Common Source AMP – Simulation



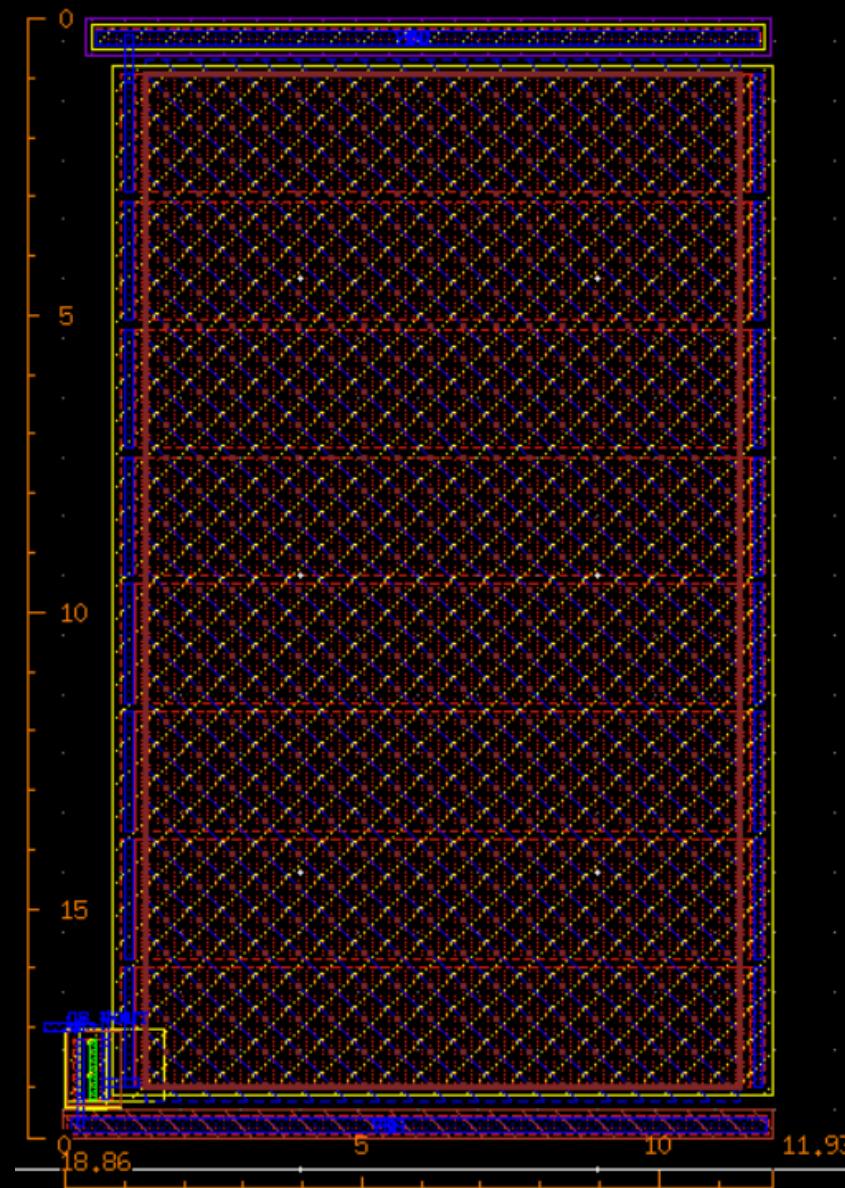
# Common Source AMP – Simulation



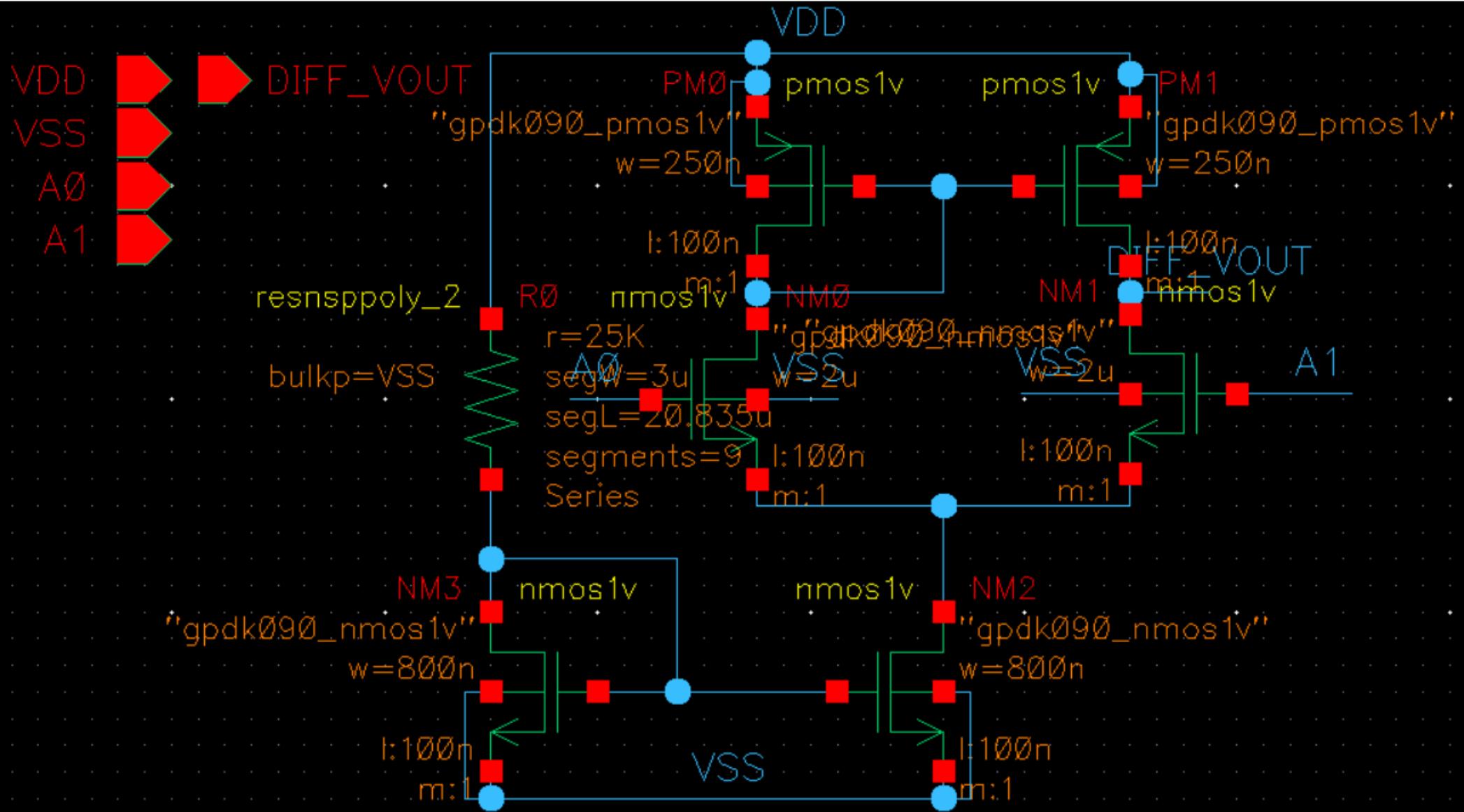
# Common Source AMP – Simulation



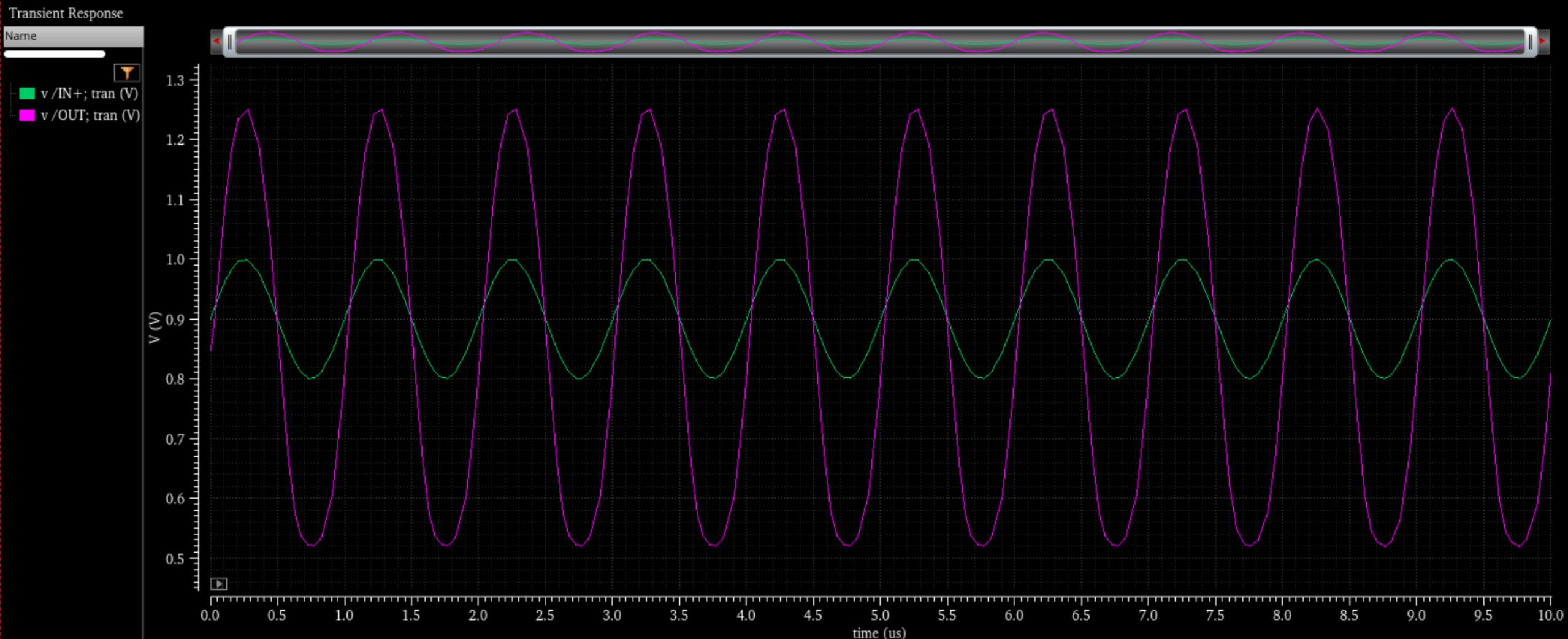
# Common Source AMP – Layout



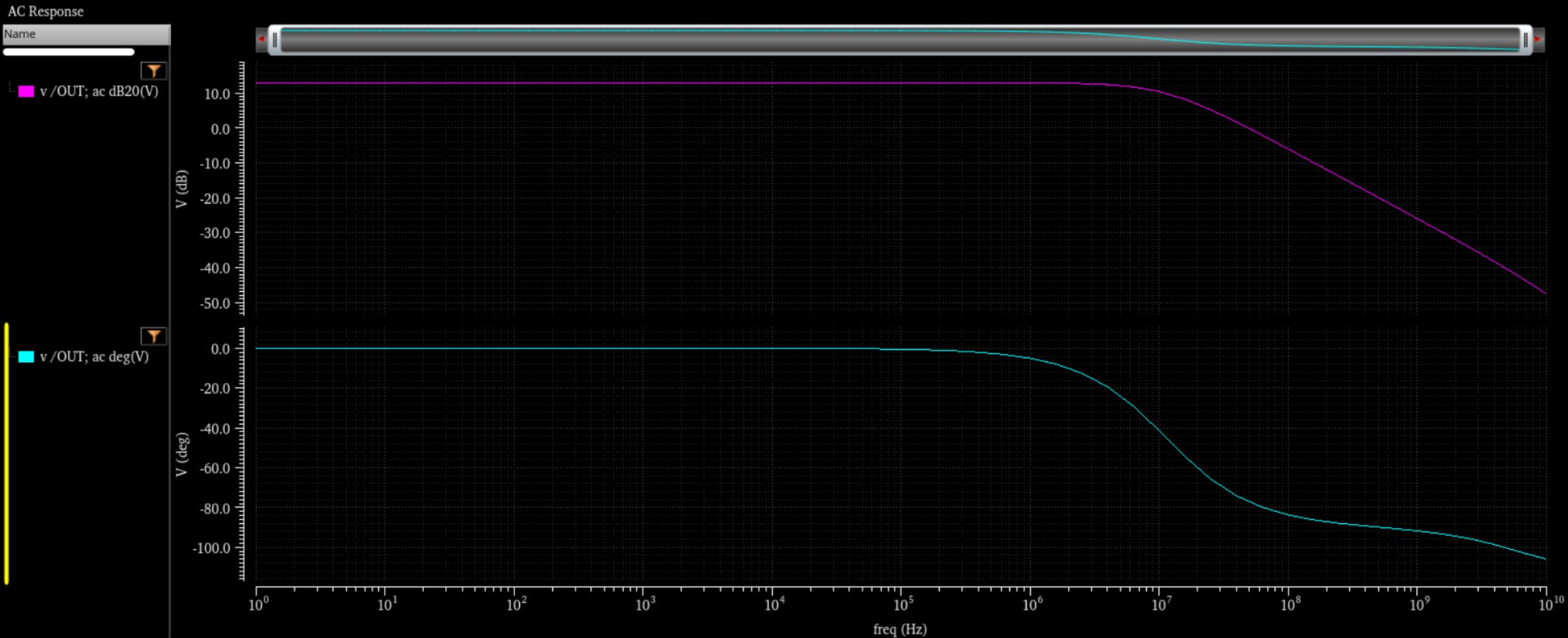
# Differential AMP – Schematics



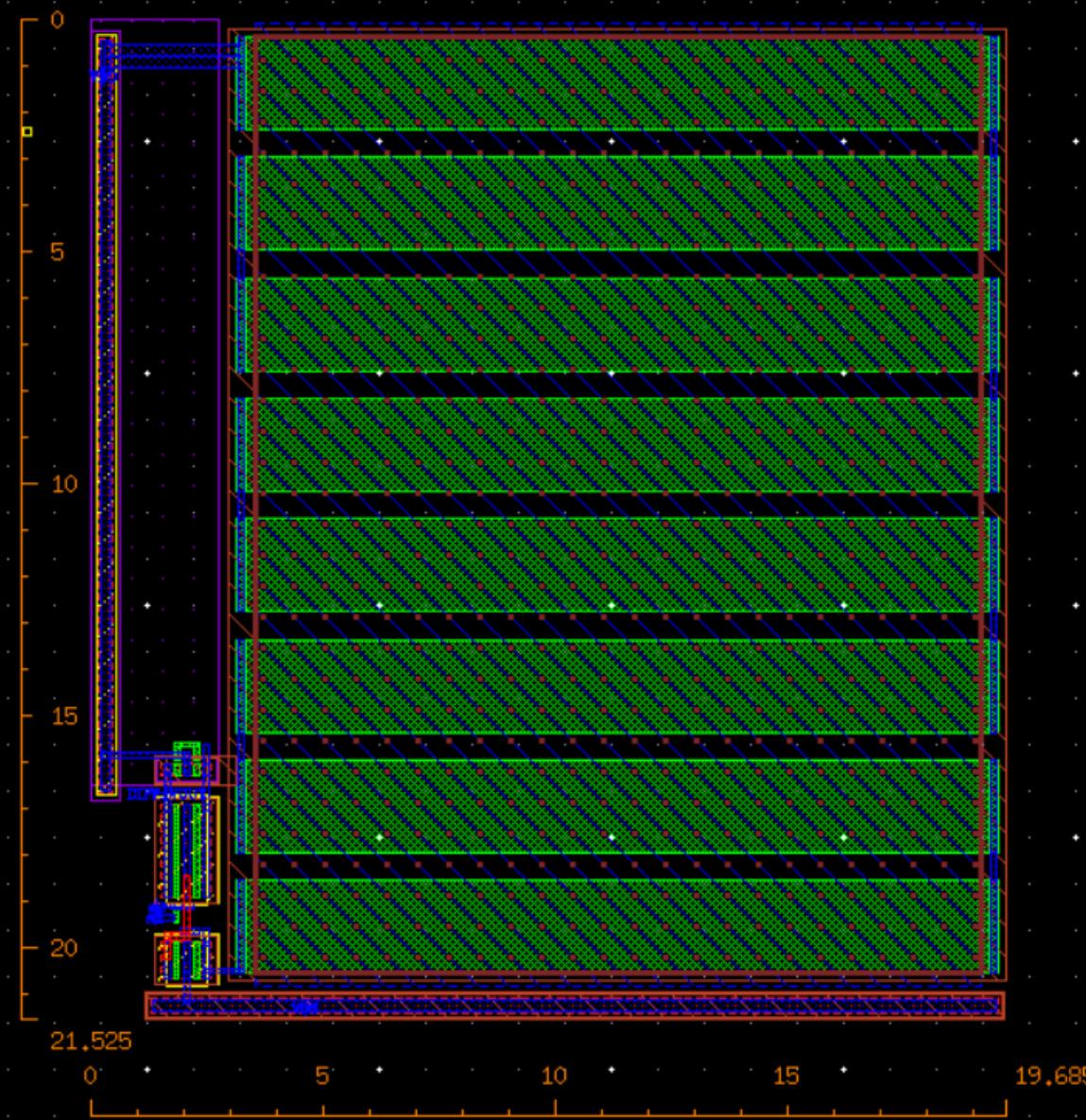
# Differential AMP – Simulation



# Differential AMP – Simulation



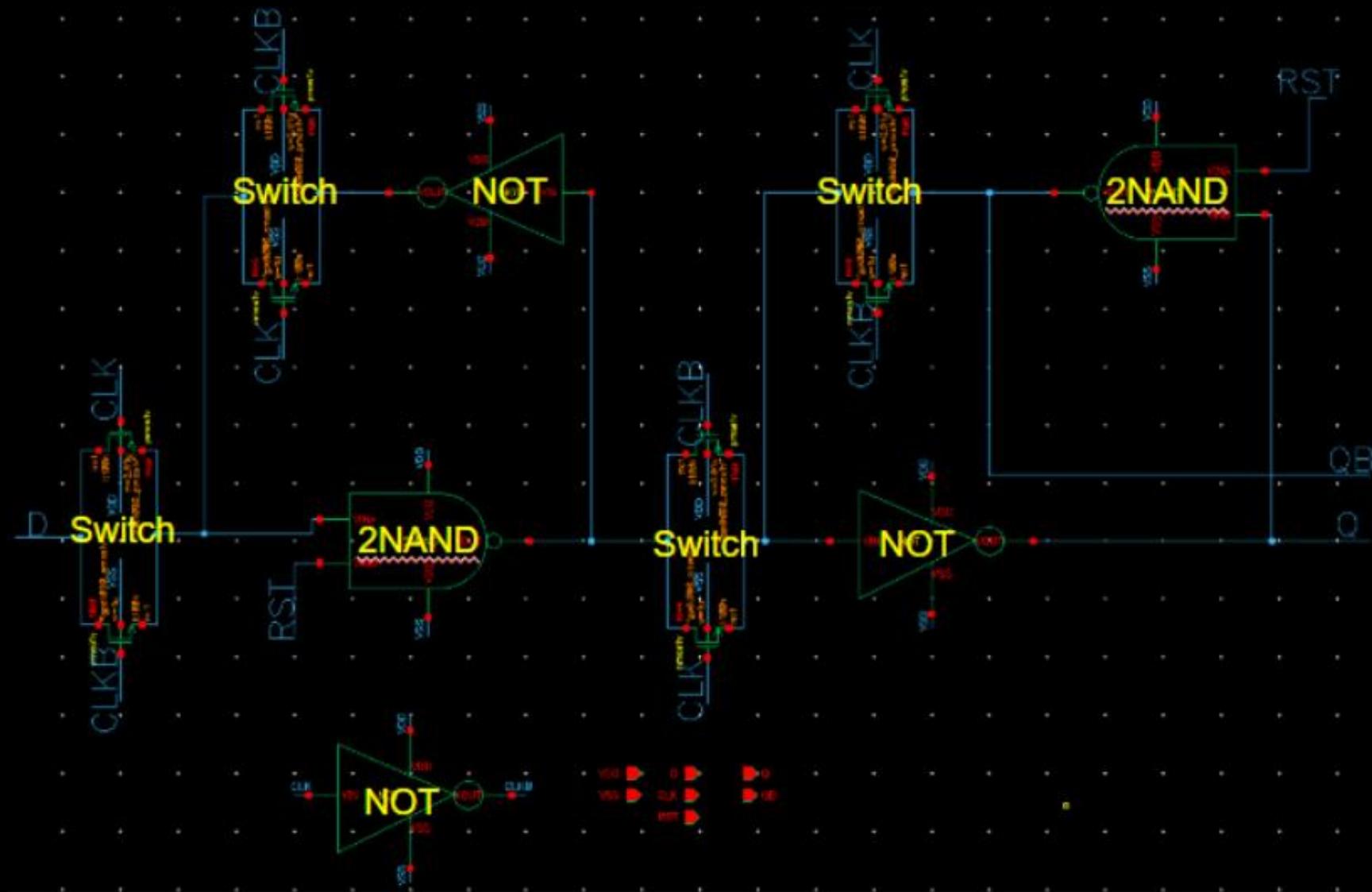
# Differential AMP – Layout



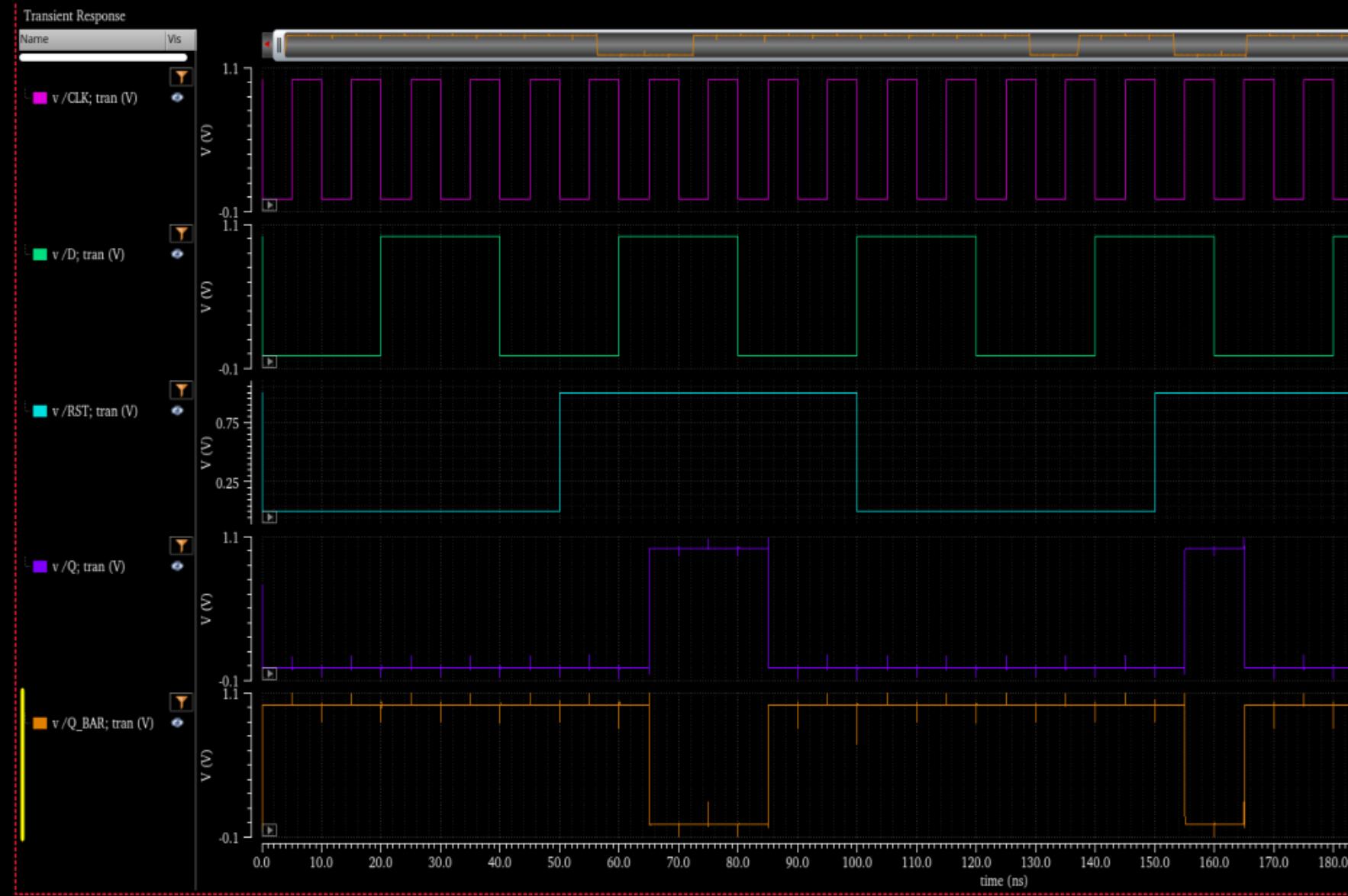
# Team Project

- D - Flip Flop
- 4Bit Sync Up Counter
- 4Bit Shift Register(PIPO)

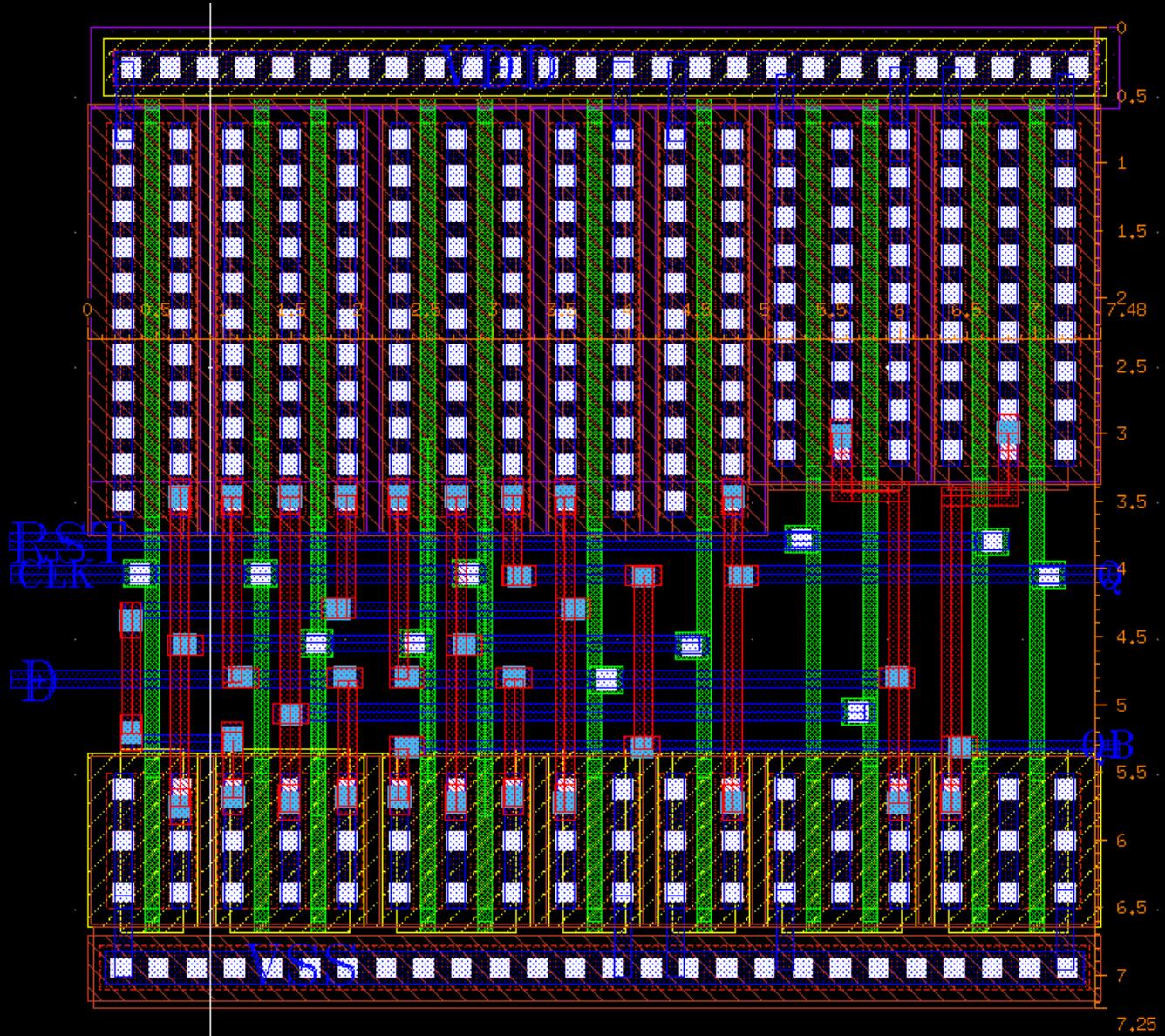
# D – Flip Flop – Schematics



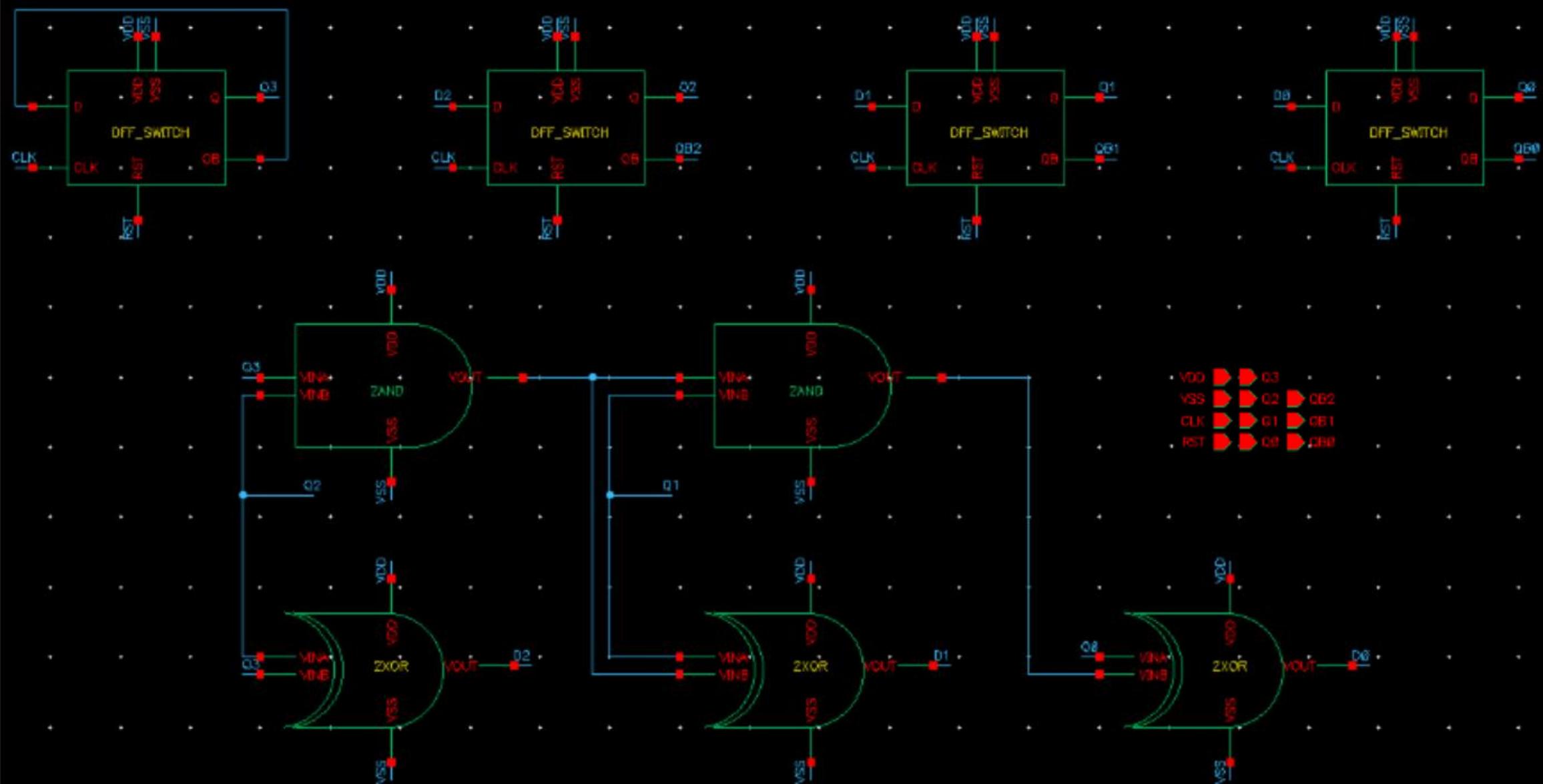
# D – Flip Flop – Simulation



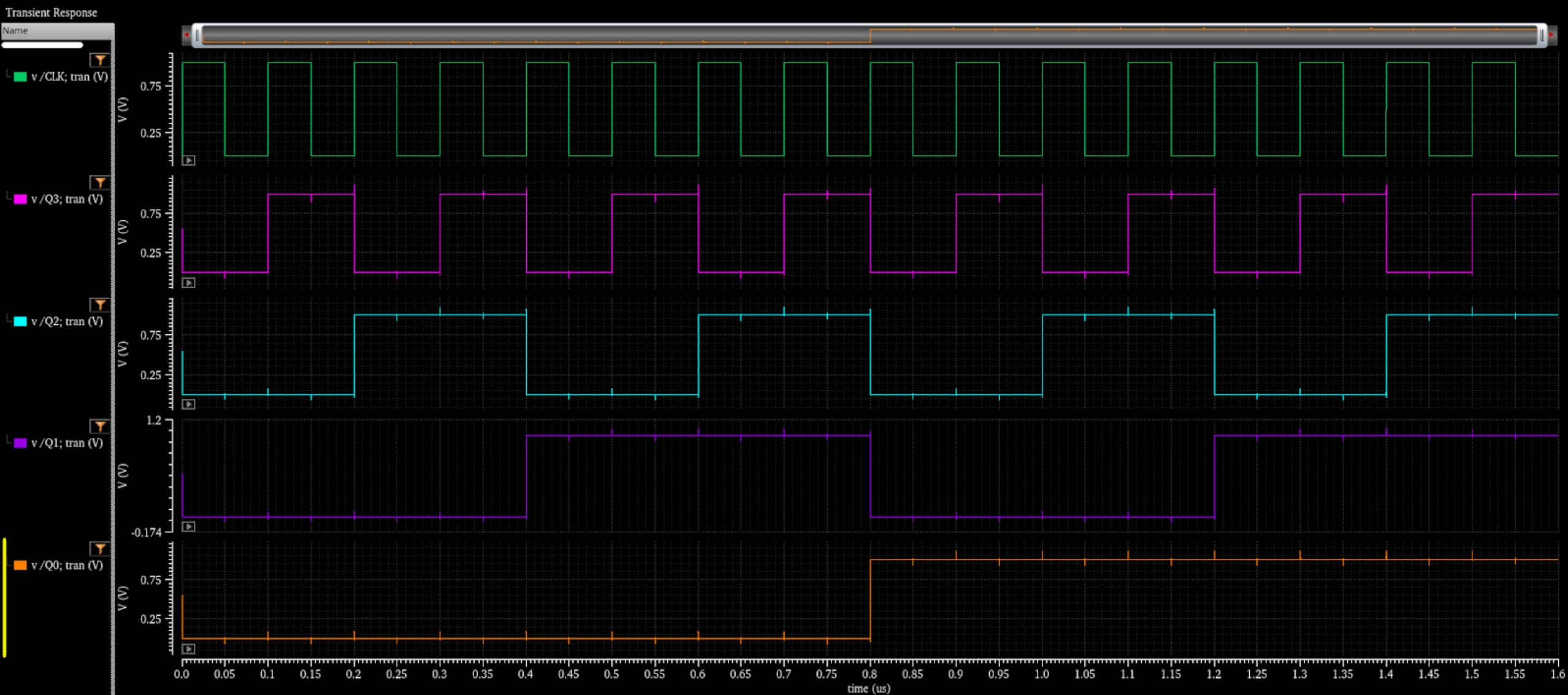
# D – Flip Flop – Layout



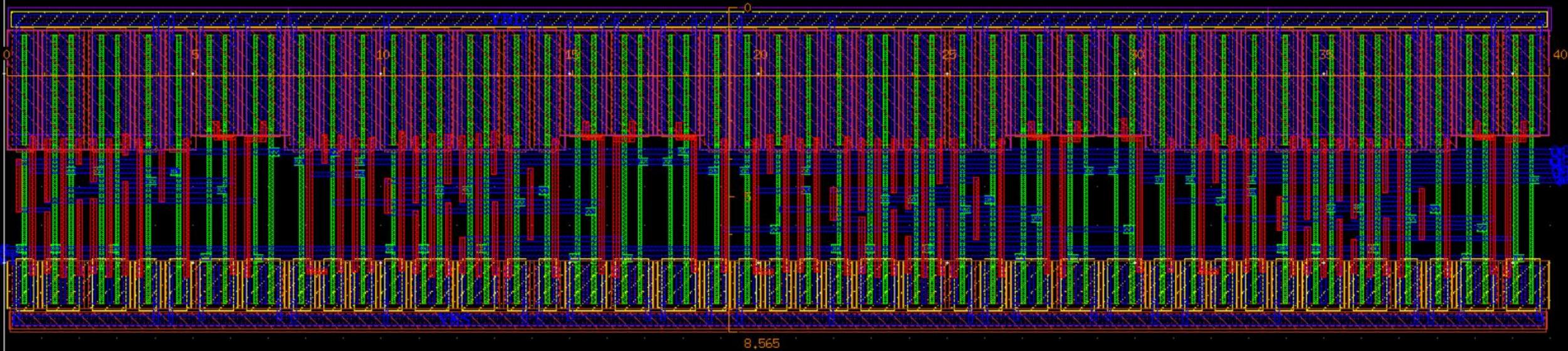
# 4BIT SYNC UP COUNTER – Schematics



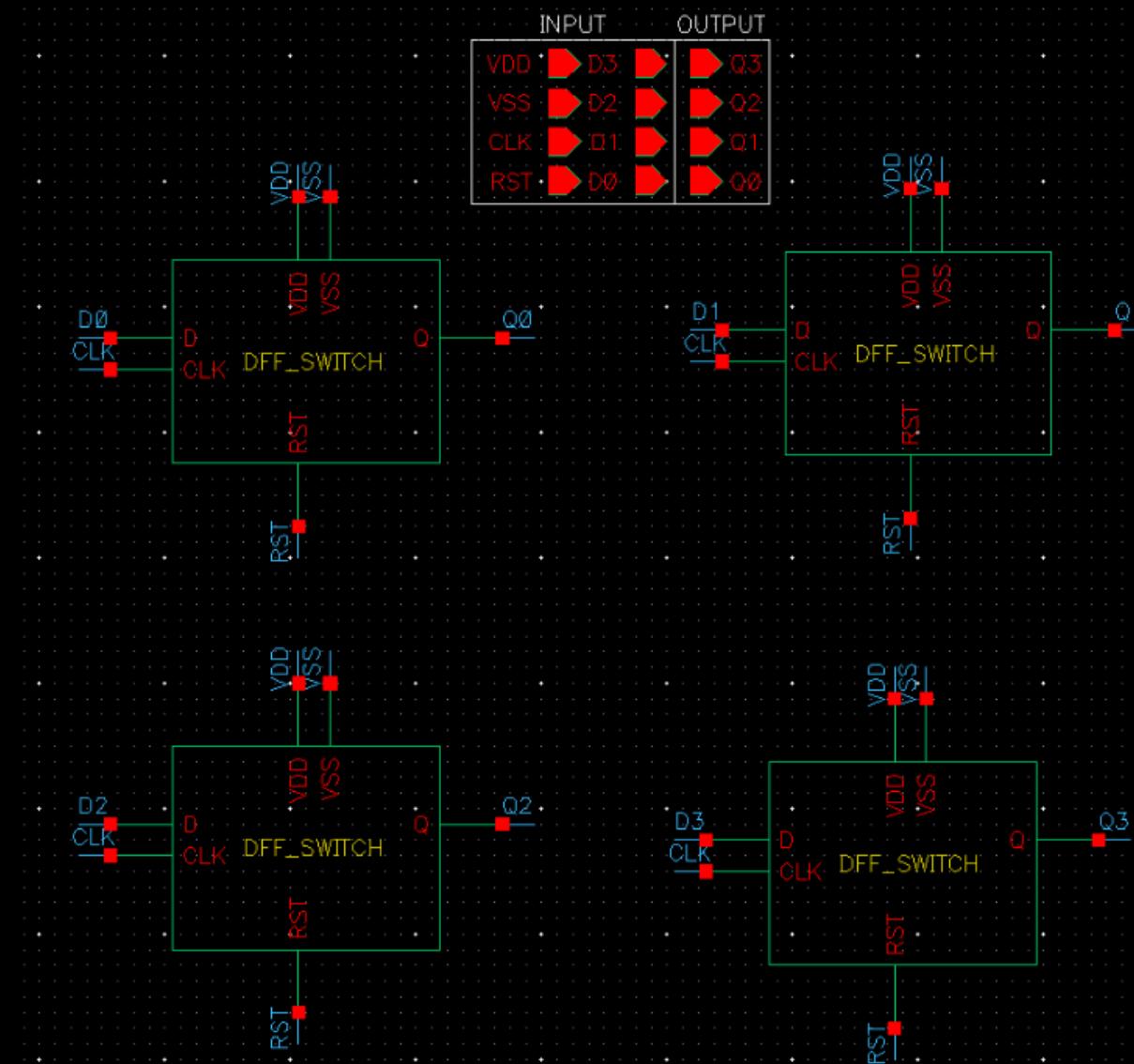
# 4BIT SYNC UP COUNTER – Simulation



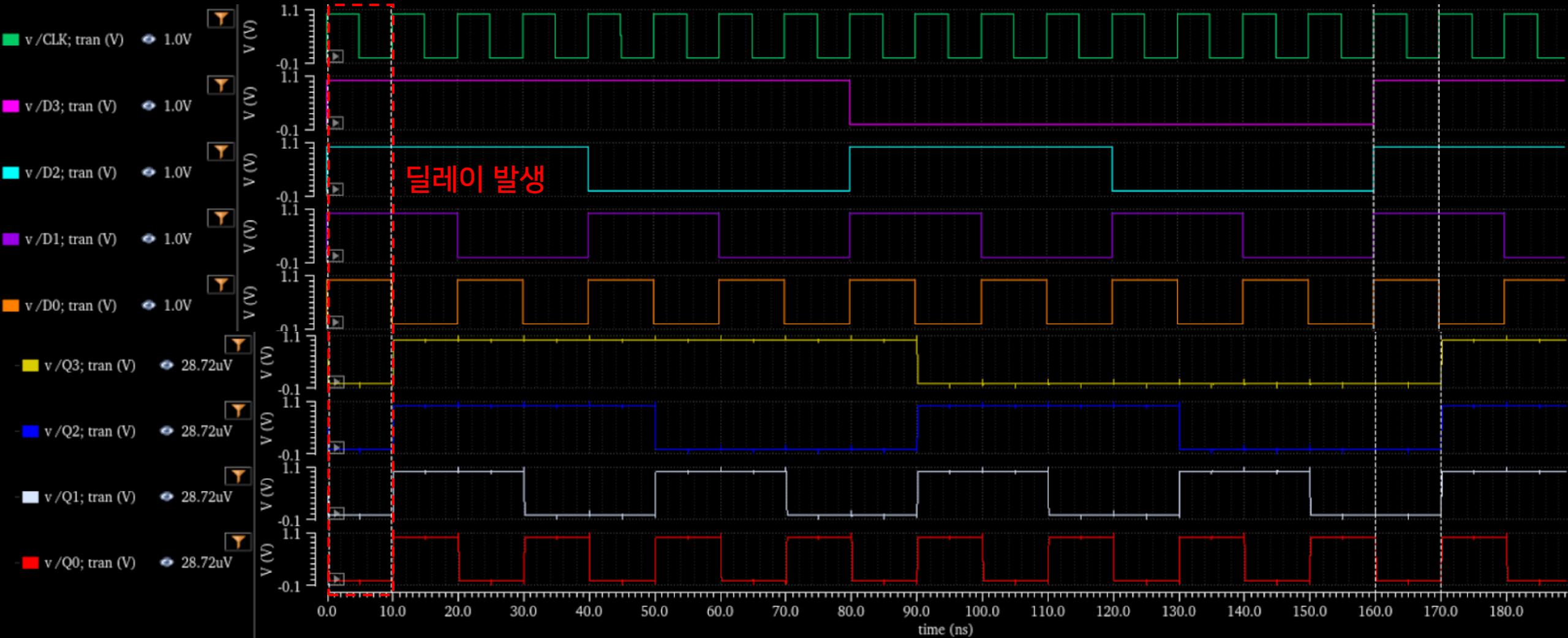
# 4BIT SYNC UP COUNTER – Layout



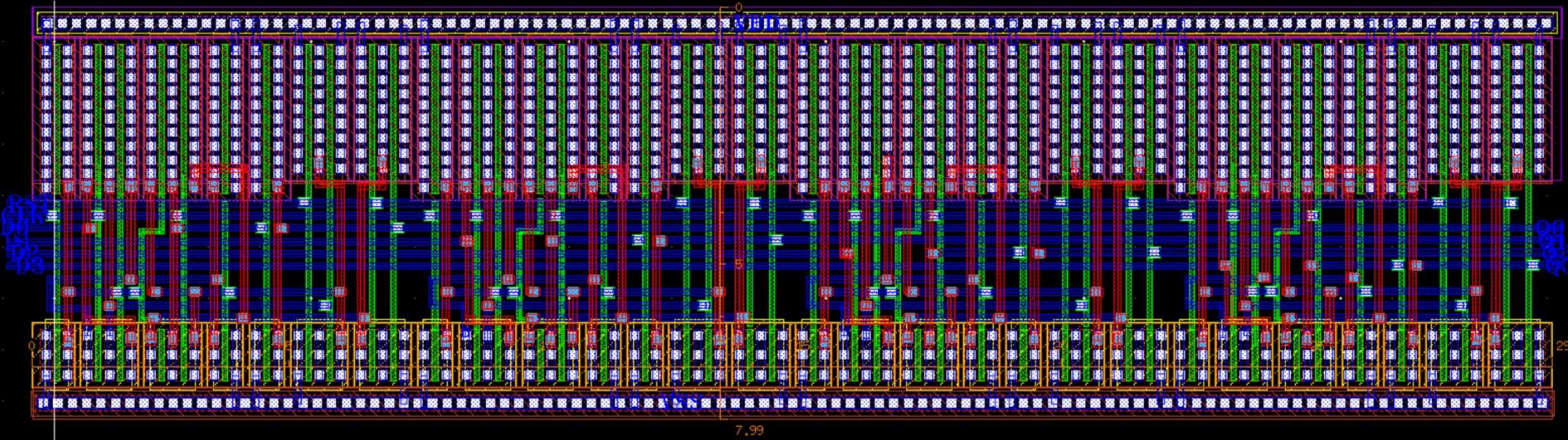
# 4BIT SHIFT REGISTER – Schematics



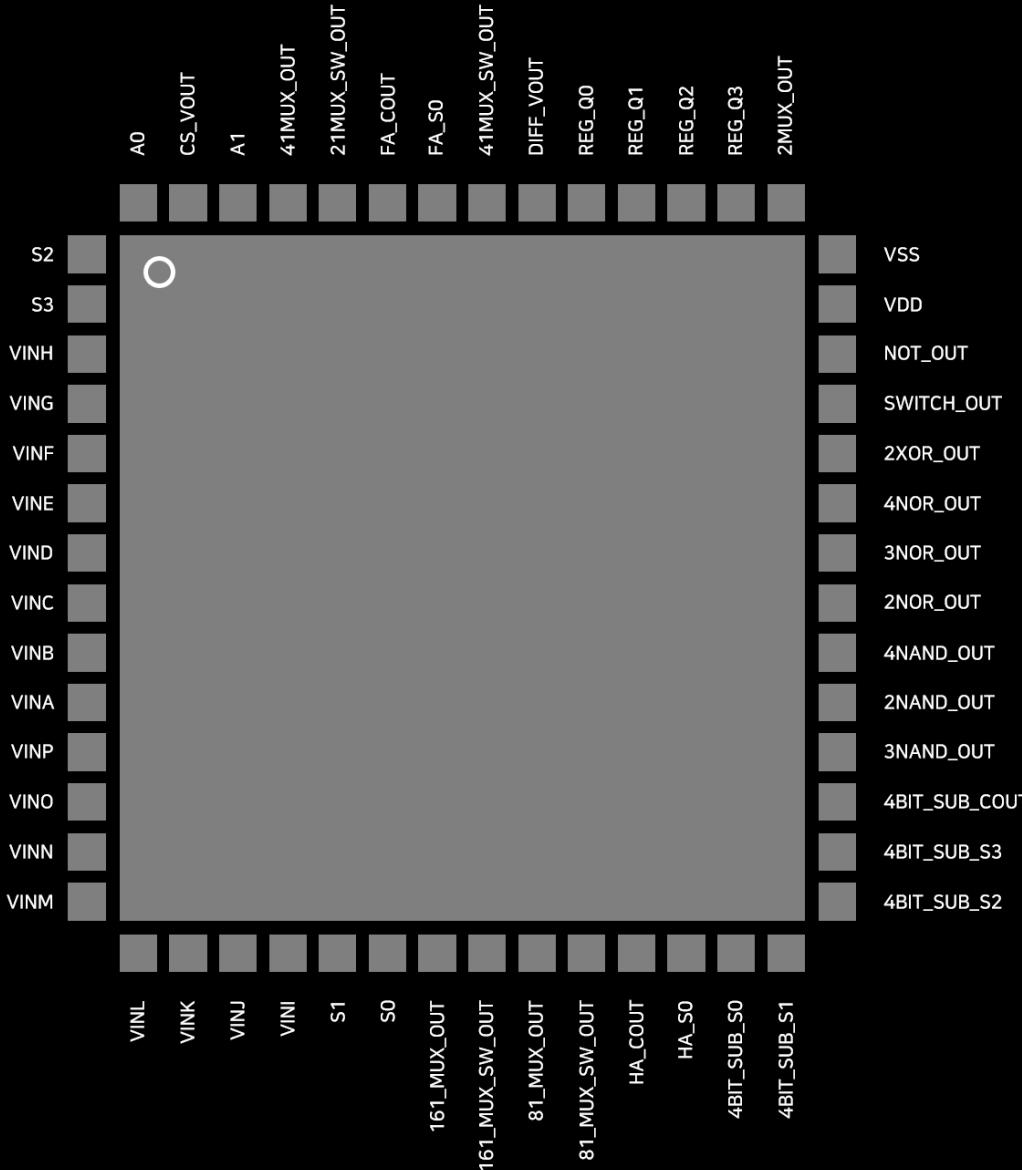
# 4BIT SHIFT REGISTER – Simulation



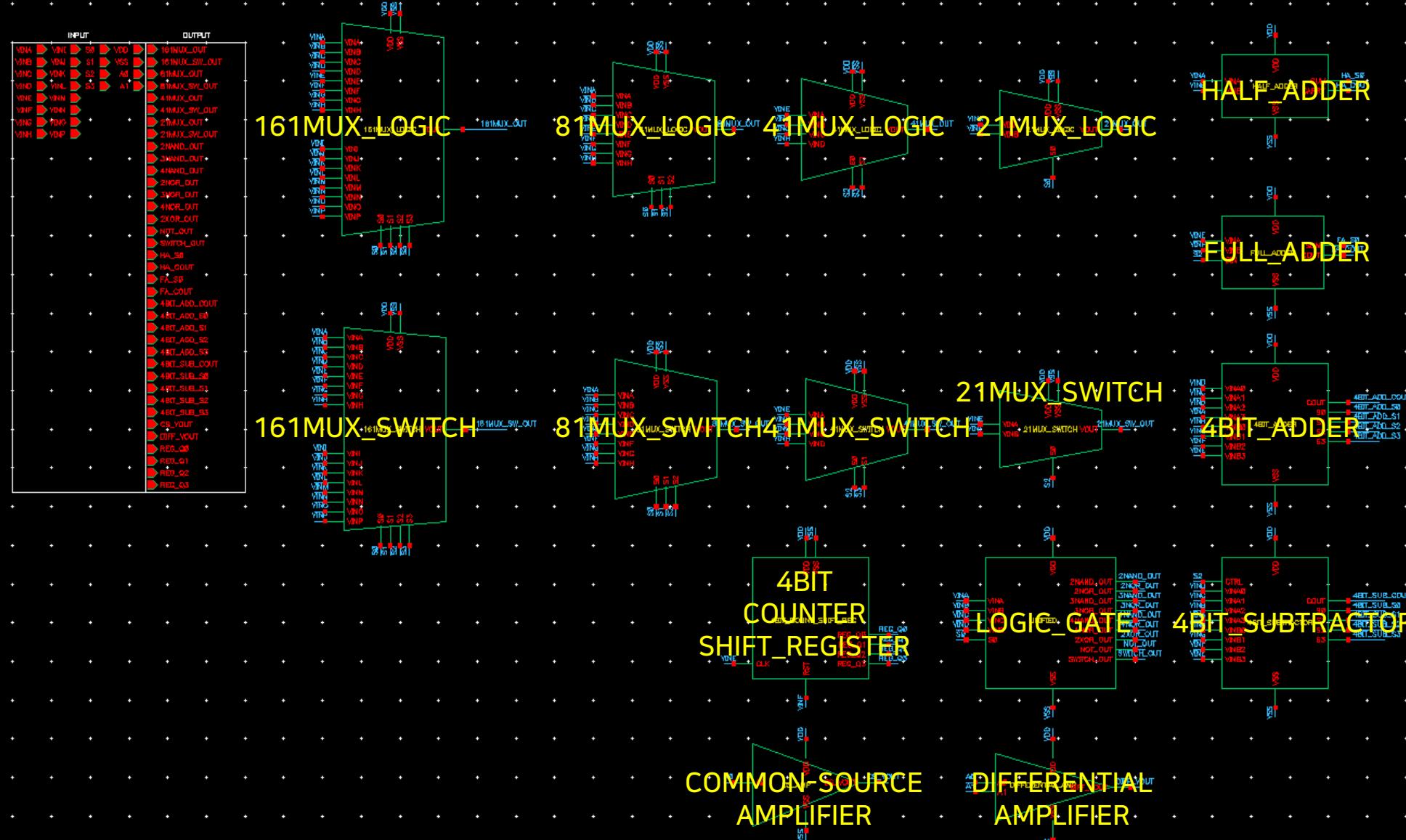
# 4BIT SHIFT REGISTER – Layout



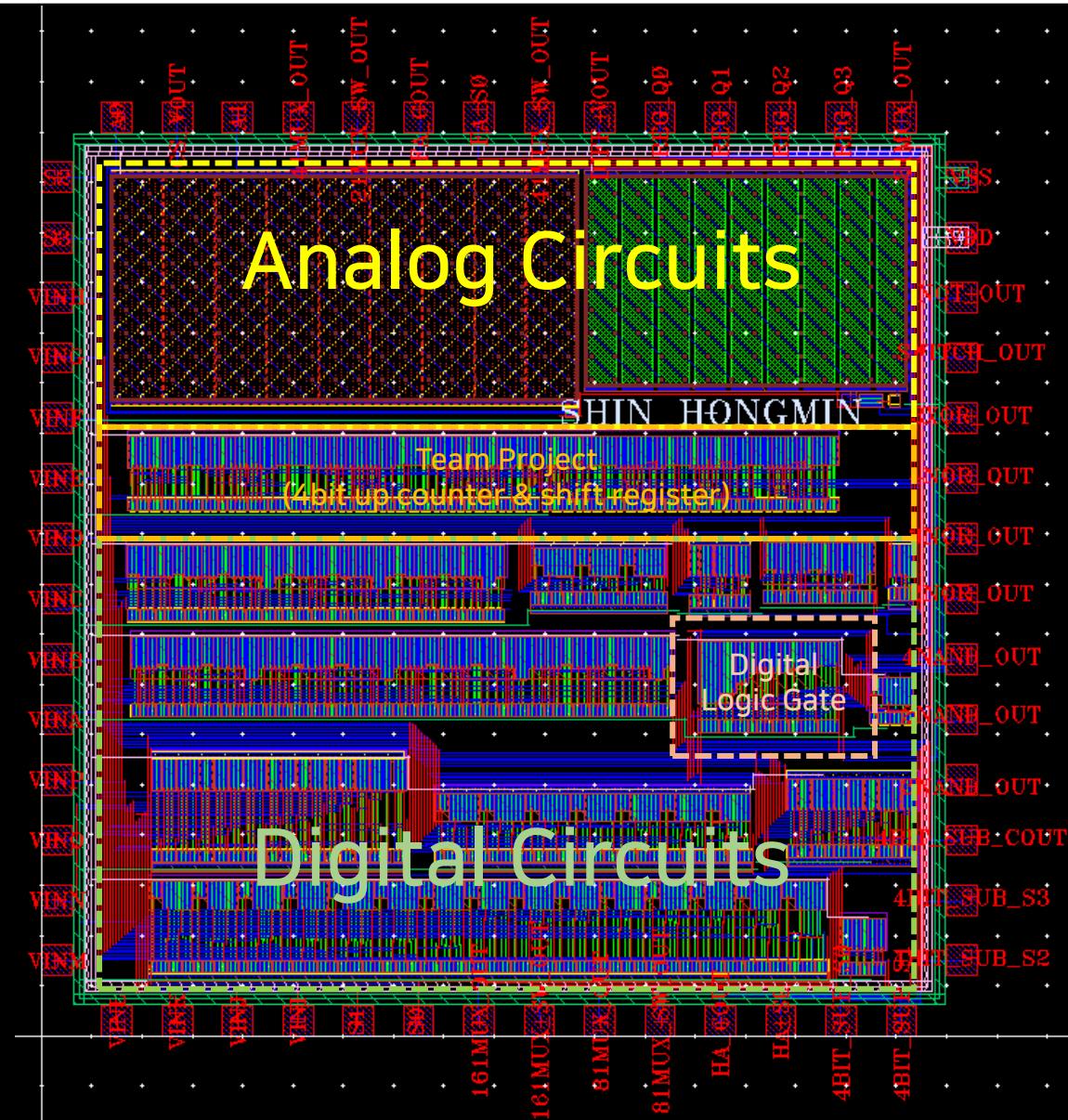
# One-Chip Design – Pin Array



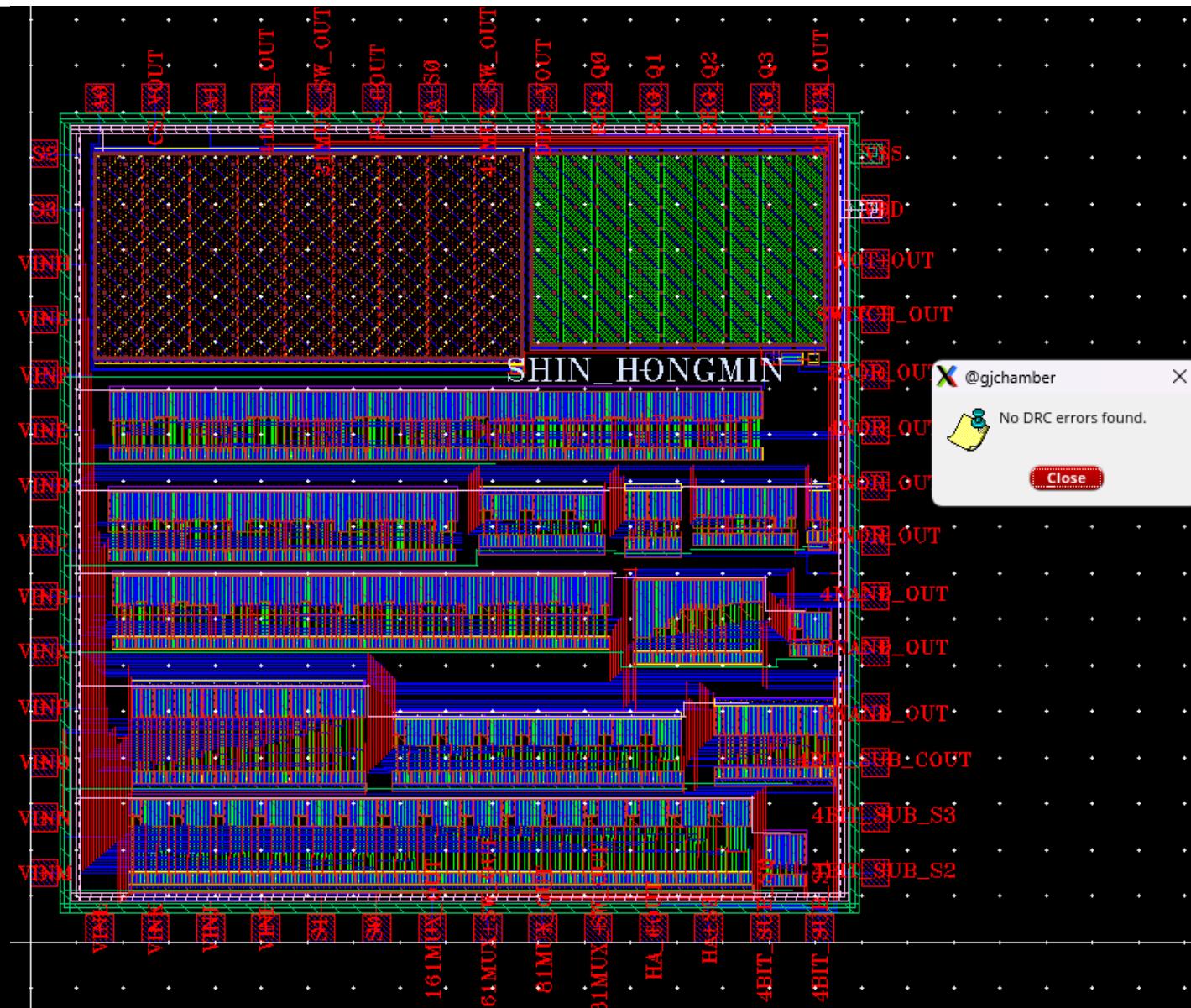
# One-Chip Design - Schematics



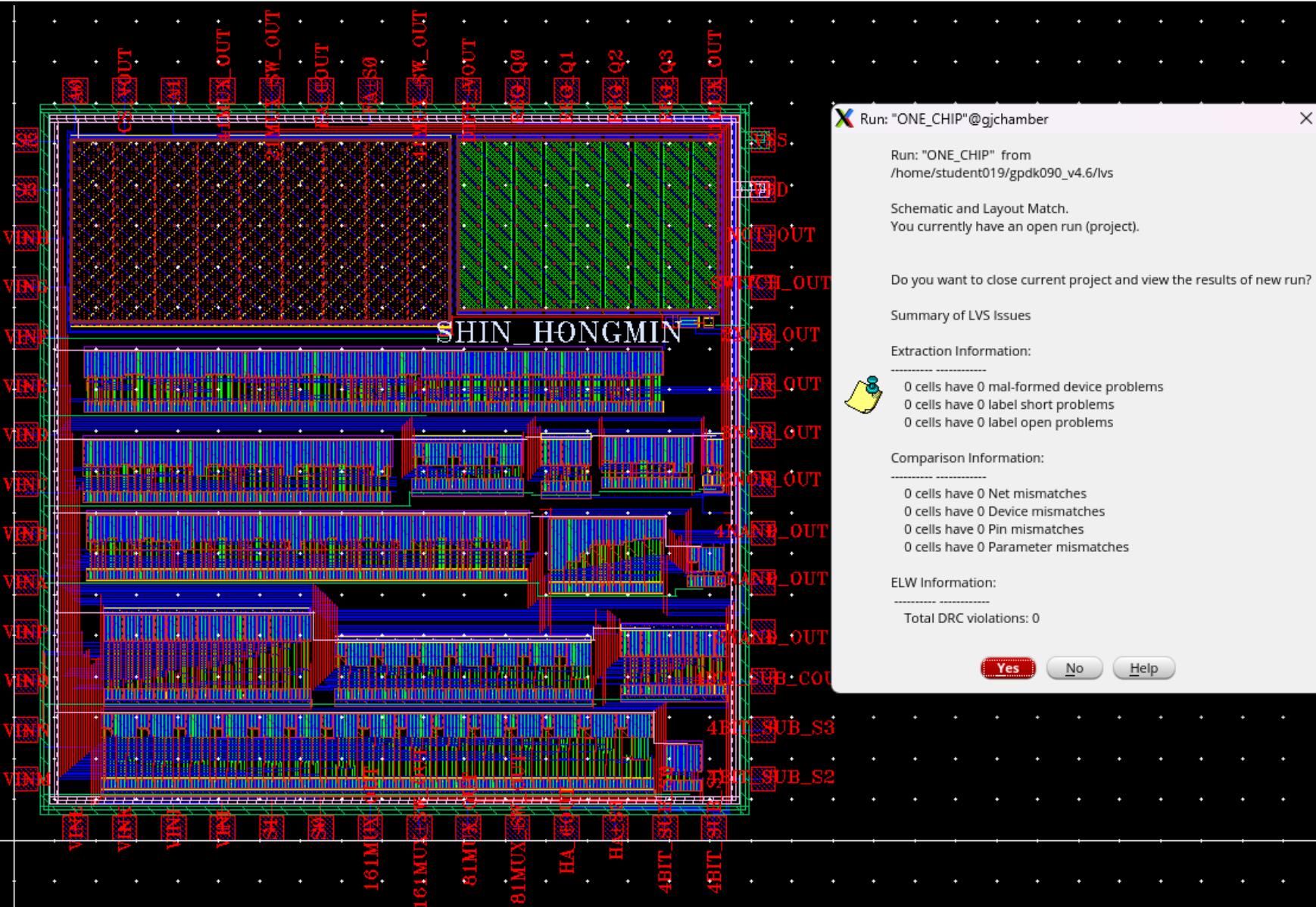
# One-Chip Design - Layout



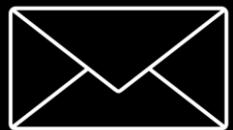
# One-Chip Design - Layout(DRC)



# One-Chip Design - Layout(LVS)



# CONTACT



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