

Cadence Full-Custom IC Design

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Introduction

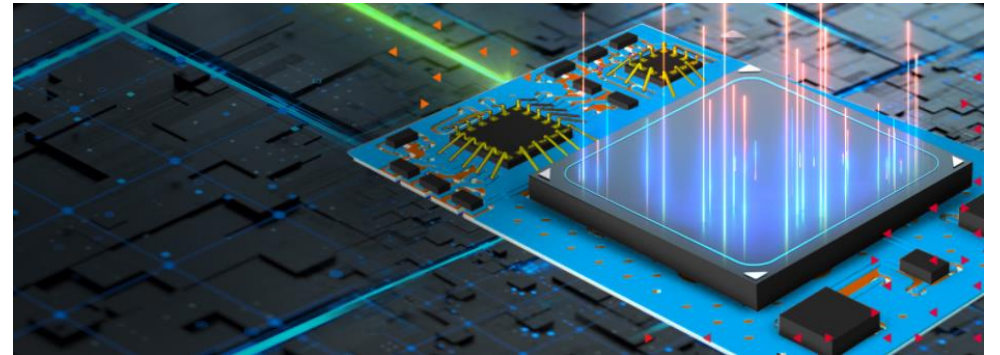
"Course

Cadence® Full-Custom IC Designer



"Tools

Cadence Virtuoso Schematic Editor / Layout Editor
Cadence Virtuoso Spectre / ADE
Assura DRC / LVS
GPDK090



Logic Gate

01

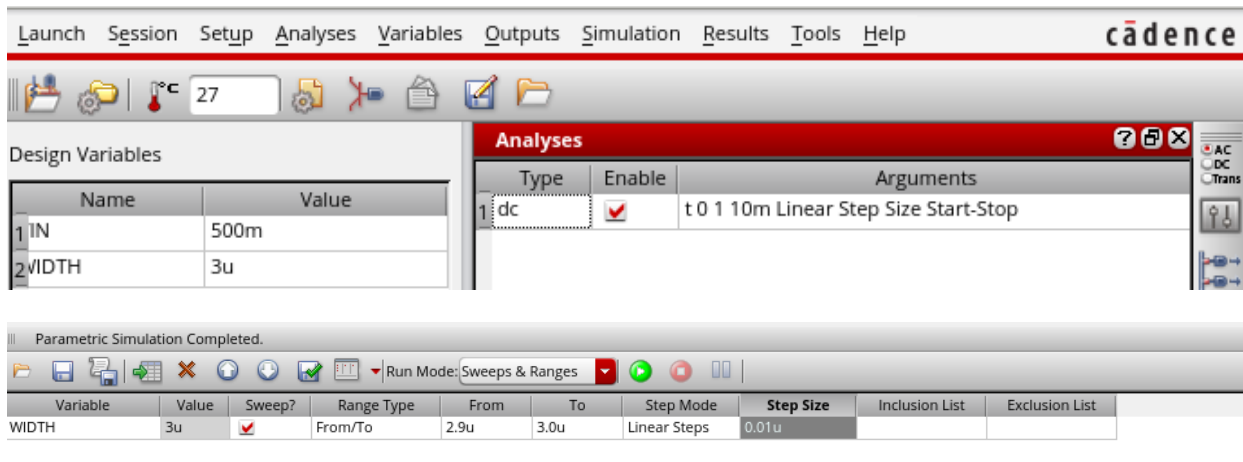
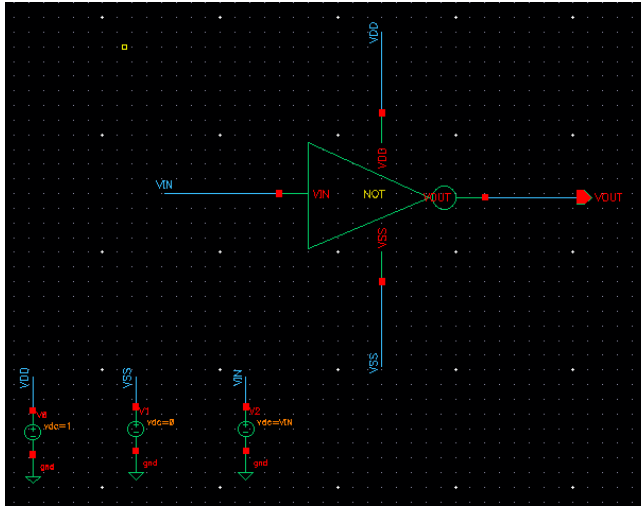
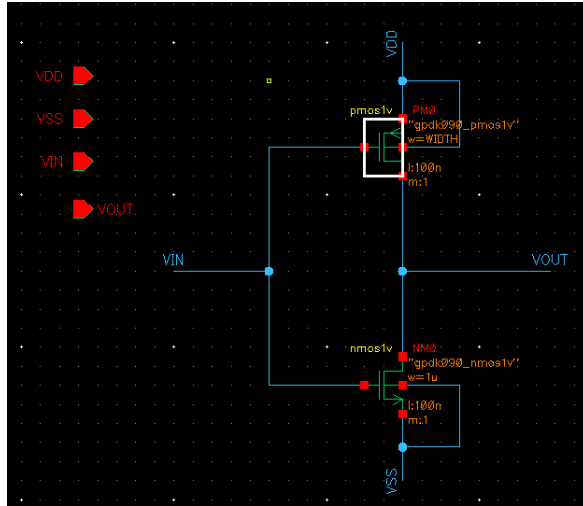
Logic Gate

02

03

04

05



[NOT Gate]

Find to PMOS width

01
SchematicNMOS => 1um
PMOS => WIDTH02
TEST SchematicVDD = 1V
VSS = 0V
VIN = VIN03
DC Analysis0V – 1V
Linear Step (0.01V)04
WIDTH Analysis

Reduce Step Size

01

Logic Gate

02

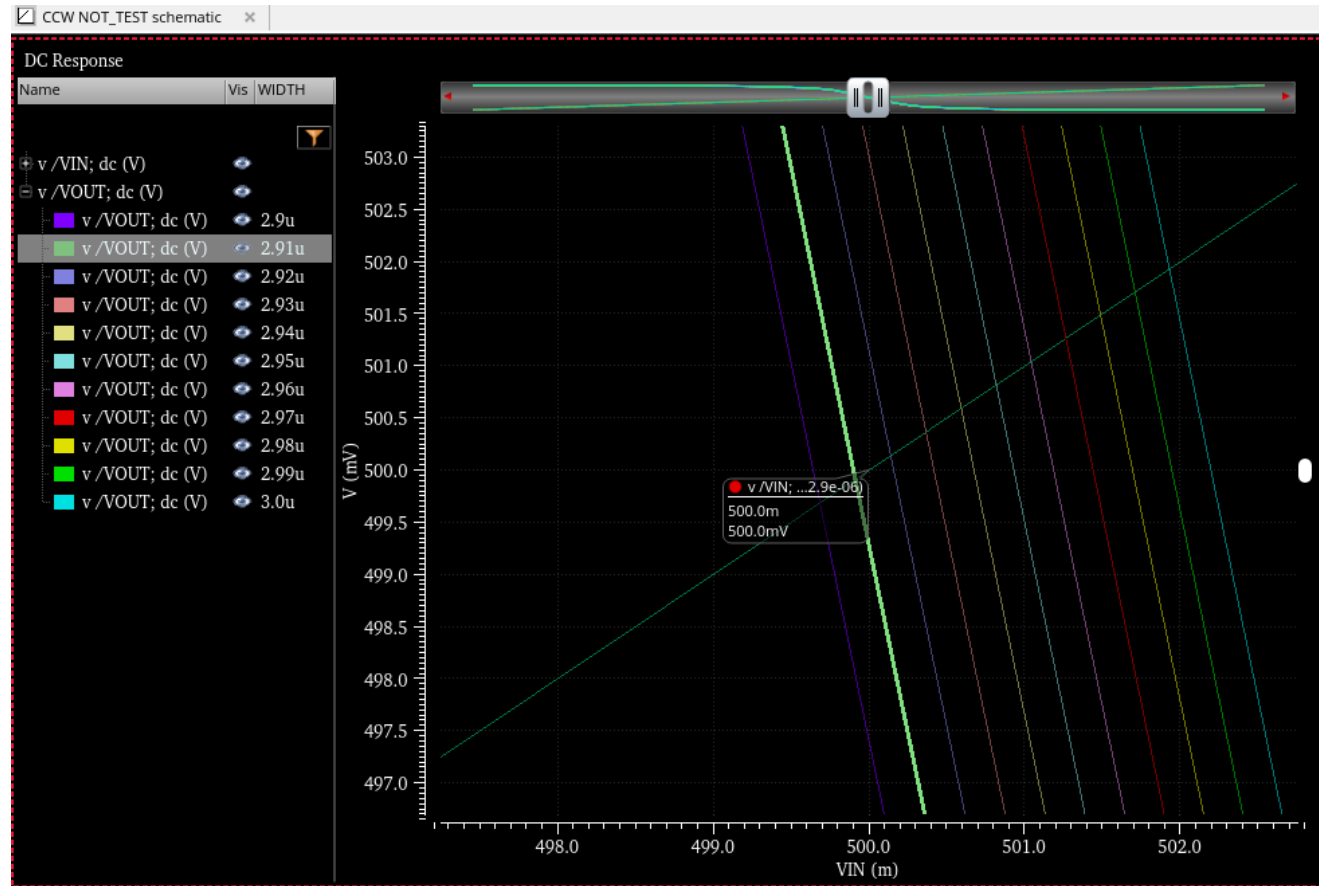
03

04

05

[NOT Gate]

Find to PMOS width

Simulation Result

PMOS WIDTH = 2.91um

01

Logic Gate

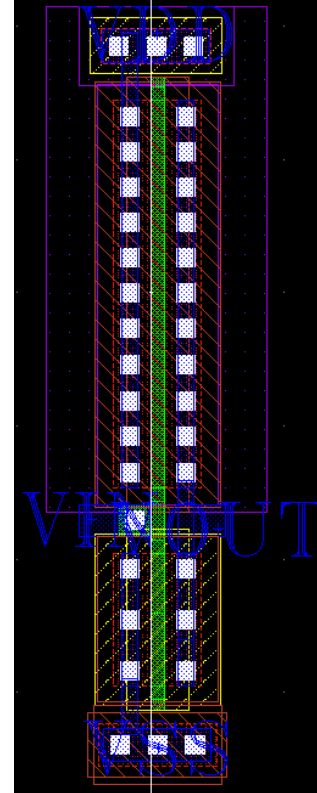
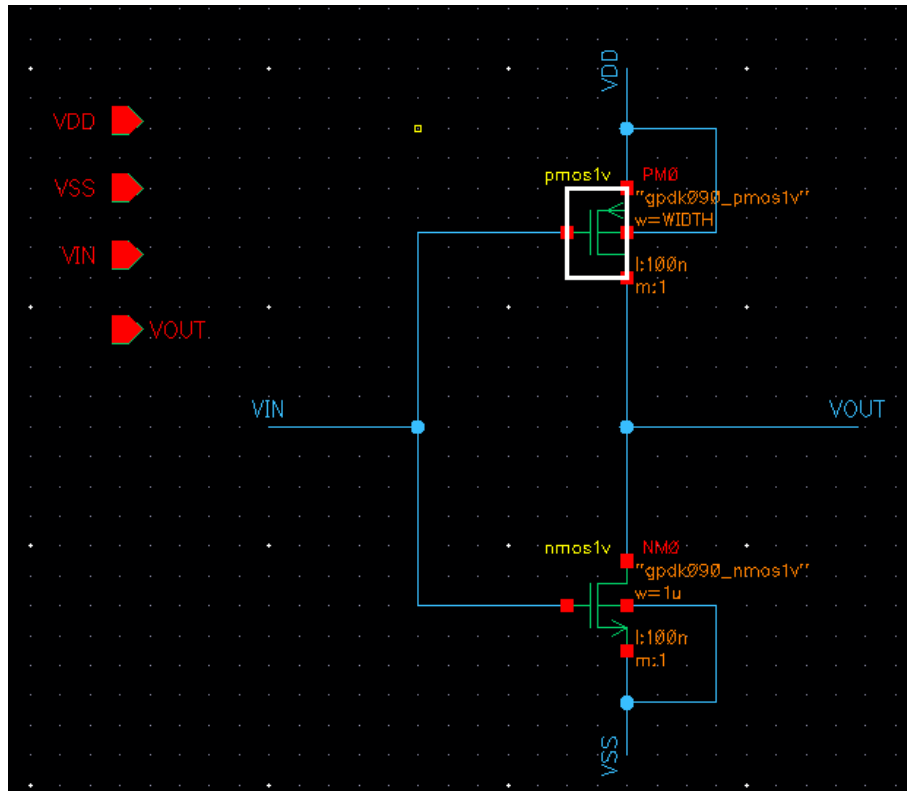
02

03

04

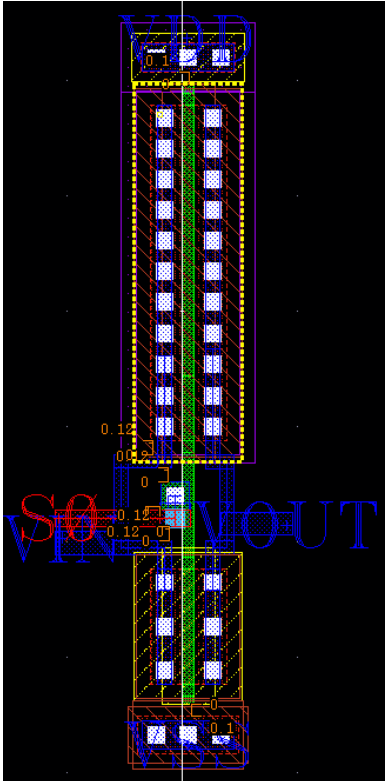
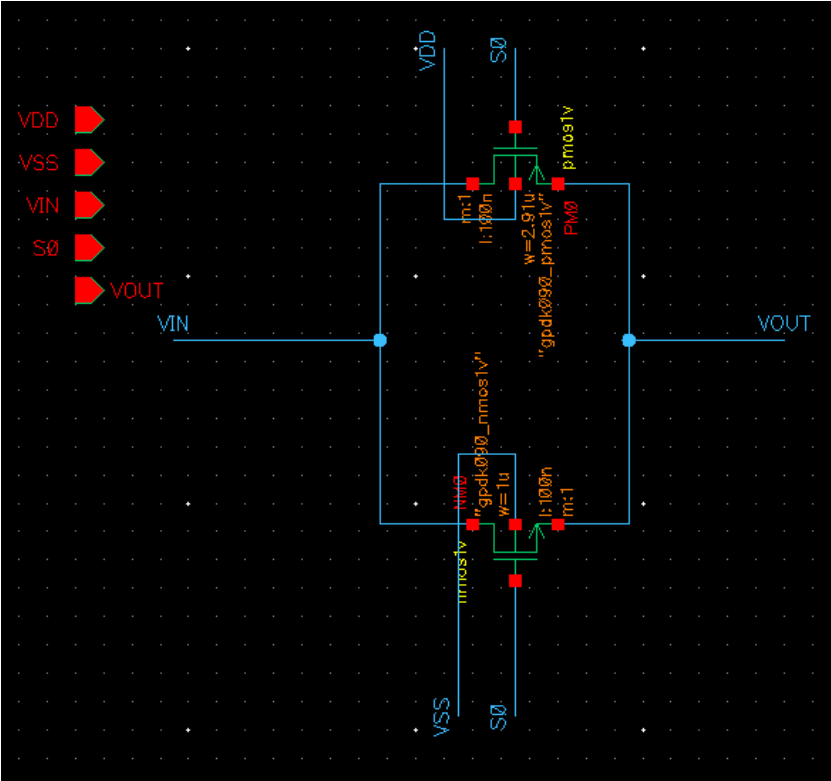
05

NOT GATE



PMOS WIDTH = 2.91um

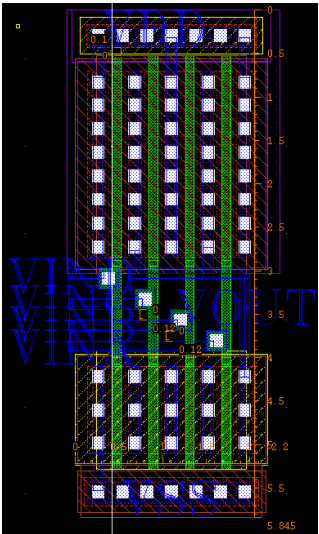
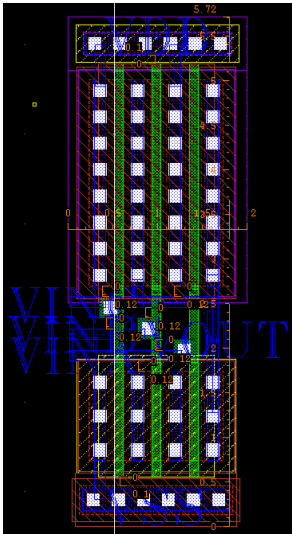
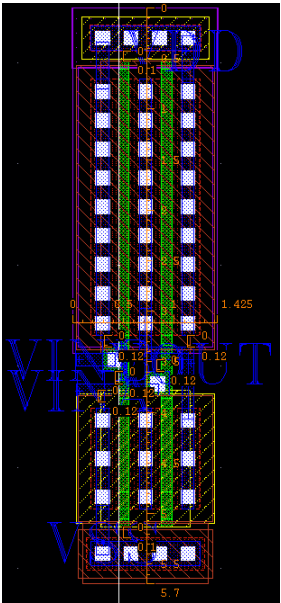
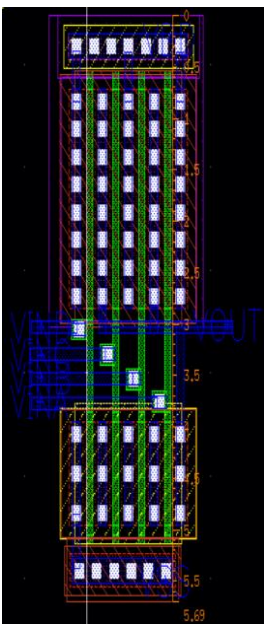
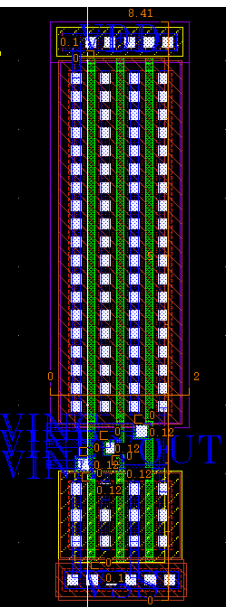
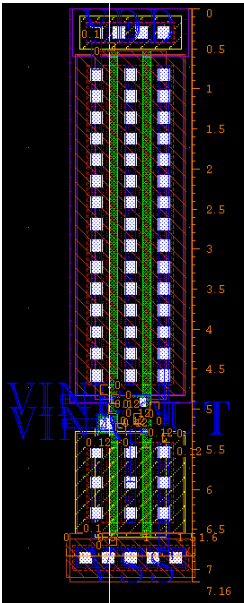
SWITCH



PMOS WIDTH = 2.91um

NAND / NOR Gate

	2NOR	3NOR	4NOR	2NAND	3NAND	4NAND
NMOS	1um	1um	1um	1um	1um	1um
PMOS	3.99um	5um	5.96um	2.53um	2.31um	2.14um



Multiplexer (MUX)

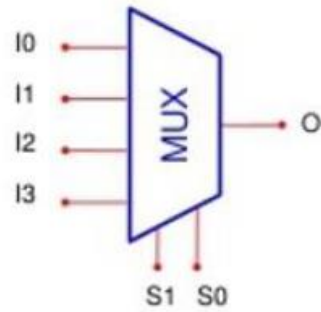
01

02

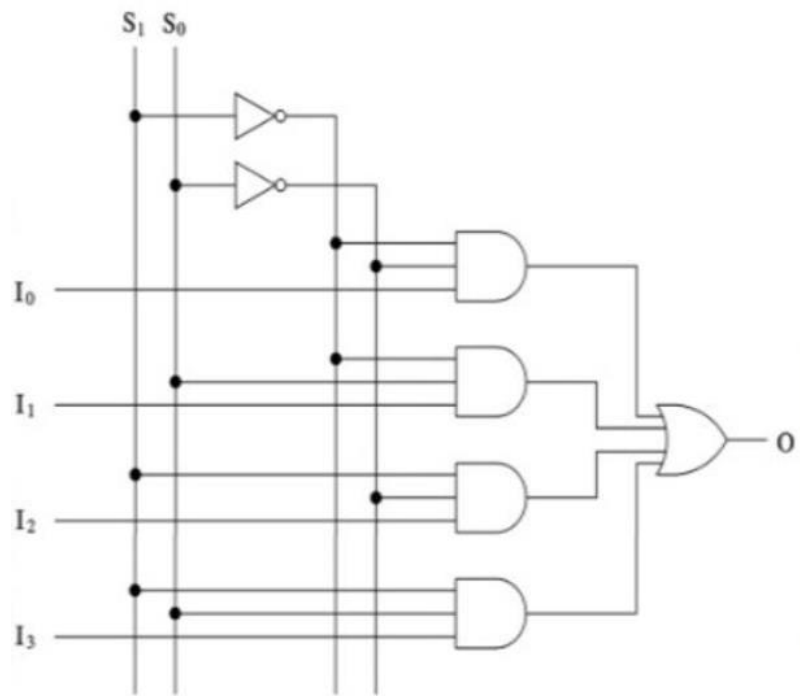
03

04

05



Multiplexer (MUX)



$$\bullet \text{ Out} = \overline{S_1}\overline{S_0}A + \overline{S_1}S_0B + S_1\overline{S_0}C + S_1S_0D$$

MUX Truth Table

S1	S0	OUT
0	0	A
0	1	B
1	0	C
1	1	D

01

Multiplexer (MUX)

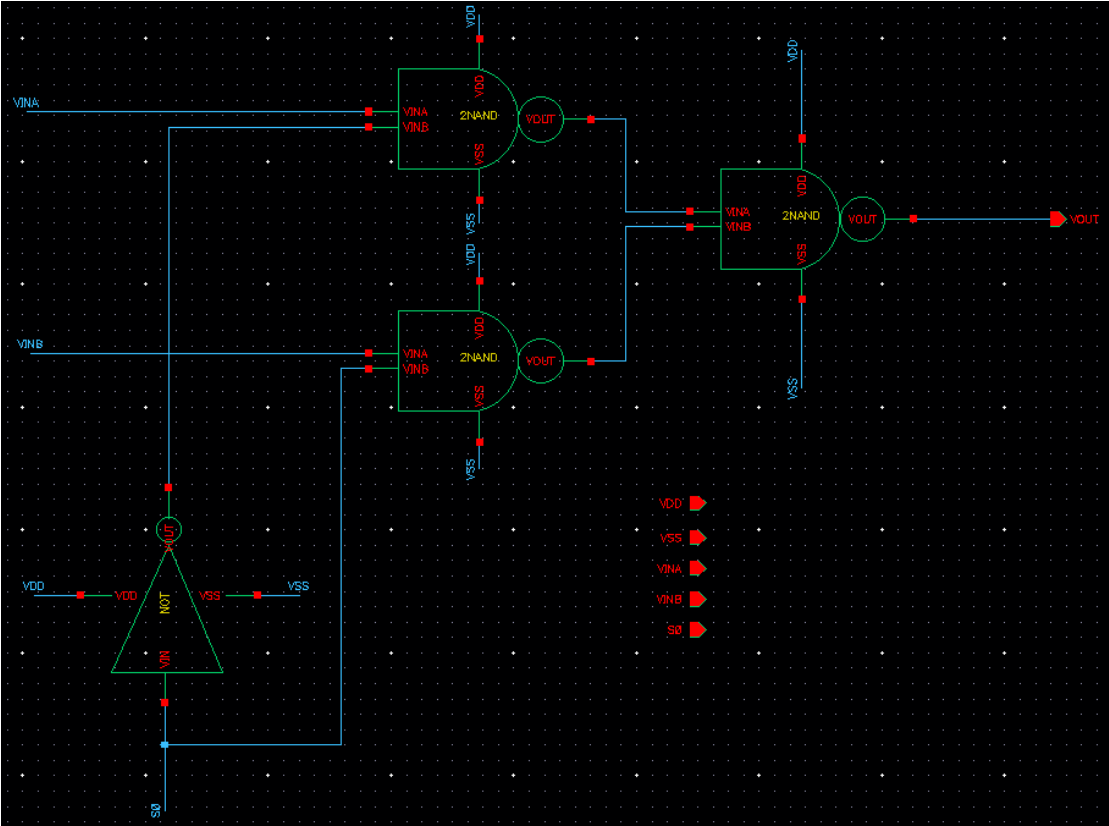
02

03

04

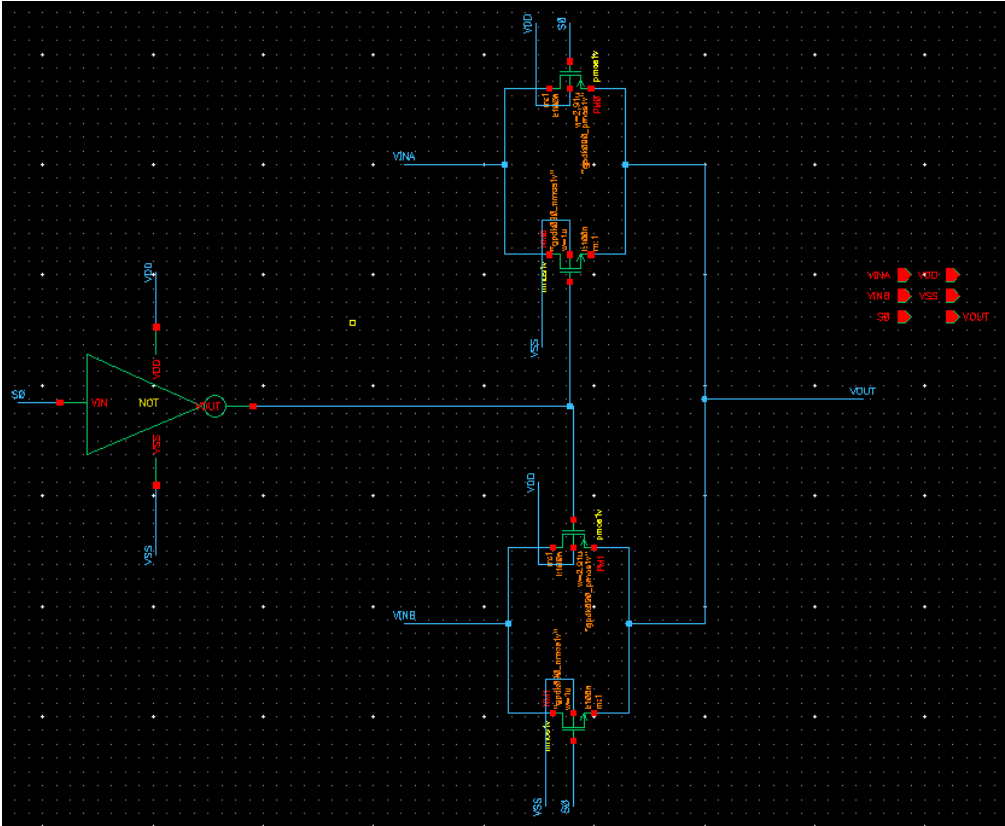
05

Logic Gate



[2x1]
Logic Gate vs Switch

Switch



01

Multiplexer (MUX)

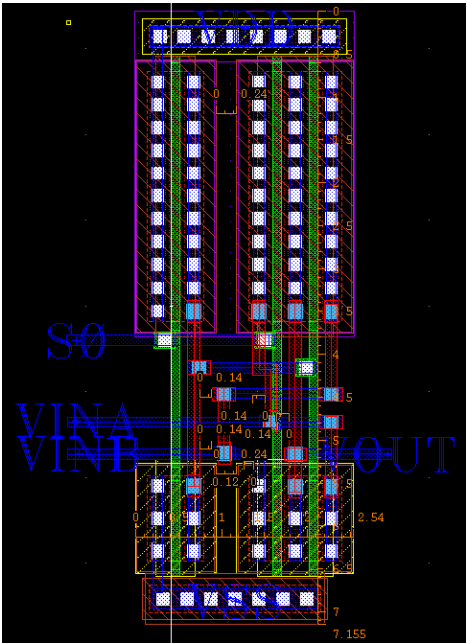
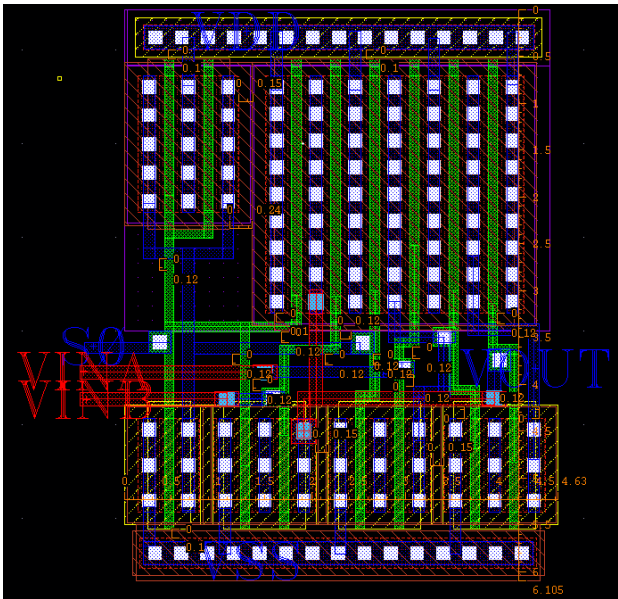
02

03

04

05

[2x1]
Logic Gate vs Switch



	Logic Gate	Switch
Length	6.305um	7.155um
Width	4.63um	2.54um
Transistor	14	6

01

Multiplexer (MUX)

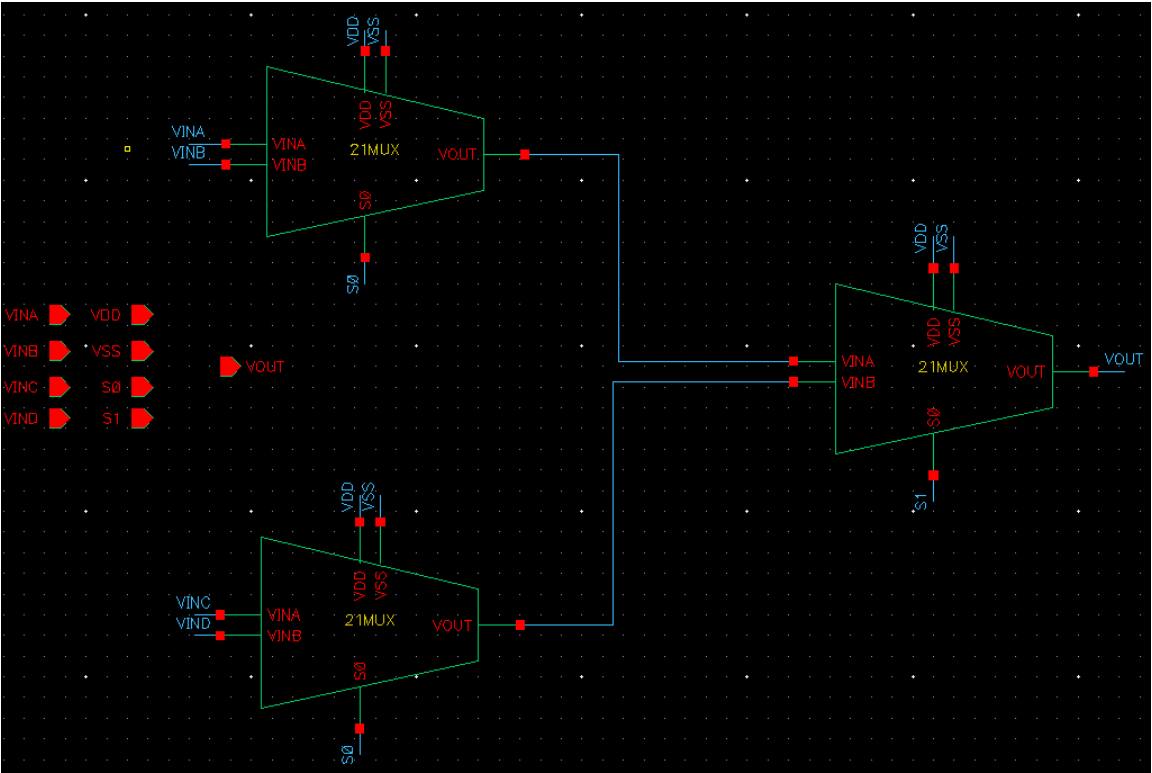
02

03

04

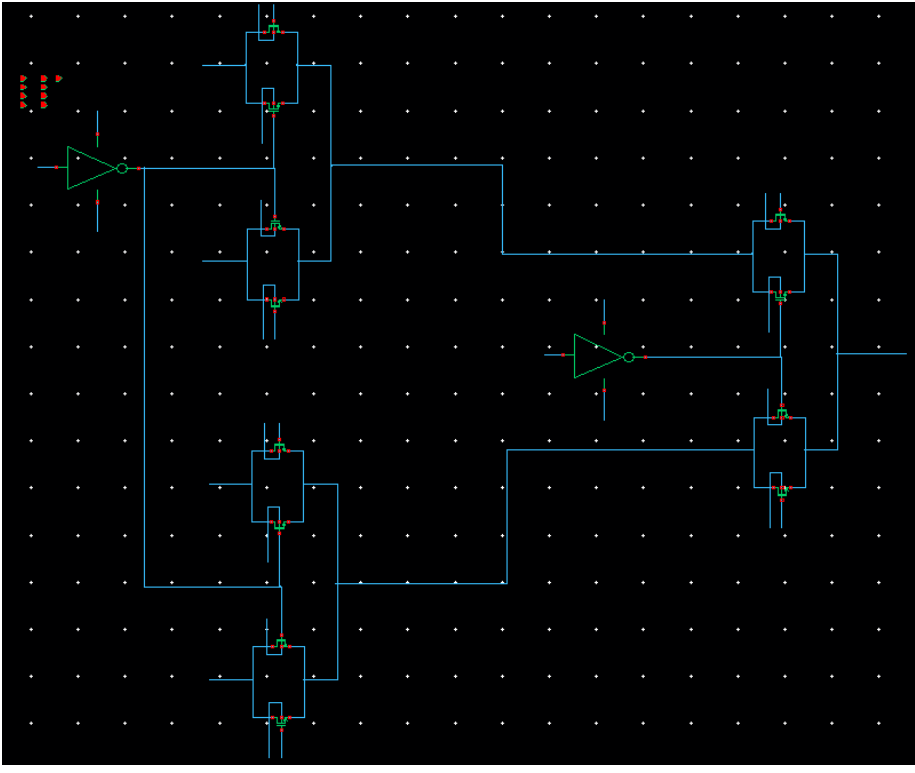
05

Logic Gate



[4x1]
Logic Gate vs Switch

Switch



Multiplexer (MUX)

[4x1] Simulation

The screenshot displays a SPICE transient simulation for a 4-to-1 multiplexer. The simulation window shows the output voltage (V) over time (0 to 0.55 ns). The input signals are labeled A, B, C, and D. The output signal is labeled OUT. The simulation results show that the output follows the input signal A for the first half of the simulation and then follows the input signal B for the second half.

The screenshot displays a SPICE transient response simulation for a 4-to-1 multiplexer. The plot shows the output voltage 'v / OUT; tran (V)' over time, with four distinct regions labeled A, B, C, and D. Region A shows a high-level signal, B shows a low-level signal, C shows a high-frequency oscillation, and D shows a low-level signal. The input signals S0 and S1 are also shown as square waves, and the control signals v / INC; tran (V) and v / INI; tran (V) are shown as high-frequency and low-frequency signals respectively.

The screenshot displays a SPICE transient response simulation for a 4-to-1 multiplexer. The plot shows the output voltage 'v / OUT; tran (V)' over time, with four distinct regions labeled A, B, C, and D. Region A shows a high-level signal, B shows a low-level signal, C shows a high-frequency oscillation, and D shows a low-level signal. The input signals S0 and S1 are also shown as square waves, and the control signals v / INC; tran (V) and v / INI; tran (V) are shown as high-frequency and low-frequency signals respectively.

01

Multiplexer (MUX)

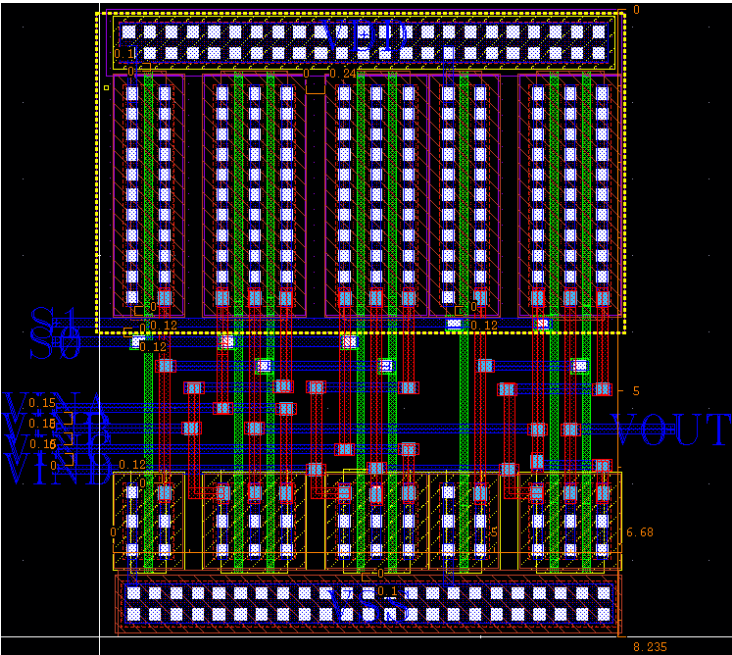
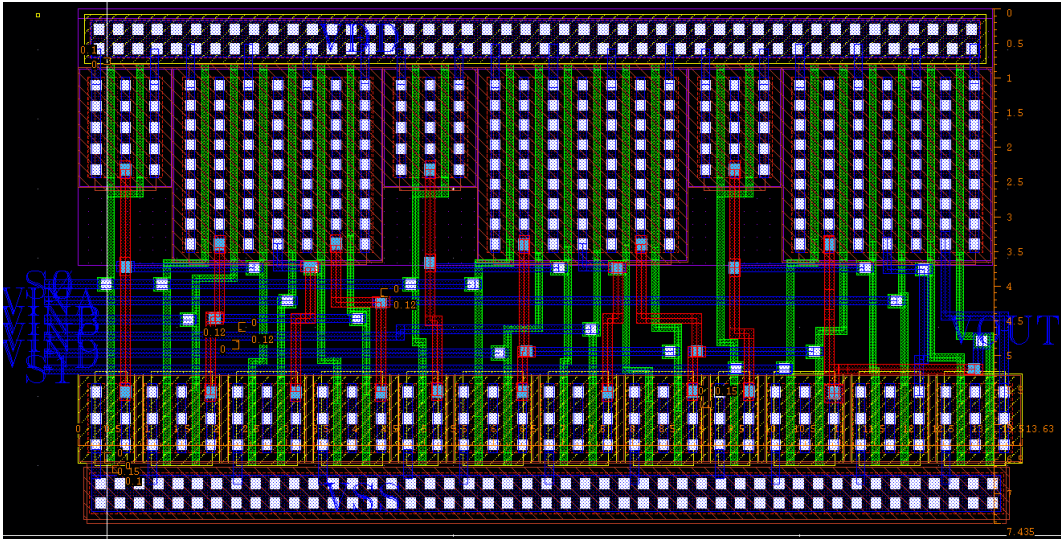
02

03

04

05

[4x1]
Logic Gate vs Switch



	Logic Gate	Switch
Length	7.435um	8.235um
Width	13.63um	6.60um
Transistor	42	16

Adder

01

02

03

04

05

Half_Adder

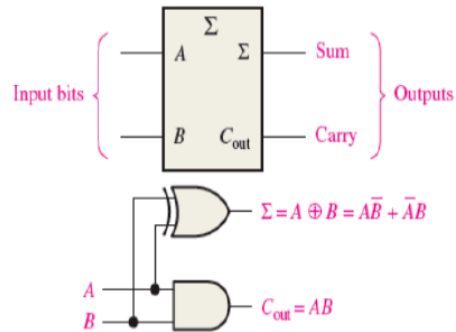
Half-adder truth table.

A	B	C _{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Σ = sum

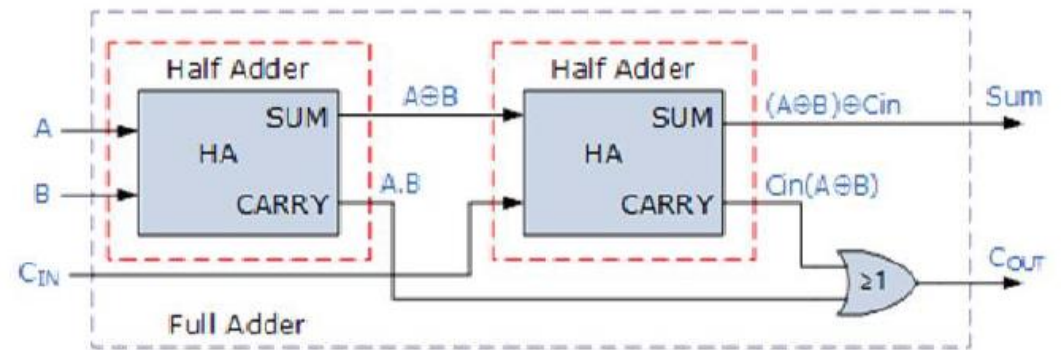
C_{out} = output carry

A and B = input variables (operands)



Adder

FULL_ADDER



4Bit Adder

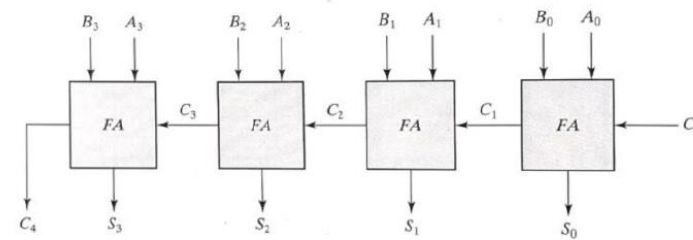
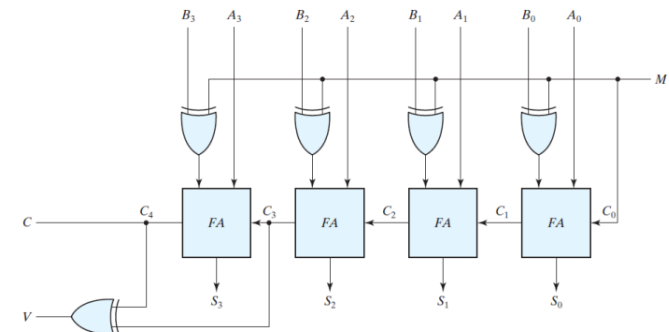


FIGURE 4.9
Four-bit adder.

4BIT Adder-Subtractor



01

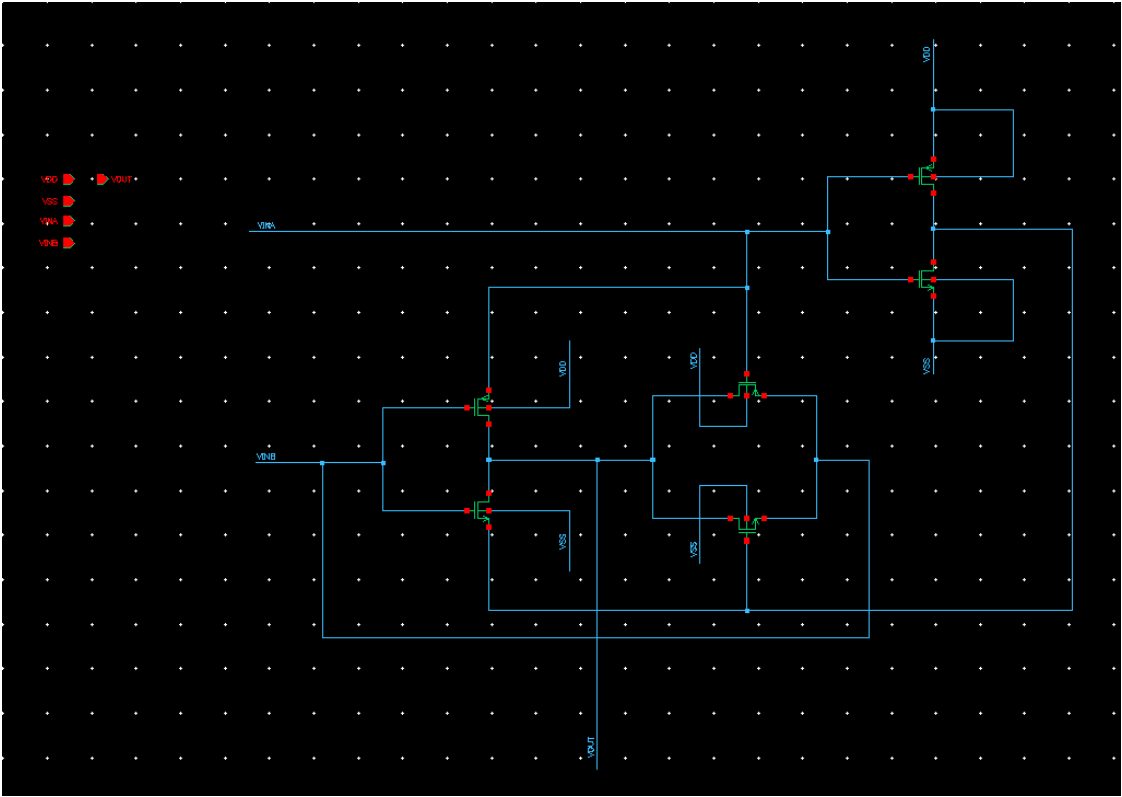
Adder

02

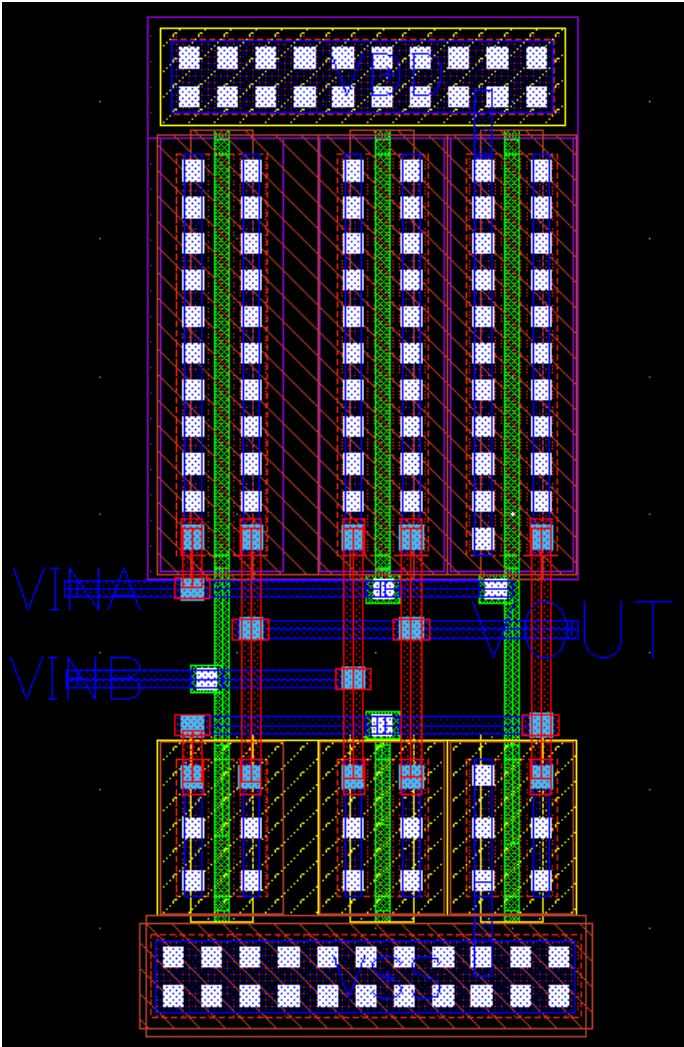
03

04

05



XOR Gate



01

Adder

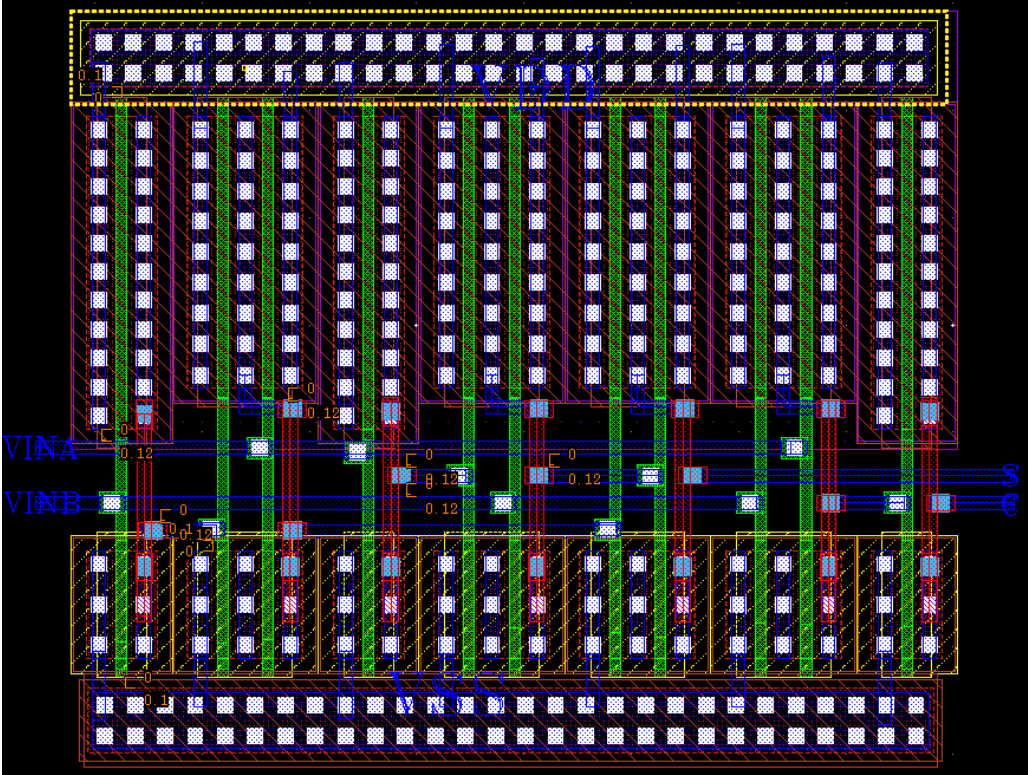
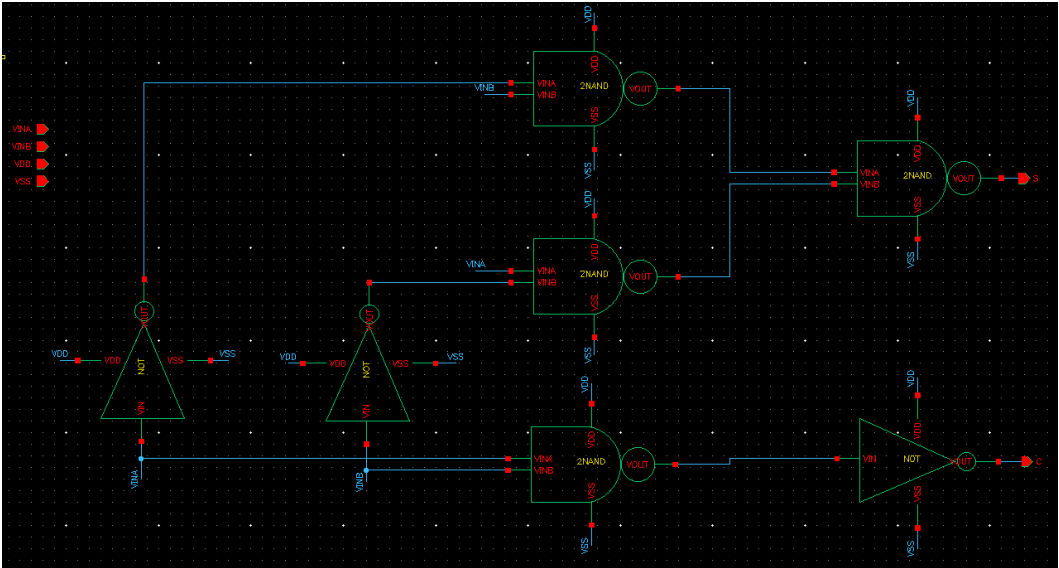
02

03

04

05

Half Adder 1



01

Adder

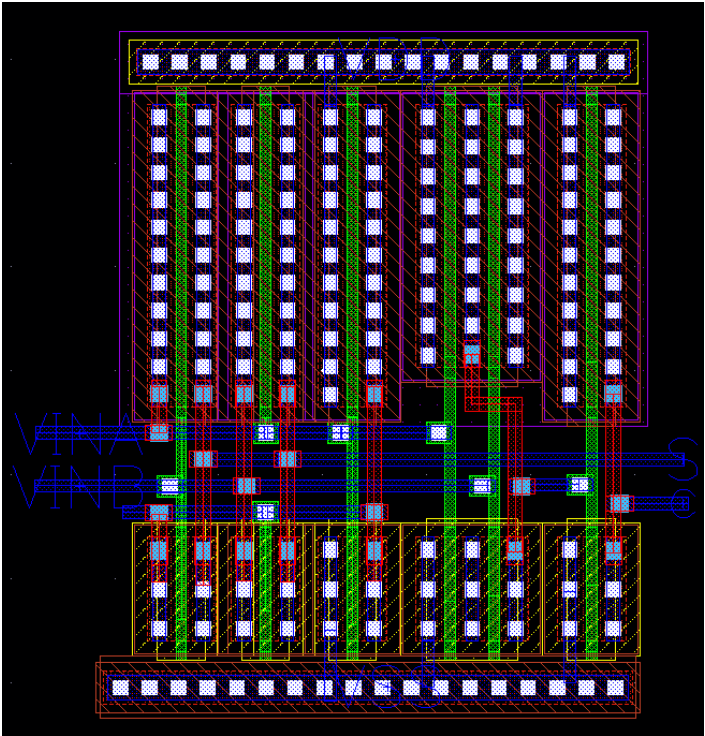
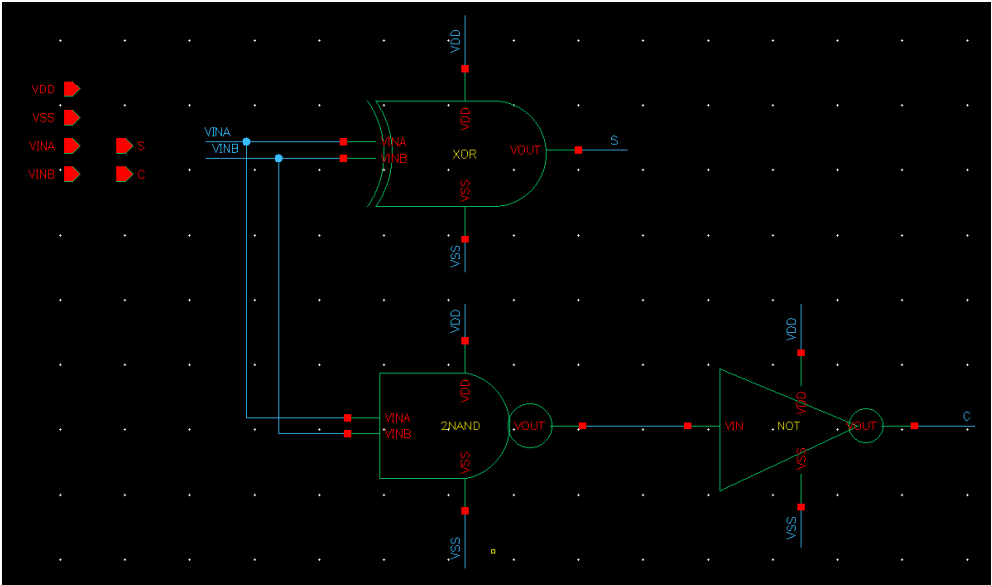
02

03

04

05

Half Adder 2



01

Adder

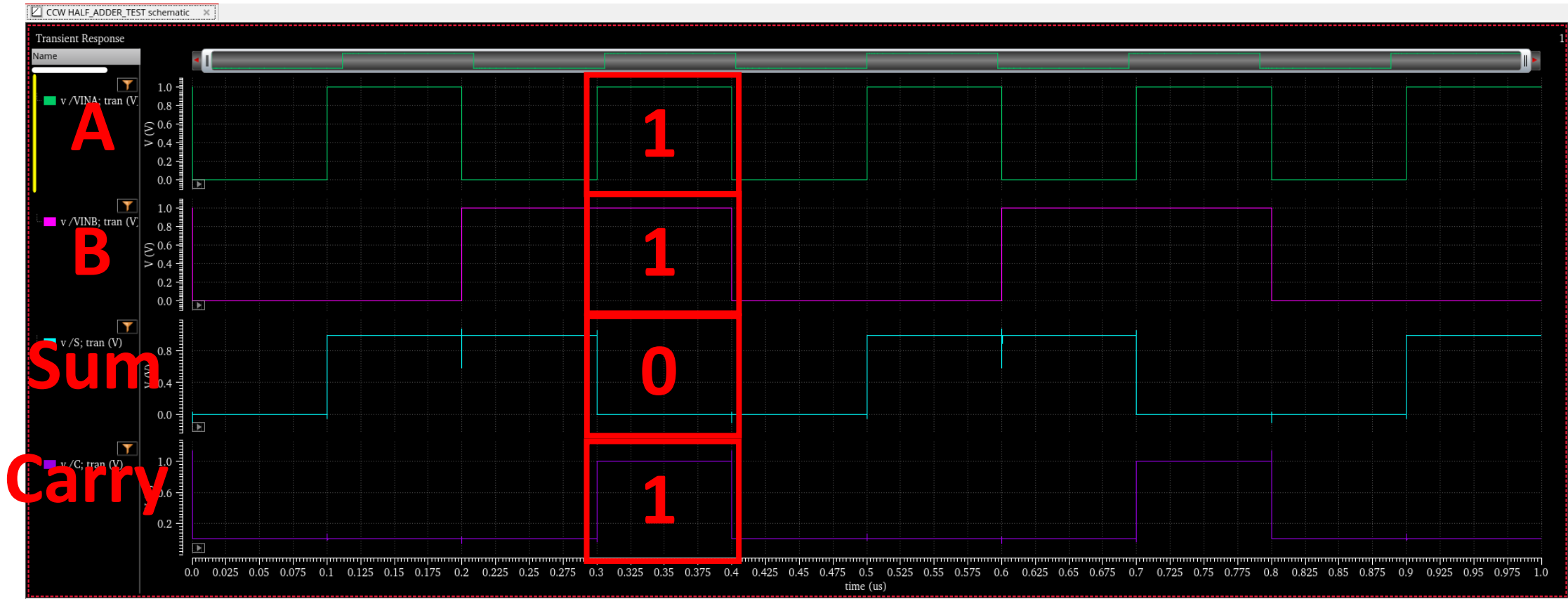
02

03

04

05

[Half Adder]
Simulation



01

Adder

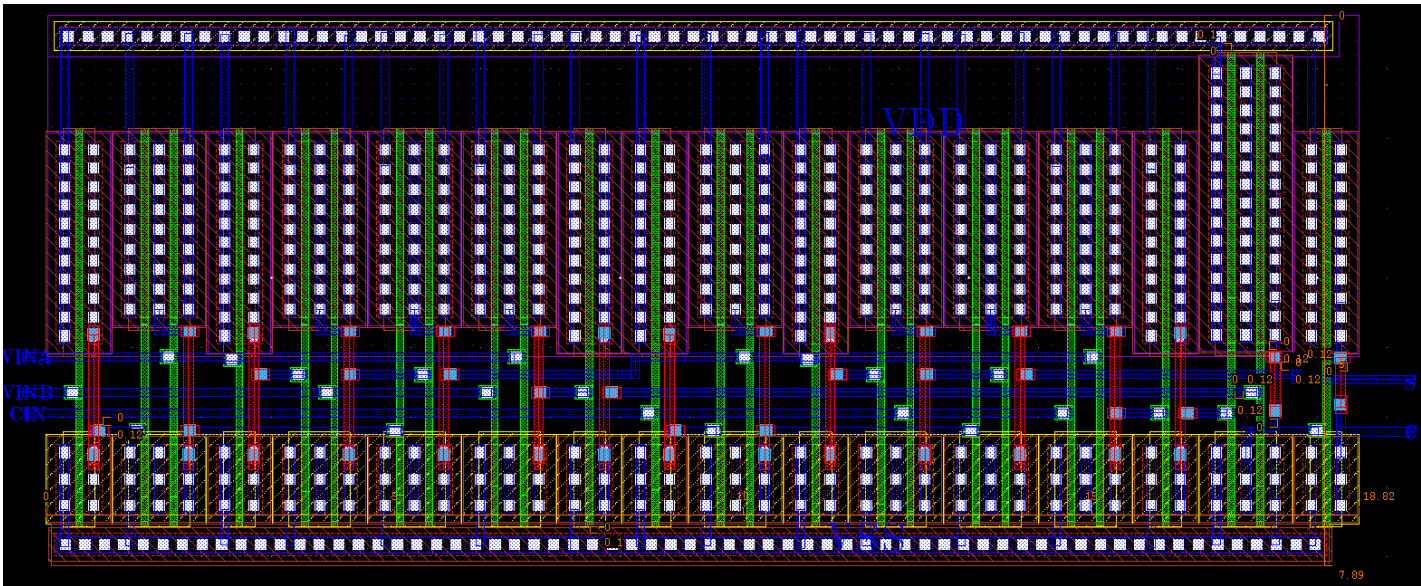
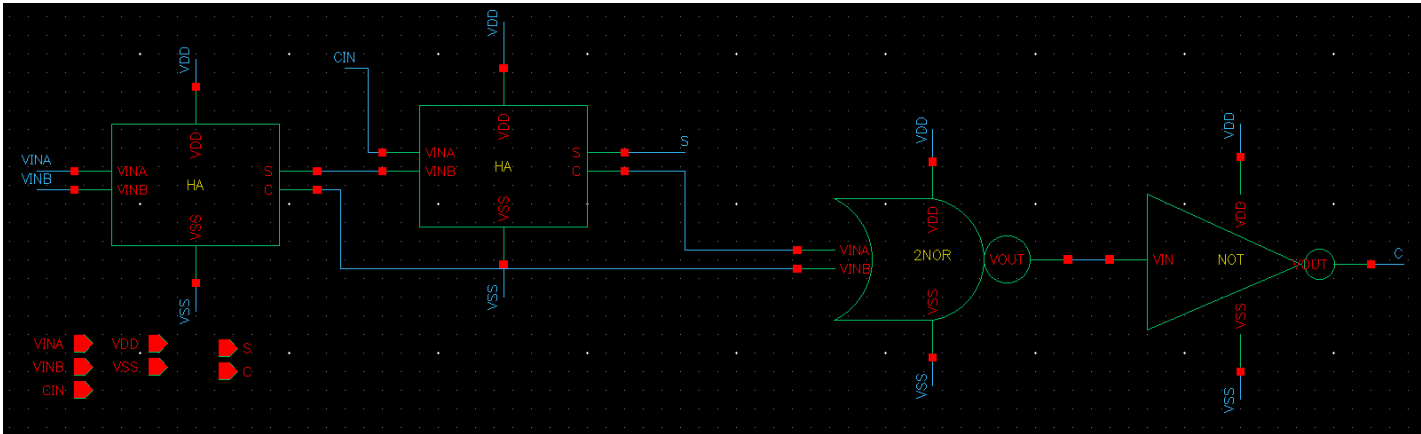
02

03

04

05

Full Adder



01

Adder

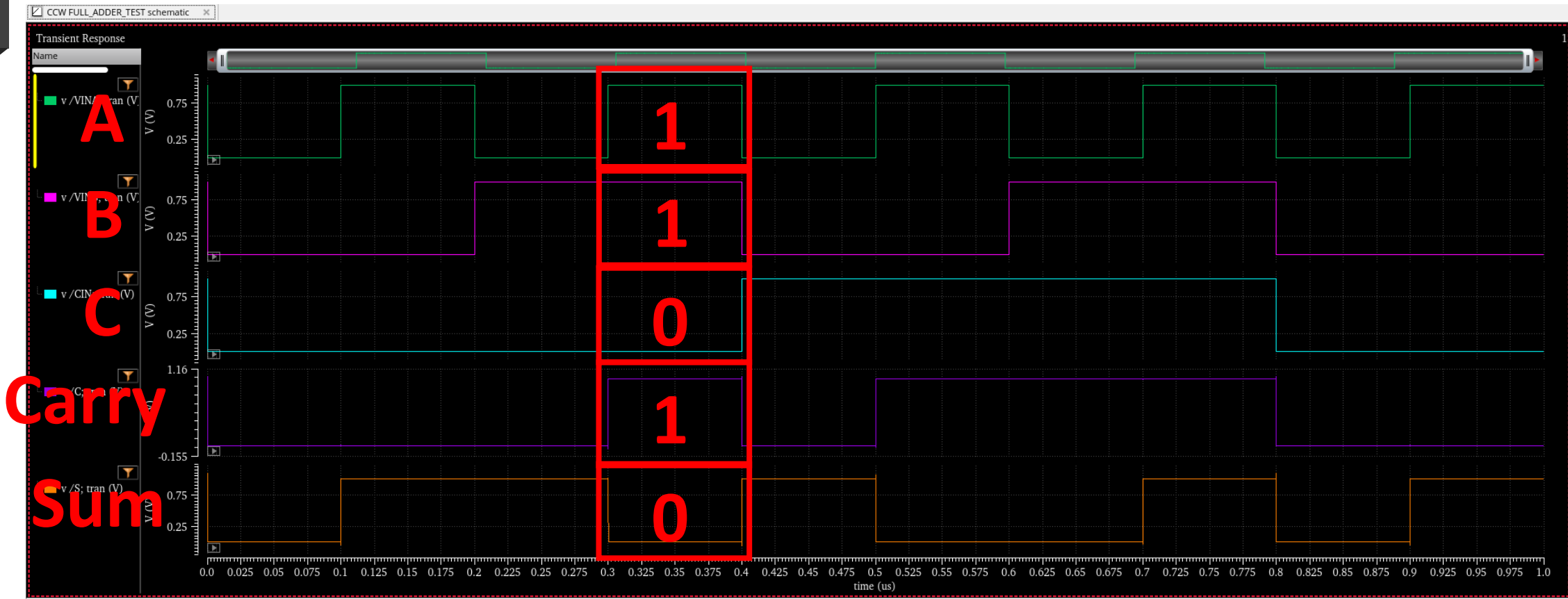
02

03

04

05

[Full Adder]
Simulation



01

Adder

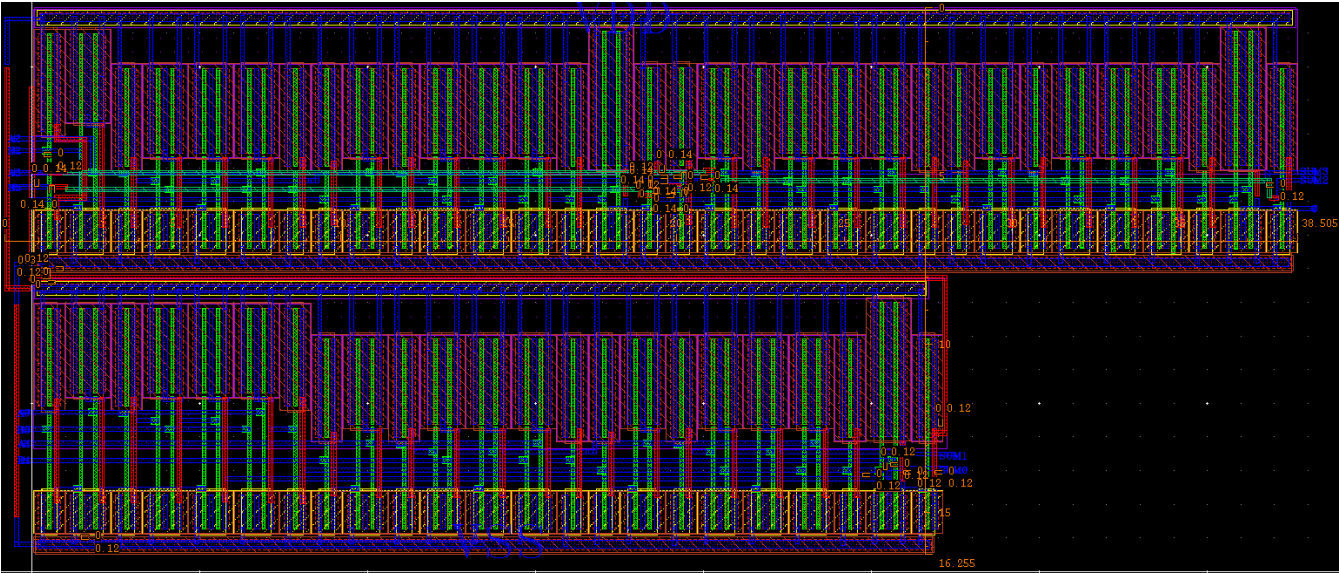
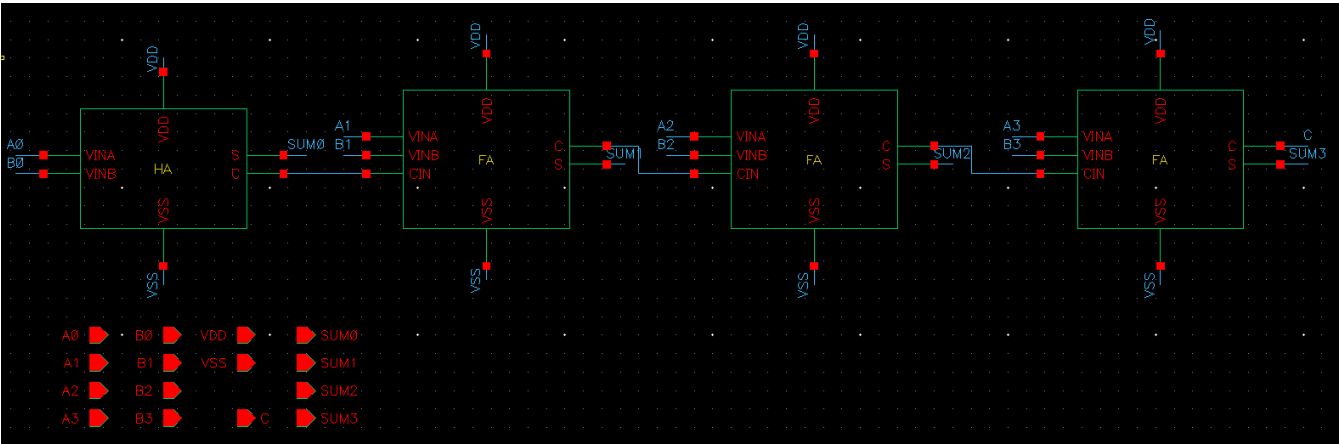
02

03

04

05

4-Bit Adder



01

Adder

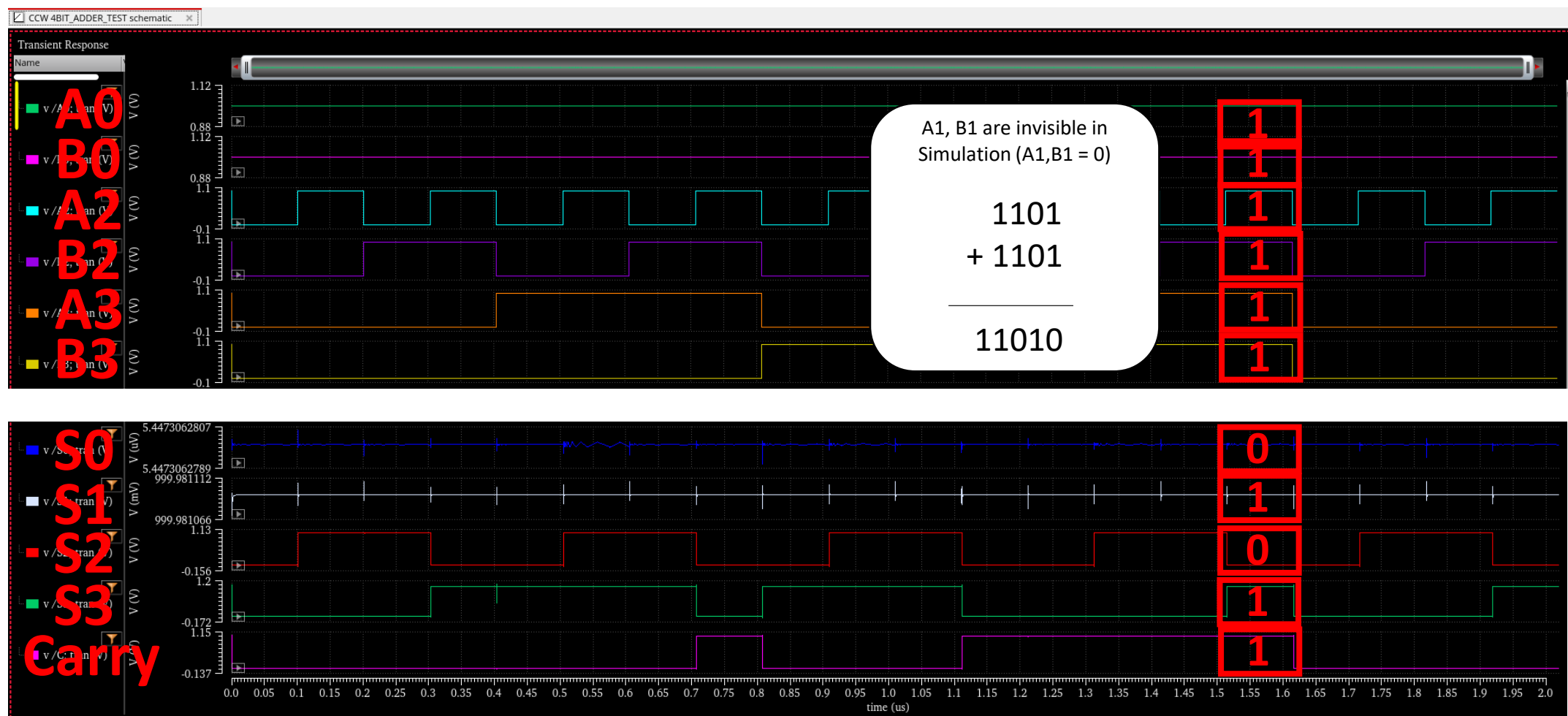
02

03

04

05

[4-Bit Adder]
Simulation



01

02

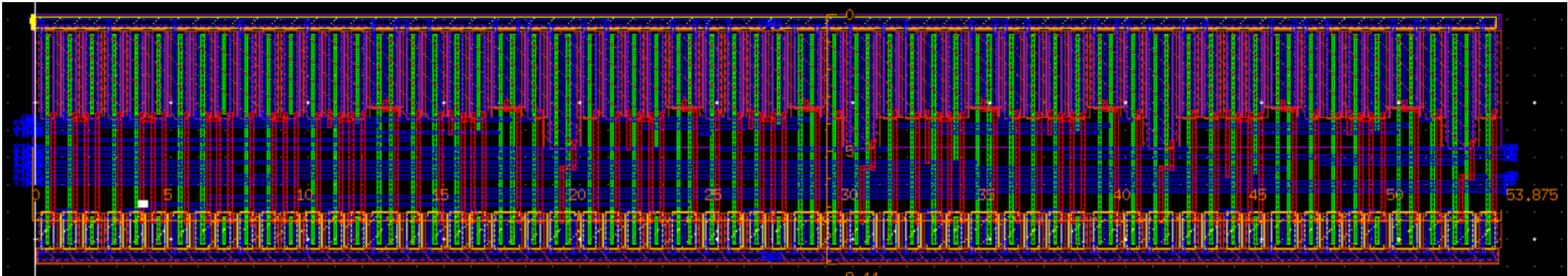
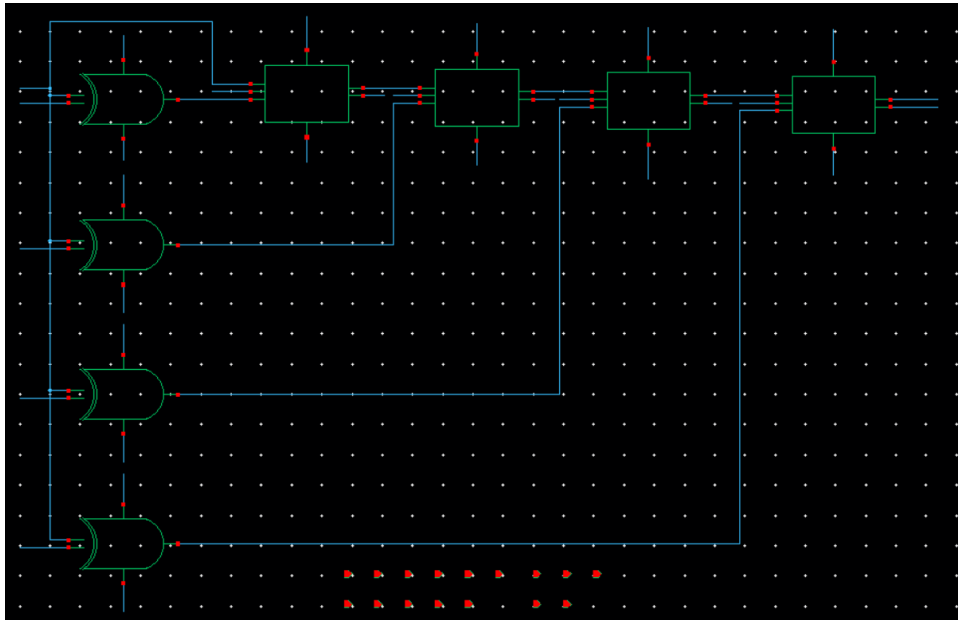
03

04

05

Adder

4Bit Adder-Subtractor



01

Adder

02

03

04

05

[4Bit Adder-Subtractor]
Simulation



01

02

03

04

05

A certificate of completion



Contact



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