

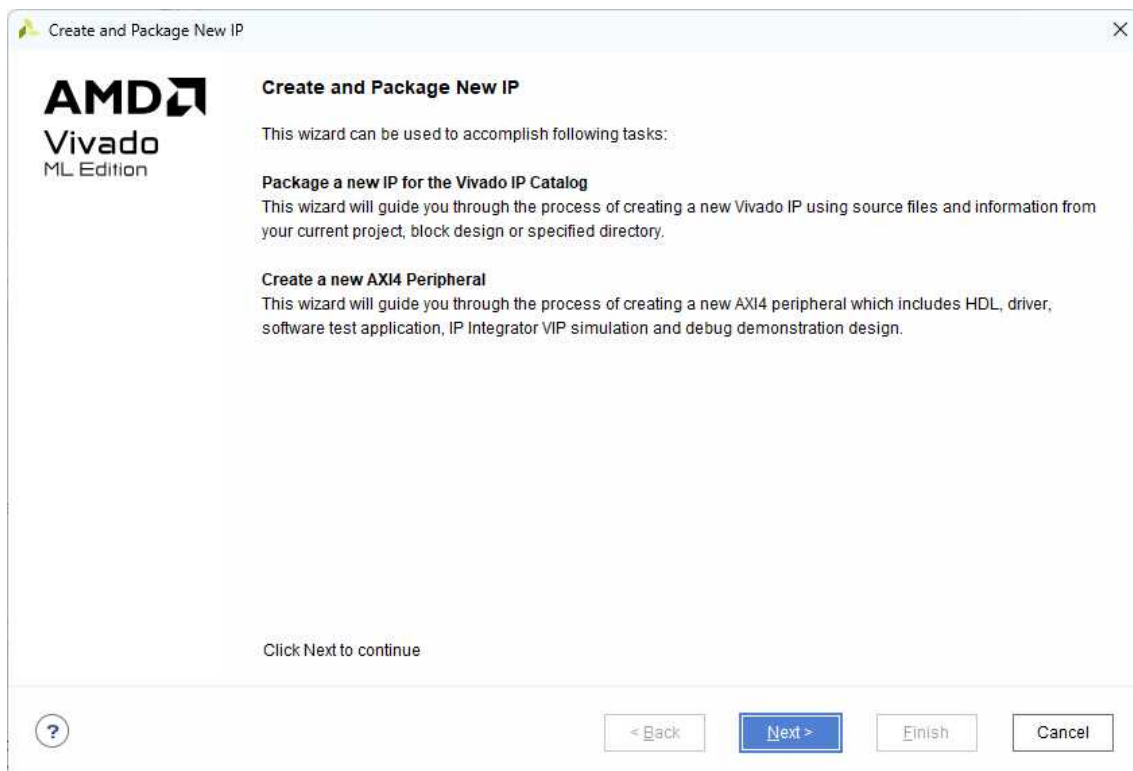
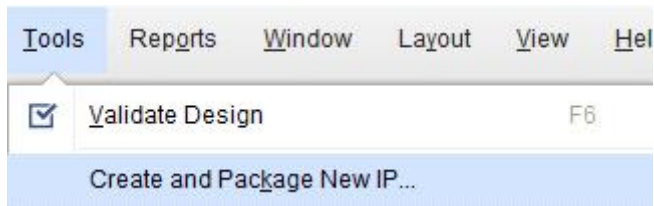
TCounter 모듈 추가하기

▼ IP INTEGRATOR

Create Block Design

[Open Block Design](#)

Generate Block Design



Create and Package New IP

Create Peripheral, Package IP or Package a Block Design

Please select one of the following tasks.

Packaging Options

☐ Package your current project

Use the project as the source for creating a new IP Definition.

☐ Package a block design from the current project

Choose a block design as the source for creating a new IP Definition.

Select a block design: design_1

☐ Package a specified directory

Choose a directory as the source for creating a new IP Definition.

Create AXI4 Peripheral

☒

Create a new AXI4 peripheral

Create an AXI4 IP, driver, software test application, IP Integrator AXI4 VIP simulation and debug demonstration design.

?

< Back

Next >

Finish

Cancel

Create and Package New IP

Peripheral Details

Specify name, version and description for the new peripheral

Name: myip_tcounter

Version: 1.0

Display name: myip_tcounter_v1.0

Description: My new AXI IP

IP location: C:/Users/edu/Desktop/HDLLabs/project_5/.../ip_repo

☐ Overwrite existing

?

< Back

Next >

Finish

Cancel

Create and Package New IP

Add Interfaces

Add AXI4 interfaces supported by your peripheral

☐ Enable Interrupt Support

+

-

Interfaces

S00_AXI

S00_AXI

myip_tcounter_v1.0

Name	S00_AXI
Interface Type	Lite
Interface Mode	Slave
Data Width (Bits)	32
Memory Size (Bytes)	64
Number of Registers	12 [4..512]

< Back Next > Finish Cancel

Create and Package New IP

Create Peripheral

AMD Vivado ML Edition

Peripheral Generation Summary

1. IP (xilinx.com:user:myip_tcounter:1.0) with 1 interface(s)
2. Driver(v1_00_a) and testapp [more info](#)
3. AXI4 VIP Simulation demonstration design [more info](#)
4. AXI4 Debug Hardware Simulation demonstration design [more info](#)

Peripheral created will be available in the catalog :

C:/Users/edu/Desktop/HDLLabs/project_5/./ip_repo

Next Steps:

☐ Add IP to the repository

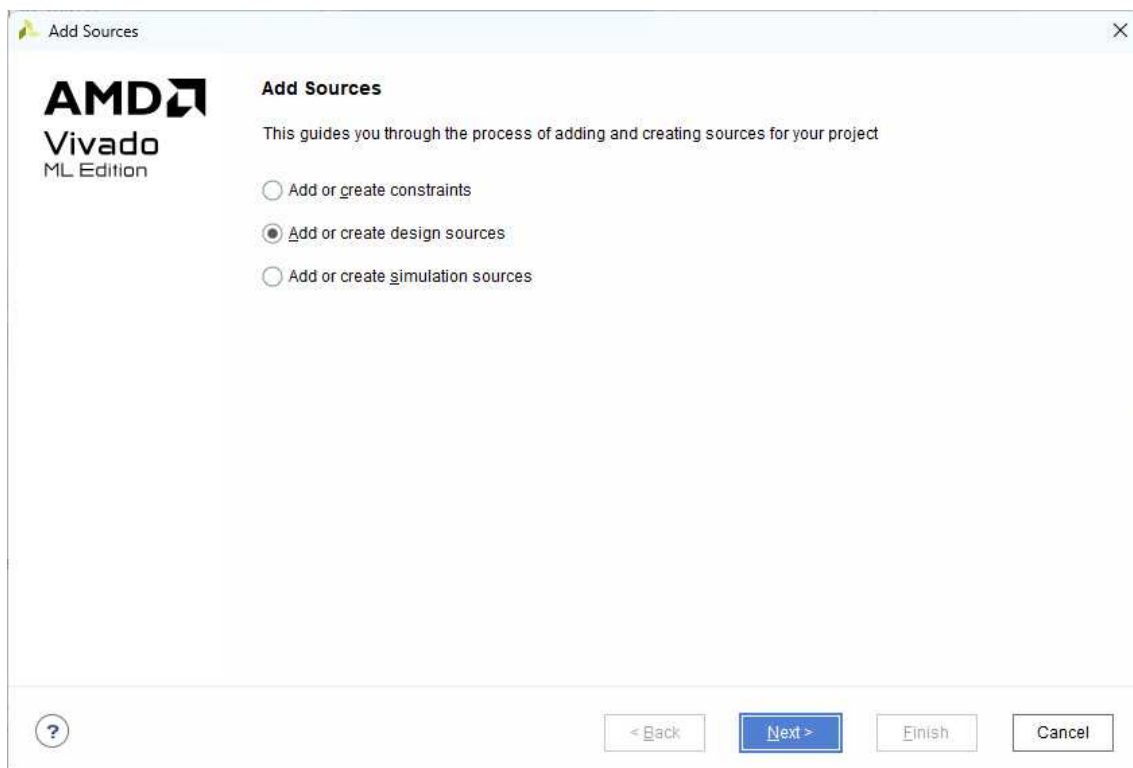
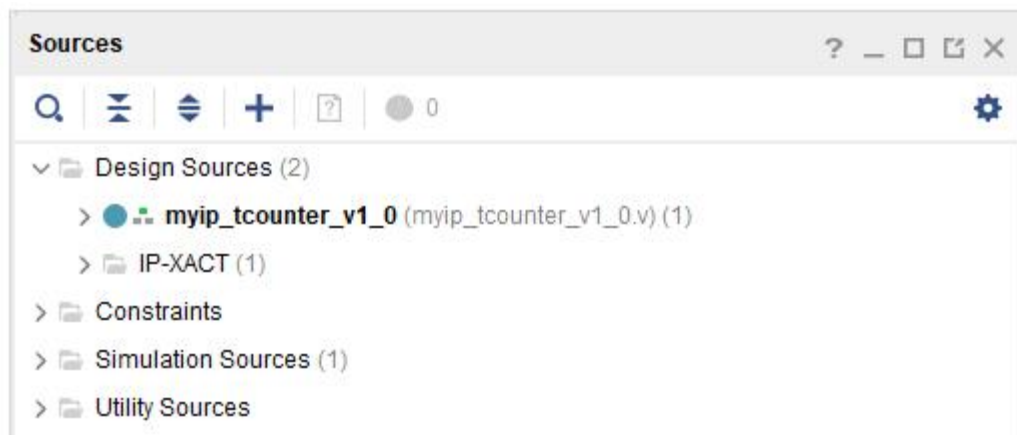
☒ Edit IP

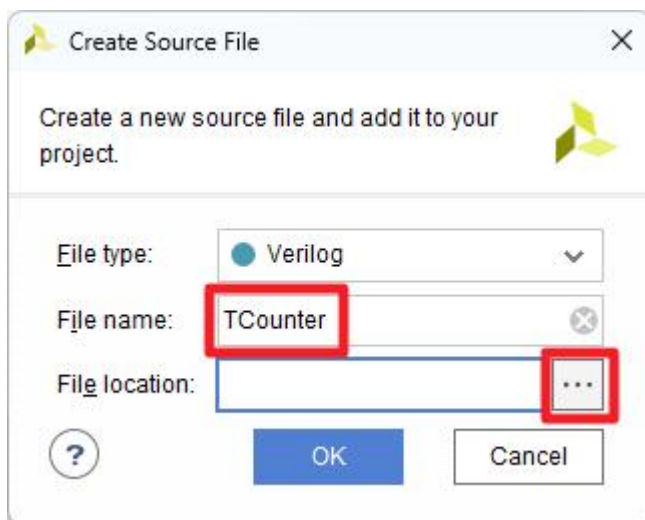
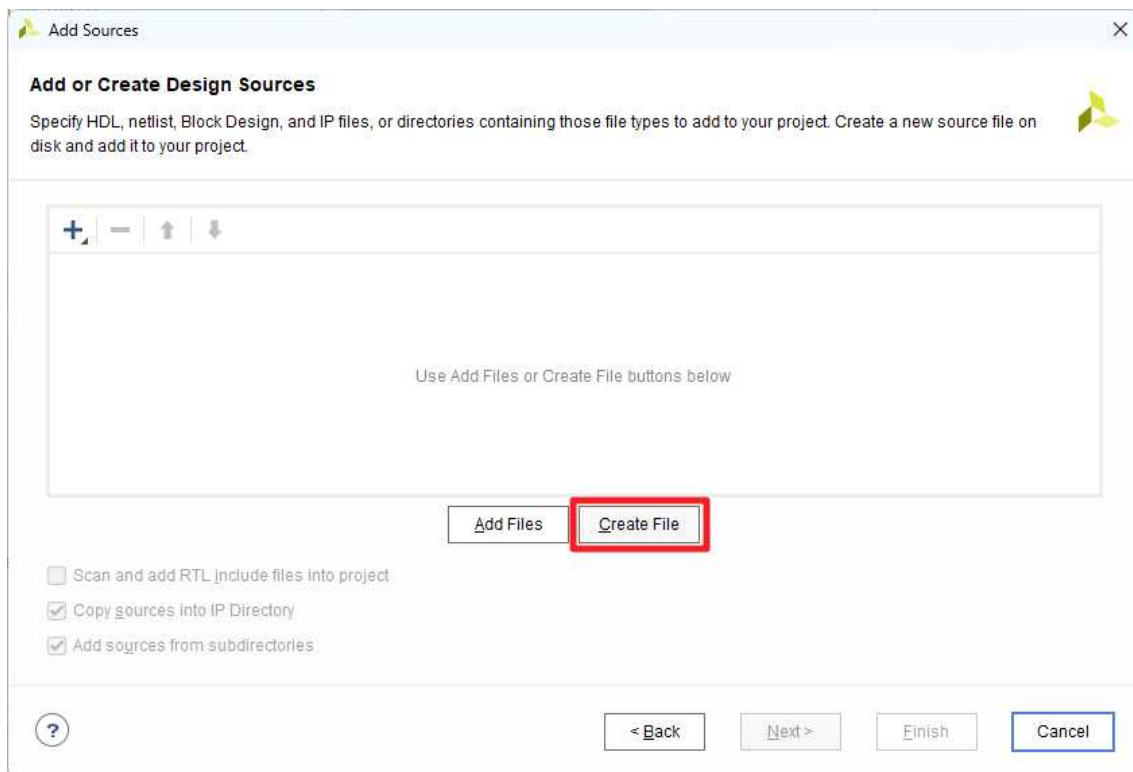
☐ Verify Peripheral IP using AXI4 VIP

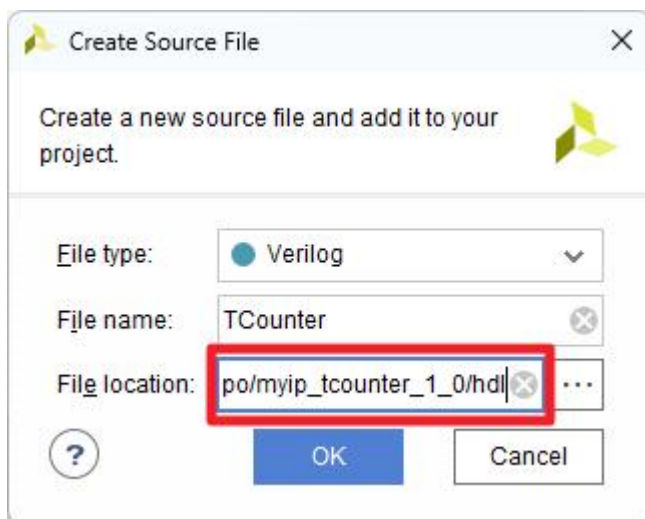
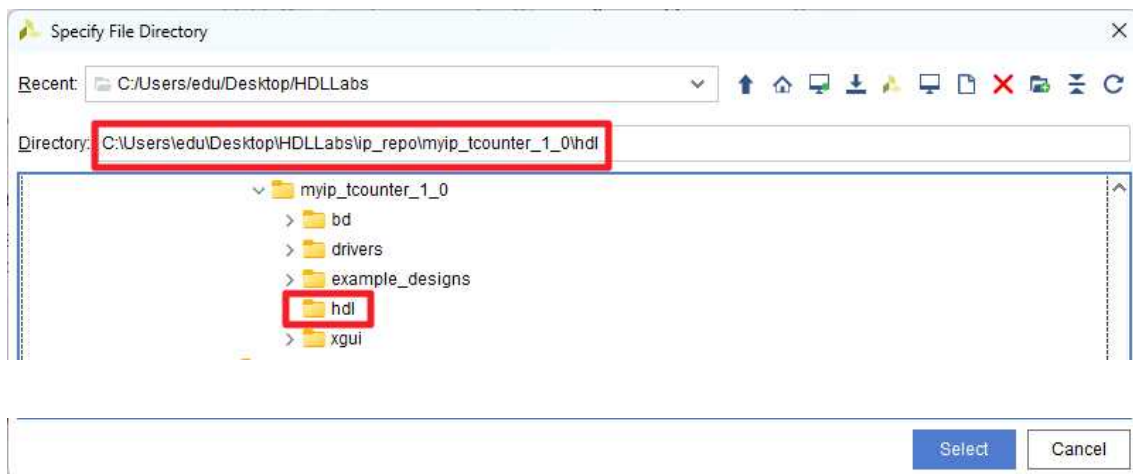
☐ Verify peripheral IP using JTAG interface

Click Finish to continue

< Back Next > Finish Cancel







Add Sources

×

Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

+

−

↑

↓

	Index	Name	Library	Location
●	1	TCounter.v	xil_defaultlib	C:/Users/edu/Desktop/HDLLabs/ip_repo/myip_tcounter_1_0/hdl

Add Files

Create File

☐ Scan and add RTL include files into project

☒ Copy sources into IP Directory

☒ Add sources from subdirectories

?

< Back

Next >

Finish

Cancel

Define Module

×

Define a module and specify I/O Ports to add to your source file.

For each port specified:

MSB and LSB values will be ignored unless its Bus column is checked.

Ports with blank names will not be written.

Module Definition

Module name:

I/O Port Definitions

+

−

↑

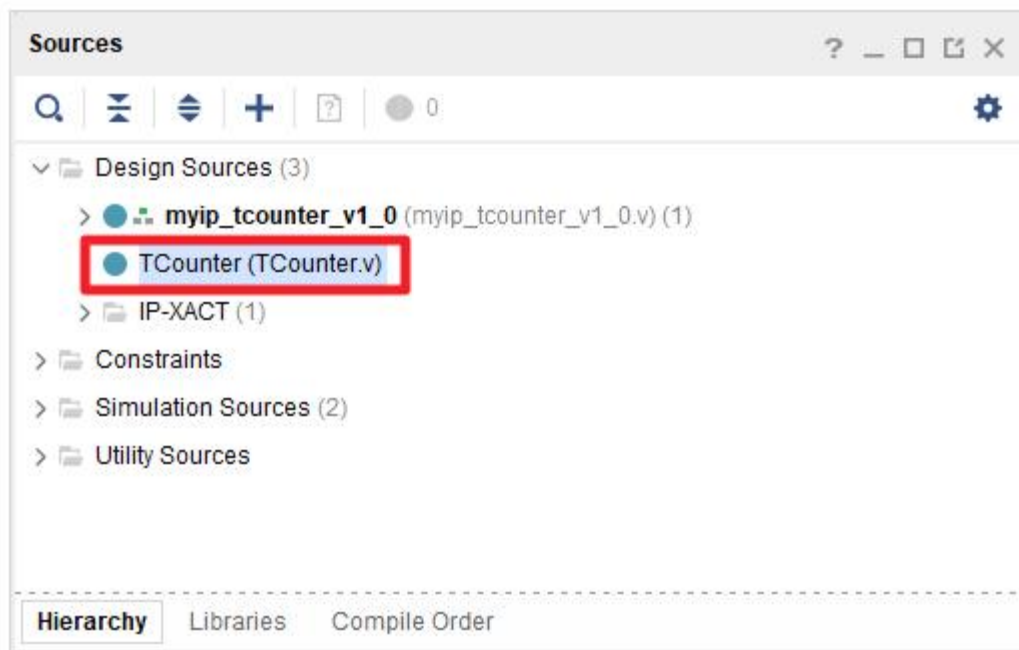
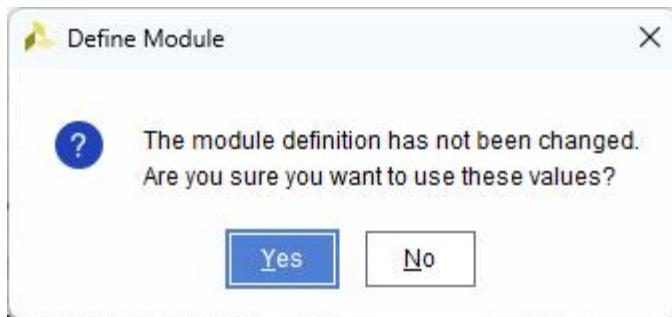
↓

Port Name	Direction	Bus	MSB	LSB
	input	<input type="checkbox"/>	0	0

?

OK

Cancel



```
module TCounter(  
    input CLK,  
    input RSTn,  
    input [31:0] top_in, // en, 4bit reserved, 27bit top  
    input [31:0] cmp_in, // 5bit reserved, 27bit cmp  
    output PWM  
);  
  
    reg [26:0] cnt; // 27비트  
    wire [26:0] top = top_in[26:0];  
    wire [26:0] cmp = cmp_in[26:0];  
    wire cnt_en = top_in[31];  
    always @(posedge CLK)  
    begin : CNT_MOD  
        if(RSTn==0) cnt<=0;
```

```

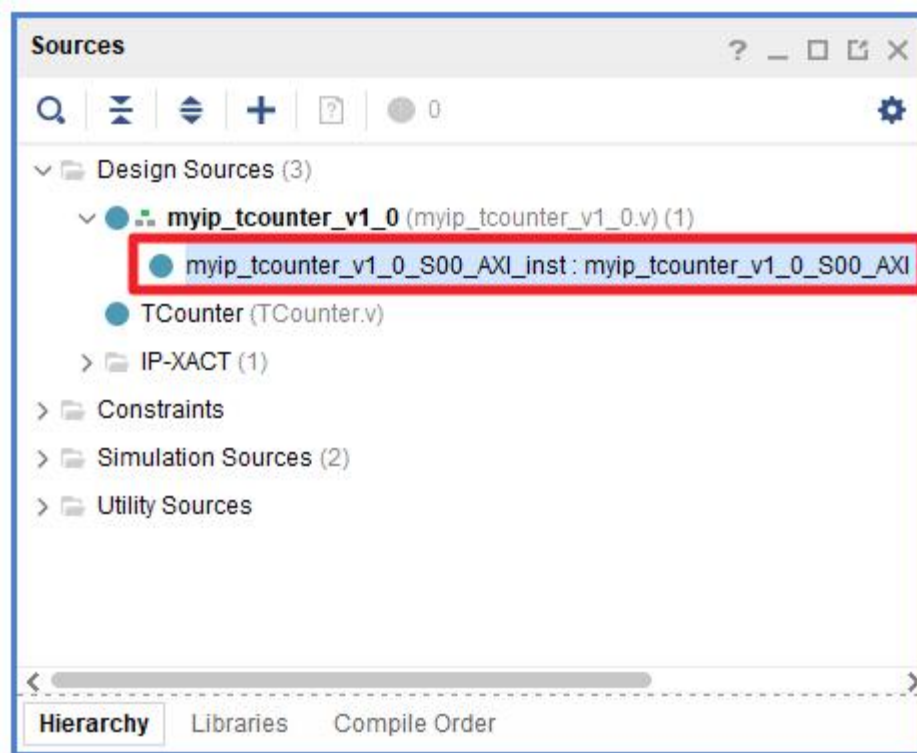
        else if(cnt_en) begin
            cnt<=cnt+1;
            if(cnt >= top)
                cnt <= 0;

        end
        else cnt<=0;
    end

    assign PWM = (cnt < cmp)?1:0;

endmodule

```



```

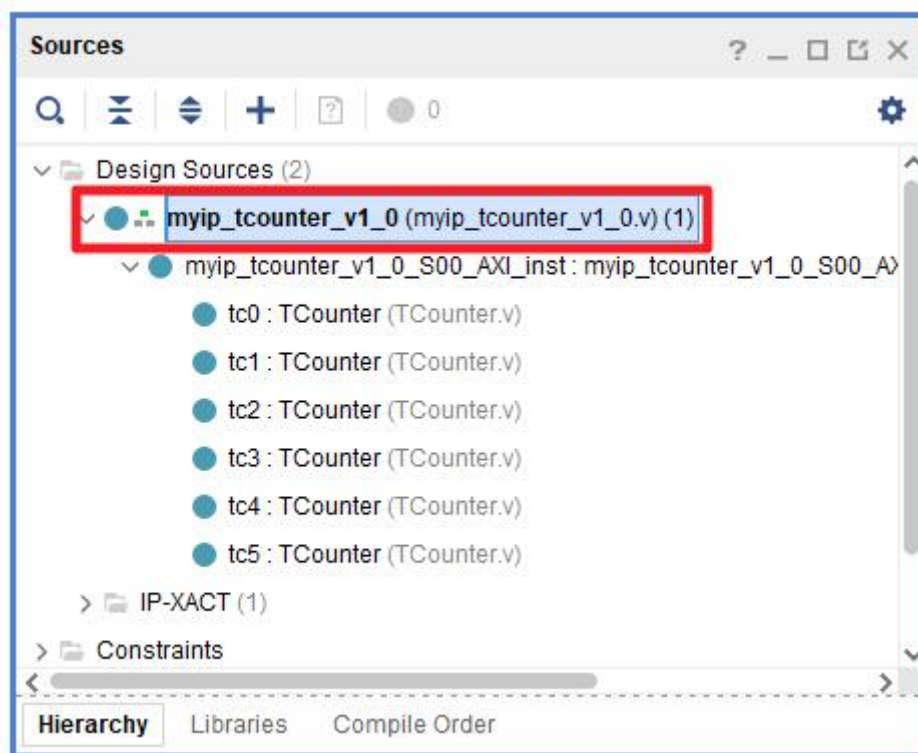
17 | // Users to add ports here
18 | output [5:0] PWM,|
19 | // User ports ends

```

```

488 // Add user logic here
489 TCounter tc0(S_AXI_ACLK,S_AXI_ARESETN,slv_reg0,slv_reg1,PWM[0]);
490 TCounter tc1(S_AXI_ACLK,S_AXI_ARESETN,slv_reg2,slv_reg3,PWM[1]);
491 TCounter tc2(S_AXI_ACLK,S_AXI_ARESETN,slv_reg4,slv_reg5,PWM[2]);
492 TCounter tc3(S_AXI_ACLK,S_AXI_ARESETN,slv_reg6,slv_reg7,PWM[3]);
493 TCounter tc4(S_AXI_ACLK,S_AXI_ARESETN,slv_reg8,slv_reg9,PWM[4]);
494 TCounter tc5(S_AXI_ACLK,S_AXI_ARESETN,slv_reg10,slv_reg11,PWM[5]);
495 // User logic ends

```



```

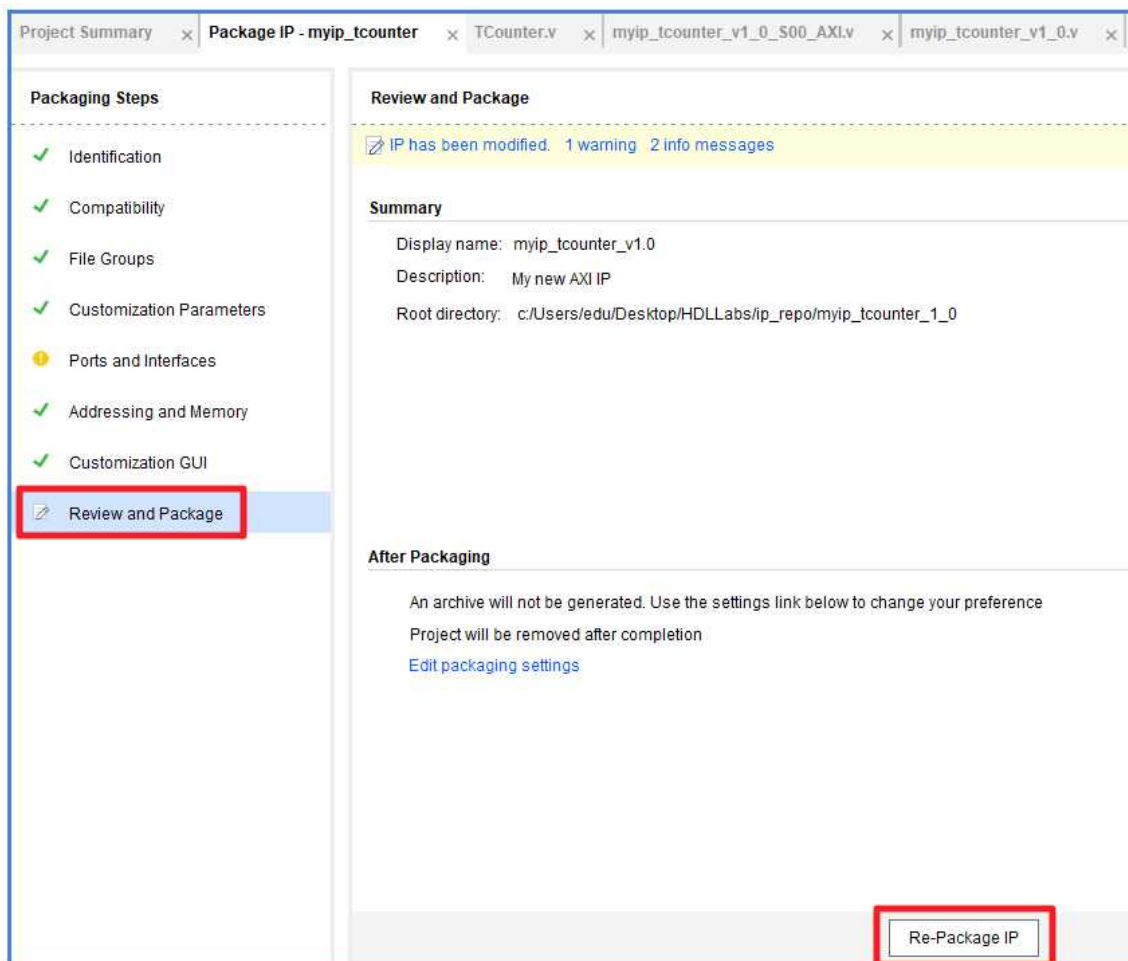
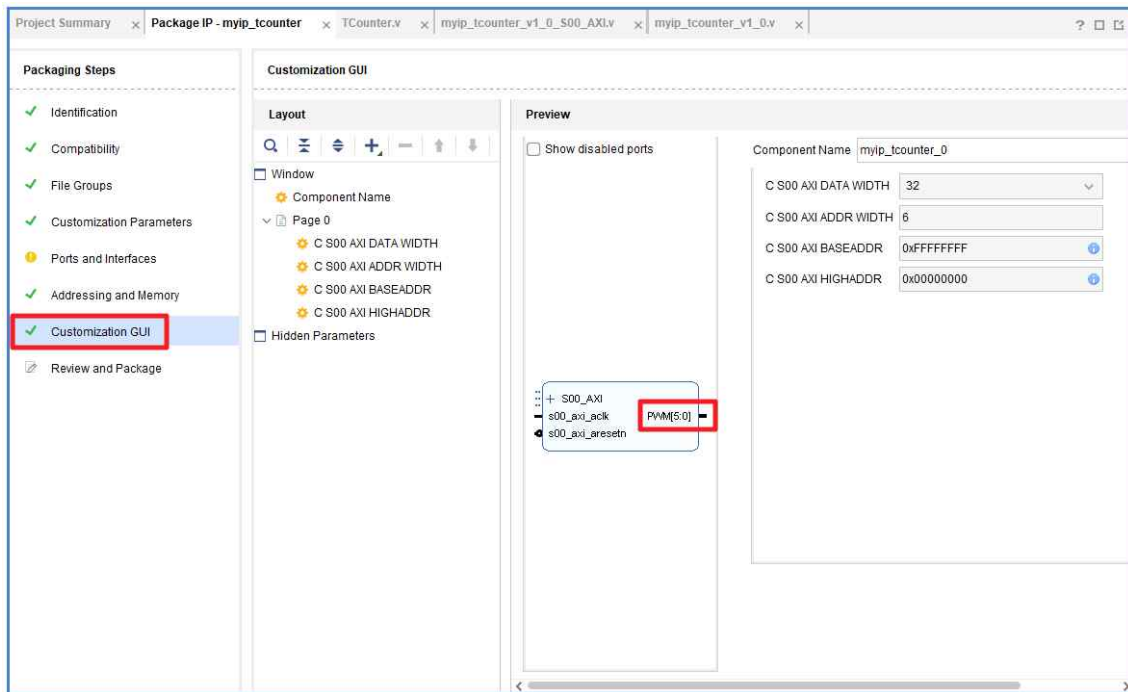
17 // Users to add ports here
18 output [5:0] PWM,
19 // User ports ends

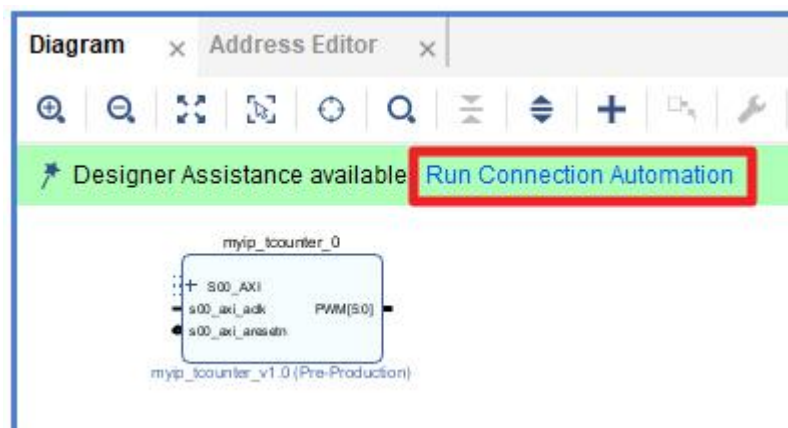
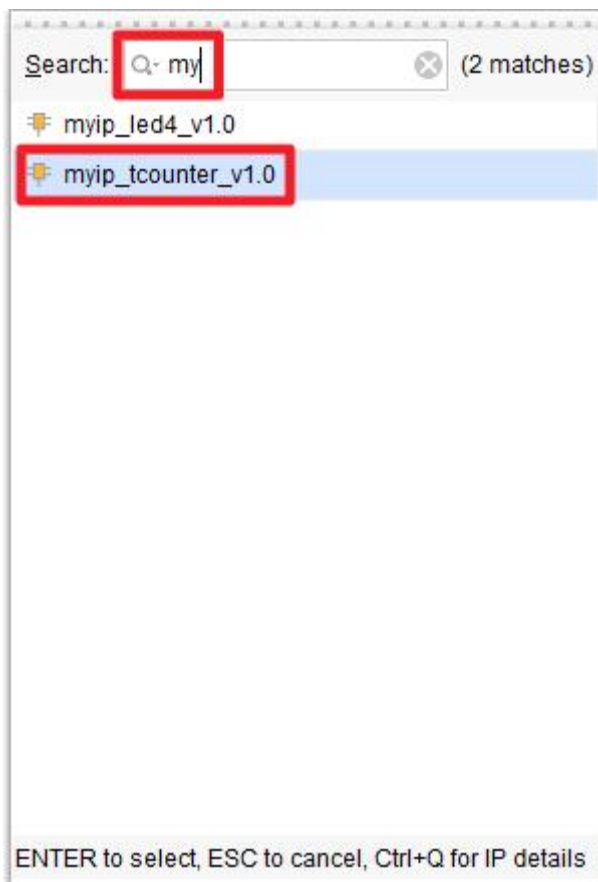
```

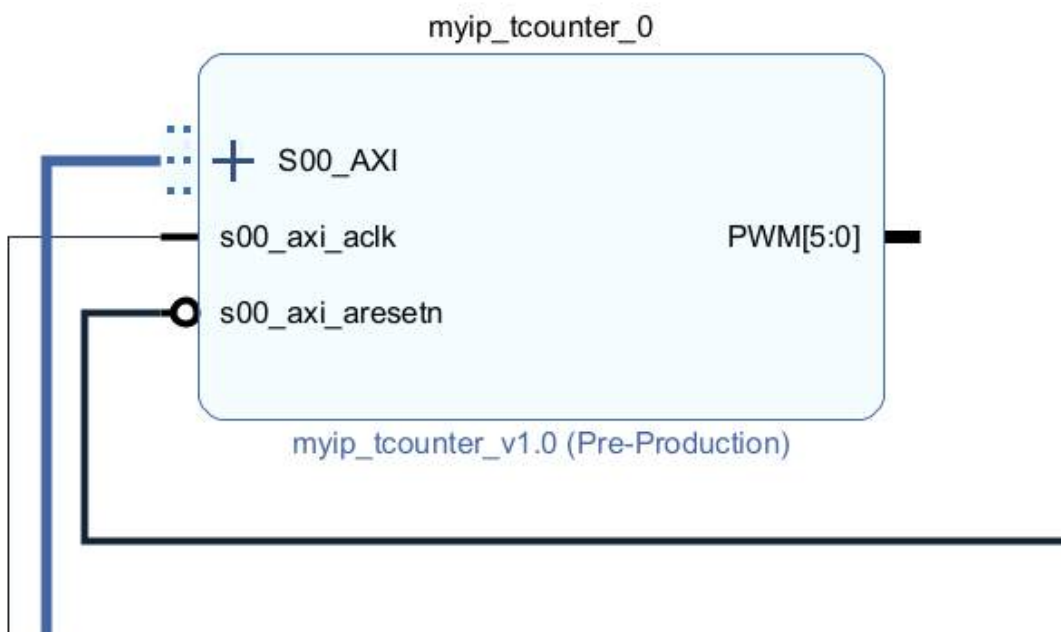
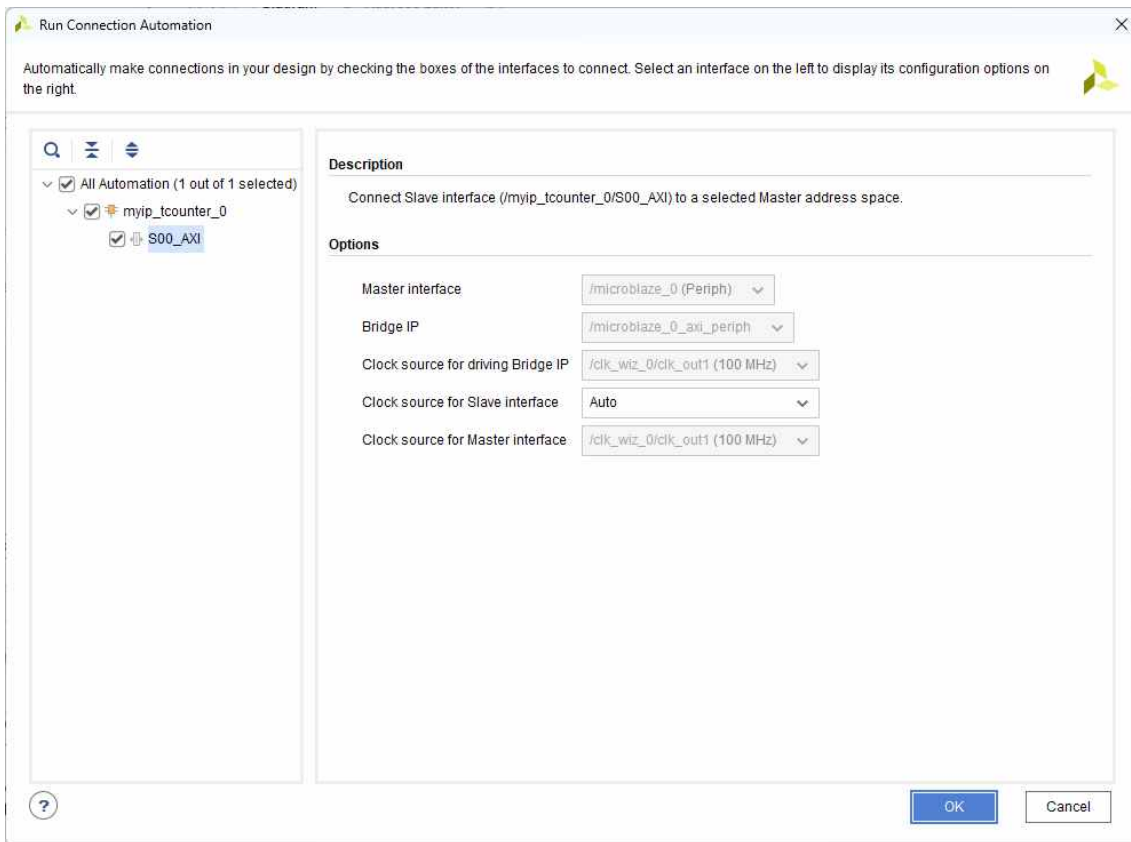
```

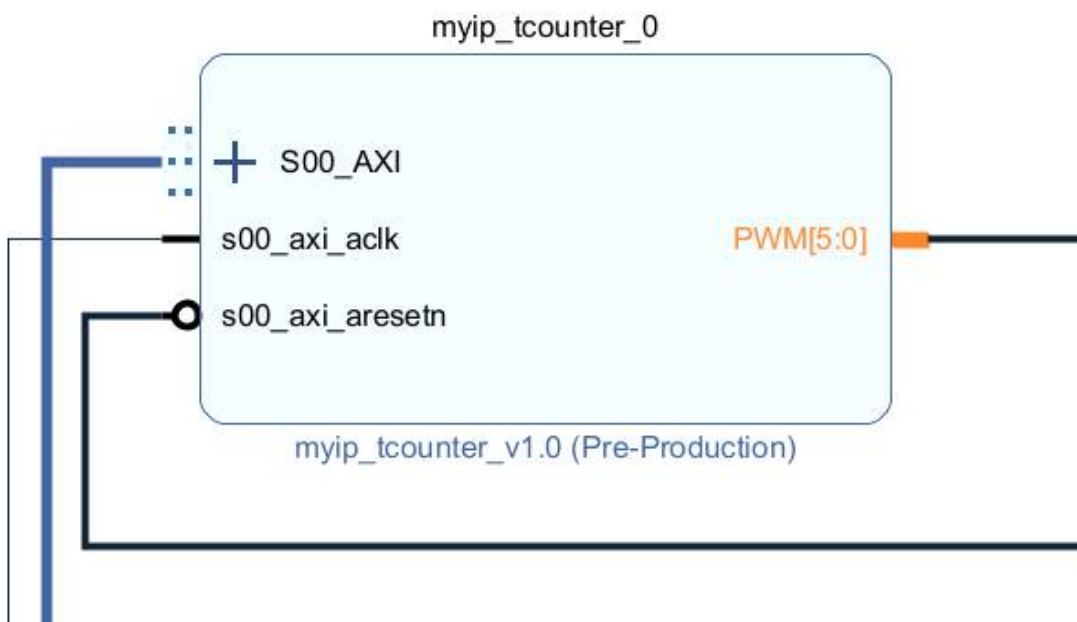
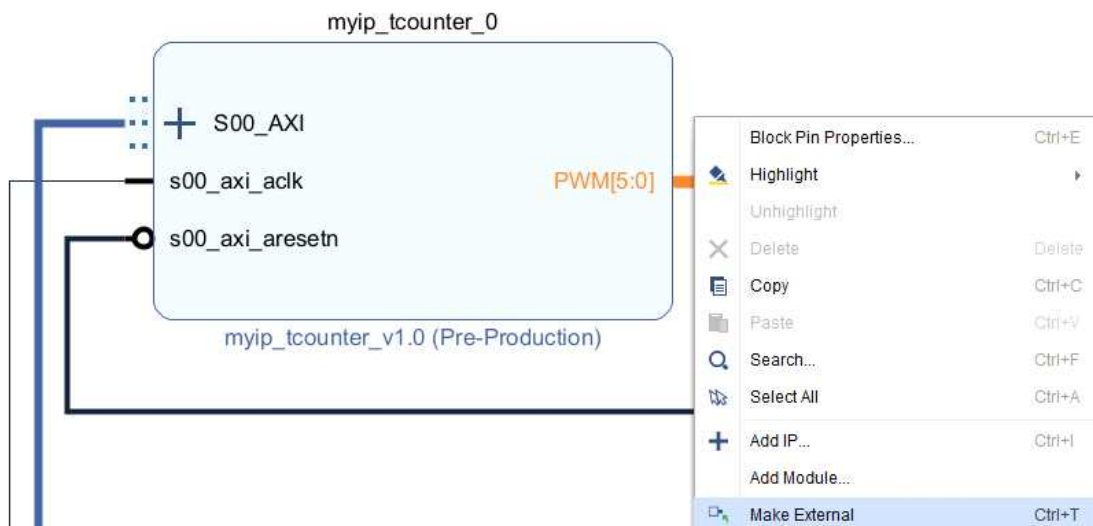
50 ) myip_tcounter_v1_0_S00_AXI_inst (
51     .PWM(PWM),|
52     .S_AXI_ACLK(s00_axi_ac1k),

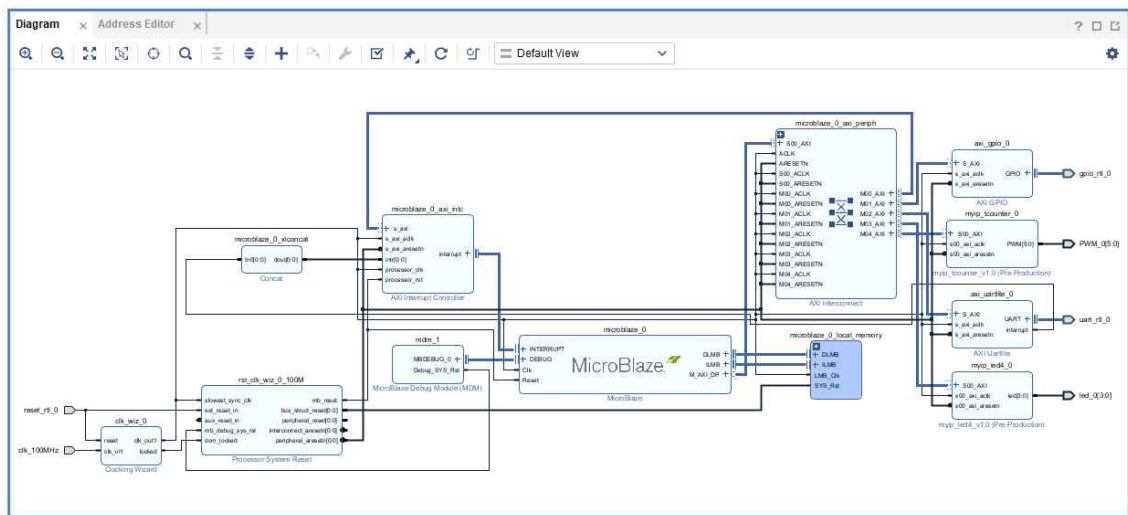
```









SYNTHESIS

[Run Synthesis](#)

> [Open Synthesized Design](#)

Save Project

Save project before launching synthesis?

Data to Save

☒ Block Design - design_1

[Save](#) [Cancel](#)

Synthesis Complete

SYNTHESIS

[Run Synthesis](#)

> [Open Synthesized Design](#)

Tcl Console Messages Log Reports Design Runs Package Pins I/O Ports x							
<div><div>Q</div><div>↔</div><div>⬇</div><div>⬆</div><div>+</div><div>⌂</div></div>							
Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	
v All ports (18)							
> CLK.CLK_100MHZ_54576 (1)	IN			<input checked="" type="checkbox"/>	34	LVCMOS33*	
> gpio_rtl_0_54576 (4)	OUT			<input checked="" type="checkbox"/>	14	LVCMOS33*	
> RST.RESET_RTL_0_54576 (1)	IN			<input checked="" type="checkbox"/>	14	LVCMOS33*	
> uart_rtl_0_54576 (2)	(Multiple)			<input checked="" type="checkbox"/>	16	LVCMOS33*	
> led_0 (4)	OUT			<input checked="" type="checkbox"/>	14	LVCMOS33*	
v PWM_0 (6)	OUT			<input checked="" type="checkbox"/>	(Multiple)	LVCMOS33*	
PWM_0[5]	OUT		L1	<input checked="" type="checkbox"/>	35	LVCMOS33*	
PWM_0[4]	OUT		P1	<input checked="" type="checkbox"/>	35	LVCMOS33*	
PWM_0[3]	OUT		N3	<input checked="" type="checkbox"/>	35	LVCMOS33*	
PWM_0[2]	OUT		P3	<input checked="" type="checkbox"/>	35	LVCMOS33*	
PWM_0[1]	OUT		U3	<input checked="" type="checkbox"/>	34	LVCMOS33*	
PWM_0[0]	OUT		W3	<input checked="" type="checkbox"/>	34	LVCMOS33*	
Scalar ports (0)							

Constraints Order Changed

All new constraints are saved to the target constraint file 'C:/Users/edu/Desktop/HDLLabs/project_5/project_5.srscs/constrs_1/new/design_1_wrapper.xdc' in constraint set 'constrs_1' which is not last in the constraints compile order. The order of the constraint files in the constraint set does not match the order in which the constraint files will be read during the next design load operation. You must validate that the saved constraints still apply correctly by reloading the design and re-validating the constraints before running synthesis or implementation.

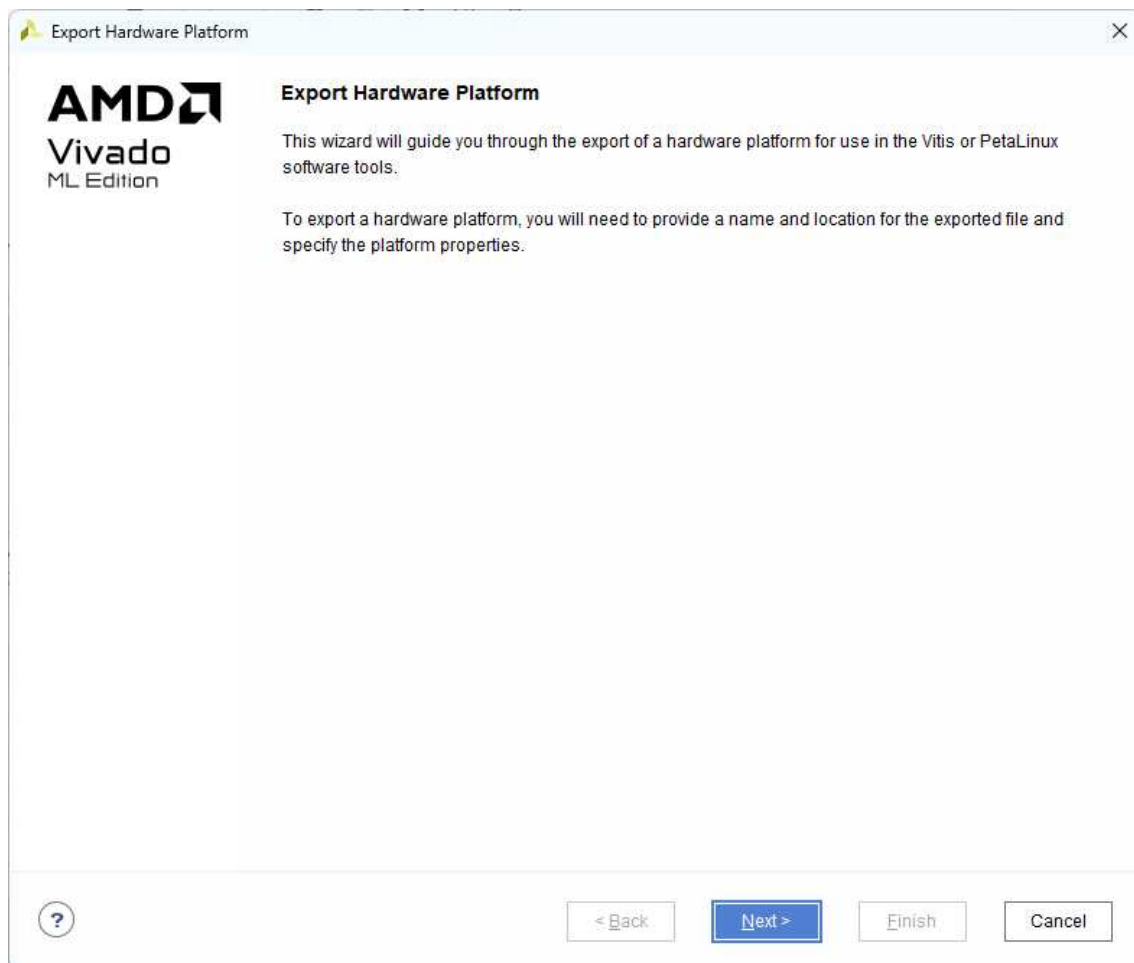
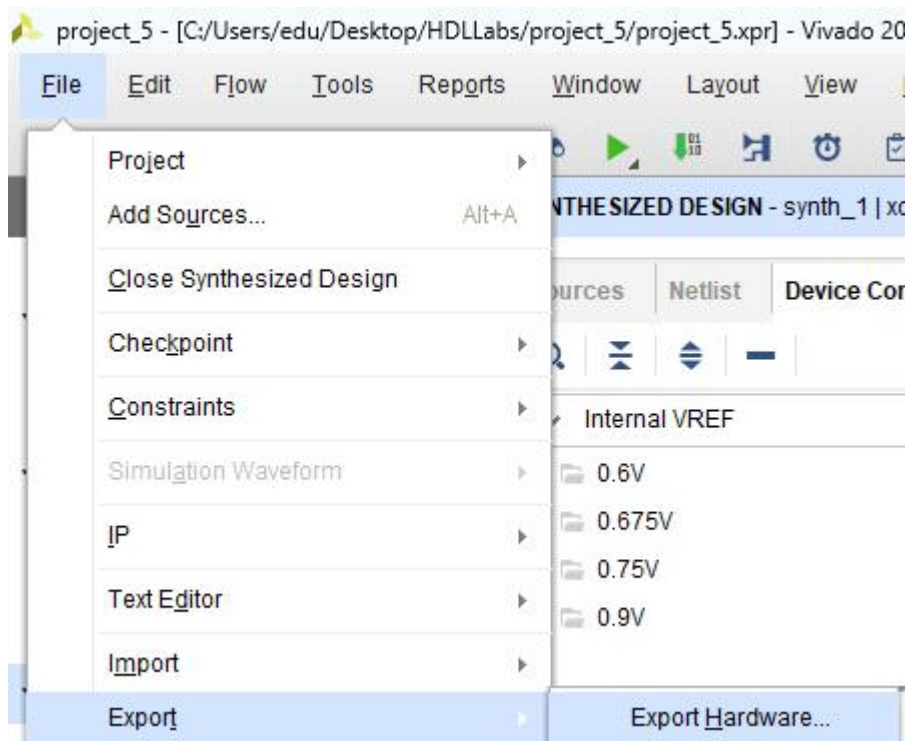
OK

PROGRAM AND DEBUG

[Generate Bitstream](#)

> [Open Hardware Manager](#)

write_bitstream Complete



Export Hardware Platform

Output

Set the platform properties to inform downstream tools of the intended use of the target platform's hardware design.

☐ Pre-synthesis

This platform includes a hardware specification for downstream software tools.

☒ Include bitstream

This platform includes the complete hardware implementation and bitstream, in addition to the hardware specification for software tools.

< Back

Next >

Finish

Cancel

Export Hardware Platform

Files

Enter the name of your hardware platform file, and the directory where the XSA file will be stored.

XSA file name:

design_1_wrapper

Export to:

C:/Users/edu/Desktop/HDLLabs/project_5

The XSA will be written to: C:\Users\edu\Desktop\HDLLabs\project_5\design_1_wrapper.xsa

< Back

Next >

Finish

Cancel

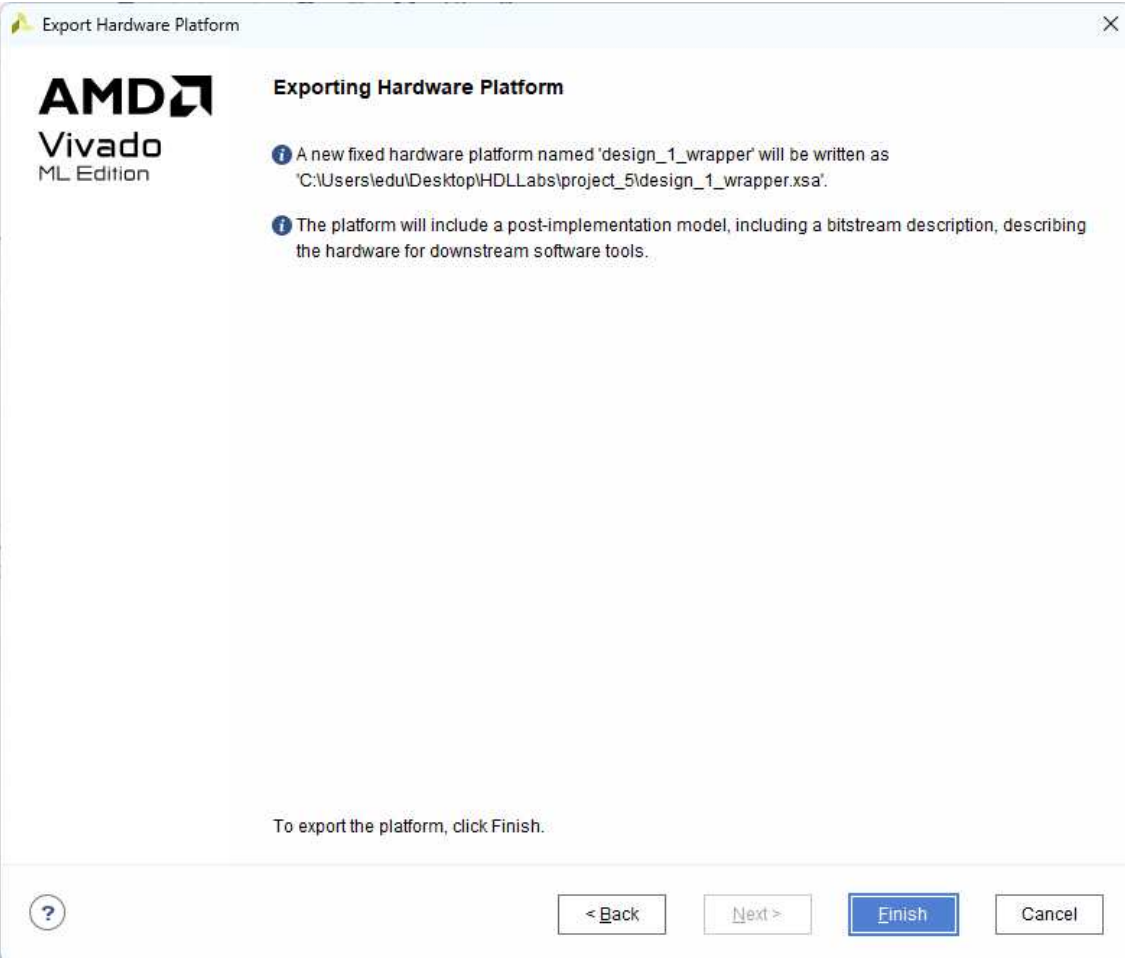
Module Already Exported

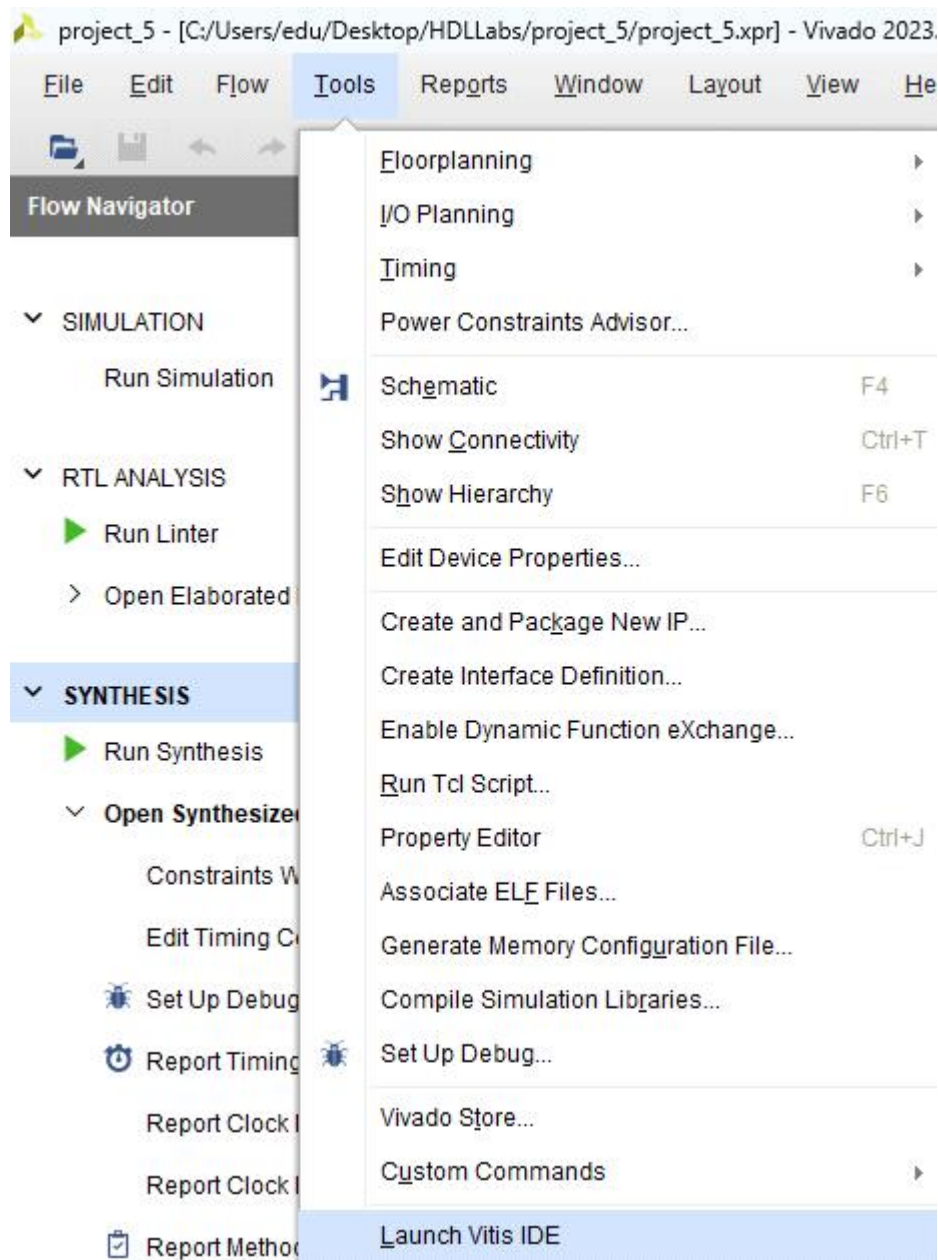
?

An exported file for this module was found at this location. Do you want to overwrite it?

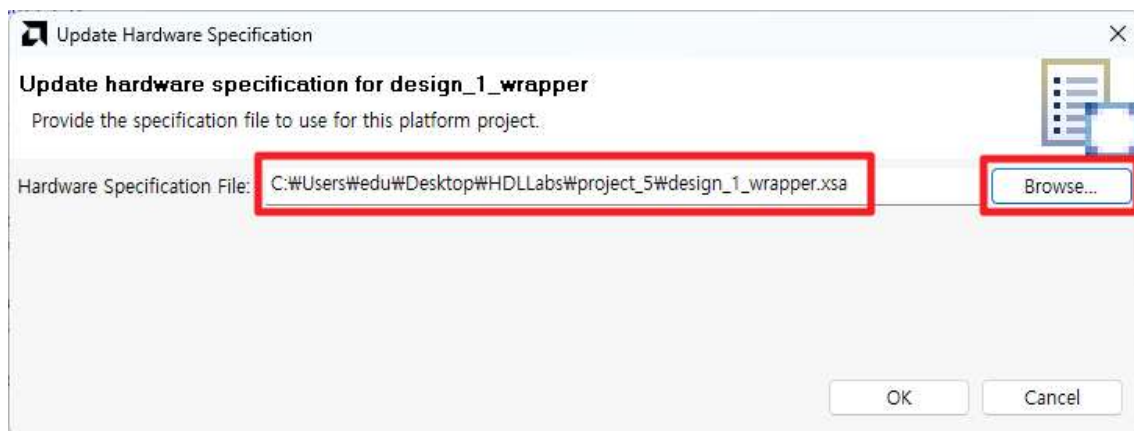
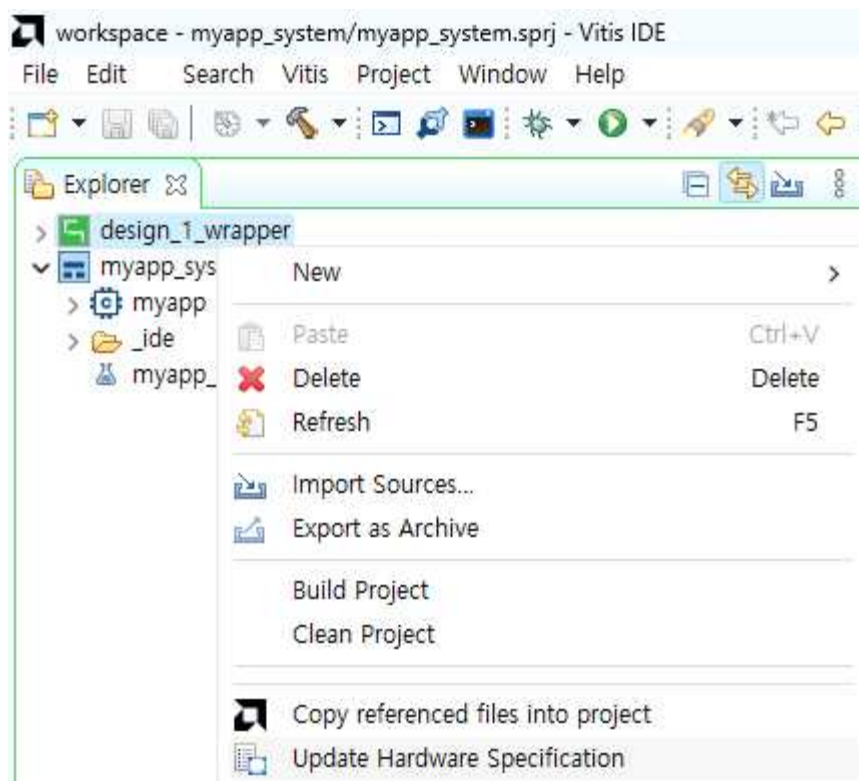
Yes

No

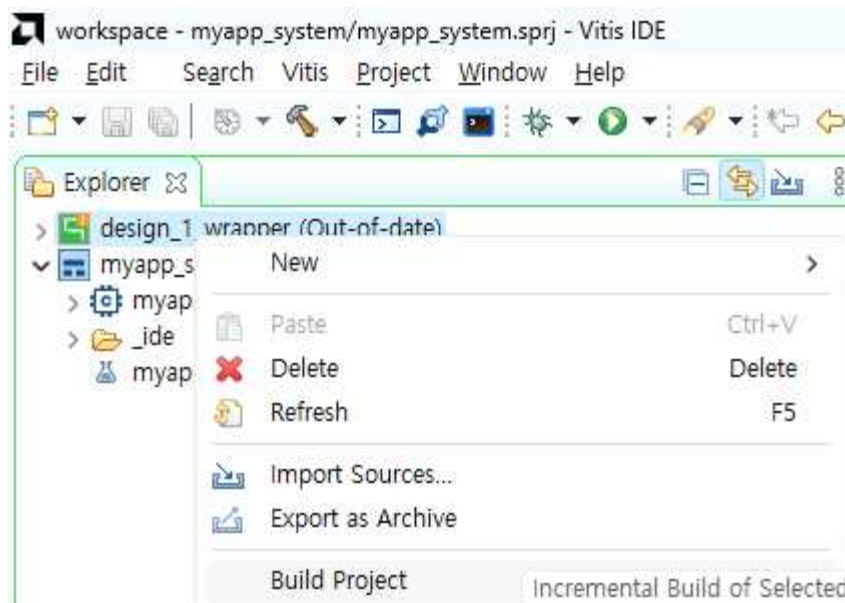




vitis가 실행되어 있지 않으면 실행시킵니다.



> design_1_wrapper (Out-of-date)

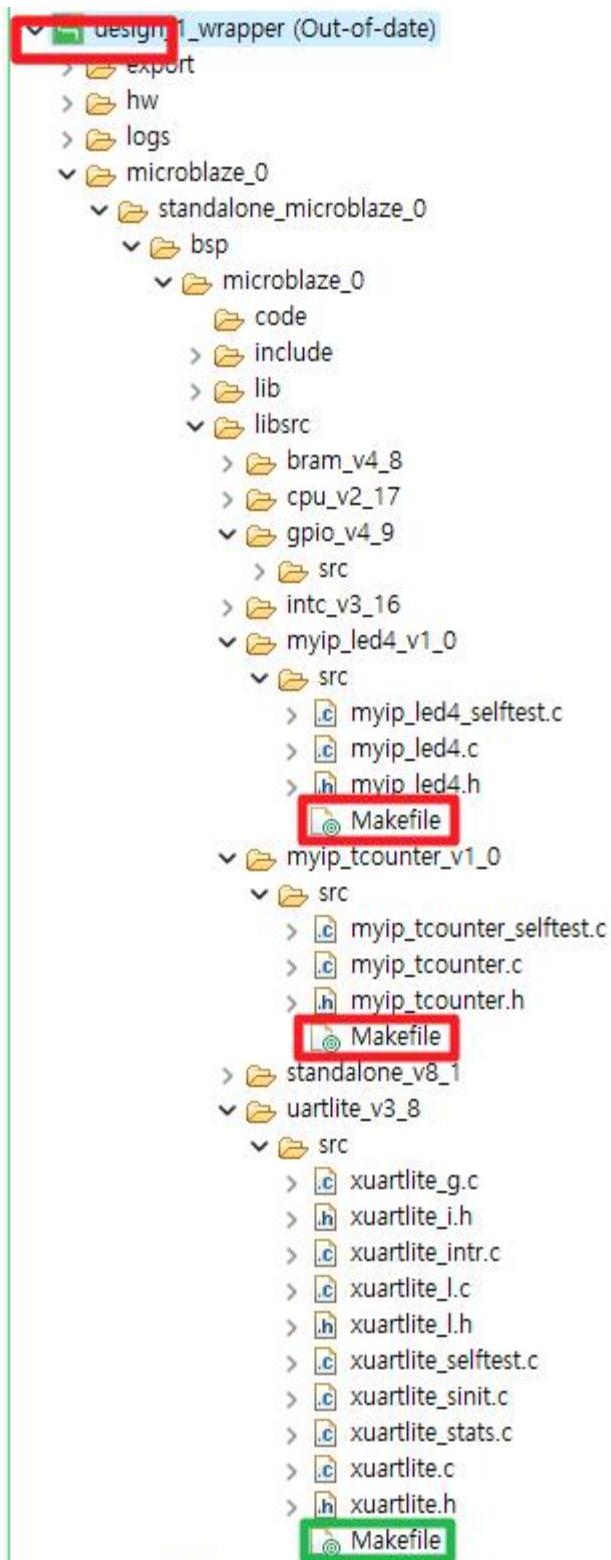


Console Problems Vitis Log Guidance

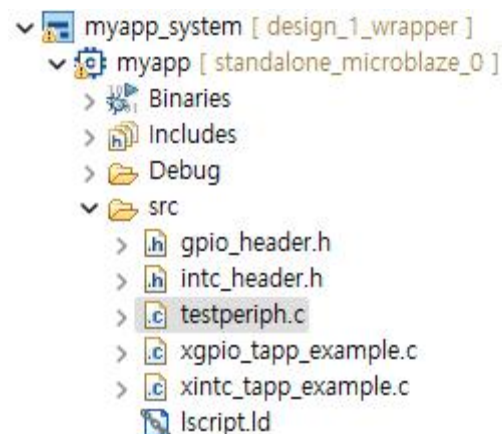
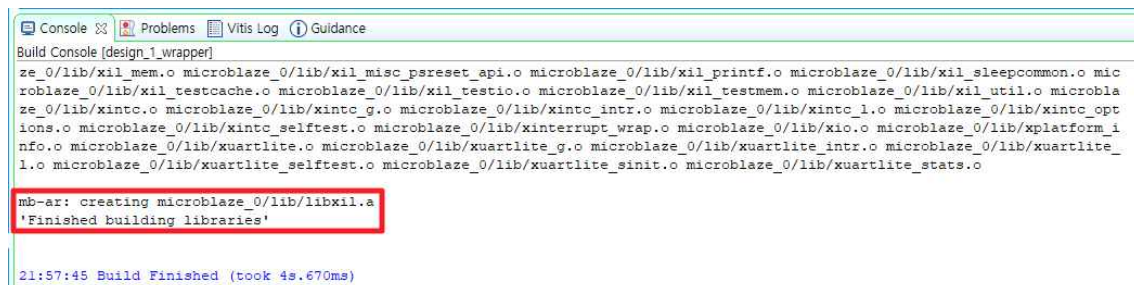
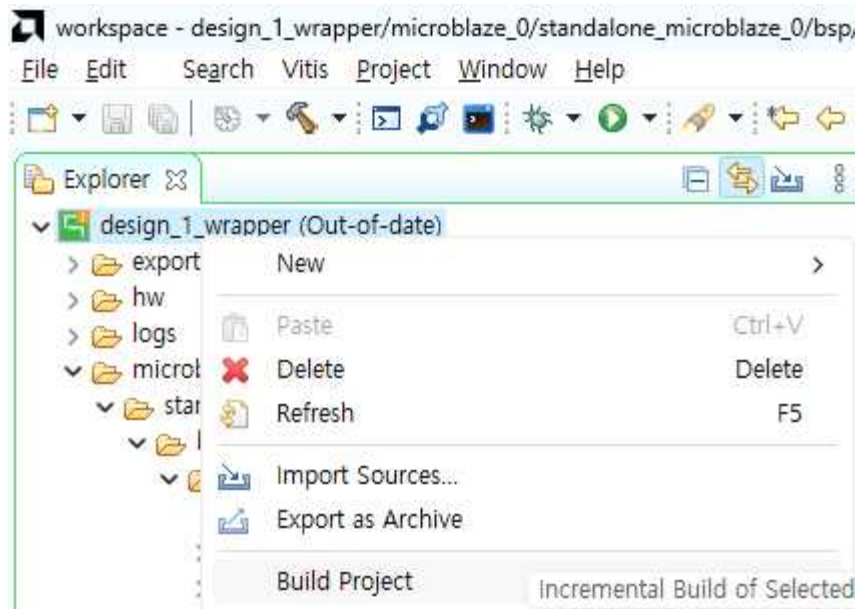
Build Console [design_1_wrapper]

"Compiling myip_led4..."

```
ccl.exe: fatal error: *.c: Invalid argument
compilation terminated.
make[2]: *** [Makefile:18: libs] Error 1
make[1]: *** [Makefile:46: microblaze_0/libsrc/myip_led4_v1_0/src/make.libs] Error 2
make: *** [Makefile:18: all] Error 2
Failed to build the bsp sources for domain - standalone_microblaze_0
Failed to generate the platform.
Reason: Failed to build the bsp sources for domain - standalone_microblaze_0
```



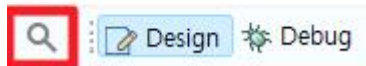
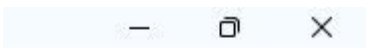
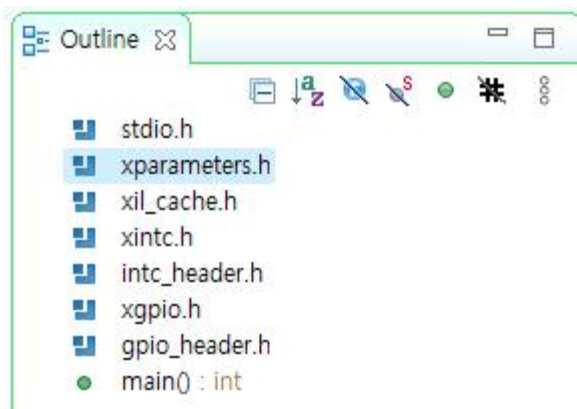
복사 후 저장해 줍니다.



```

37 int main ()
38 {
39     static XIntc intc;
40     Xil_ICacheEnable();
41     Xil_DCacheEnable();
42     print("---Entering main---\n\r");
43
44     *(unsigned int *)XPAR_GPIO_0_BASEADDR = 0xff;
45     *(unsigned int *)XPAR_MYIP_LED4_0_S00_AXI_BASEADDR = 0xff;
46
47     unsigned int * tcReg = (unsigned int *)XPAR_MYIP_TIMER_0_S00_AXI_BASEADDR;
48     tcReg[0] = (1<<31)|(100000000-1); // tc0.top
49     tcReg[1] = 100000000/2-1; // tc0.cmp

```

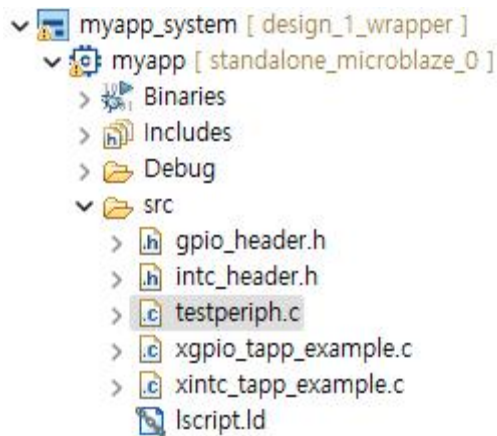


창이 없을 경우 돋보기를 눌러 Outline을 검색하여 추가한다.

```

652 /* Definitions for driver MYIP_TCOUNTER */
653 #define XPAR_MYIP_TCOUNTER_NUM_INSTANCES 1
654
655 /* Definitions for peripheral MYIP_TCOUNTER_0 */
656 #define XPAR_MYIP_TCOUNTER_0_DEVICE_ID 0
657 #define XPAR_MYIP_TCOUNTER_0_S00_AXI_BASEADDR 0x44A10000
658 #define XPAR_MYIP_TCOUNTER_0_S00_AXI_HIGHADDR 0x44A1FFFF

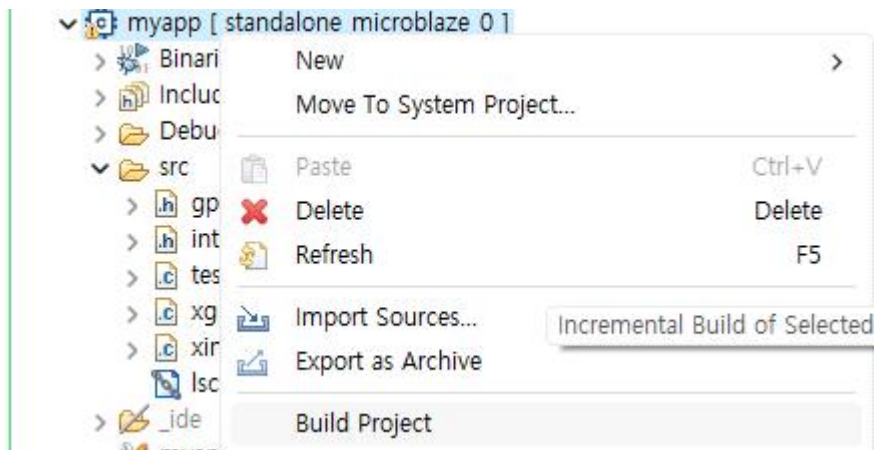
```



```

37 int main ()
38 {
39     static XIntc intc;
40     Xil_ICacheEnable();
41     Xil_DCacheEnable();
42     print("---Entering main---\n\r");
43
44     *(unsigned int *)XPAR_GPIO_0_BASEADDR = 0xff;
45     *(unsigned int *)XPAR_MYIP_LED4_0_S00_AXI_BASEADDR = 0xff;
46
47     unsigned int * tcReg = (unsigned int *)XPAR_MYIP_TCOUNT_0_S00_AXI_BASEADDR;
48     tcReg[0] = (1<<31)|(100000000-1); // tc0.top
49     tcReg[1] = 100000000/2-1; // tc0.cmp
50
51     {

```



Console Problems Vitis Log Guidance

Build Console [myapp, Debug]

'Invoking: MicroBlaze gcc linker'
mb-gcc -Wl,-T -Wl,../src/lscrip.ld -LC:/Users/edu/work
'Finished building target: myapp.elf'
' '
'Invoking: MicroBlaze Print Size'
mb-size myapp.elf |tee "myapp.elf.size"
text data bss dec hex filename
4768 320 3280 8368 20b0 myapp.elf
'Finished building: myapp.elf.size'
' '

22:05:12 Build Finished (took 1s.324ms)

myapp_system [design 1 wranner 1]

myapp

Bina

Inclu

Deb

src

g

ir

ti

x

x

ls

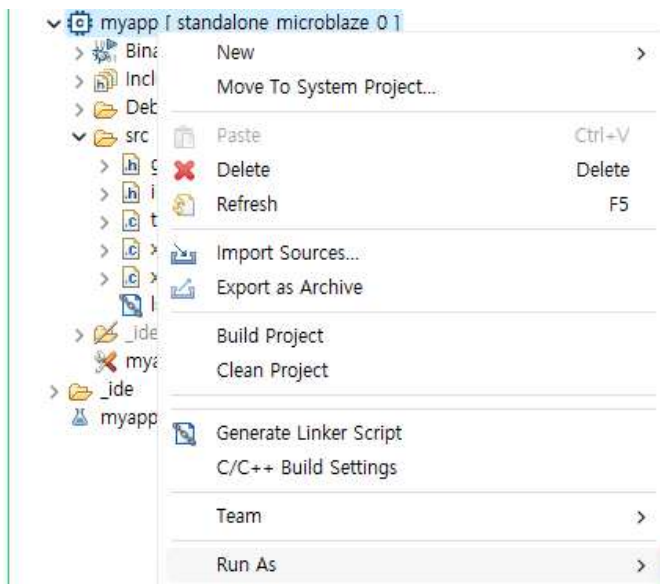
_ide

mya

_ide

myapp

New
Add Application Project...
Add Library Project...
Paste Ctrl+V
Delete Delete
Refresh F5
Import Sources...
Export as Archive
Close System Project
Build Project
Clean Project
Program Device



```

63 unsigned int * tcReg
64 tcReg[0] = (1<<31)|(.
65 tcReg[1] = 100000000,
66
67 {
68     int status;
69
70     print("\r\n Runni
71
72     status = IntcSelf:
73
74     if (status == 0)
75         print("IntcSel:
76     }
77     else {
78         print("IntcSel:
79     }
80 }
81
82 {

```

1 Launch Hardware (Single Application Debug)

```

36 #include "gpio_header.h"
37
38 typedef struct _MYIP_TIMER {
39     volatile uint32_t slv_reg0;
40     volatile uint32_t slv_reg1;
41     volatile uint32_t slv_reg2;
42     volatile uint32_t slv_reg3;
43     volatile uint32_t slv_reg4;
44     volatile uint32_t slv_reg5;
45     volatile uint32_t slv_reg6;
46     volatile uint32_t slv_reg7;
47     volatile uint32_t slv_reg8;
48     volatile uint32_t slv_reg9;
49     volatile uint32_t slv_reg10;
50     volatile uint32_t slv_reg11;
51 } MYIP_TIMER;
52
53 int main ()

```

```

53 int main ()
54 {
55     static XIntc intc;
56     Xil_ICacheEnable();
57     Xil_DCacheEnable();
58     print ("---Entering main---\n\r");
59
60     *(unsigned int *)XPAR_GPIO_0_BASEADDR = 0xff;
61     *(unsigned int *)XPAR_MYIP_LED4_0_S00_AXI_BASEADDR = 0xff;
62
63     unsigned int * tcReg = (unsigned int *)XPAR_MYIP_TCOUNT_0_S00_AXI_BASEADDR;
64     tcReg[0] = (1<<31)|(100000000-1); // tc0.top
65     tcReg[1] = 100000000/2-1; // tc0.cmp
66
67     MYIP_TIMER * myip_timer = (MYIP_TIMER *)XPAR_MYIP_TCOUNT_0_S00_AXI_BASEADDR;
68     myip_timer->slv_reg2 = (1<<31)|(100000000-1);
69     myip_timer->slv_reg3 = (100000000/2-1);
70
71     {

```