Lecture 3: CMOS Transistor Theory

# Outline

- ❑ Introduction
- ❑ MOS Capacitor
- ❑ nMOS I-V Characteristics
- ❑ pMOS I-V Characteristics
- ❑ Gate and Diffusion Capacitance
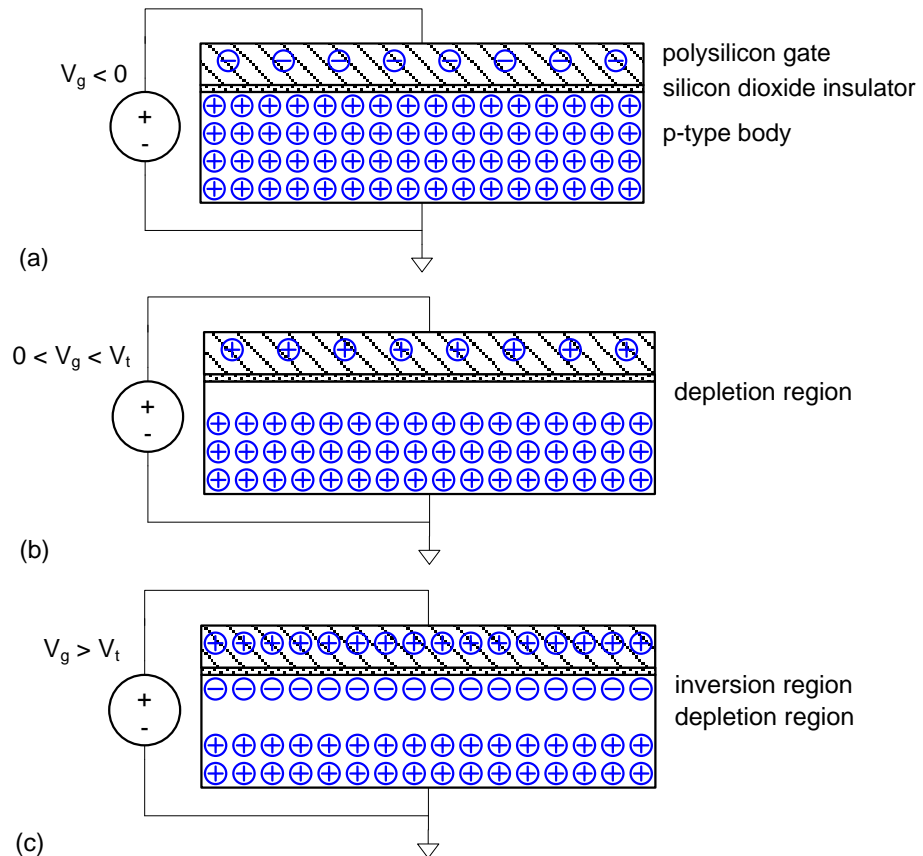
Introduction

❑ So far, we have treated transistors as ideal switches

❑ An ON transistor passes a finite amount of current
  – Depends on terminal voltages
  – Derive current-voltage (I-V) relationships

❑ Transistor gate, source, drain all have capacitance
  – I = C ($\Delta V / \Delta t$) -> Δt = (C/I) ΔV
  – Capacitance and current determine speed
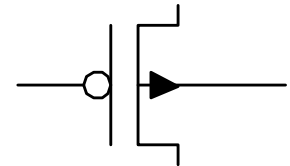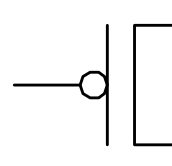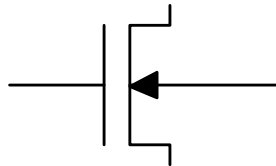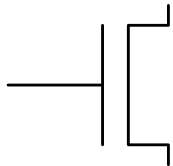
MOS Capacitor

- ❏ Gate and body form MOS capacitor
- ❏ Operating modes
  - – Accumulation
  - – Depletion
  - – Inversion

$V_g < 0$

polysilicon gate
silicon dioxide insulator
p-type body

(a)

$0 < V_g < V_t$

depletion region

(b)

$V_g > V_t$

inversion region
depletion region

(c)

Terminal Voltages

- ❑ Mode of operation depends on V_g, V_d, V_s
  - – $V_{gs} = V_g - V_s$
  - – $V_{gd} = V_g - V_d$
  - – $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- ❑ Source and drain are symmetric diffusion terminals
  - – By convention, source is terminal at lower voltage
  - – Hence $V_{ds} \geq 0$
- ❑ nMOS body is grounded. First assume source is 0 too.
- ❑ Three regions of operation
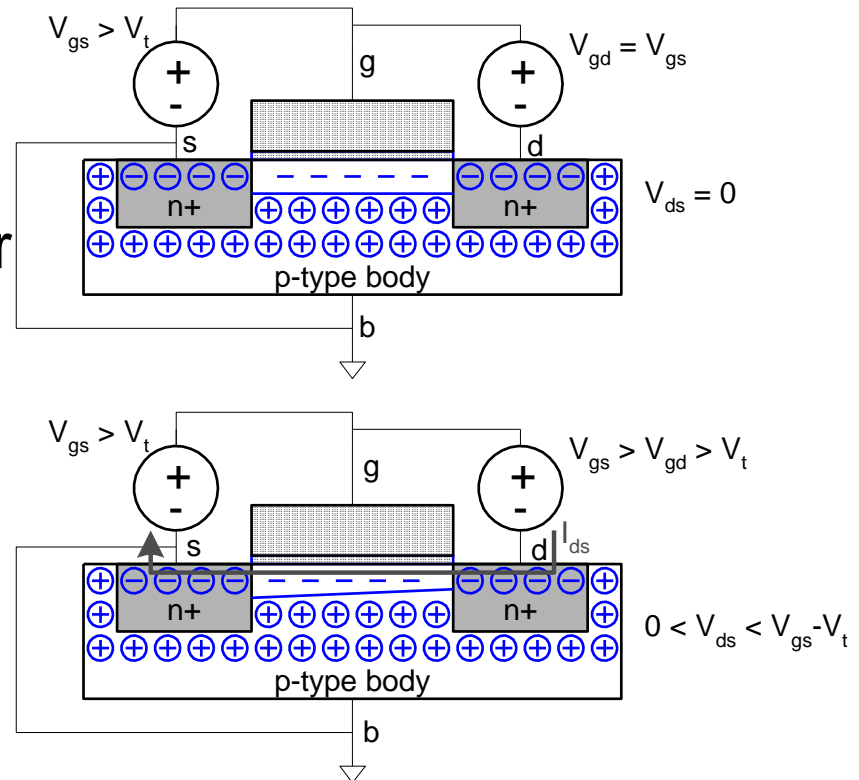 - – *Cutoff*
  - – *Linear*
  - – *Saturation*
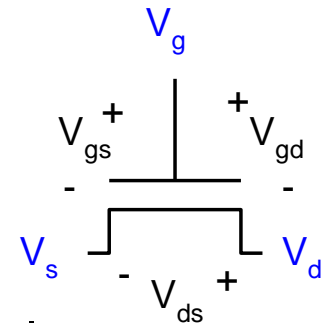
nMOS Cutoff

❑ No channel

❑ $I_{ds} \approx 0$
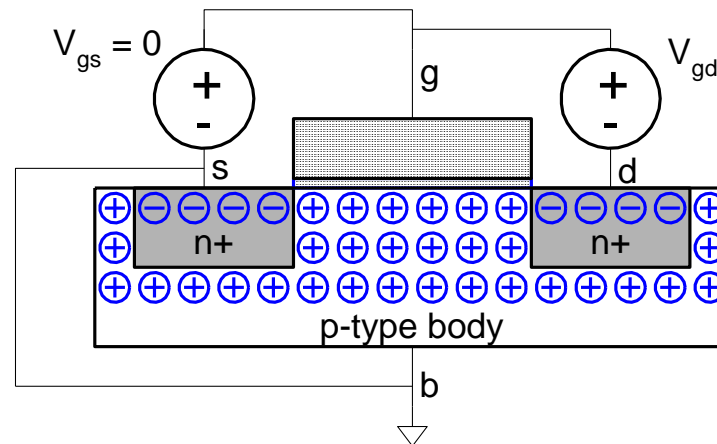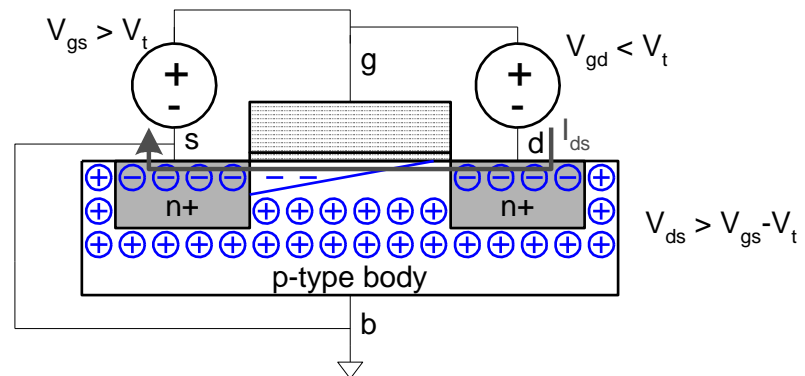
nMOS Linear

- ❑ Channel forms
- ❑ Current flows from d to s
  - – e⁻ from s to d
- ❑ I_{ds} increases with V_{ds}
- ❑ Similar to linear resistor

$V_{gs} > V_t$

$V_{gd} = V_{gs}$

+ -

+ -

g

s

d

n+

n+

$V_{ds} = 0$

p-type body

b

$V_{gs} > V_t$

$V_{gs} > V_{gd} > V_t$

+ -

+ -

g

s

d

I_{ds}

n+

n+

$0 < V_{ds} < V_{gs} - V_t$

p-type body

b

nMOS Saturation

❑ Channel pinches off

❑ I_{ds} independent of V_{ds}

❑ We say current *saturates*

❑ Similar to current source

$V_{gs} > V_t$ g $V_{gd} < V_t$

s   d I_{ds}

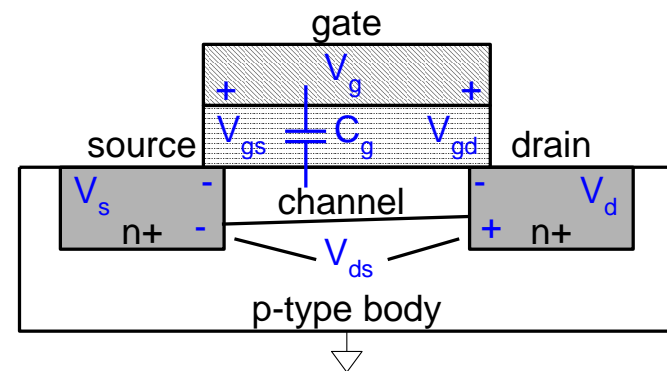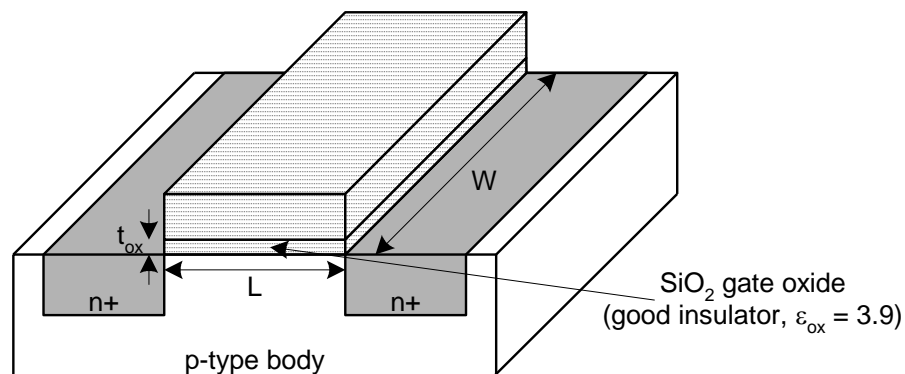n+   n+ $V_{ds} > V_{gs}-V_t$

p-type body

b

I-V Characteristics

❑ In Linear region, I_{ds} depends on
   – How much charge is in the channel?
   – How fast is the charge moving?

Channel Charge

- ❑ MOS structure looks like parallel plate capacitor while operating in inversions
    - – Gate – oxide – channel
- ❑ $Q_{channel} =$
- ❑ :
- ❑

W

t_{ox}

L

n+   n+

p-type body

SiO$_2$ gate oxide
(good insulator, ε_{ox} = 3.9)

gate

V_g

+   +

source V_{gs} C_g V_{gd} drain

V_s -   channel   - V_d

n+   -   +   n+
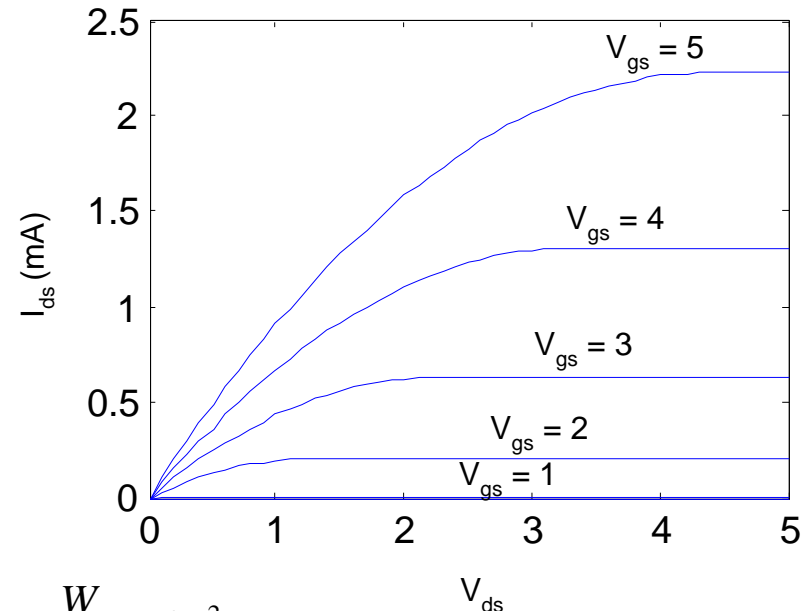
V_{ds}

p-type body

nMOS I-V Summary

❑ *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta\left(V_{gs} - V_t - \dfrac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \dfrac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

Example

❑ We will be using a 0.6 μm process for your project
  – From AMI Semiconductor
  – t_{ox} = 100 Å
  – μ = 350 cm^2/V*s
  – V_t = 0.7 V
❑ Plot I_{ds} vs. V_{ds}
  – V_{gs} = 0, 1, 2, 3, 4, 5
  – Use W/L = 4/2 λ

$$\beta = \mu C_{ox} \frac{W}{L} = (350)\left(\frac{3.9 \times 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}}\right)\left(\frac{W}{L}\right) = 120 \frac{W}{L} \mu\text{A/V}^2$$

pMOS I-V

❑ All dopings and voltages are inverted for pMOS
  – Source is the more positive terminal
❑ Mobility μ_p is determined by holes
  – Typically 2-3x lower than that of electrons μ_n
  – 120 cm^2/V•s in AMI 0.6 μm process
❑ Thus pMOS must be wider to provide same current
 – In this class, assume
    $\mu_n / \mu_p = 2$
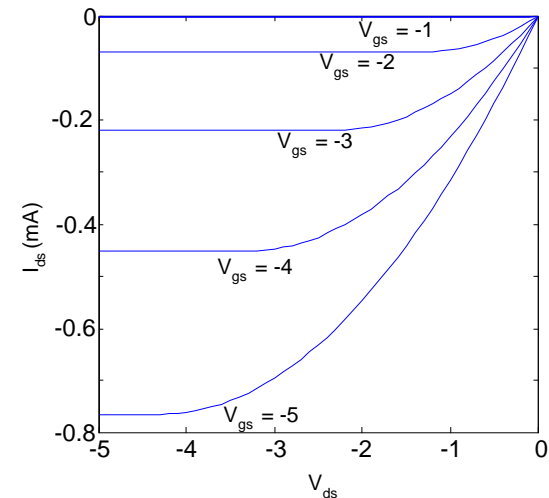
Capacitance

- ❑ Any two conductors separated by an insulator have capacitance

- ❑ Gate to channel capacitor is very important
  - – Creates channel charge necessary for operation

- ❑ Source and drain have capacitance to body
  - – Across reverse-biased diodes
  - – Called diffusion capacitance because it is associated with source/drain diffusion

Gate Capacitance

❑ Approximate channel as connected to source

❑ $C_{gs} = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL = C_{permicron}W$

❑ $C_{permicron}$ is typically about 2 fF/μm

W

t_{ox}

L

n+

n+

p-type body

SiO$_2$ gate oxide
(good insulator, $\varepsilon_{ox} = 3.9\varepsilon_0$)
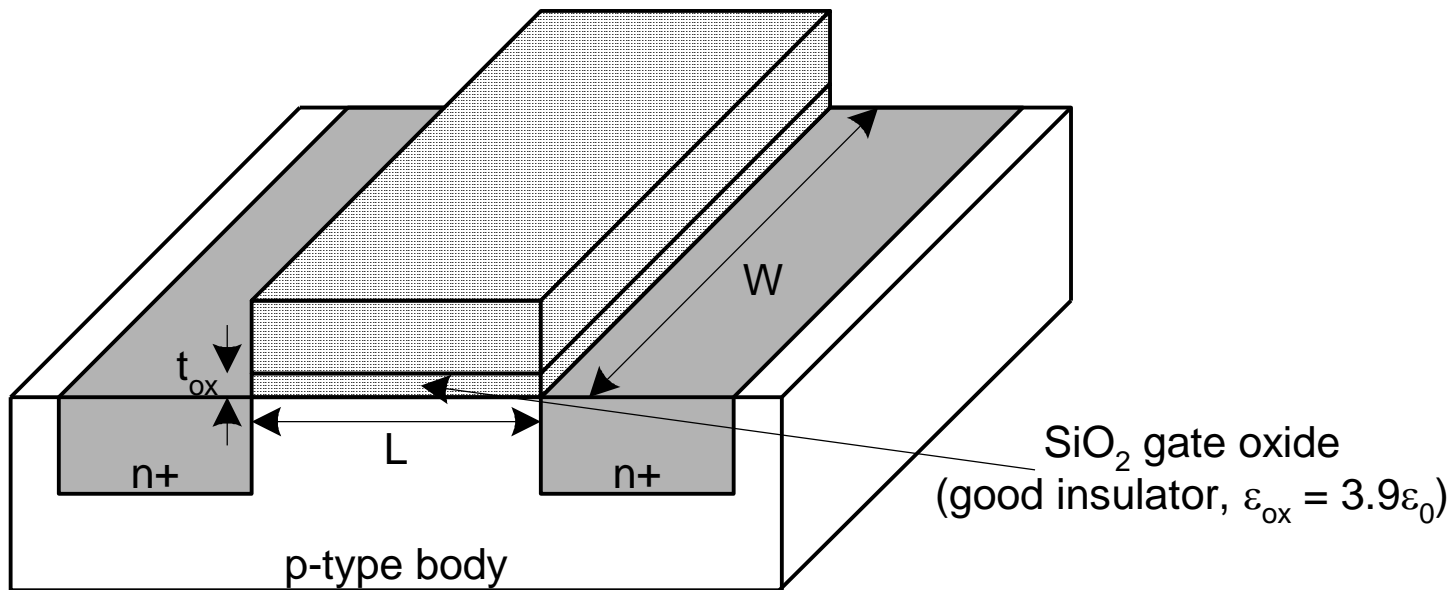
Diffusion Capacitance

- C_{sb}, C_{db}
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to C_g for contacted diff
  - ½ C_g for uncontacted
  - Varies with process