

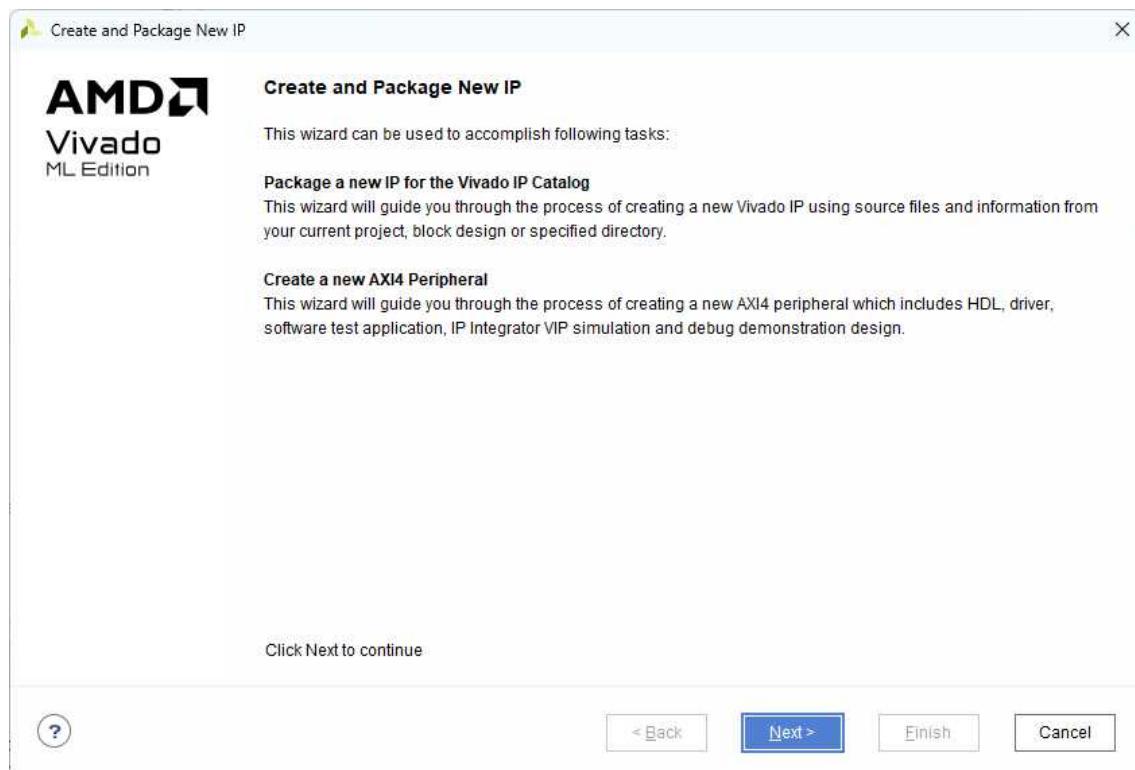
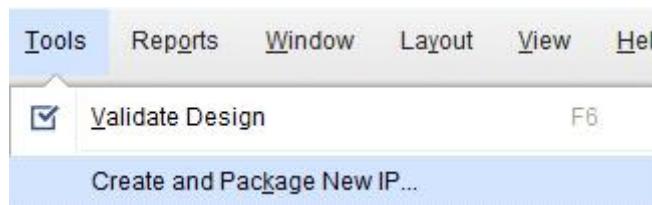
TCounter 모듈 추가하기

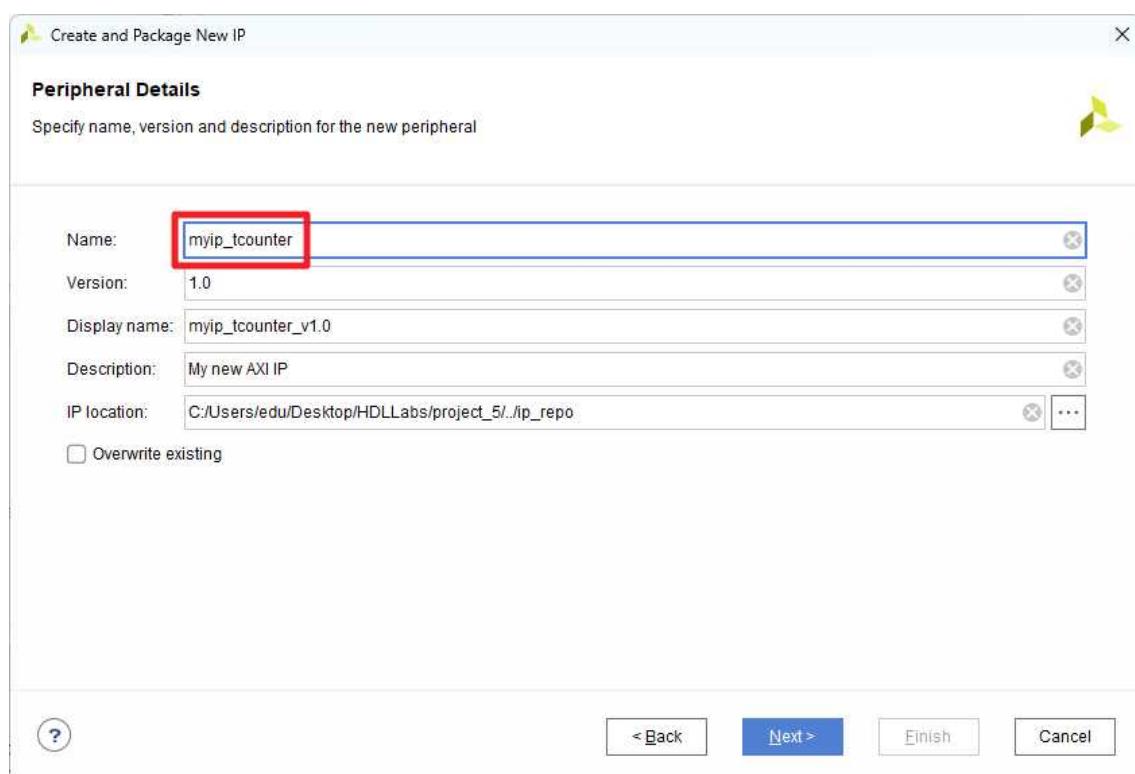
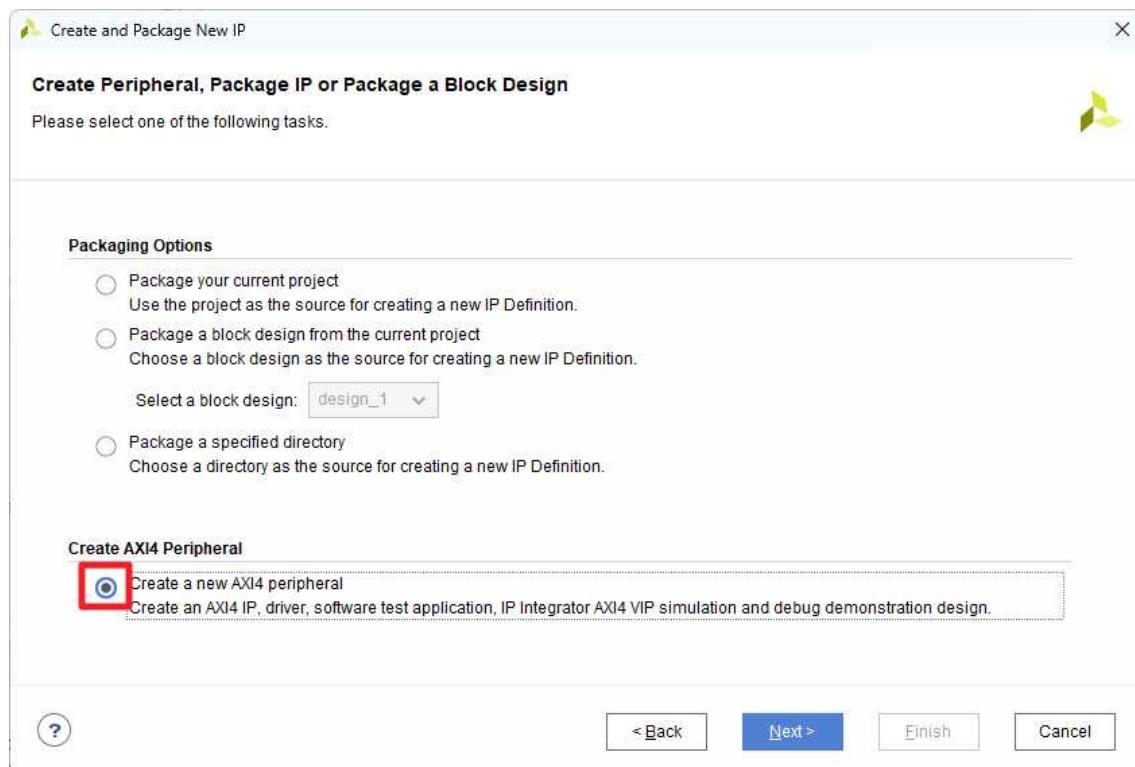
▼ IP INTEGRATOR

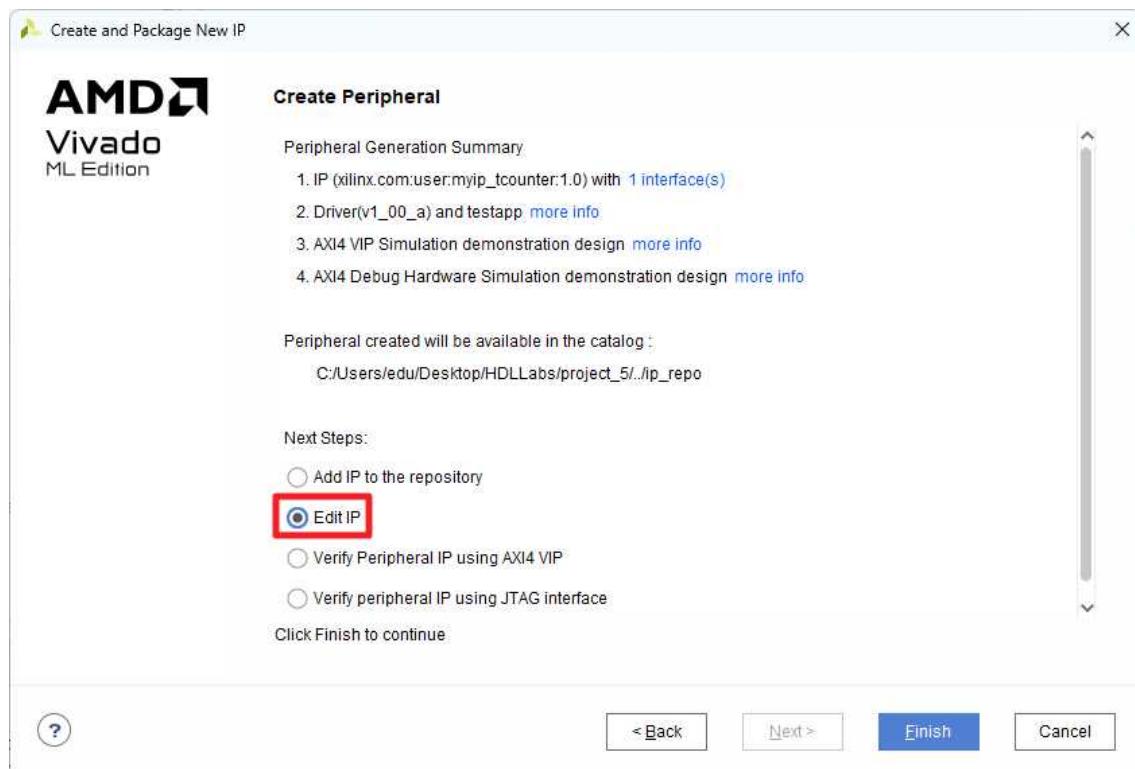
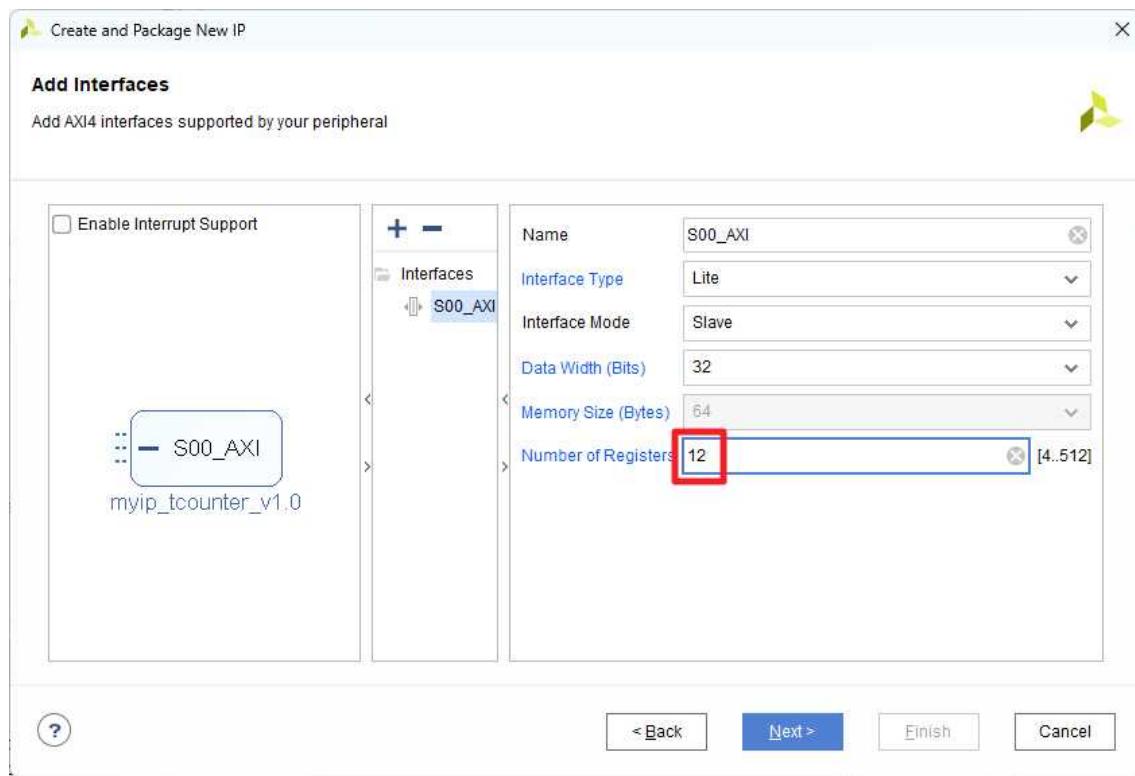
[Create Block Design](#)

[Open Block Design](#)

[Generate Block Design](#)







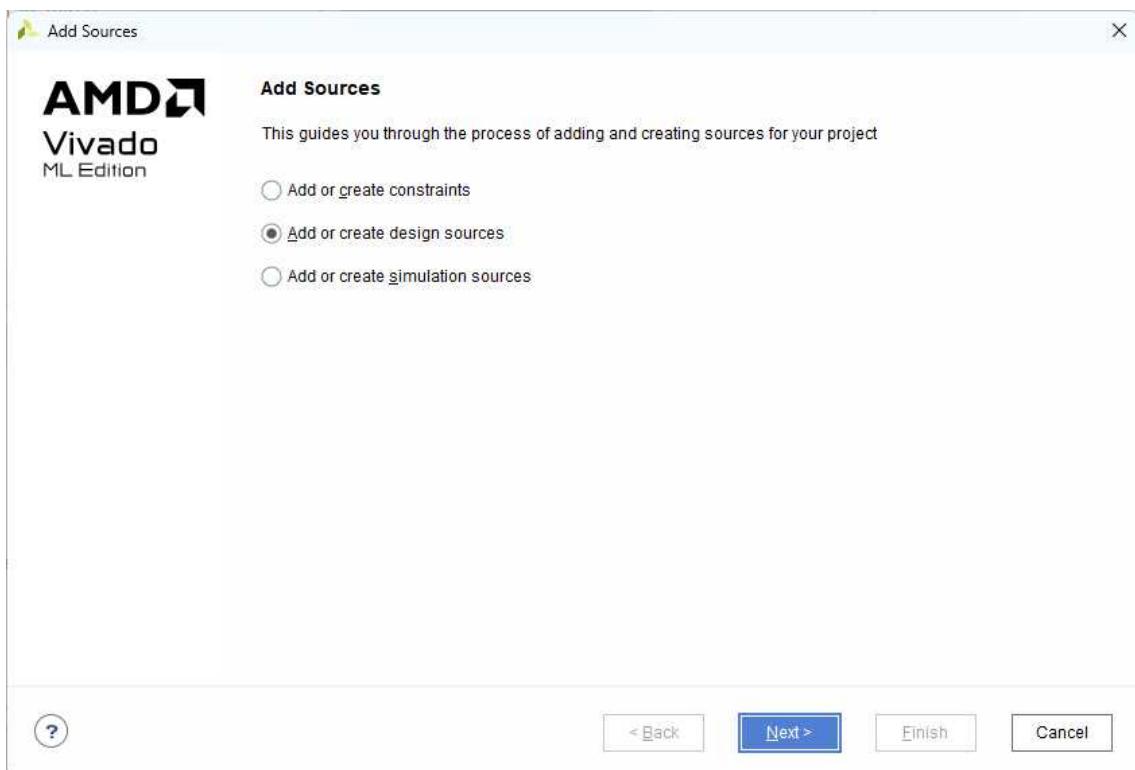


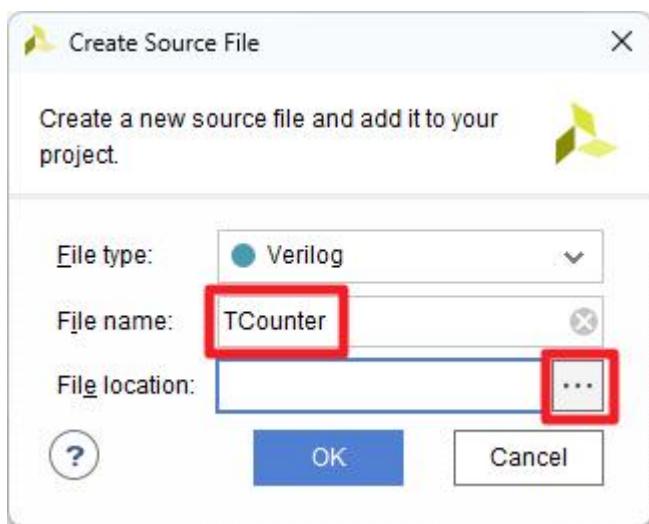
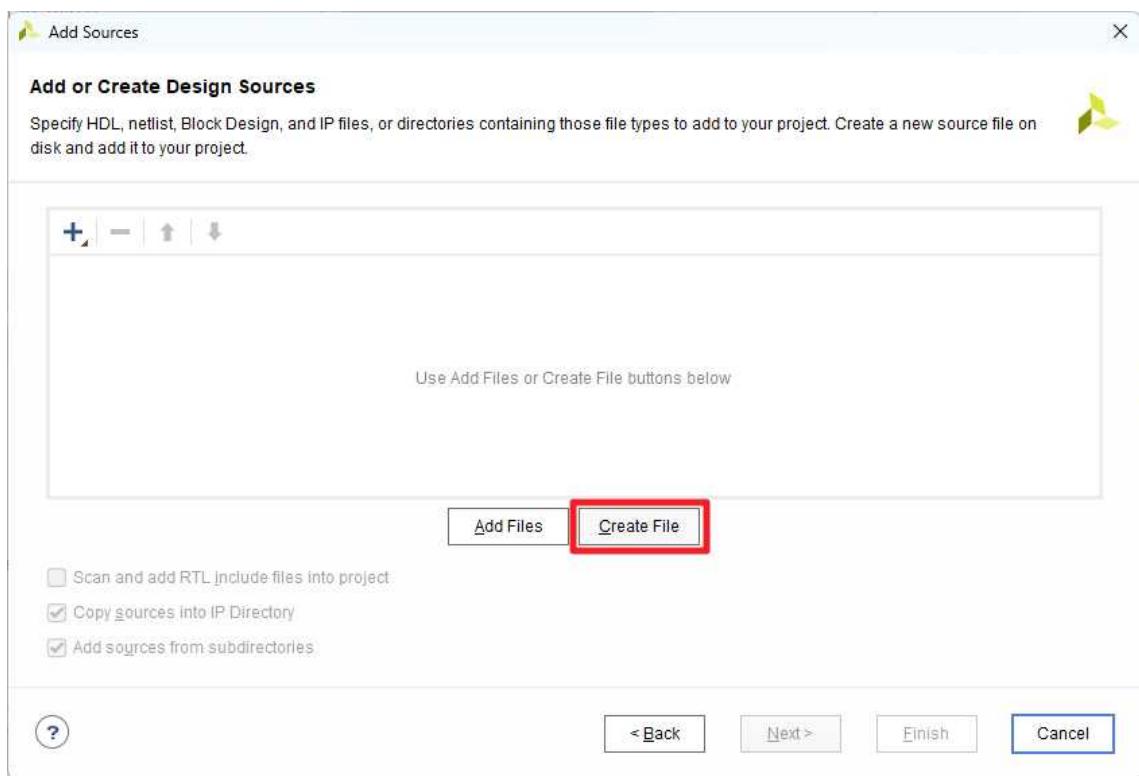
▼ PROJECT MANAGER

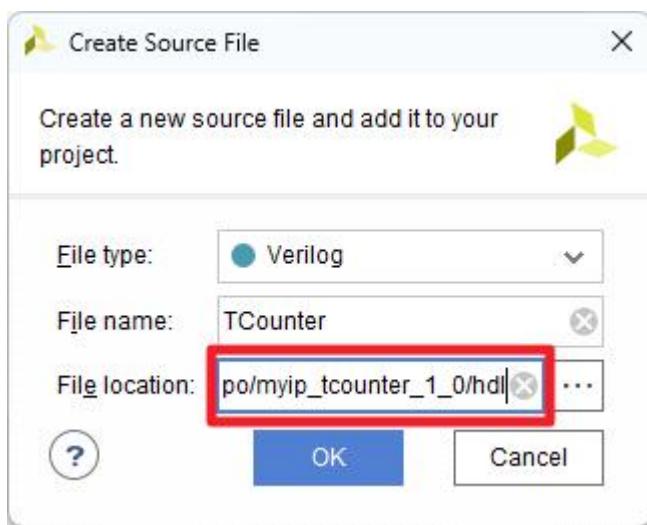
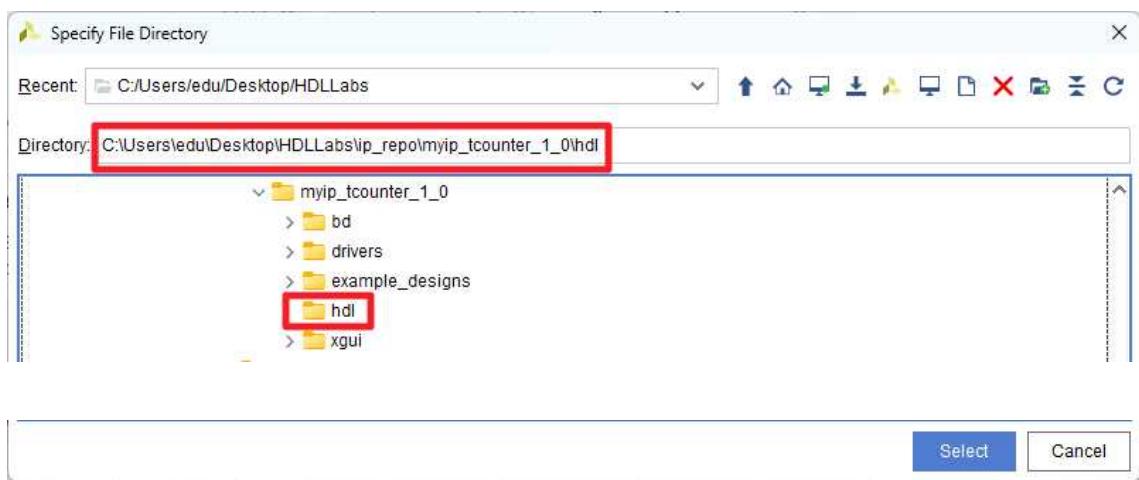
Settings

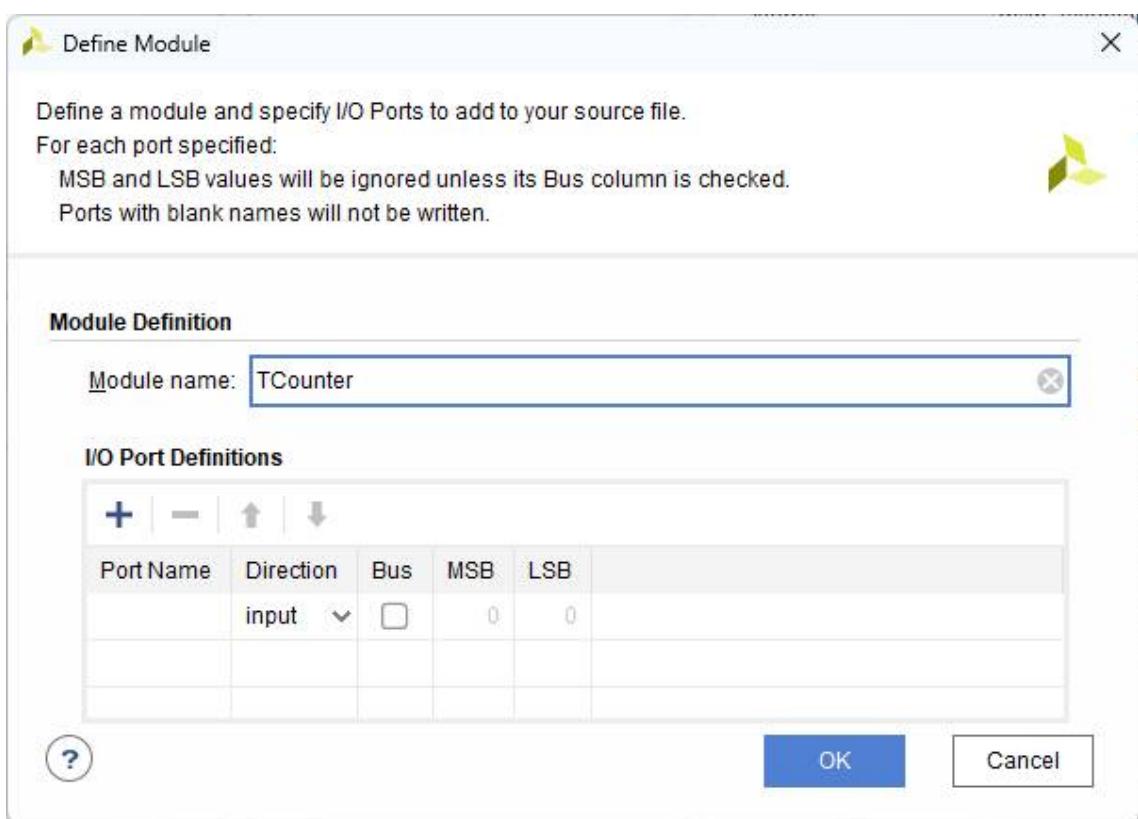
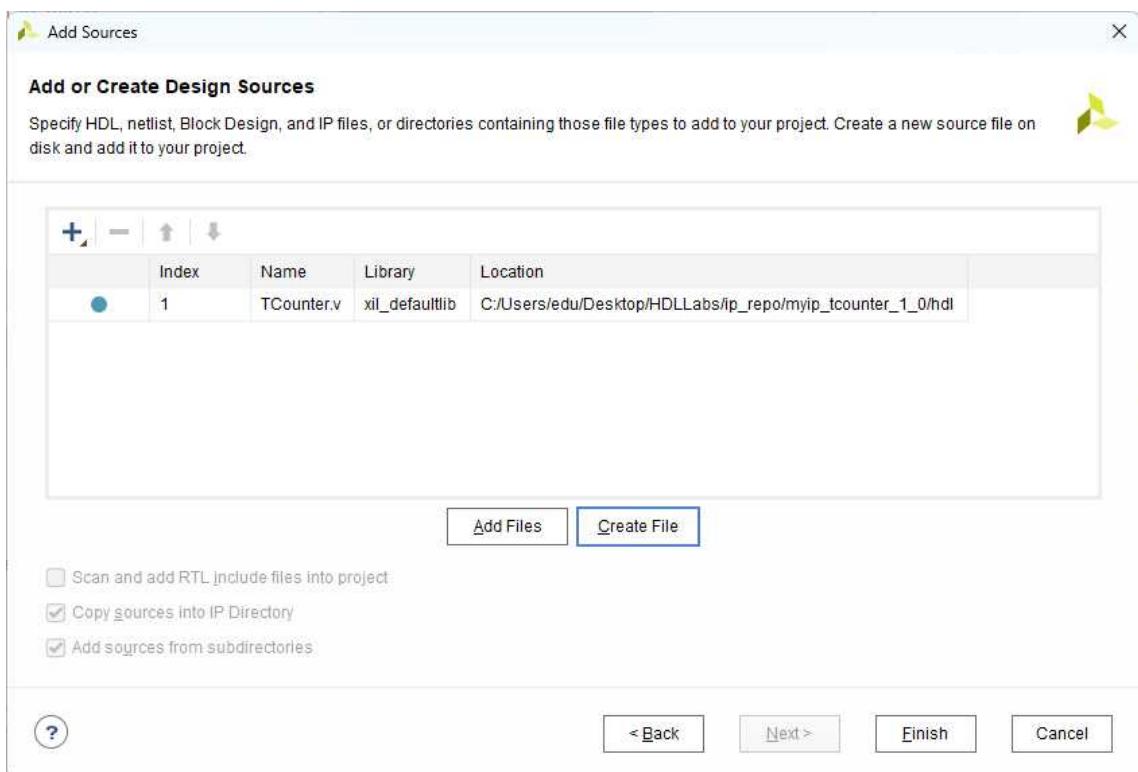
[Add Sources](#)

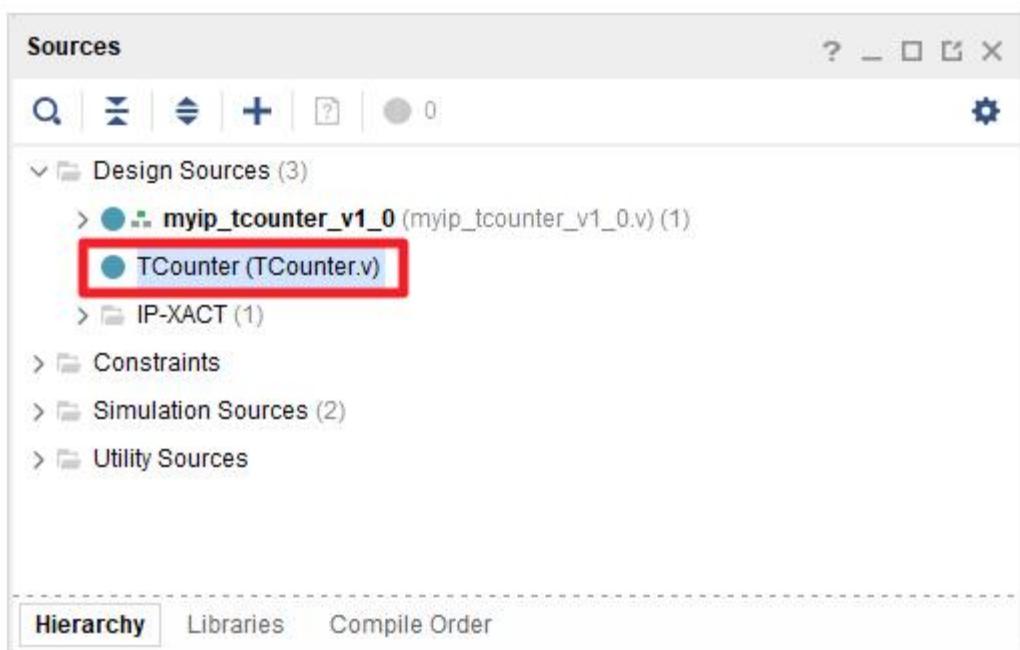
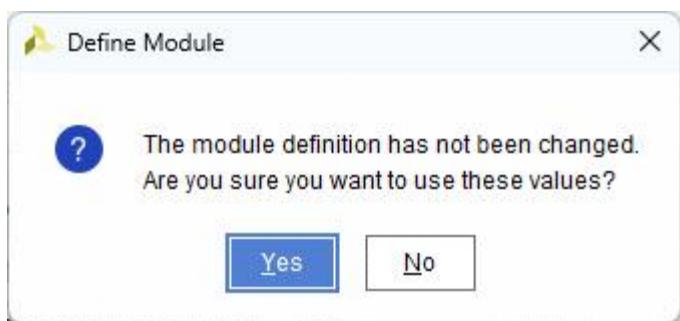
Language Templates











```
module TCounter(
    input CLK,
    input RSTn,
    input [31:0] top_in, // en, 4bit reserved, 27bit top
    input [31:0] cmp_in, // 5bit reserved, 27bit cmp
    output PWM
);

    reg [26:0] cnt; // 27bit
    wire [26:0] top = top_in[26:0];
    wire [26:0] cmp = cmp_in[26:0];
    wire cnt_en = top_in[31];
    always @(posedge CLK)
        begin : CNT_MOD
            if(RSTn==0) cnt<=0;
            else if(cnt_en) cnt = top;
            else if(cmp>cnt) cnt = cmp;
        end
endmodule
```

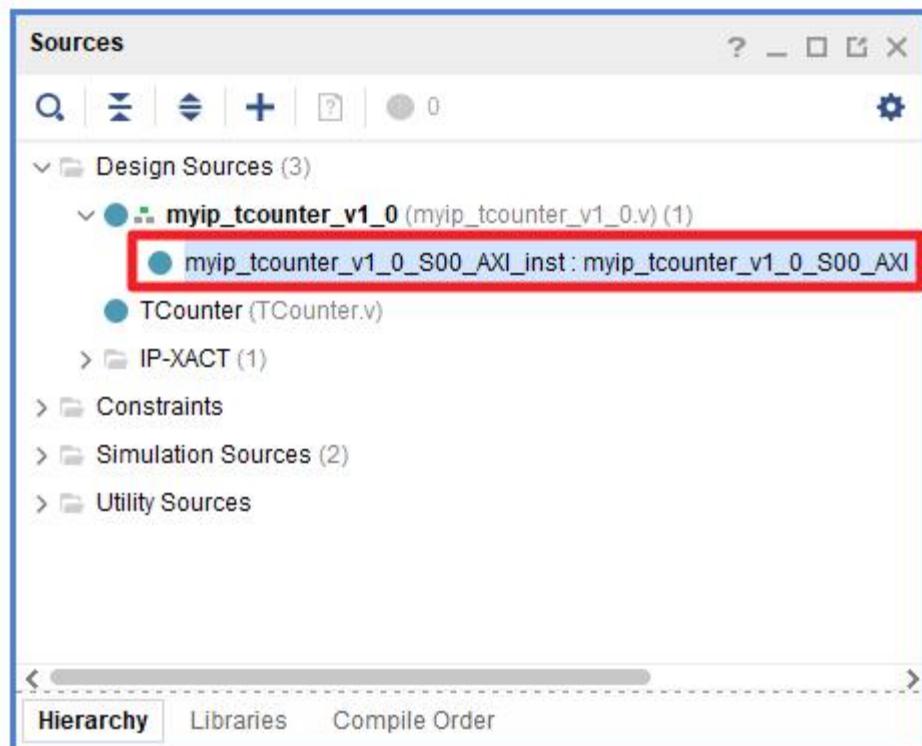
```

        else if(cnt_en) begin
            cnt<=cnt+1;
            if(cnt >= top)
                cnt <= 0;
        end
        else cnt<=0;
    end

    assign PWM = (cnt < cmp)?1:0;

endmodule

```



```

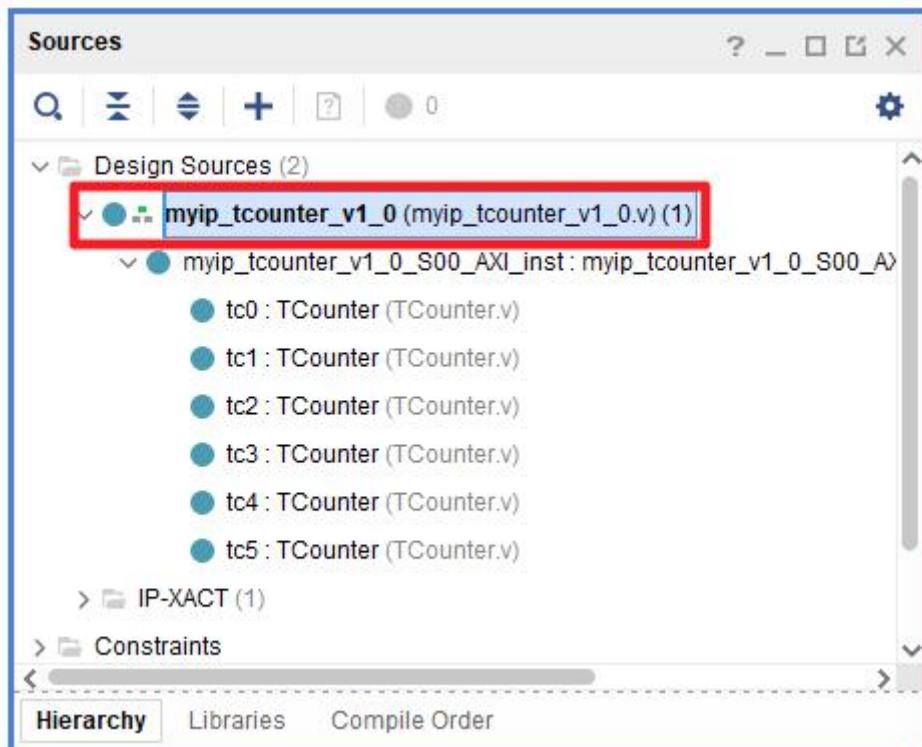
17      // Users to add ports here
18      output [5:0] PWM,
19      // User ports ends

```

```

488 // Add user logic here
489 TCounter tc0(S_AXI_ACLK,S_AXI_ARESETN,slv_reg0,slv_reg1,PWM[0]);
490 TCounter tc1(S_AXI_ACLK,S_AXI_ARESETN,slv_reg2,slv_reg3,PWM[1]);
491 TCounter tc2(S_AXI_ACLK,S_AXI_ARESETN,slv_reg4,slv_reg5,PWM[2]);
492 TCounter tc3(S_AXI_ACLK,S_AXI_ARESETN,slv_reg6,slv_reg7,PWM[3]);
493 TCounter tc4(S_AXI_ACLK,S_AXI_ARESETN,slv_reg8,slv_reg9,PWM[4]);
494 TCounter tc5(S_AXI_ACLK,S_AXI_ARESETN,slv_reg10,slv_reg11,PWM[5]);
495 // User logic ends

```



```

17 // Users to add ports here
18 output [5:0] PWM,
19 // User ports ends

50 ) myip_tcounter_v1_0_S00_AXI_inst (
51 .PWM(PWM),
52 .S_AXI_ACLK(s00_axi_aclk),

```

Project Summary x Package IP - myip_tcounter x TCounter.v x myip_tcounter_v1_0_S00_AXI.v x myip_tcounter_v1_0.v >

Packaging Steps

- ✓ Identification
- ✓ Compatibility
- File Groups**
- ✗ Customization Parameters
- ✗ Ports and Interfaces
- ✓ Addressing and Memory
- ✗ Customization GUI
- ✗ Review and Package

File Groups

⚠ Merge changes from File Groups Wizard

Name	Library Name	Type	Is Include	File Group Name	Model Name
Standard			<input type="checkbox"/>		
Advanced			<input type="checkbox"/>		
Verilog Synthesis (2)			<input type="checkbox"/>	myip_tcounter_v1_0	
Verilog Simulation (2)			<input type="checkbox"/>	myip_tcounter_v1_0	
Software Driver (6)			<input type="checkbox"/>		
UI Layout (1)			<input type="checkbox"/>		
Block Diagram (1)			<input type="checkbox"/>		

Project Summary x Package IP - myip_tcounter x TCounter.v x myip_tcounter_v1_0_S00_AXI.v x myip_tcounter_v1_0.v >

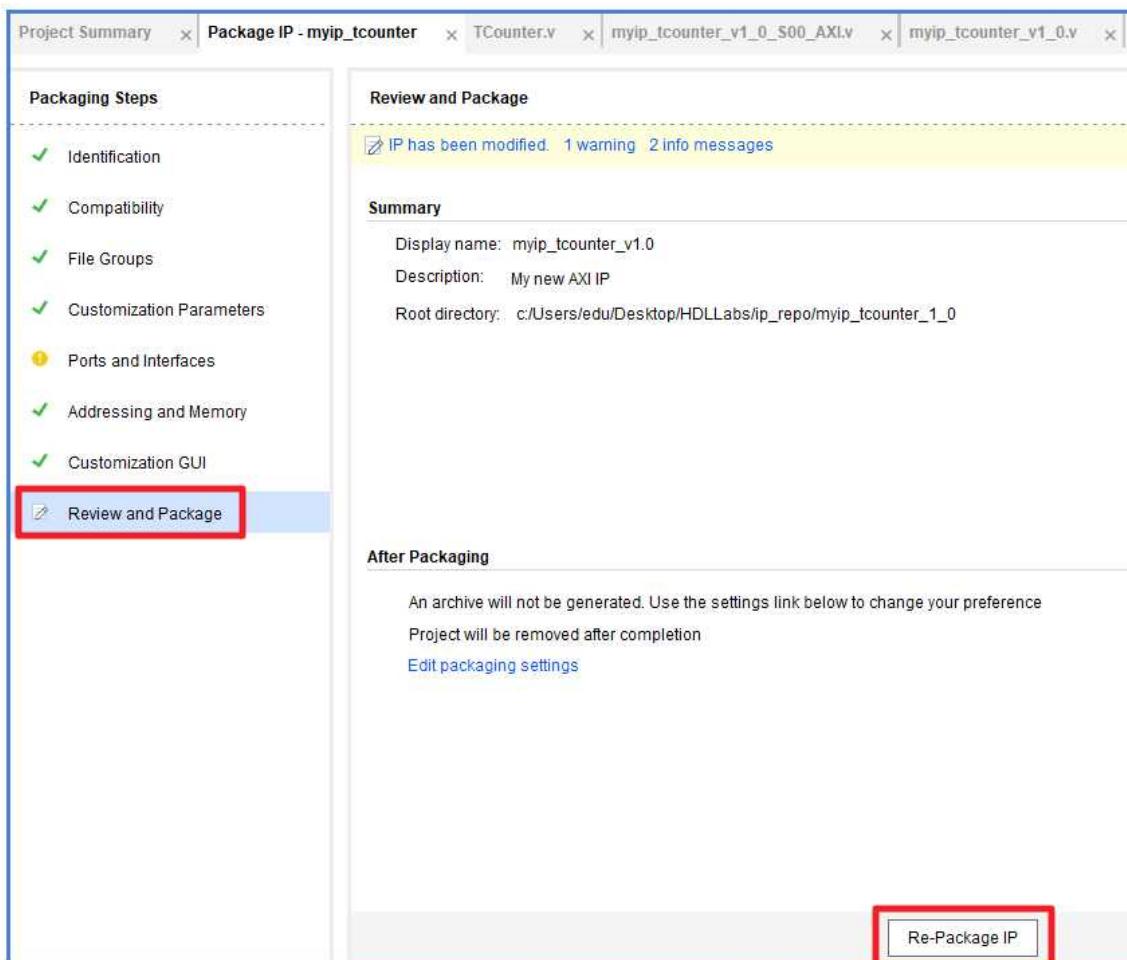
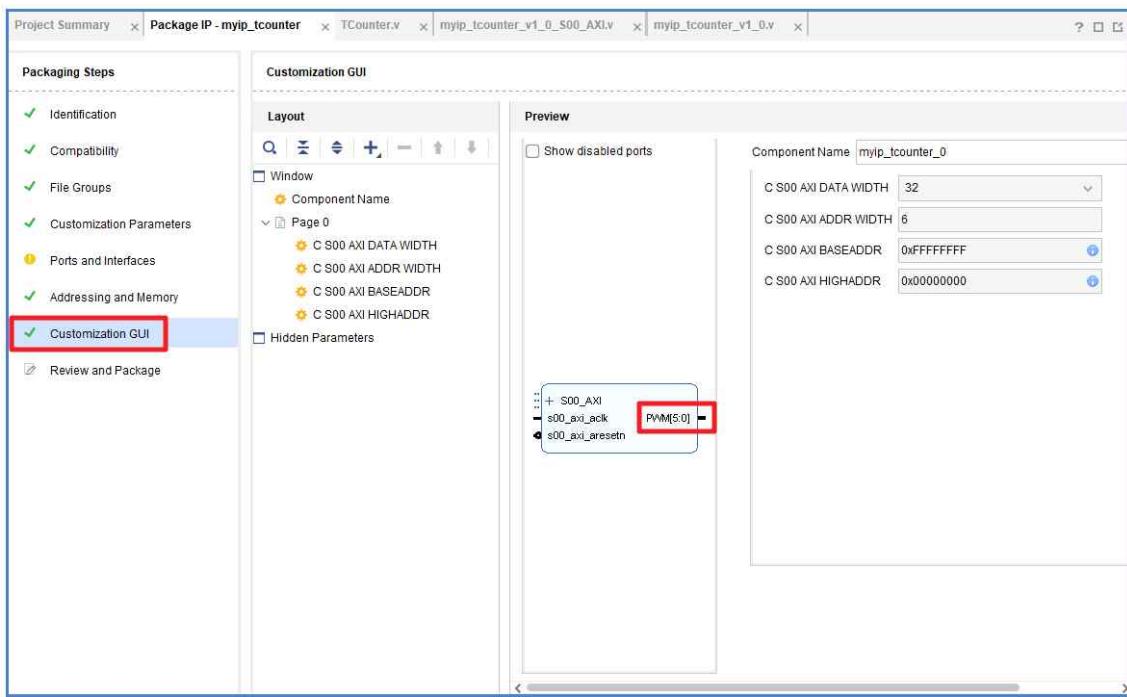
Packaging Steps

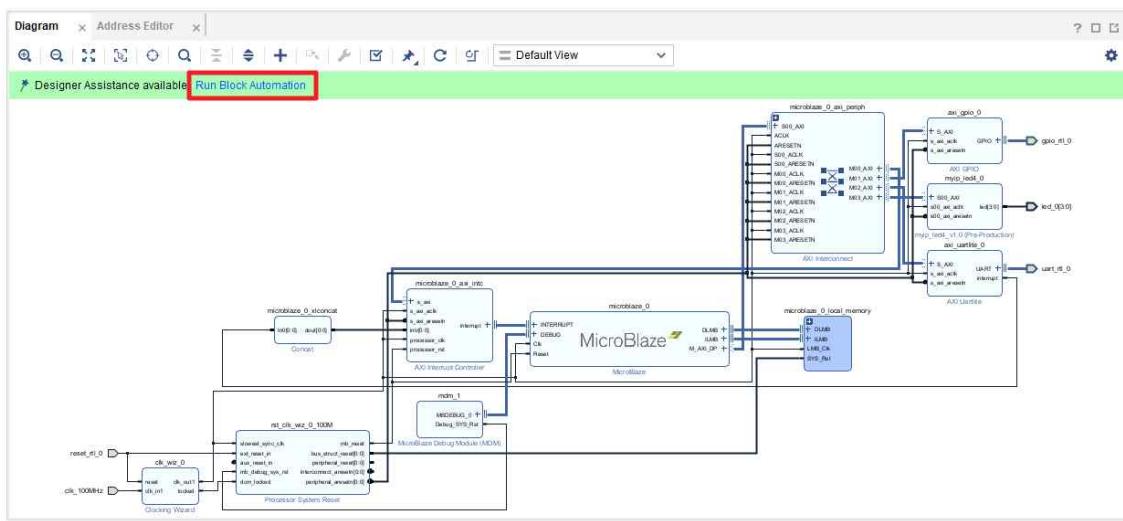
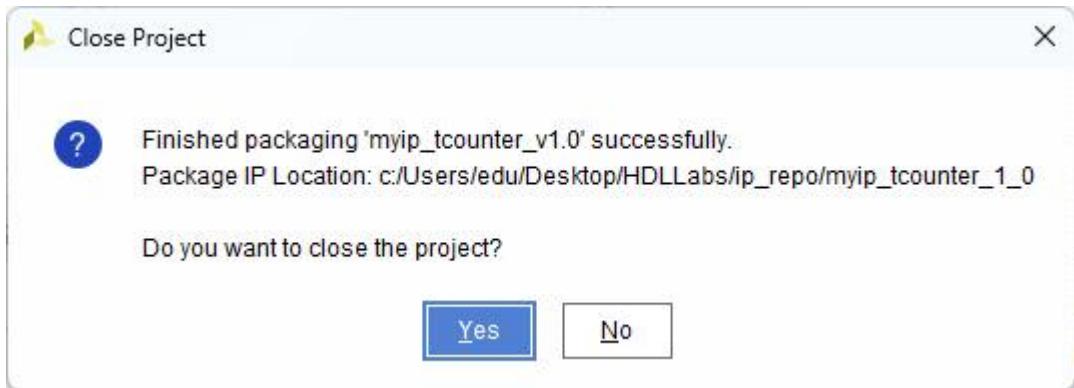
- ✓ Identification
- ✓ Compatibility
- ✓ File Groups
- Customization Parameters**
- ✗ Customization Parameters
- ✗ Ports and Interfaces
- ✓ Addressing and Memory
- ✗ Customization GUI
- ✗ Review and Package

Customization Parameters

⚠ Merge changes from Customization Parameters Wizard

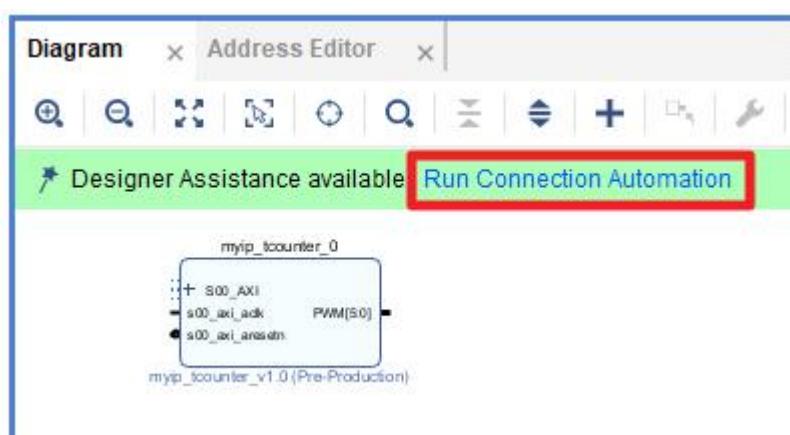
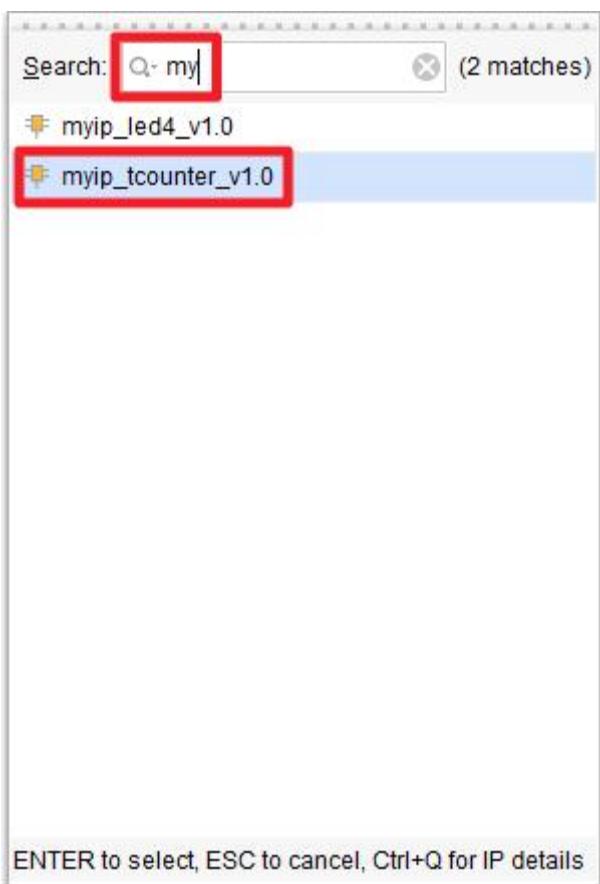
Name	Description	Display Name	Value	Value Bit String Length
C_S00_AXI_DATA_WIDTH	Width of S_AXI data bus	C S00 AXI DATA WIDTH	32	0
C_S00_AXI_ADDR_WIDTH	Width of S_AXI address bus	C S00 AXI ADDR WIDTH	6	0
C_S00_AXI_BASEADDR		C S00 AXI BASEADDR	0xFFFFFFFF	32
C_S00_AXI_HIGHADDR		C S00 AXI HIGHADDR	0x00000000	32

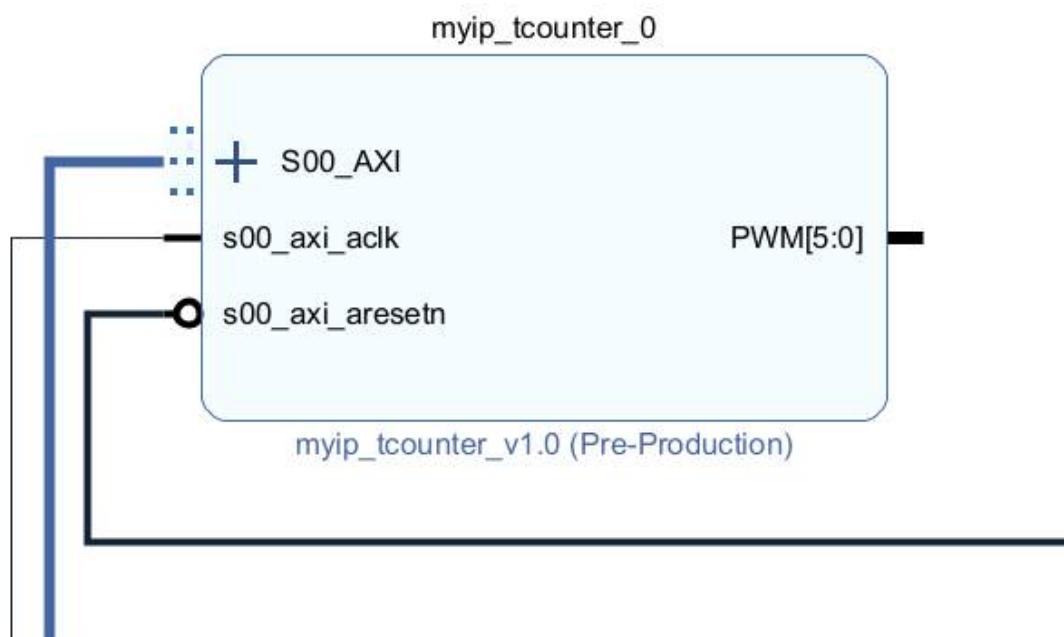
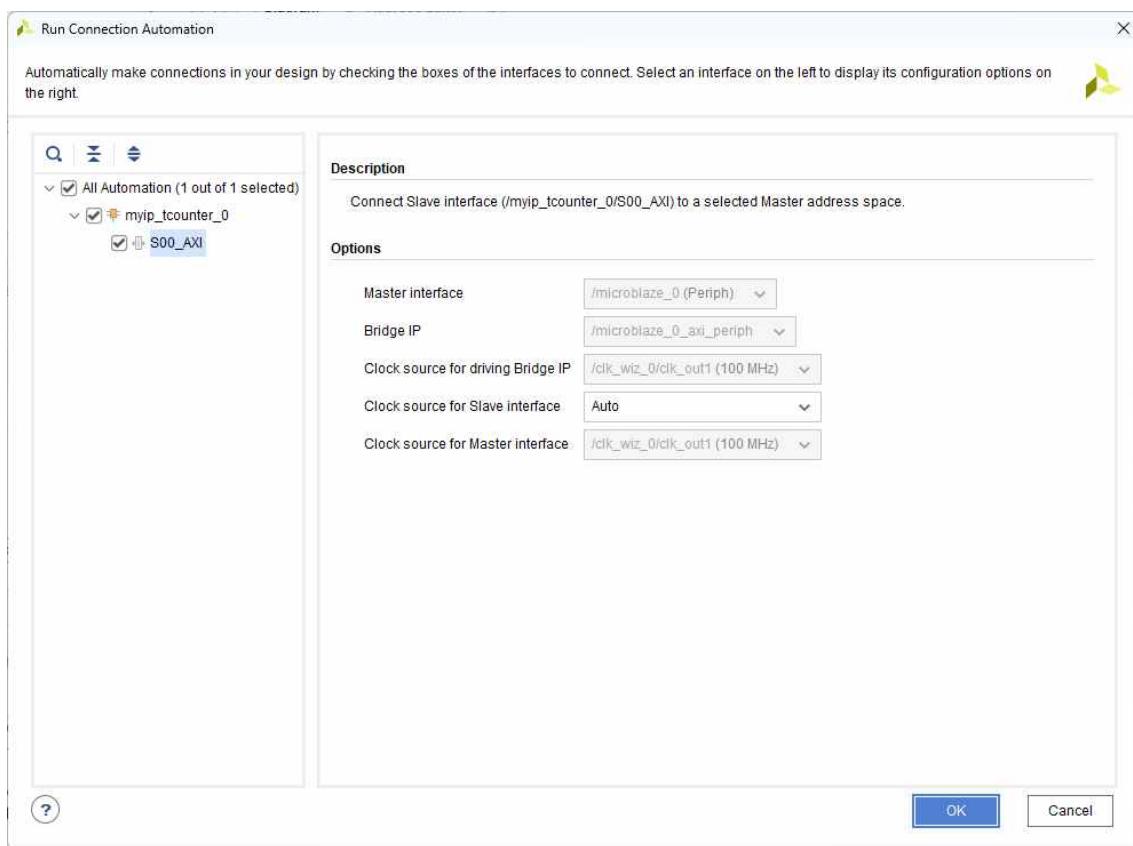


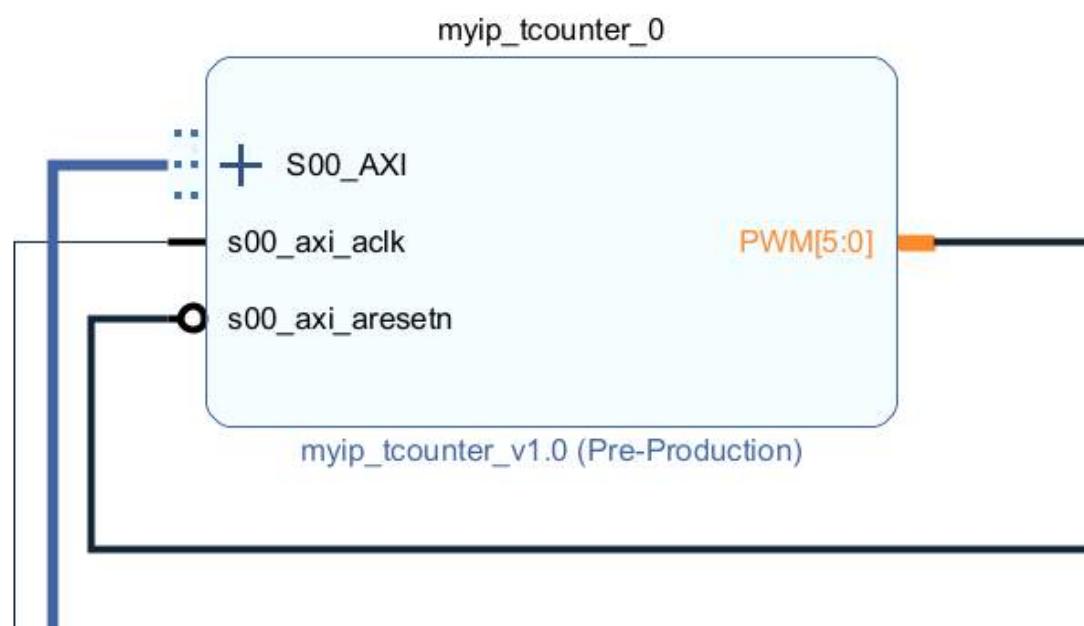
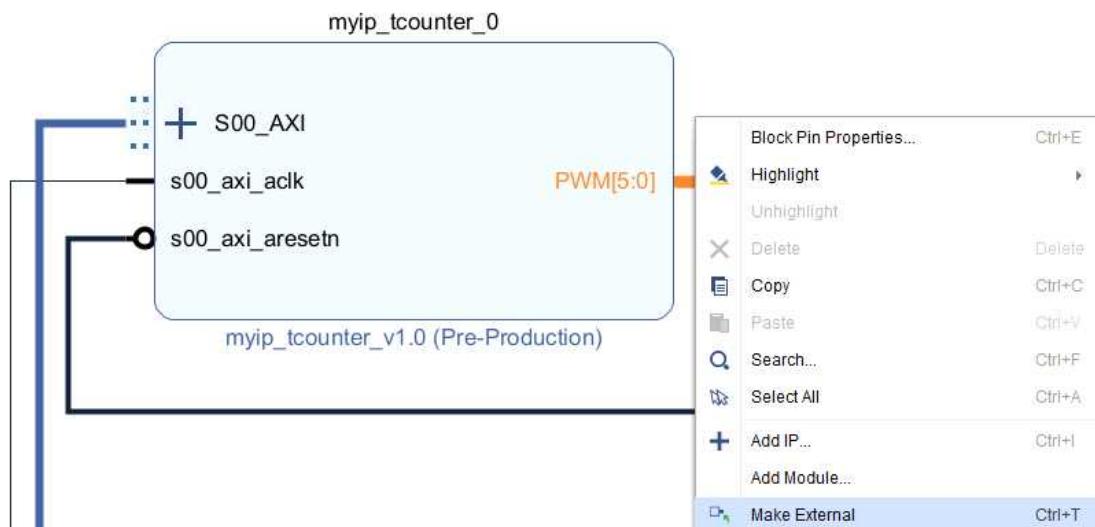


반응이 없으면 다음으로 넘어갑니다.

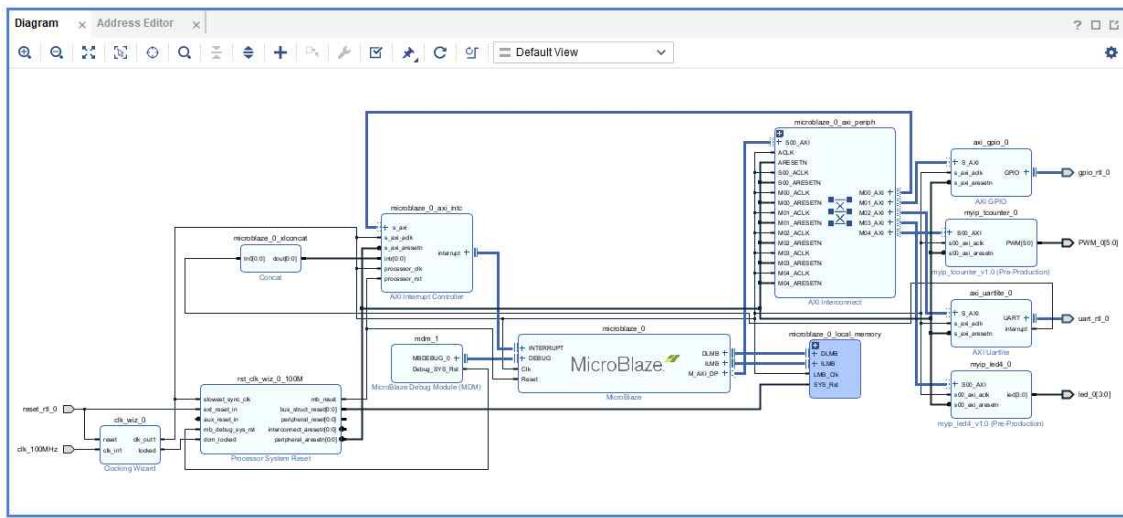








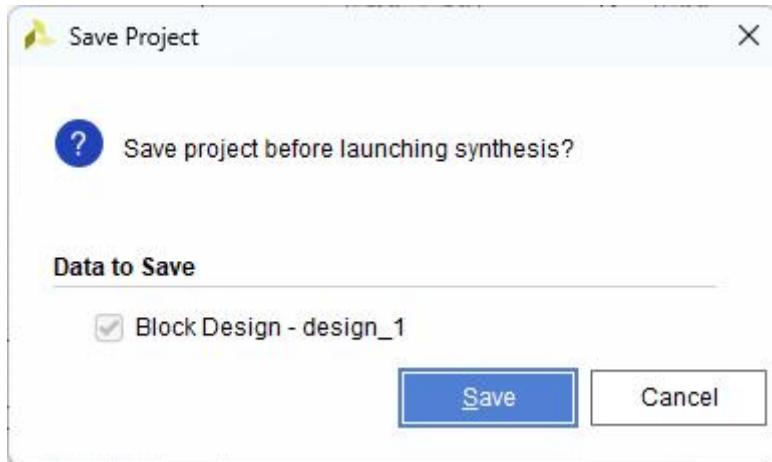
| C |



▼ SYNTHESIS

▶ [Run Synthesis](#)

➤ [Open Synthesized Design](#)



Synthesis Complete ✓

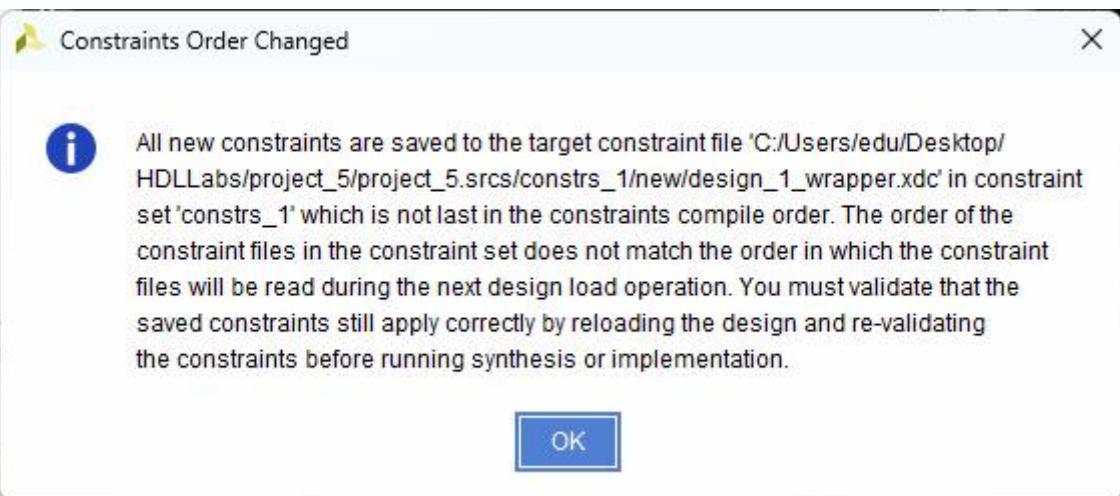
▼ SYNTHESIS

▶ [Run Synthesis](#)

➤ [Open Synthesized Design](#)

I/O Ports

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
All ports (18)						
> CLK.CLK_100MHZ_54576 (1)	IN			<input checked="" type="checkbox"/>	34	LVC MOS33*
> gpio_rtl_0_54576 (4)	OUT			<input checked="" type="checkbox"/>	14	LVC MOS33*
> RST.RESET_RTL_0_54576 (1)	IN			<input checked="" type="checkbox"/>	14	LVC MOS33*
> uart_rtl_0_54576 (2)	(Multiple)			<input checked="" type="checkbox"/>	16	LVC MOS33*
> led_0 (4)	OUT			<input checked="" type="checkbox"/>	14	LVC MOS33*
> PWM_0 (6)		OUT		<input checked="" type="checkbox"/>	(Multiple)	LVC MOS33*
<input checked="" type="checkbox"/> PWM_0[5]	OUT	L1		<input checked="" type="checkbox"/>	35	LVC MOS33*
<input checked="" type="checkbox"/> PWM_0[4]	OUT	P1		<input checked="" type="checkbox"/>	35	LVC MOS33*
<input checked="" type="checkbox"/> PWM_0[3]	OUT	N3		<input checked="" type="checkbox"/>	35	LVC MOS33*
<input checked="" type="checkbox"/> PWM_0[2]	OUT	P3		<input checked="" type="checkbox"/>	35	LVC MOS33*
<input checked="" type="checkbox"/> PWM_0[1]	OUT	U3		<input checked="" type="checkbox"/>	34	LVC MOS33*
<input checked="" type="checkbox"/> PWM_0[0]	OUT	W3		<input checked="" type="checkbox"/>	34	LVC MOS33*
Scalar ports (0)						

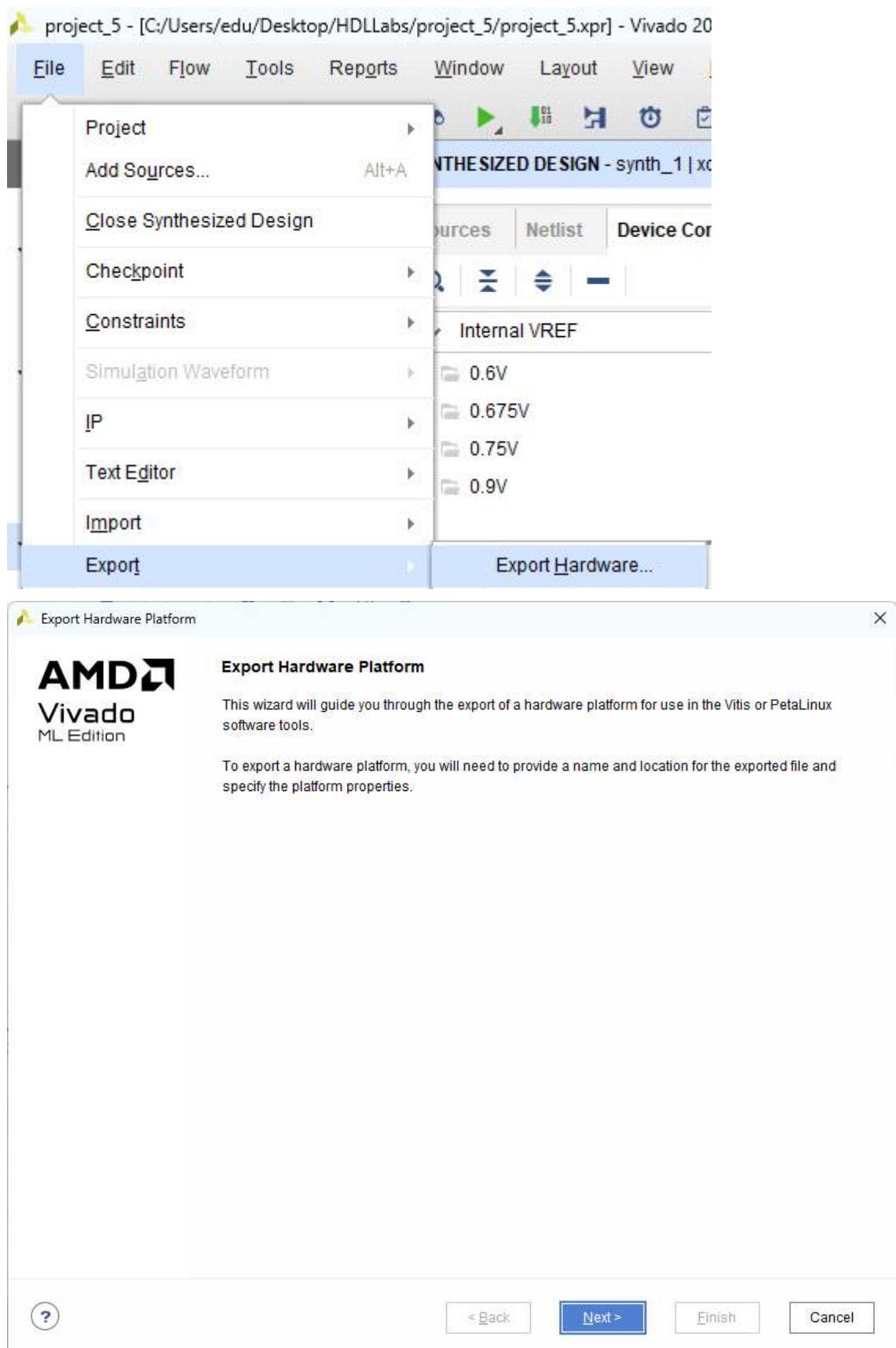


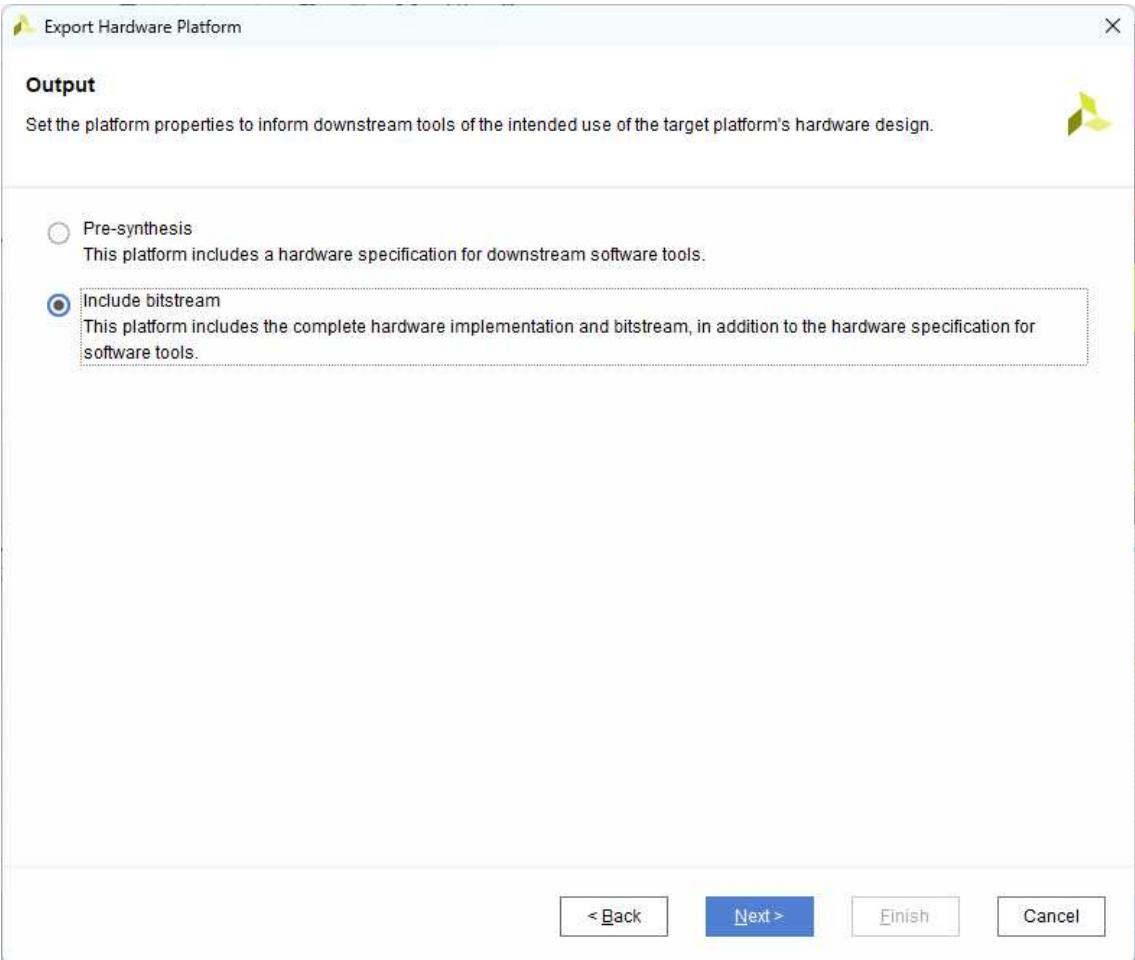
PROGRAM AND DEBUG

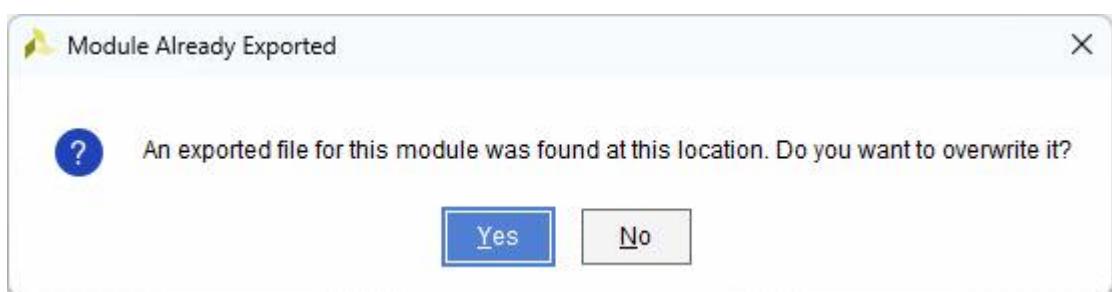
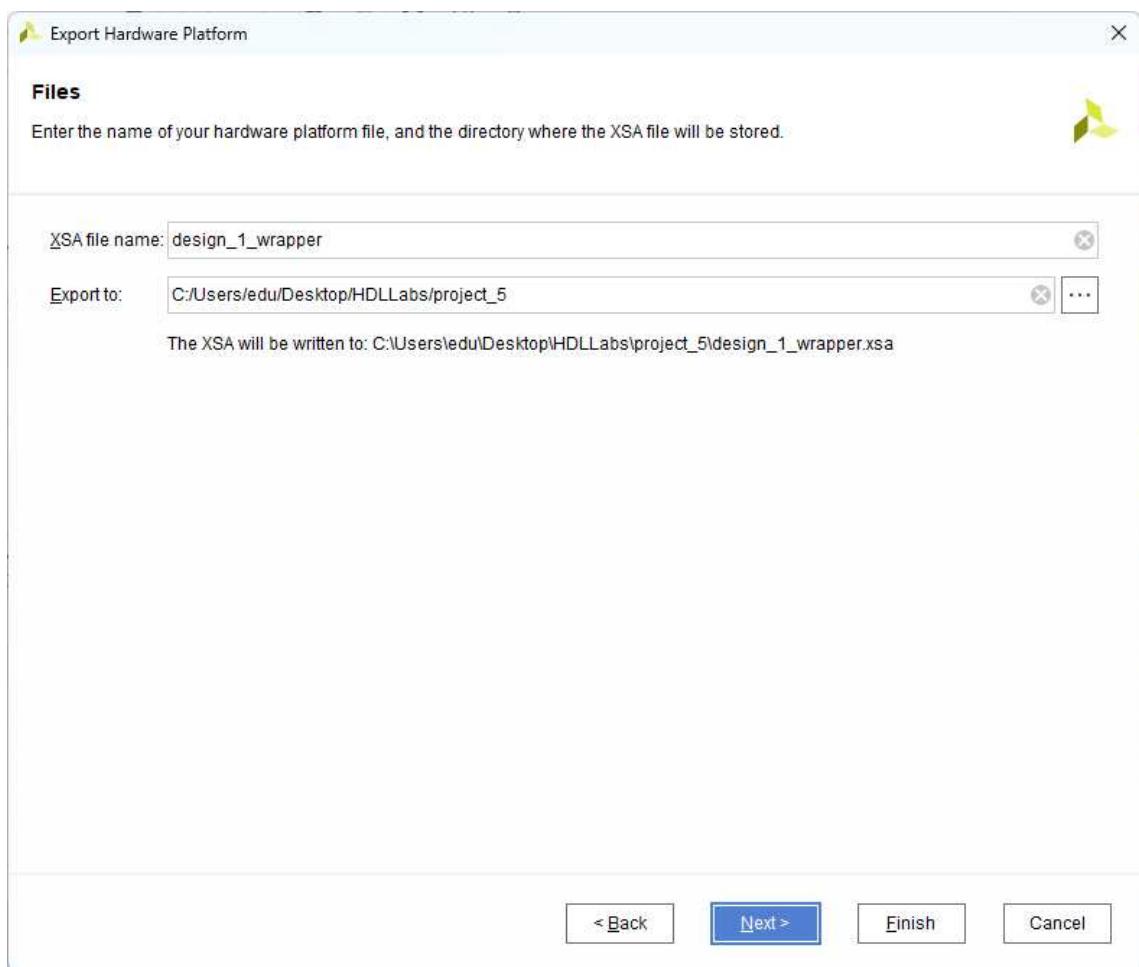
 [Generate Bitstream](#)

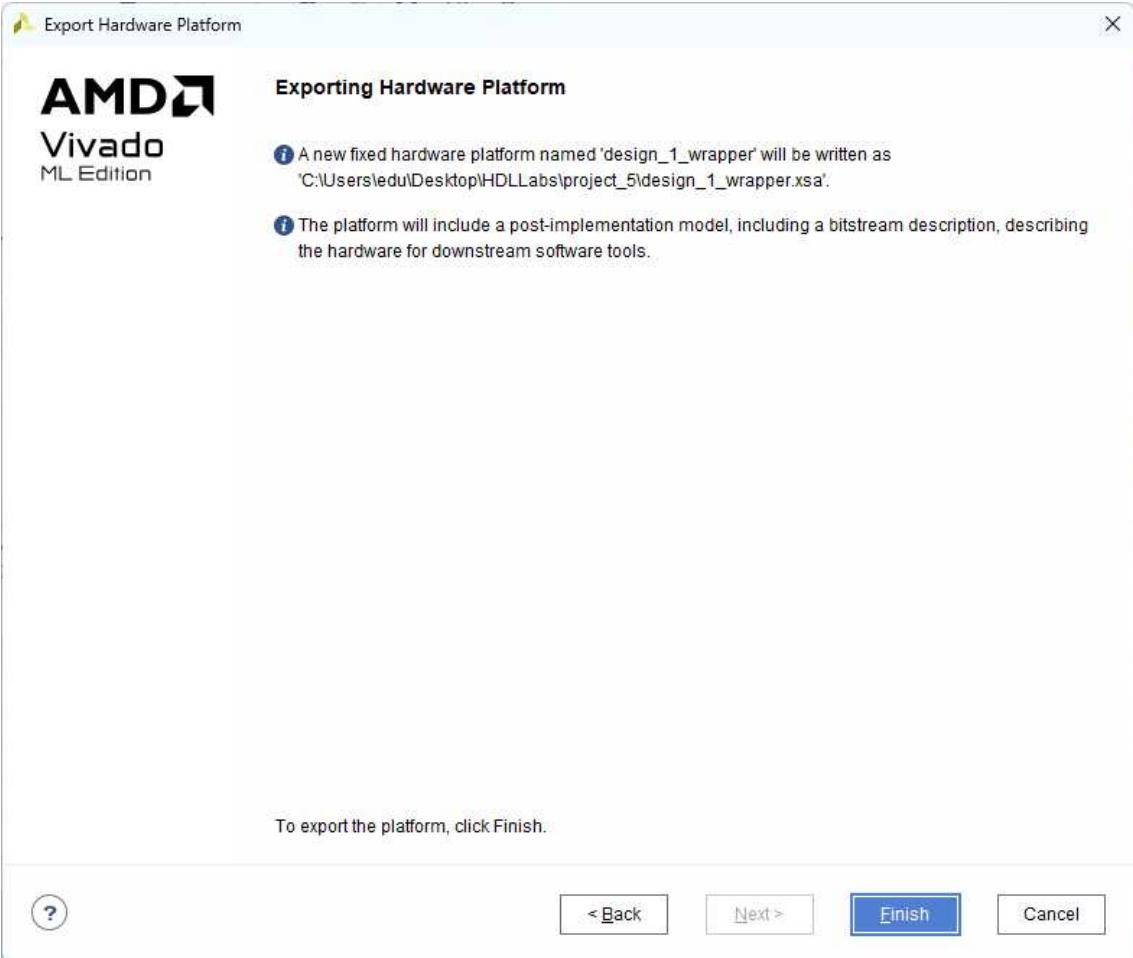
> [Open Hardware Manager](#)

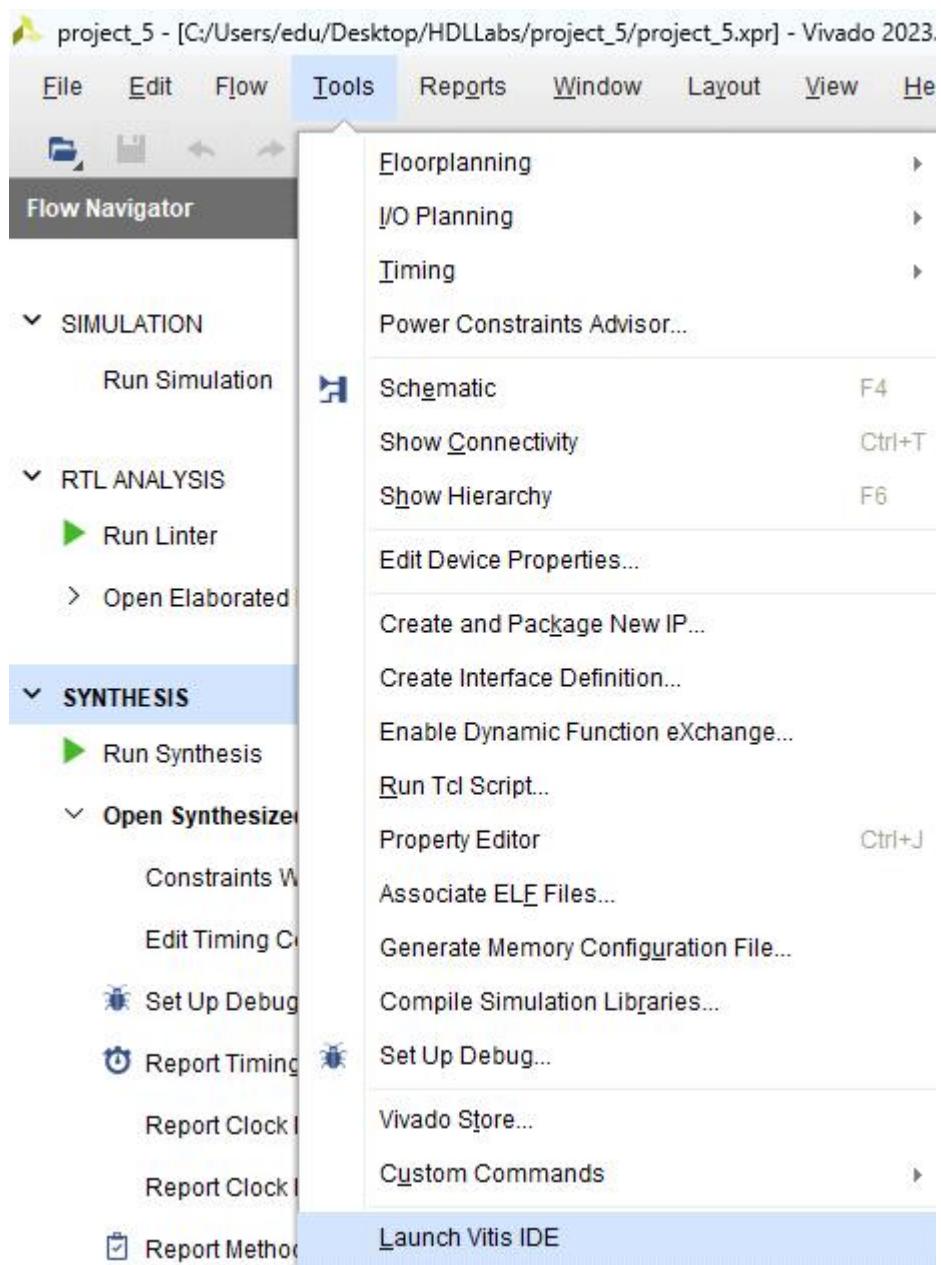
write_bitstream Complete ✓











vitis가 실행되어 있지 않으면 실행시킵니다.

workspace - myapp_system/myapp_system.sprj - Vitis IDE

File Edit Search Vitis Project Window Help

Explorer

- > design_1_wrapper
- myapp_sys
 - New
 - myapp
 - _ide
 - myapp_

Paste Ctrl+V

Delete F5

Refresh

Import Sources...

Export as Archive

Build Project

Clean Project

Copy referenced files into project

Update Hardware Specification

Update Hardware Specification

Update hardware specification for design_1_wrapper

Provide the specification file to use for this platform project.

Hardware Specification File: C:\Users\edu\Desktop\HDL Labs\project_5\design_1_wrapper.xsa

Browse...

OK Cancel

Update Hardware Specification

Hardware specification for platform project 'design_1_wrapper' is updated.

OK

design_1_wrapper (Out-of-date)

workspace - myapp_system/myapp_system.sprj - Vitis IDE

File Edit Search Vitis Project Window Help

Explorer X

design_1 wrapper (Out-of-date)

myapp_s New

myap

_ide

myap

Paste Ctrl+V

Delete Delete

Refresh F5

Import Sources...

Export as Archive

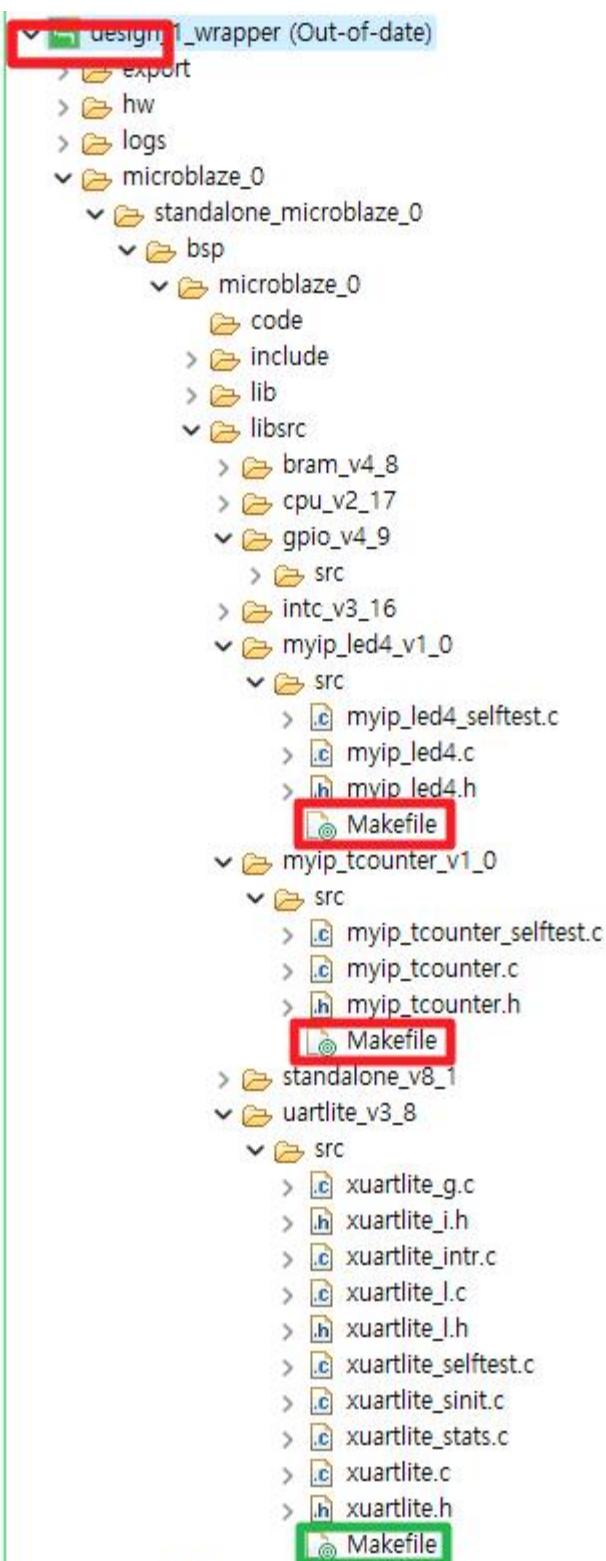
Build Project Incremental Build of Selected

Console X Problems Vitis Log Guidance

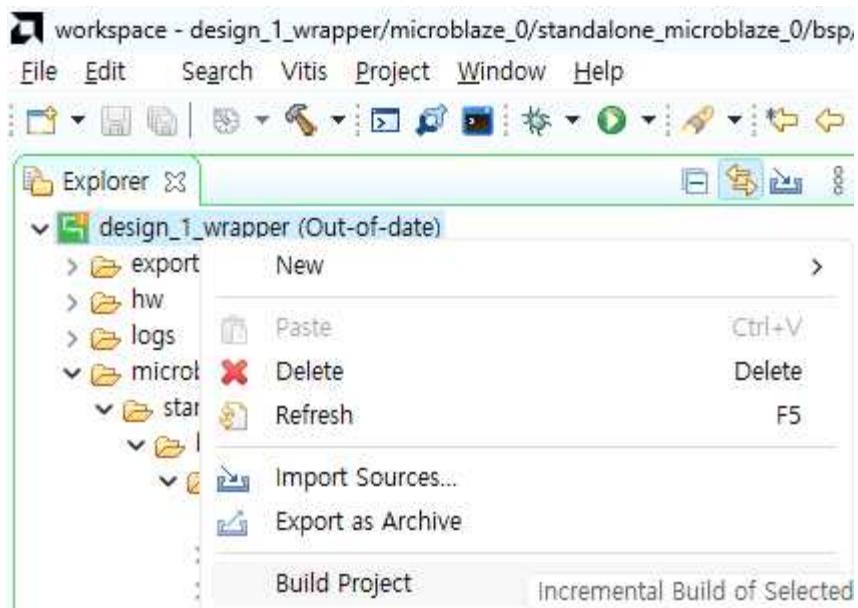
Build Console [design_1_wrapper]

"Compiling myip_led4..."

```
ccl.exe: fatal error: *.c: Invalid argument
compilation terminated.
make[2]: *** [Makefile:18: libs] Error 1
make[1]: *** [Makefile:46: microblaze_0/libsrc/myip_led4_v1_0/src/make.libs] Error 2
make: *** [Makefile:18: all] Error 2
Failed to build the bsp sources for domain - standalone_microblaze_0
Failed to generate the platform.
Reason: Failed to build the bsp sources for domain - standalone_microblaze_0
```

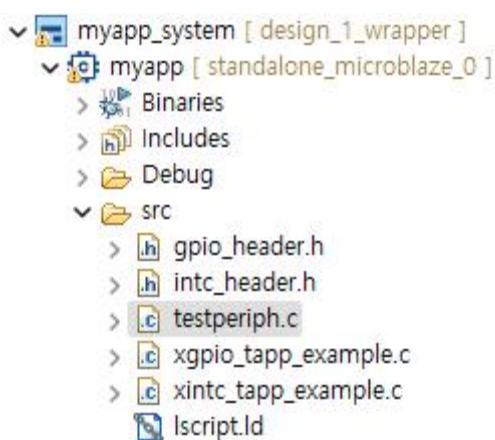


복사 후 저장해 줍니다.



```
Build Console [design_1_wrapper]
Build Console [design_1_wrapper]
mb-ar: creating microblaze_0/lib/libxil.a
'Finished building libraries'

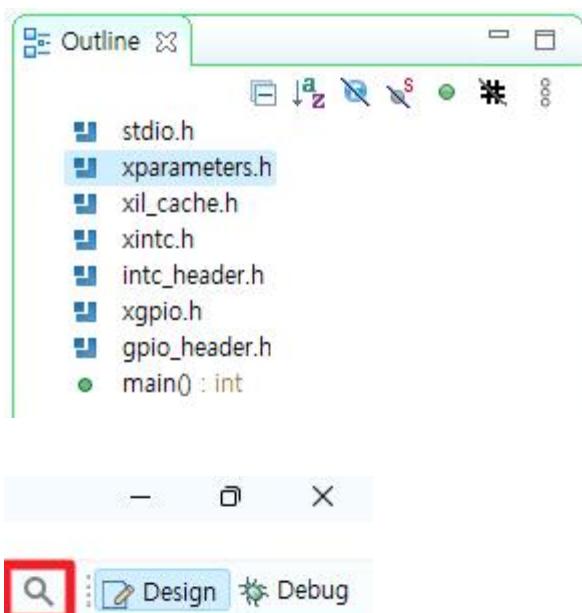
21:57:45 Build Finished (took 4s, 670ms)
```



```

37 int main ()
38 {
39     static XIntc intc;
40     Xil_ICacheEnable();
41     Xil_DCacheEnable();
42     print("---Entering main---\n\r");
43
44     *(unsigned int *)XPAR_GPIO_0_BASEADDR = 0xff;
45     *(unsigned int *)XPAR_MYIP_LED4_0_S00_AXI_BASEADDR = 0xff;
46
47     unsigned int * tcReg = (unsigned int *)XPAR_MYIP_TIMER_0_S00_AXI_BASEADDR;
48     tcReg[0] = (1<<31)|(100000000-1); // tc0.top
49     tcReg[1] = 100000000/2-1; // tc0.cmp

```

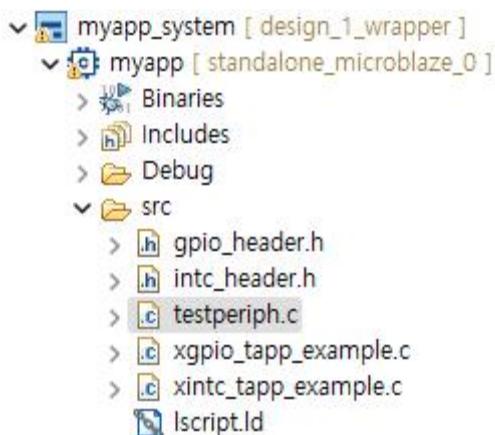


창이 없을 경우 돋보기를 눌러 Outline을 검색하여 추가한다.

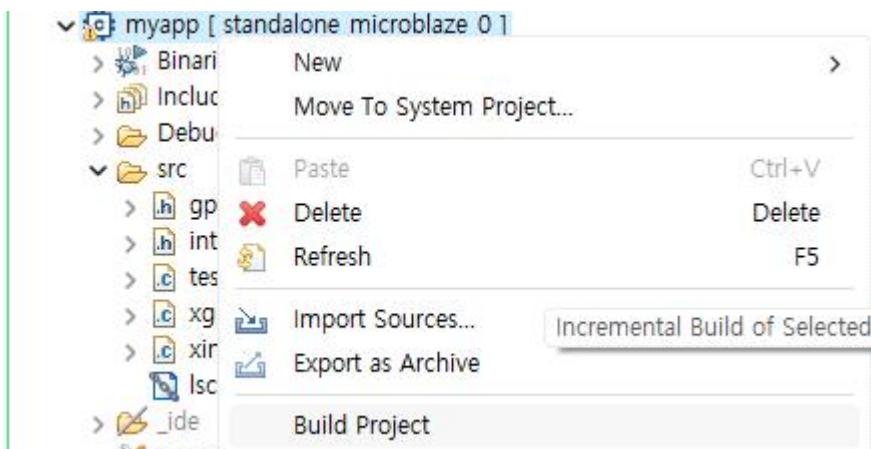
```

652 /* Definitions for driver MYIP_TCOUNTER */
653 #define XPAR_MYIP_TCOUNTER_NUM_INSTANCES 1
654
655 /* Definitions for peripheral MYIP_TCOUNTER_0 */
656 #define XPAR_MYIP_TCOUNTER_0_DEVICE_ID 0
657 #define XPAR_MYIP_TCOUNTER_0_S00_AXI_BASEADDR 0x44A10000
658 #define XPAR_MYIP_TCOUNTER_0_S00_AXI_HIGHADDR 0x44A1FFFF

```



```
37④ int main ()
38 {
39     static XIntc intc;
40     Xil_ICacheEnable();
41     Xil_DCacheEnable();
42     print("----Entering main---\n\r");
43
44     *(unsigned int *)XPAR_GPIO_0_BASEADDR = 0xff;
45     *(unsigned int *)XPAR_MYIP_LED4_0_S00_AXI_BASEADDR = 0xff;
46
47     unsigned int * tcReg = (unsigned int *)XPAR_MYIP_TCOUNTER_0_S00_AXI_BASEADDR;
48     tcReg[0] = (1<<31)|(100000000-1); // tc0.top
49     tcReg[1] = 100000000/2-1; // tc0.cmp
50
51 }
```



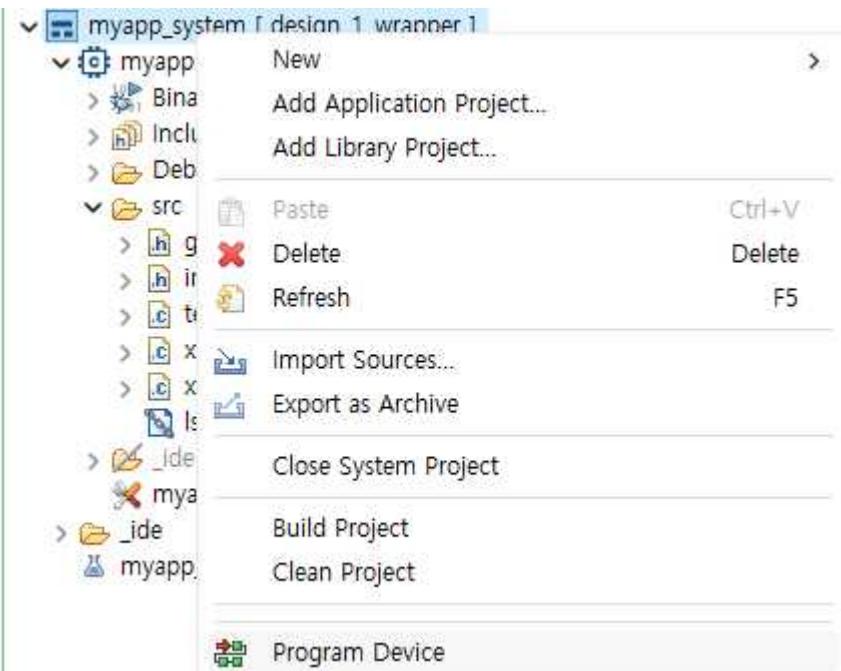
Console Problems Vitis Log Guidance

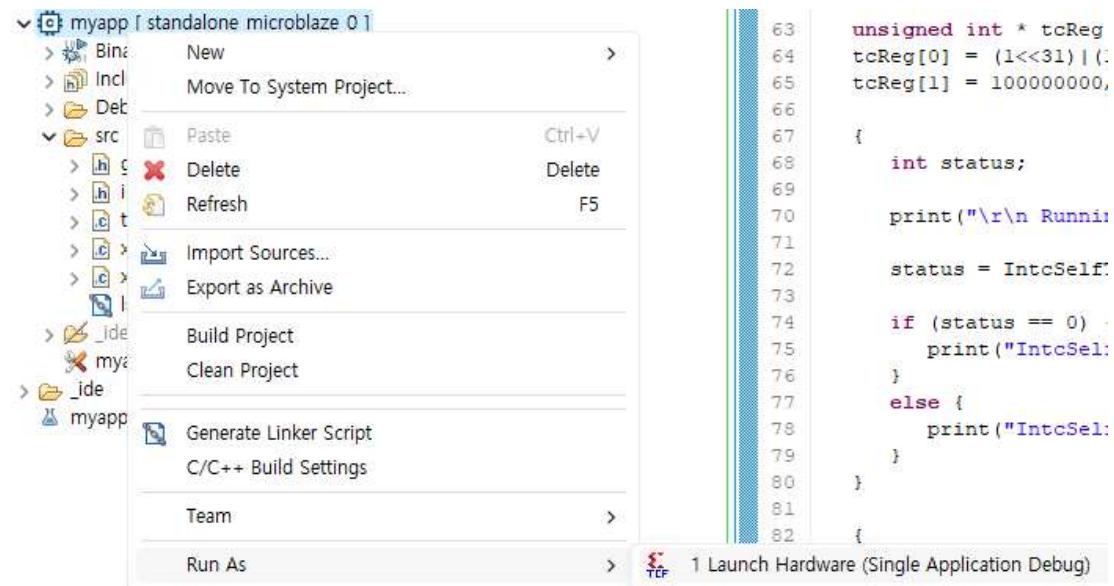
Build Console [myapp, Debug]

```
'Invoking: MicroBlaze gcc linker'
mb-gcc -Wl,-T -Wl,.../src/lscript.ld -LC:/Users/edu/wor
'Finished building target: myapp.elf'
'

'Invoking: MicroBlaze Print Size'
mb-size myapp.elf |tee "myapp.elf.size"
    text      data      bss      dec      hex filename
    4768      320     3280     8368     20b0 myapp.elf
'Finished building: myapp.elf.size'
'

22:05:12 Build Finished (took 1s.324ms)
```





```
36 #include "gpio_header.h"
37
38 typedef struct _MYIP_TIMER {
39     volatile uint32_t slv_reg0;
40     volatile uint32_t slv_reg1;
41     volatile uint32_t slv_reg2;
42     volatile uint32_t slv_reg3;
43     volatile uint32_t slv_reg4;
44     volatile uint32_t slv_reg5;
45     volatile uint32_t slv_reg6;
46     volatile uint32_t slv_reg7;
47     volatile uint32_t slv_reg8;
48     volatile uint32_t slv_reg9;
49     volatile uint32_t slv_reg10;
50     volatile uint32_t slv_reg11;
51 } MYIP_TIMER;
52
53 int main ()
```

```
63 unsigned int * tcReg
64 tcReg[0] = (1<<31) | (1<<31);
65 tcReg[1] = 100000000,
66
67 {
68     int status;
69
70     print("\r\n Running...\n");
71
72     status = IntcSelf();
73
74     if (status == 0) {
75         print("IntcSel: 0\n");
76     }
77     else {
78         print("IntcSel: 1\n");
79     }
80 }
81
82 {
```

```
53 ⊕ int main ()
54 {
55     static XIntc intc;
56     Xil_ICacheEnable();
57     Xil_DCacheEnable();
58     print("----Entering main---\n\r");
59
60     *(unsigned int *)XPAR_GPIO_0_BASEADDR = 0xff;
61     *(unsigned int *)XPAR_MYIP_LED4_0_S00_AXI_BASEADDR = 0xff;
62
63     unsigned int * tcReg = (unsigned int *)XPAR_MYIP_TCOUNTER_0_S00_AXI_BASEADDR;
64     tcReg[0] = (1<<31)|(100000000-1); // tc0.top
65     tcReg[1] = 100000000/2-1; // tc0.cmp
66
67     MYIP_TIMER * myip_timer = (MYIP_TIMER *)XPAR_MYIP_TCOUNTER_0_S00_AXI_BASEADDR;
68     myip_timer->slv_reg2 = (1<<31)|(10000000-1);
69     myip_timer->slv_reg3 = (10000000/2-1);
70
71 }
```