

Lecture 5: DC & Transient Response

Outline

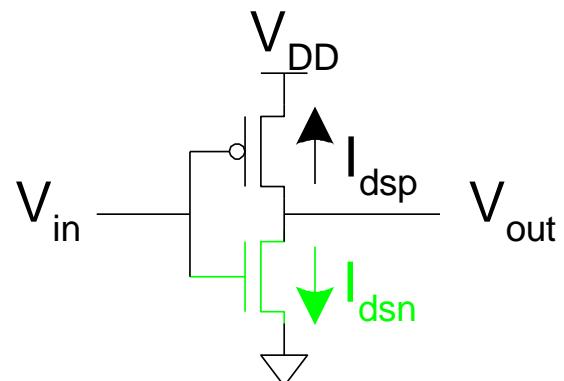
- Pass Transistors
- DC Response
- Logic Levels and Noise Margins
- Transient Response
- RC Delay Models
- Delay Estimation

Transistor Operation

- Current depends on region of transistor behavior
- For what V_{in} and V_{out} are nMOS and pMOS in
 - Cutoff?
 - Linear?
 - Saturation?

nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} <$	$V_{gsn} >$ $V_{dsn} <$	$V_{gsn} >$ $V_{dsn} >$



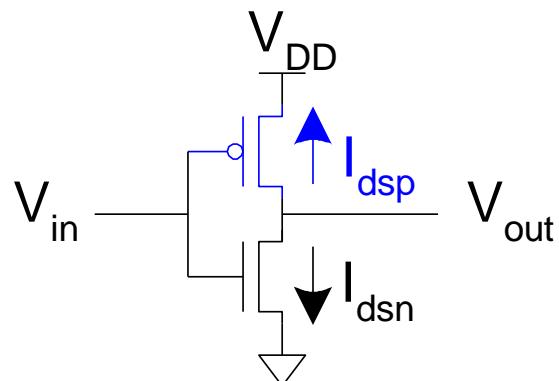
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

$$V_{gsp} = V_{in} - V_{DD}$$

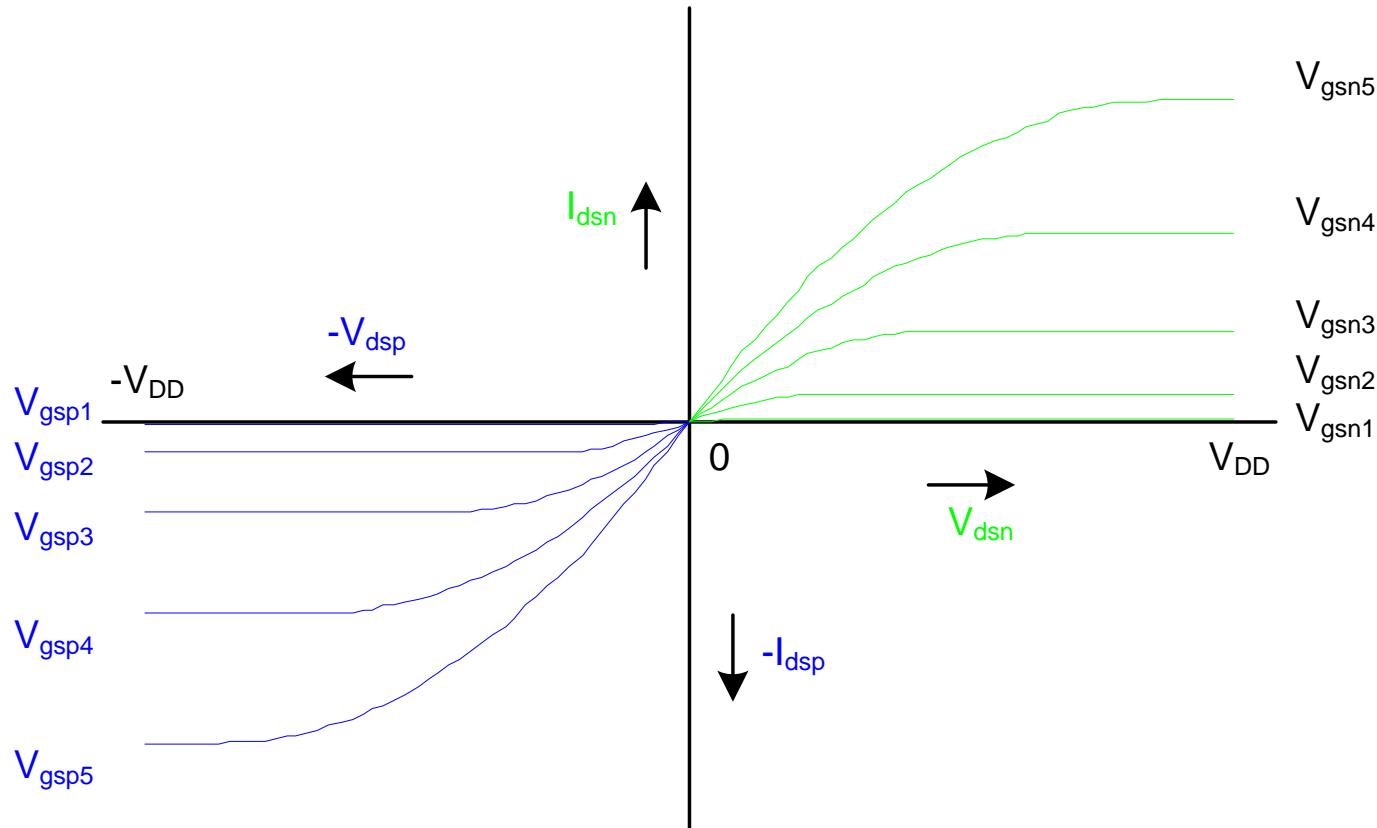
$$V_{tp} < 0$$

$$V_{dsp} = V_{out} - V_{DD}$$

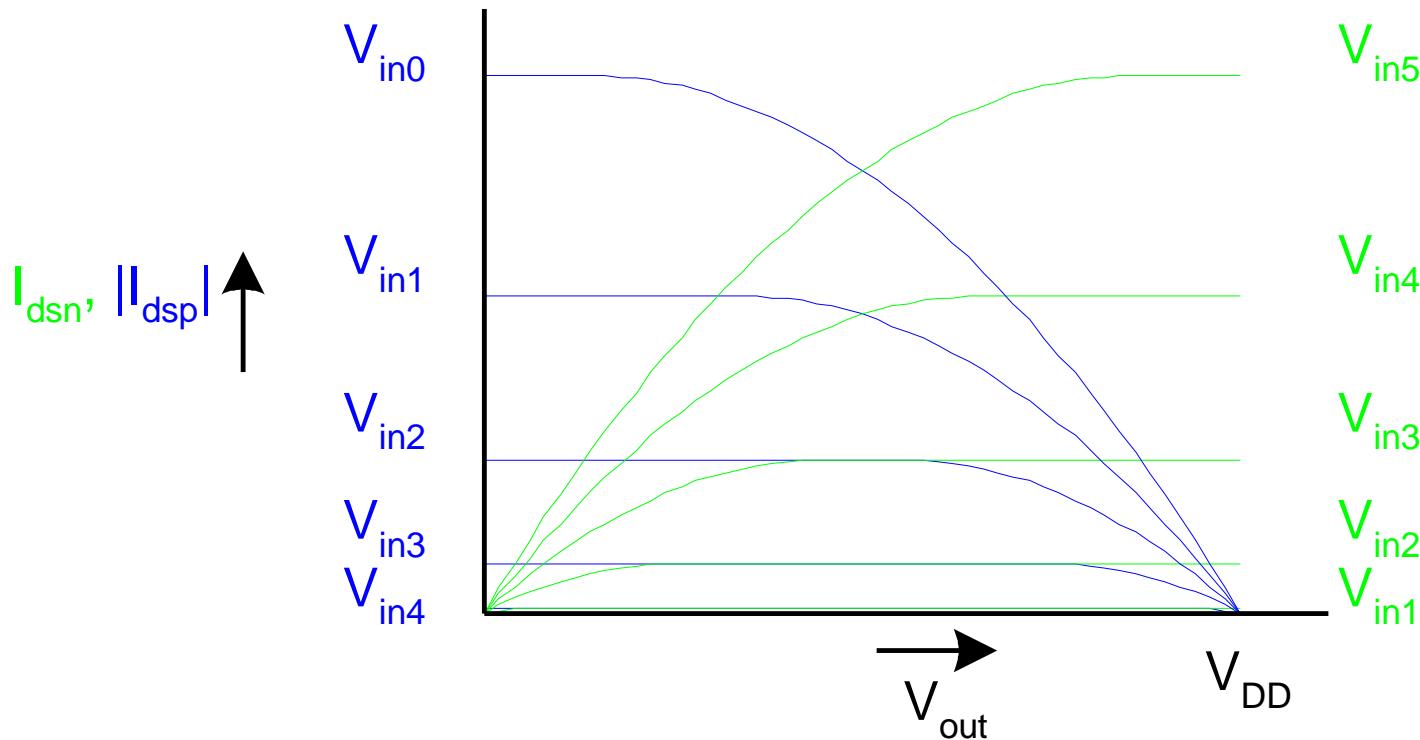


I-V Characteristics

- Make pMOS is wider than nMOS such that $\beta_n = \beta_p$

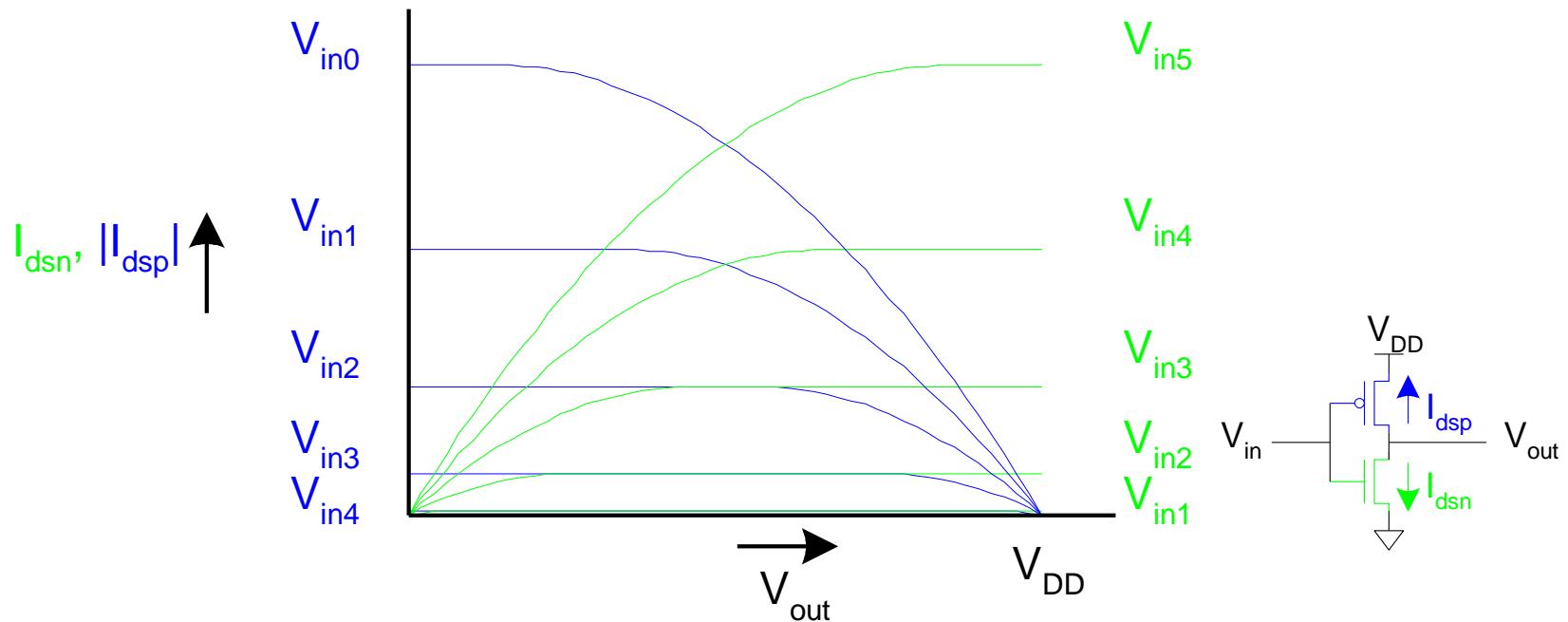


Current vs. V_{out} , V_{in}

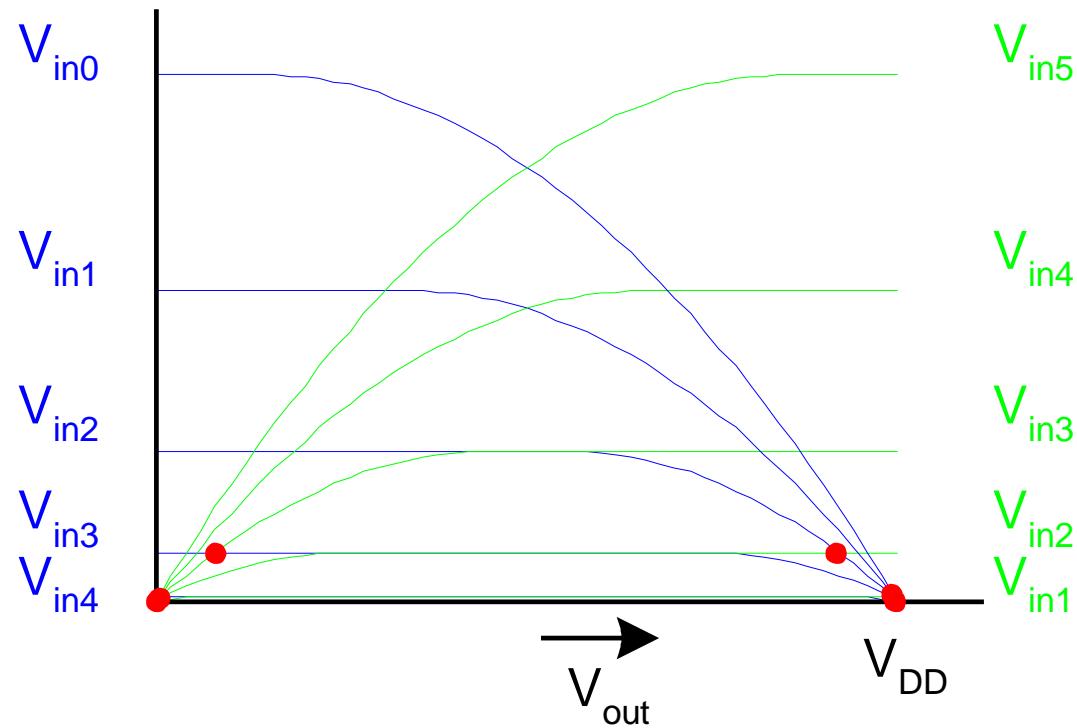


Load Line Analysis

- For a given V_{in} :
 - Plot I_{dsn}, I_{dsp} vs. V_{out}
 - V_{out} must be where |currents| are equal in

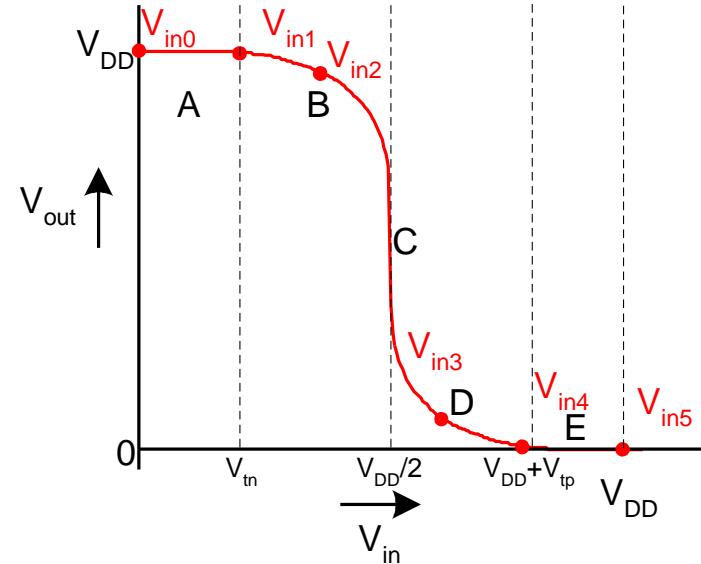
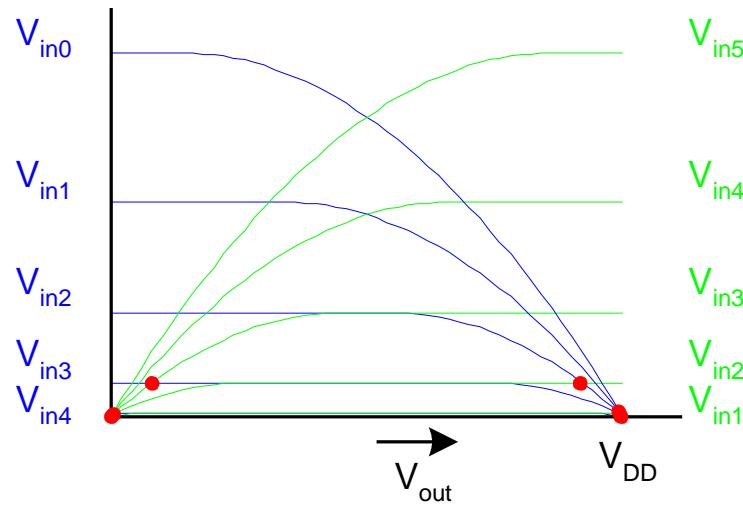


Load Line Analysis



DC Transfer Curve

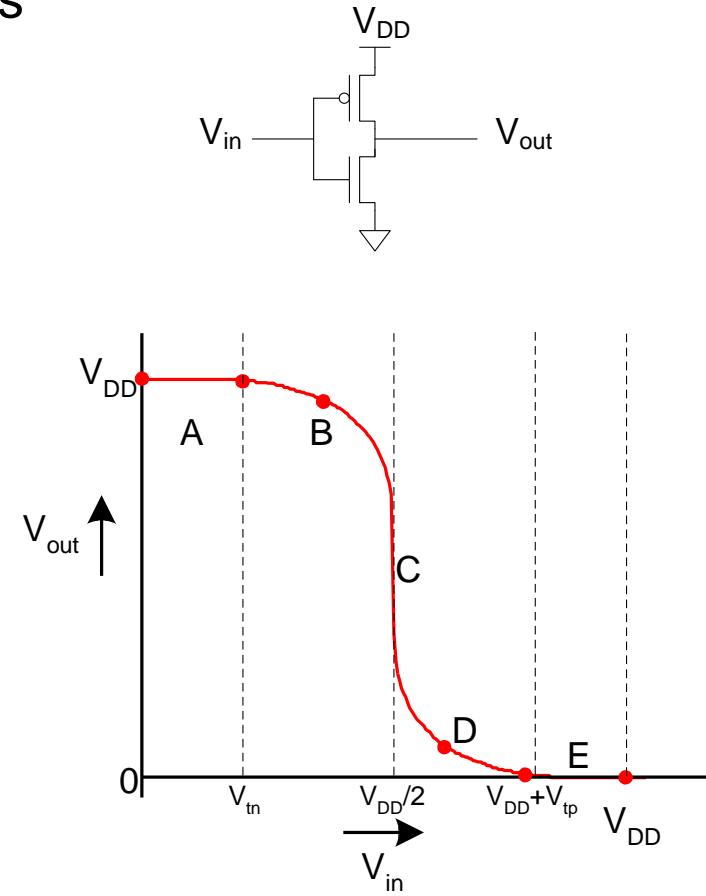
- Transcribe points onto V_{in} vs. V_{out} plot



Operating Regions

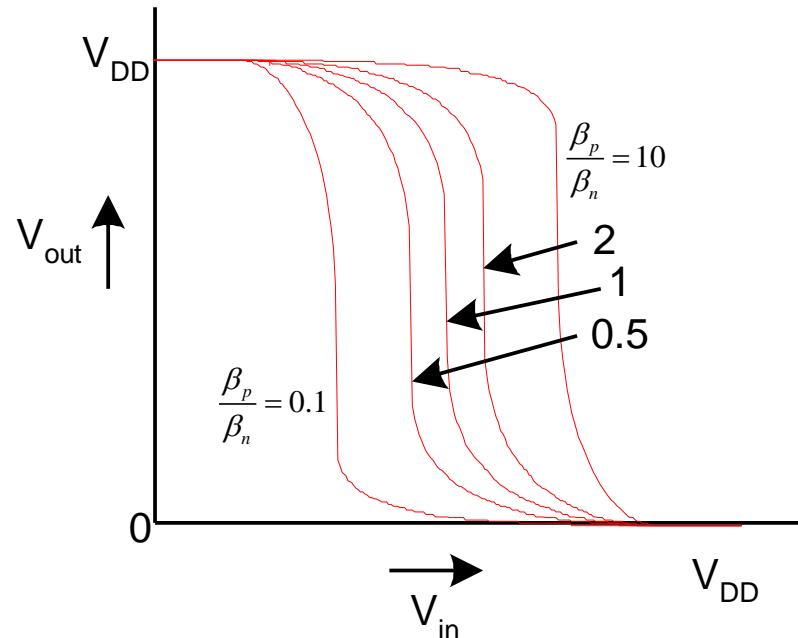
- Revisit transistor operating regions

Region	nMOS	pMOS
A		
B		
C		
D		
E		



Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed gate*
- Other gates: collapse into equivalent inverter



Layout Comparison

- Which layout is better?

