Cadence Full-Custom IC Design

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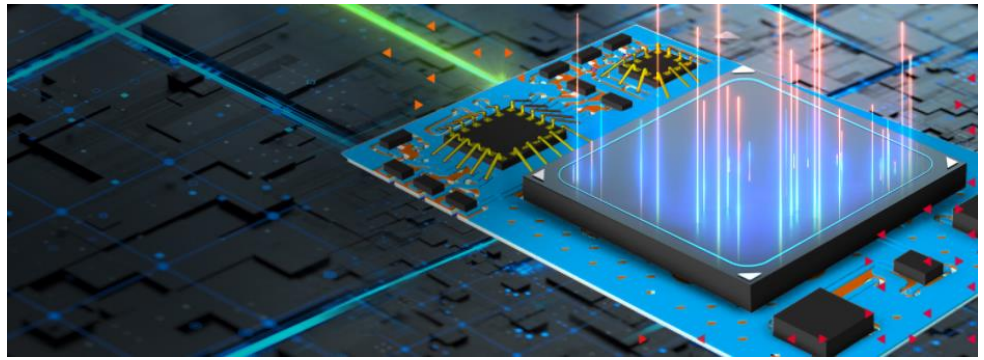
Introduction

Course

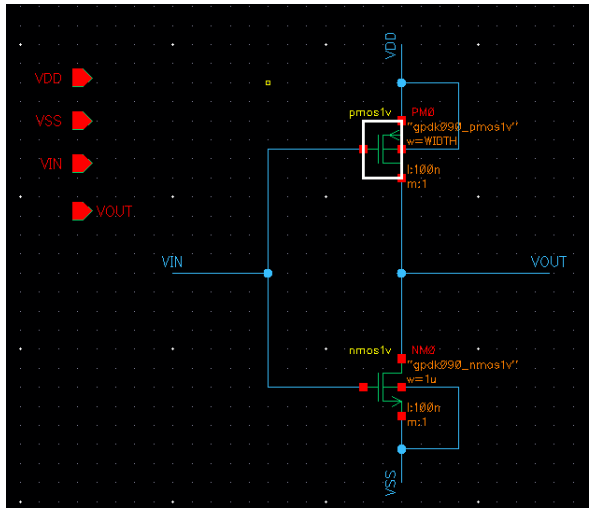
Cadence® Full-Custom IC Designer

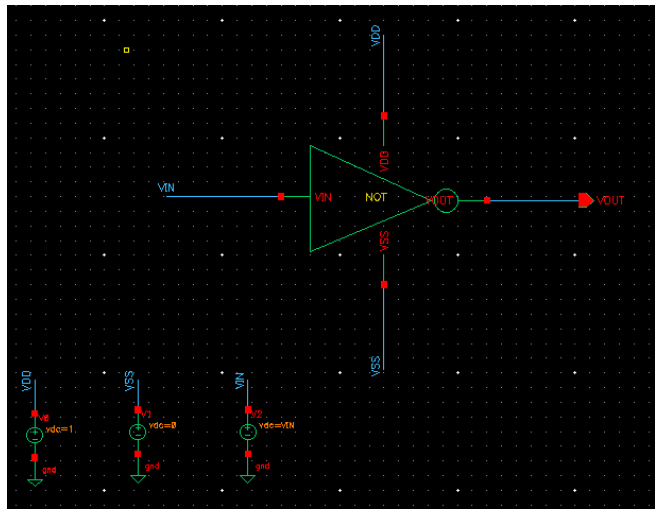
Tools

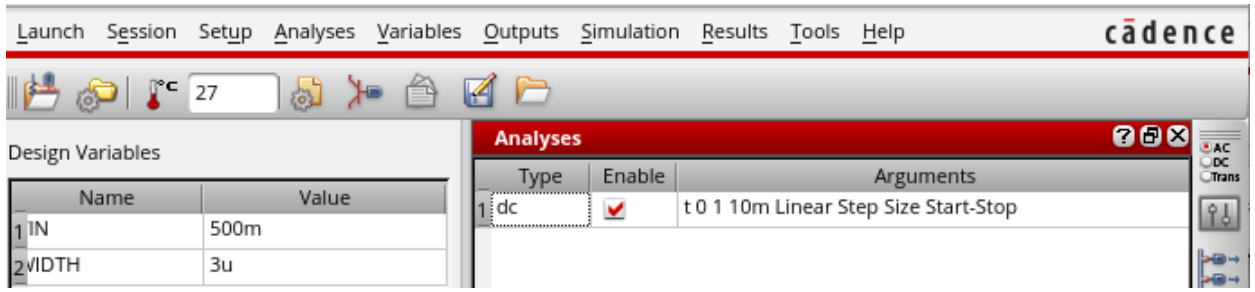
Cadence Virtuoso Schematic Editor / Layout Editor
Cadence Virtuoso Spectre / ADE
Assura DRC / LVS
GPDK090



Logic Gate







[NOT Gate]

Find to PMOS width

01 Schematic

NMOS => 1um
PMOS => WIDTH

02 TEST Schematic

VDD = 1V
VSS = 0V
VIN = VIN

03 DC Analysis

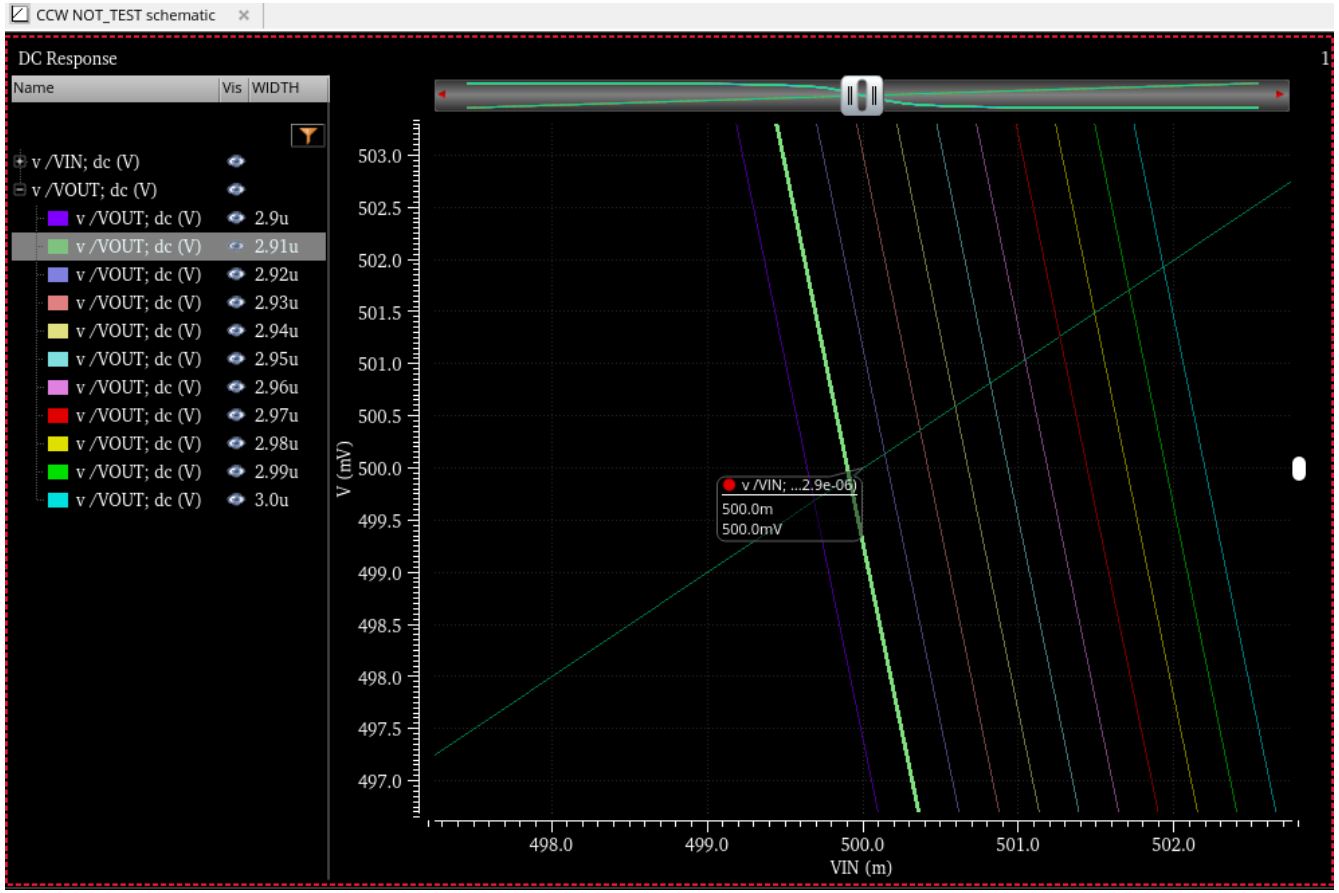
0V – 1V
Linear Step (0.01V)

04 WIDTH Analysis

Reduce Step Size

[NOT Gate]

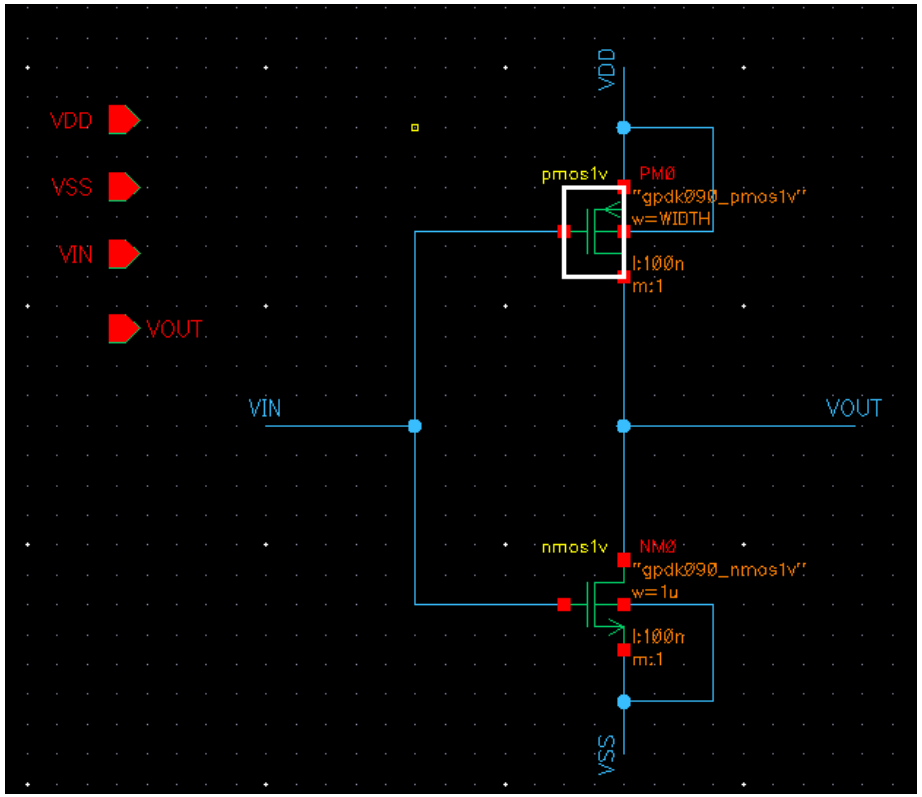
Find to PMOS width

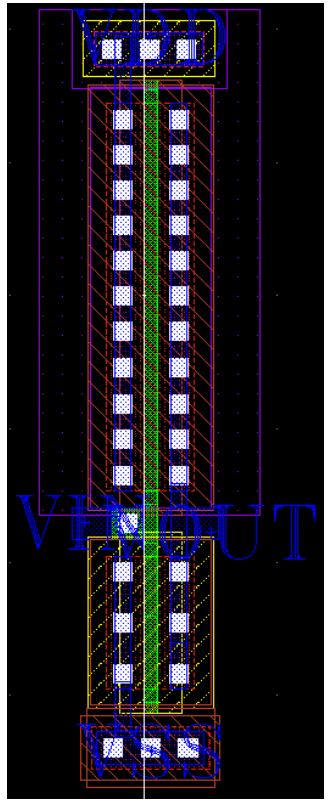


Simulation Result

PMOS WIDTH = 2.91um

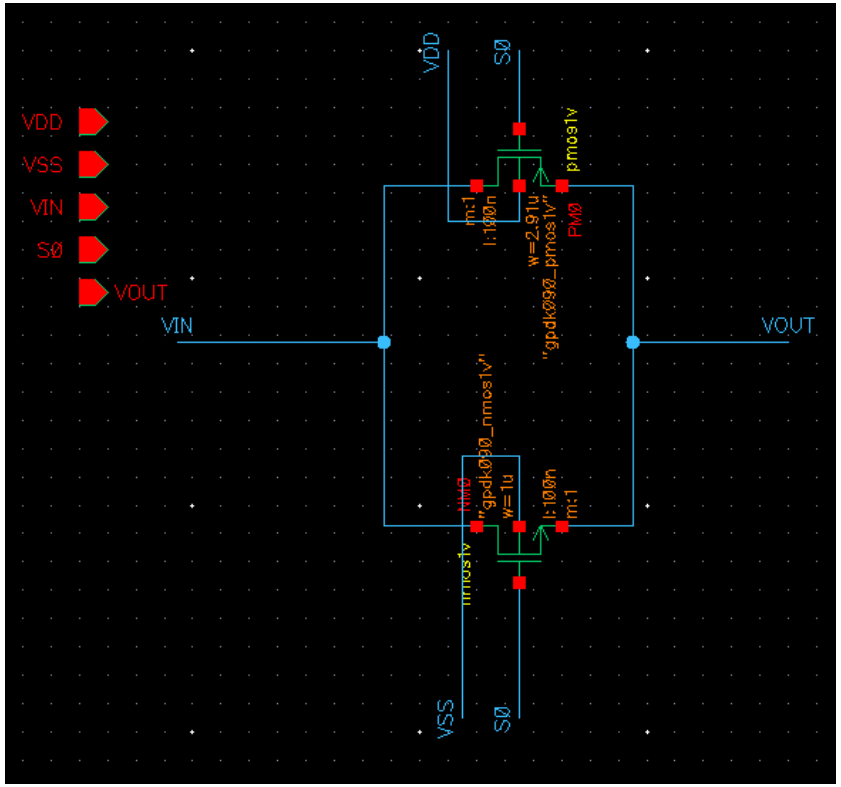
NOT GATE

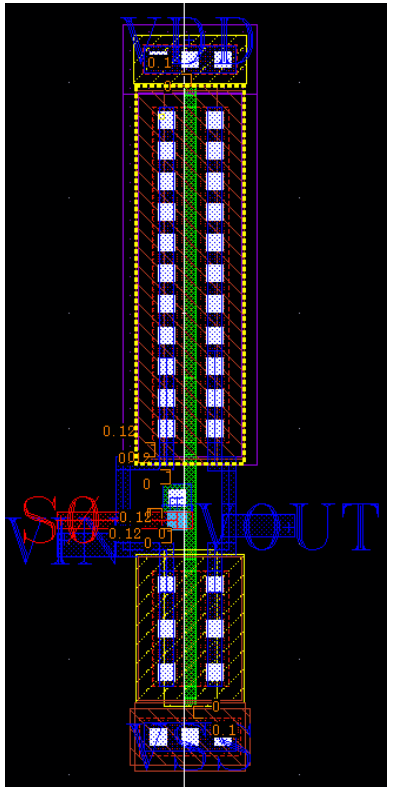




PMOS WIDTH = 2.91um

SWITCH

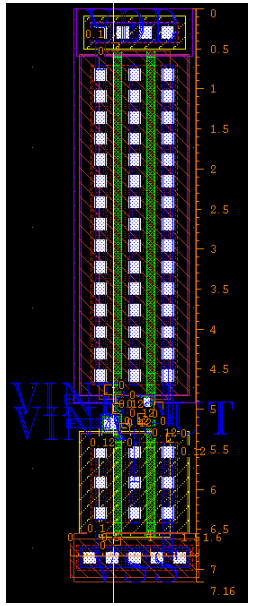
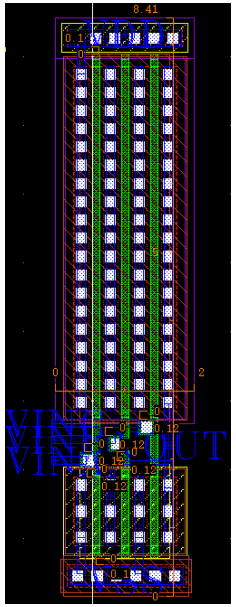
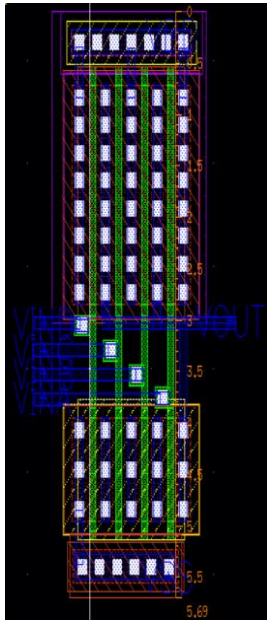
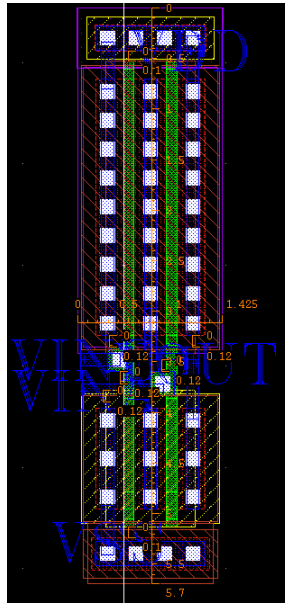
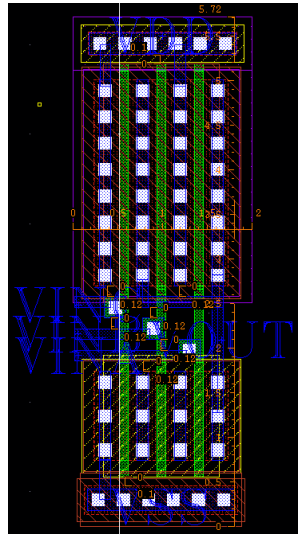
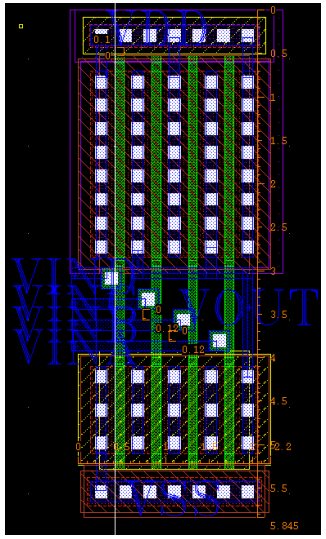




PMOS WIDTH = 2.91um

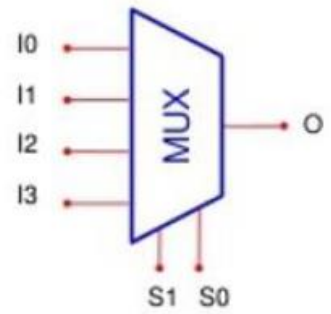
NAND / NOR Gate

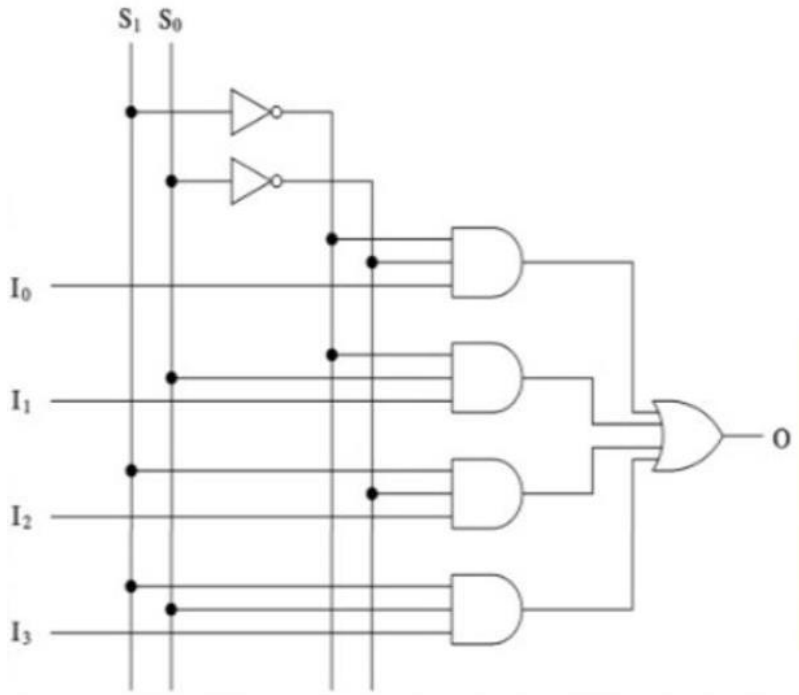
	2NOR	3NOR	4NOR	2NAND	3NAND	4NAND
NMOS	1um	1um	1um	1um	1um	1um
PMOS	3.99um	5um	5.96um	2.53um	2.31um	2.14um

Multiplexer (MUX)

Multiplexer (MUX)





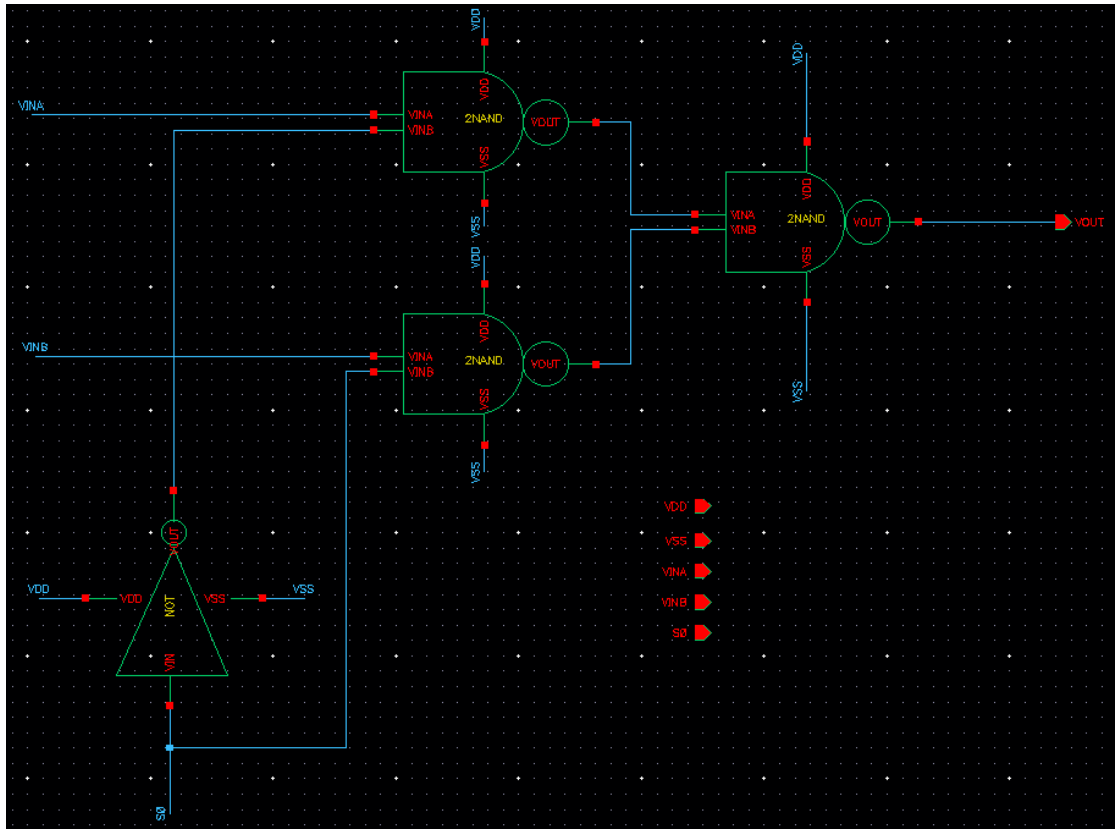
- $Out = \overline{S_1 S_0} A + \overline{S_1} S_0 B + S_1 \overline{S_0 C} + S_1 S_0 D$

MUX Truth Table		
S1	S0	OUT
0	0	A
0	1	B
1	0	C
1	1	D

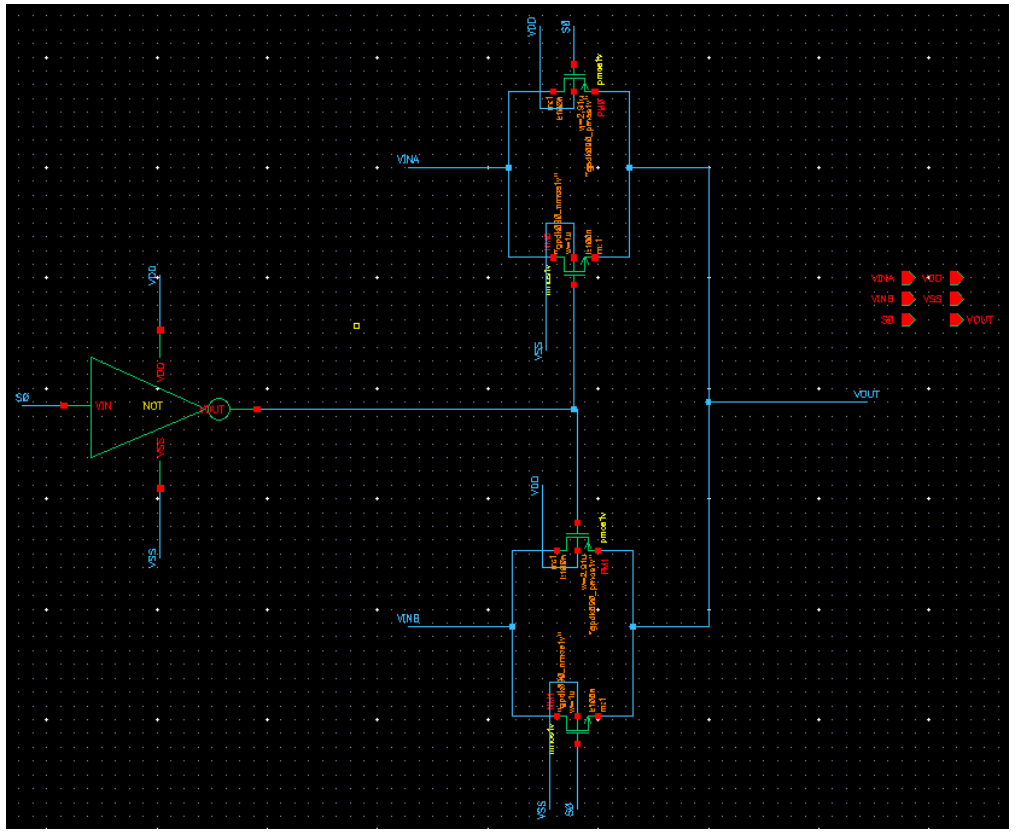
[2x1]

Logic Gate vs Switch

Logic Gate



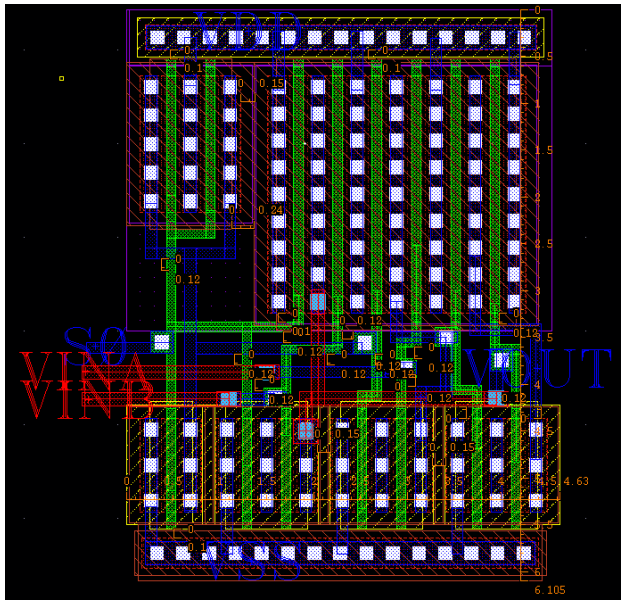
Switch

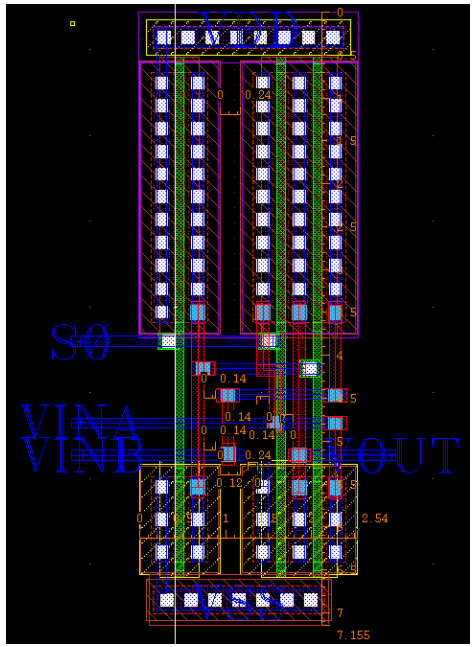


Multiplexer (MUX)

[2x1]

Logic Gate vs Switch

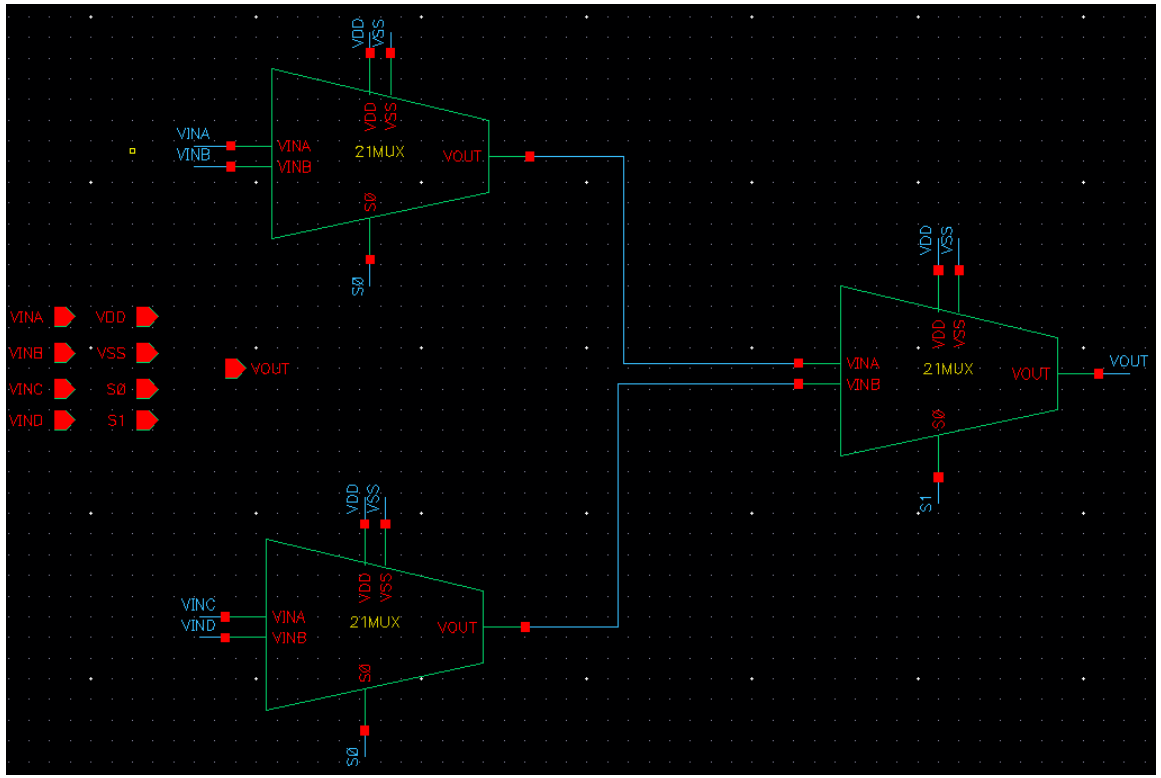




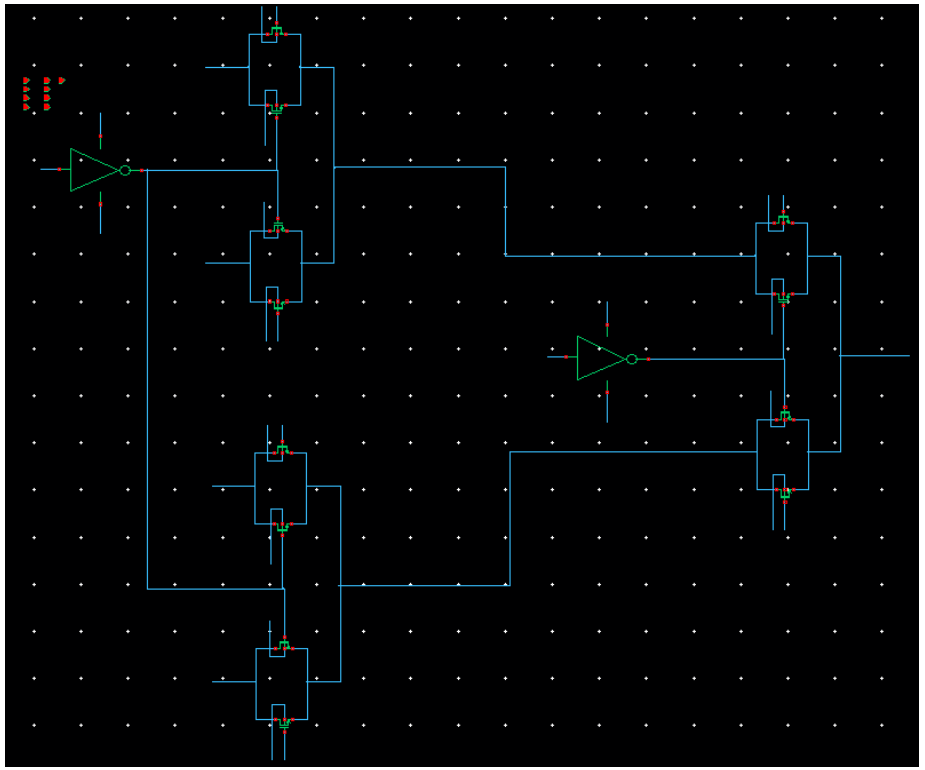
	Logic Gate	Switch
Length	6.305um	7.155um
Width	4.63um	2.54um
Transistor	14	6

[4x1]
Logic Gate vs Switch

Logic Gate

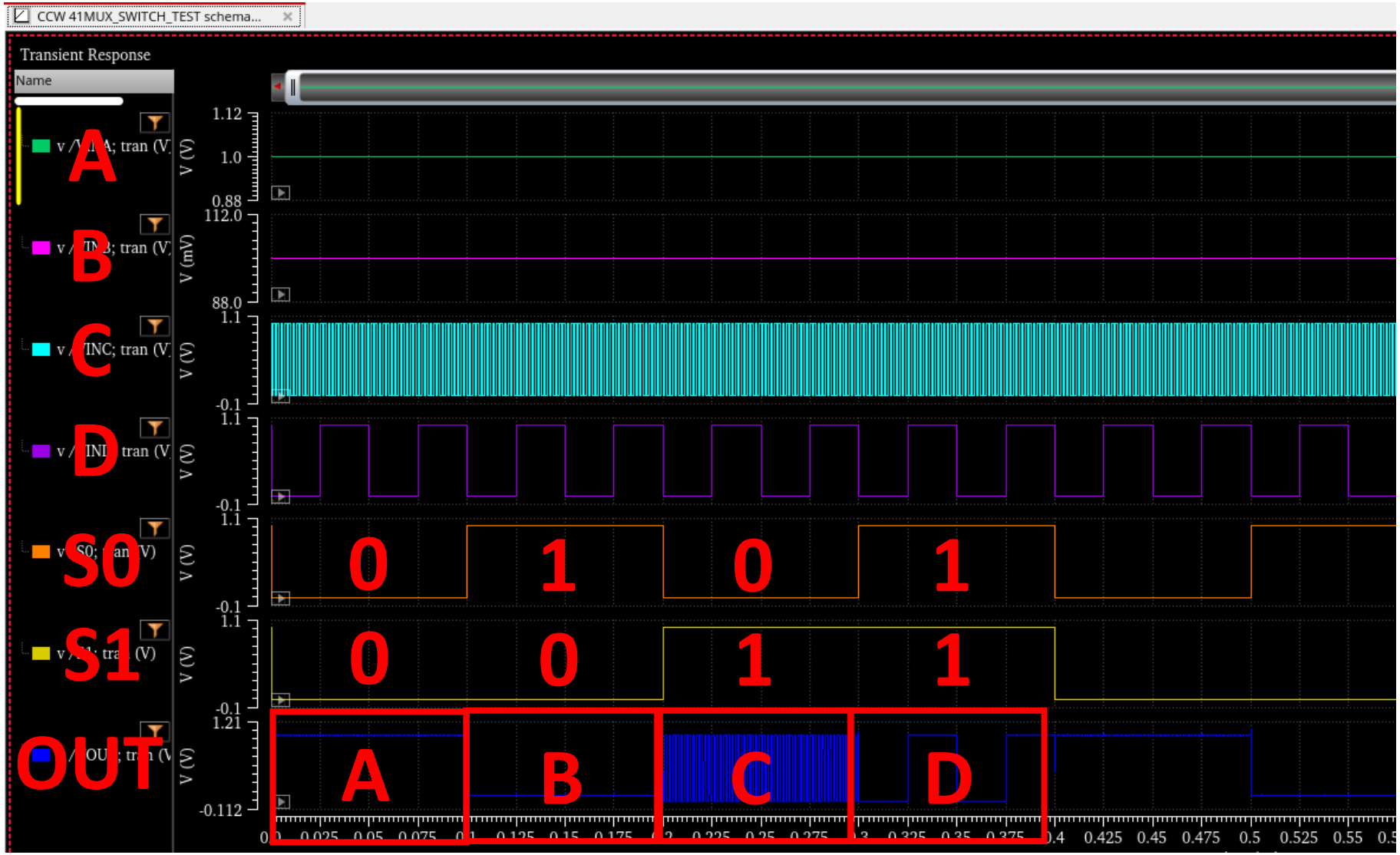


Switch



Multiplexer (MUX)

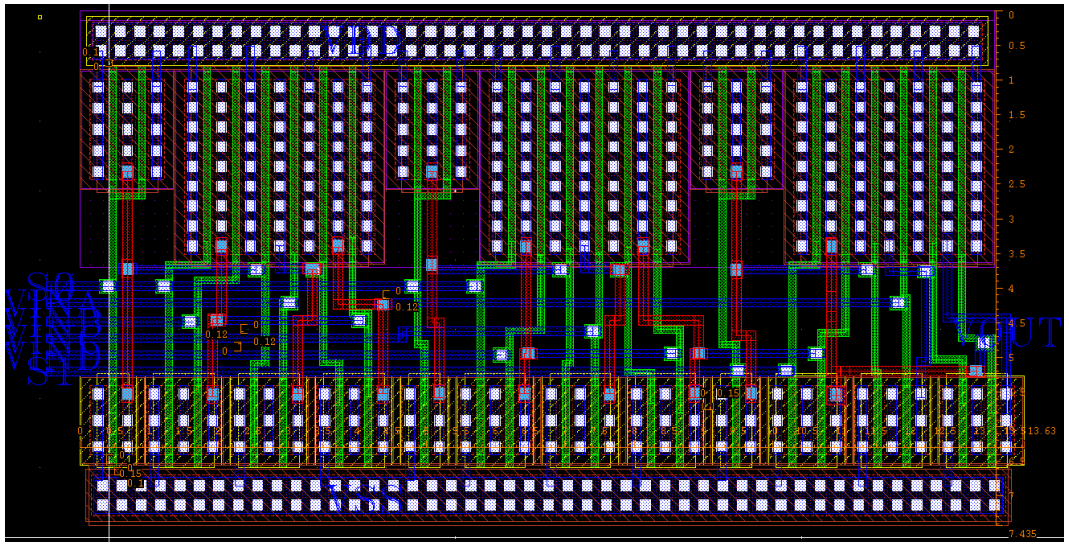
[4x1]
Simulation

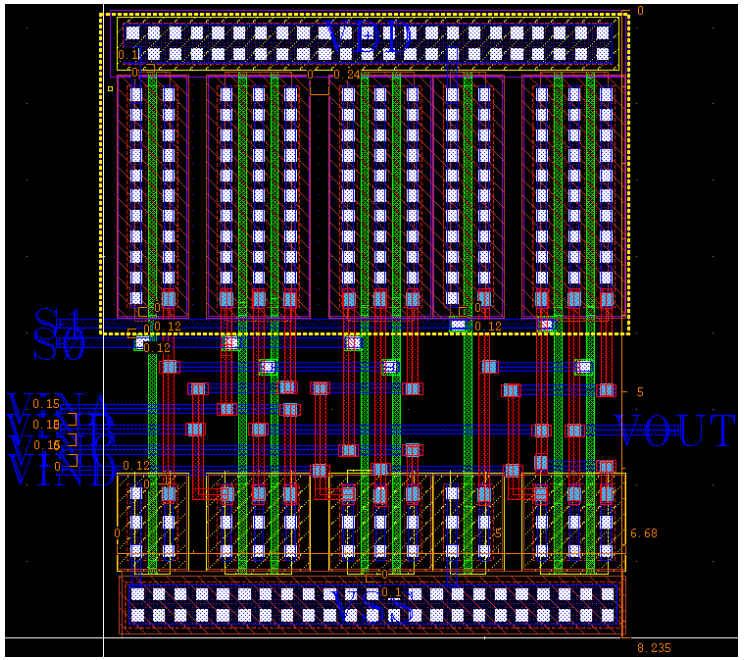


Multiplexer (MUX)

[4x1]

Logic Gate vs Switch





	Logic Gate	Switch
Length	7.435um	8.235um
Width	13.63um	6.60um
Transistor	42	16

Adder

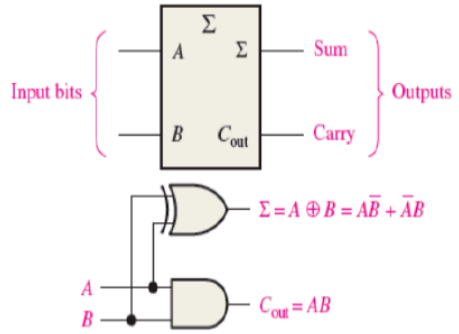
Adder

Half_Adder

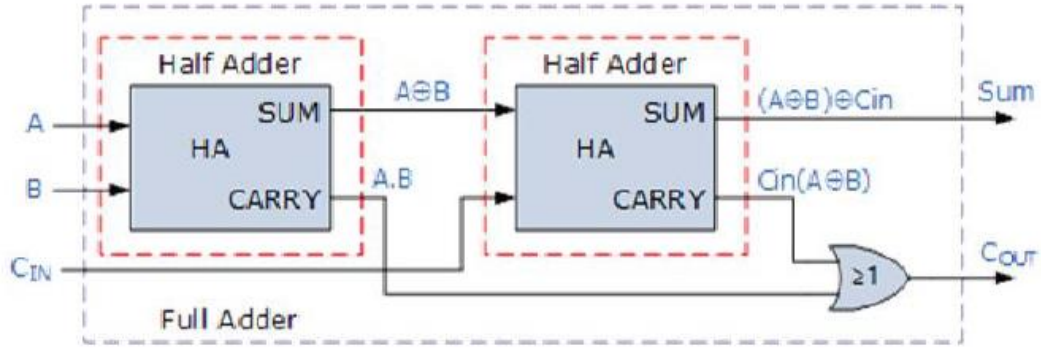
Half-adder truth table.

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Σ = sum
C_{out} = output carry
A and B = input variables (operands)



FULL_ADDER



4Bit Adder

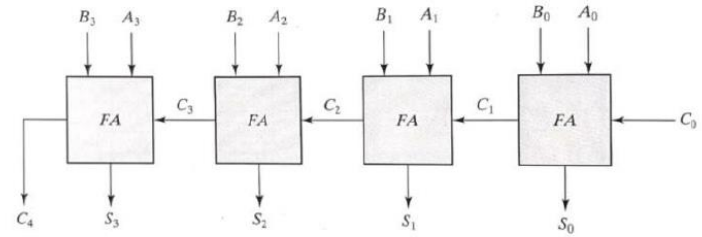
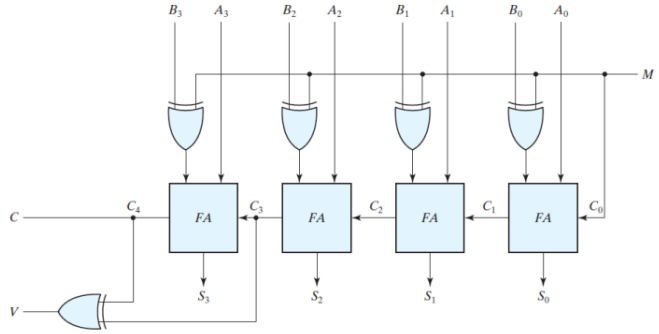
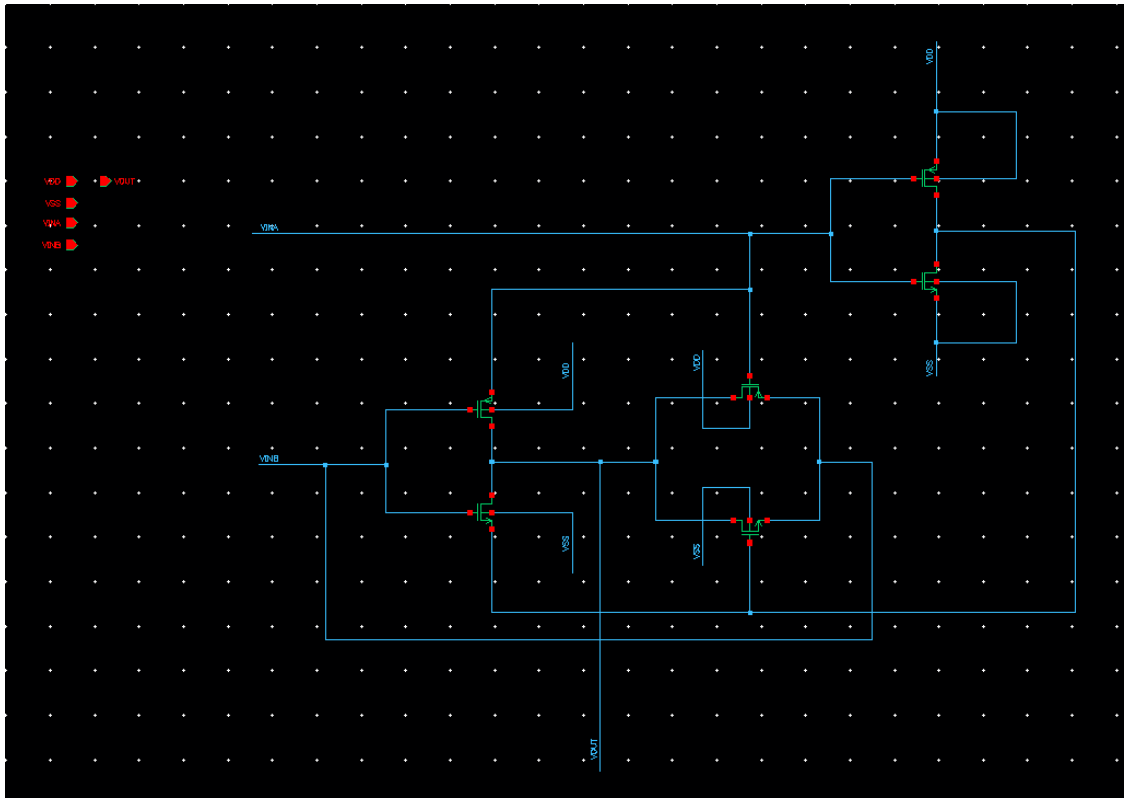


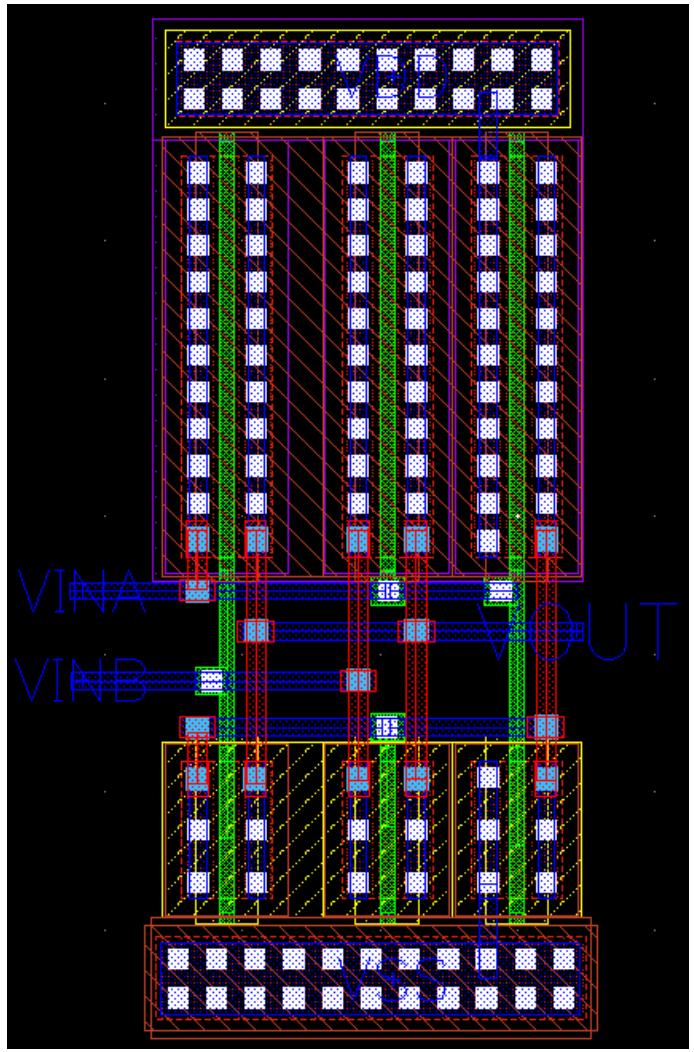
FIGURE 4.9
Four-bit adder

4BIT Adder-Substractor



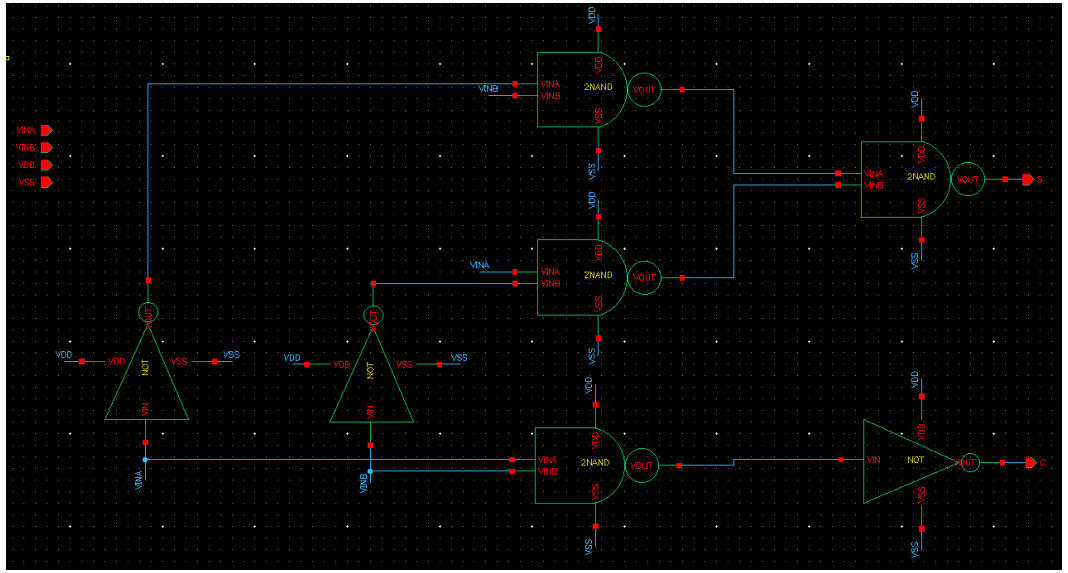

VDD
VOUT
VSS
VINA
VINB
VDD
VDD
VDD
VSS
VSS
VSS
VOUT

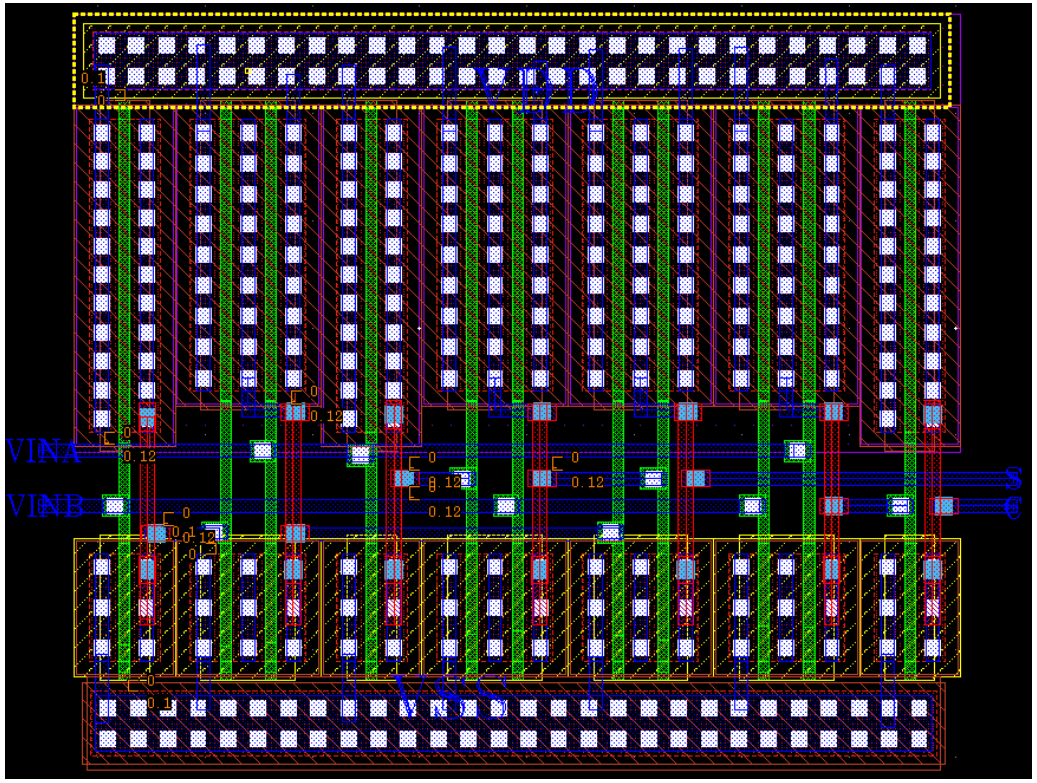
XOR Gate


VINA
VINB
VOUT

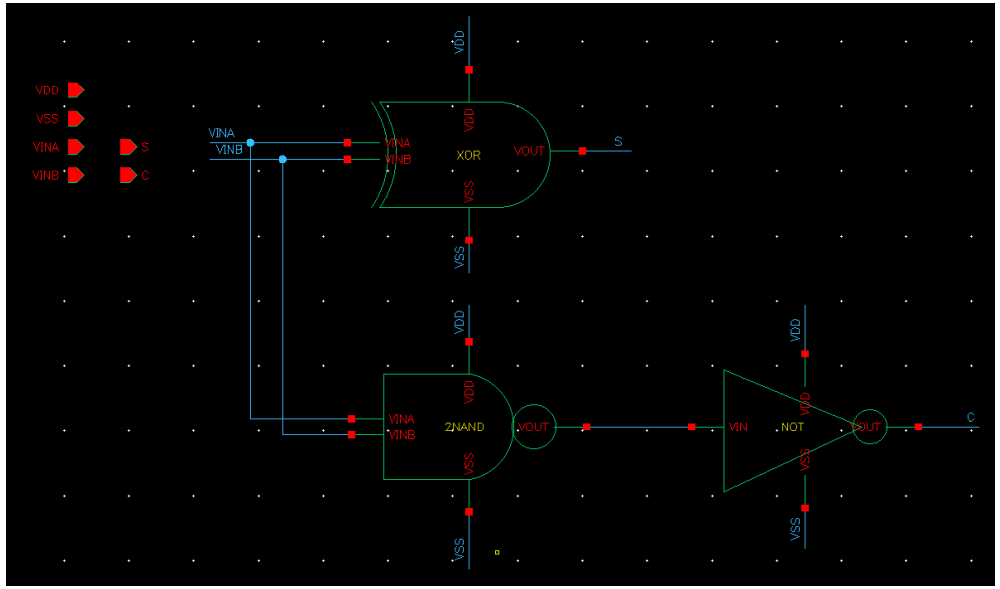
Adder

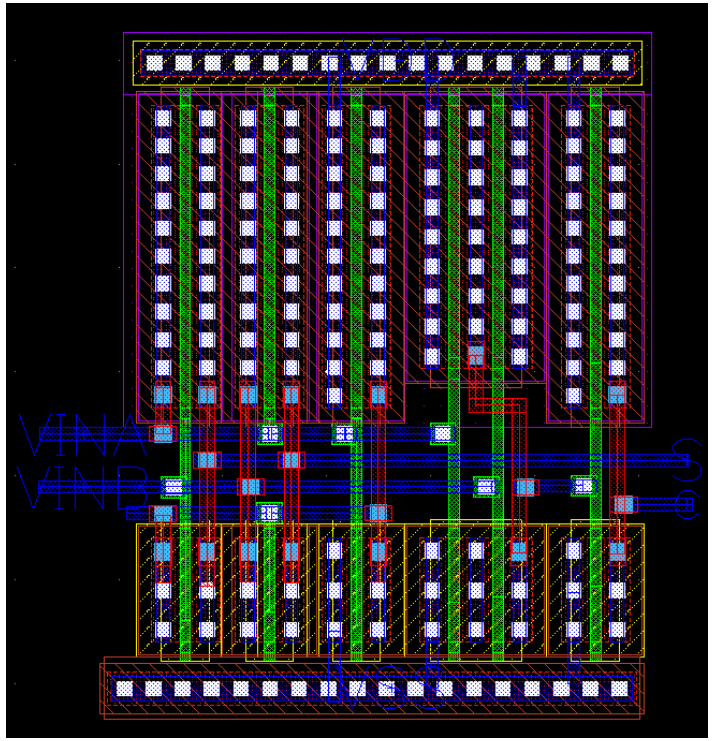
Half Adder 1





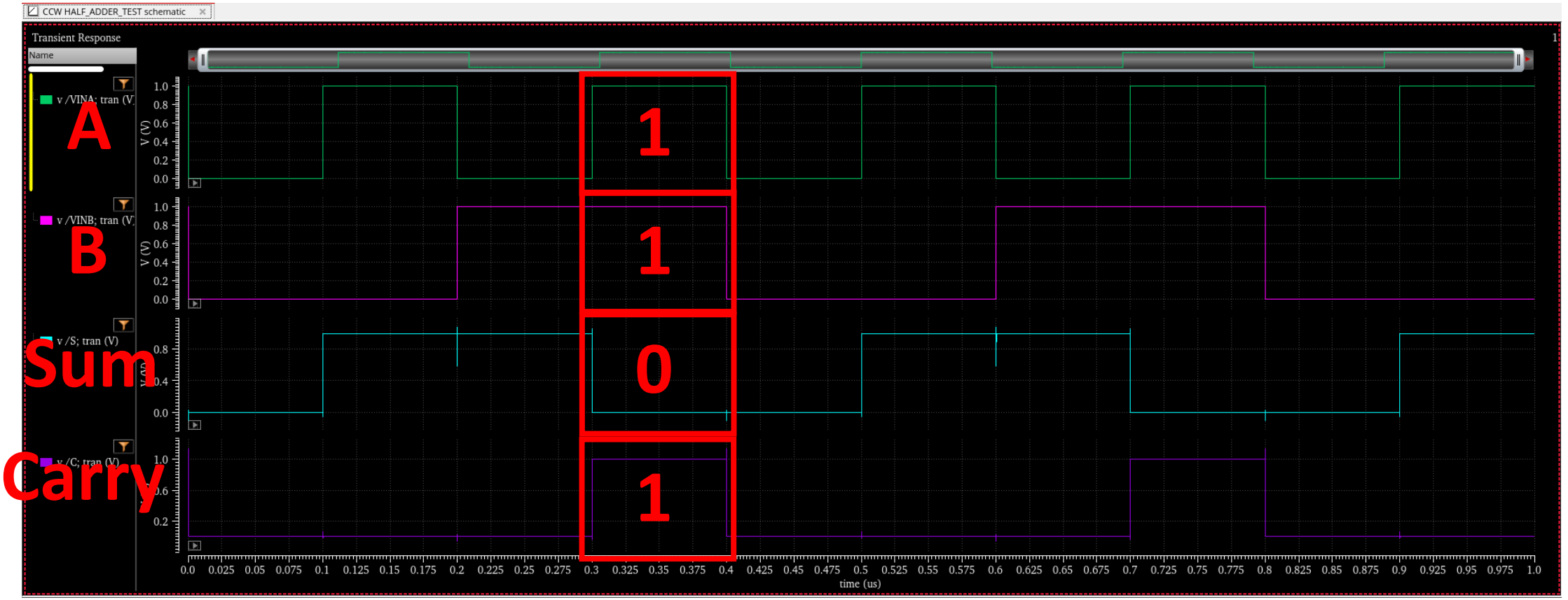
Half Adder 2



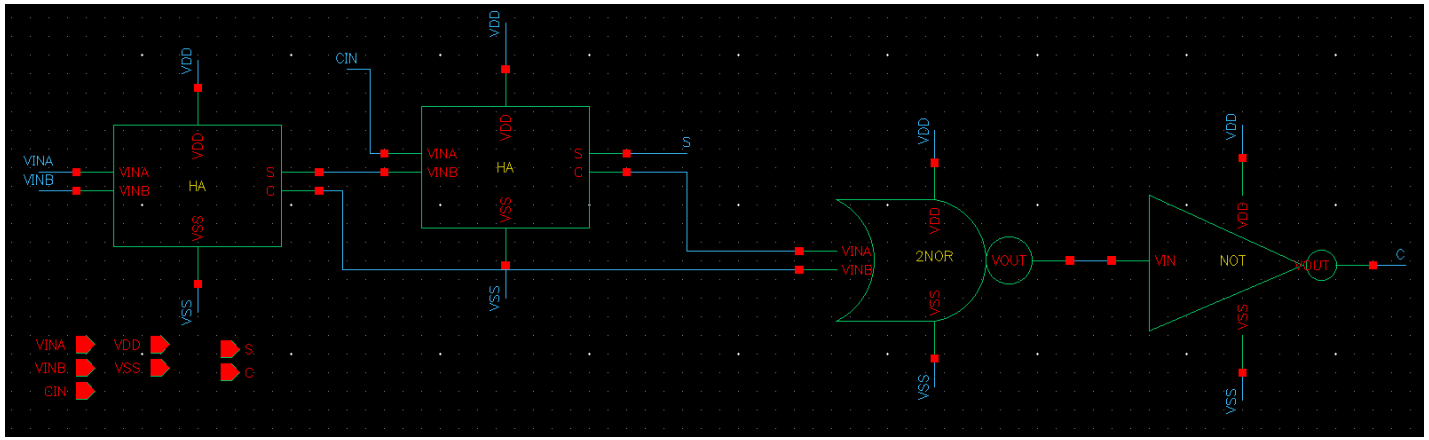


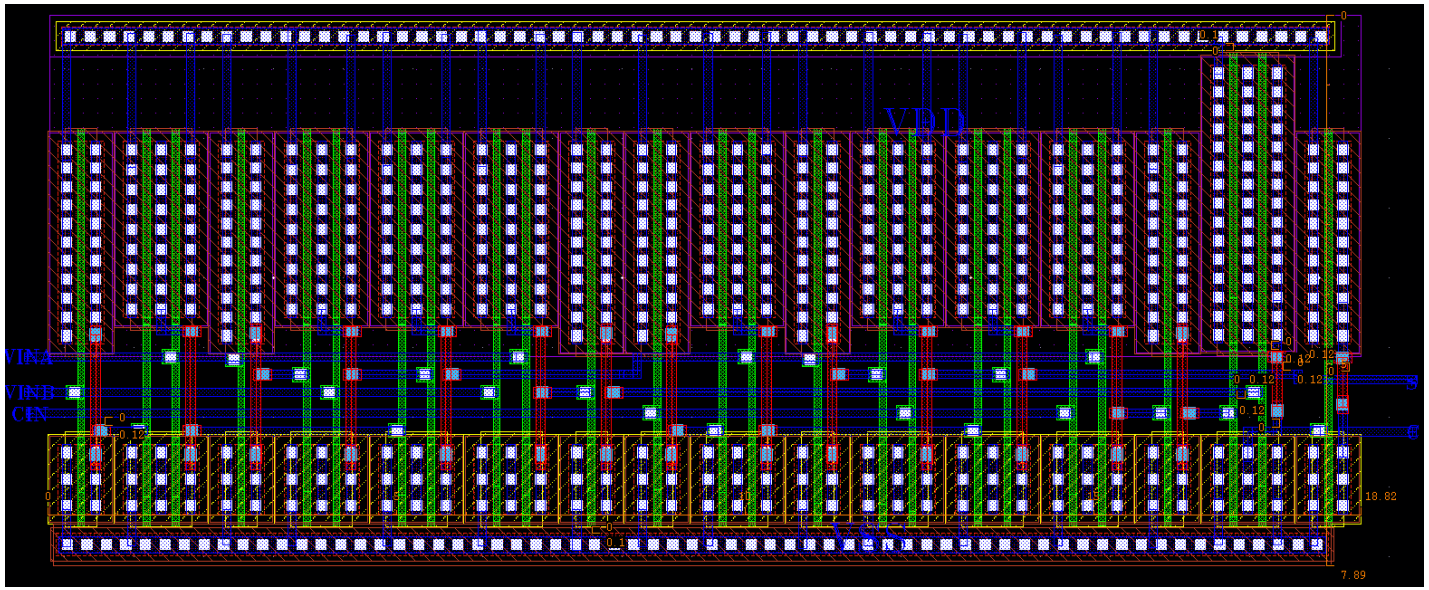
[Half Adder]

Simulation



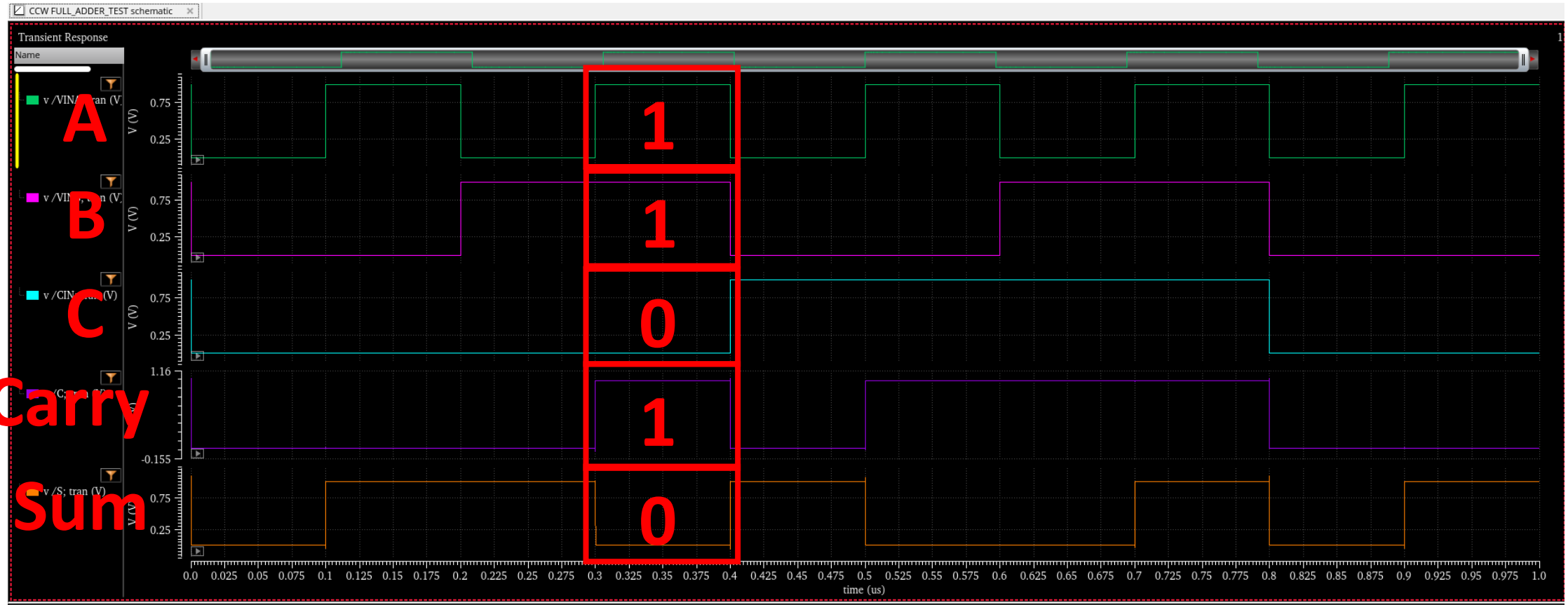
Full Adder


VDD
CIN
VINA
VINB
HA
S
C
VSS
2NOR
VOUT
VIN
NOT
VDD
VSS

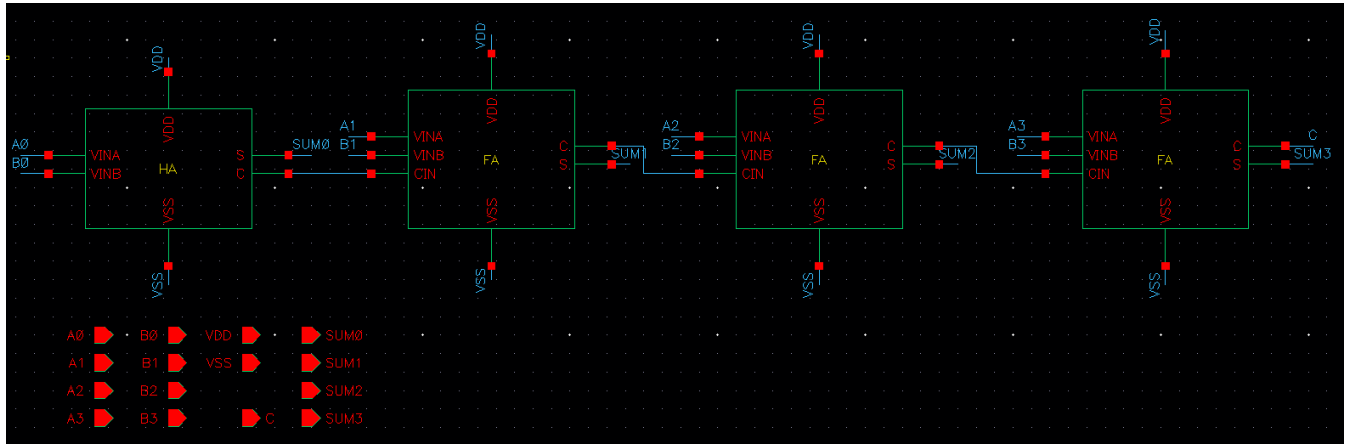

VDD
VINA
VINB
CIN
VSS
18.82
7.89

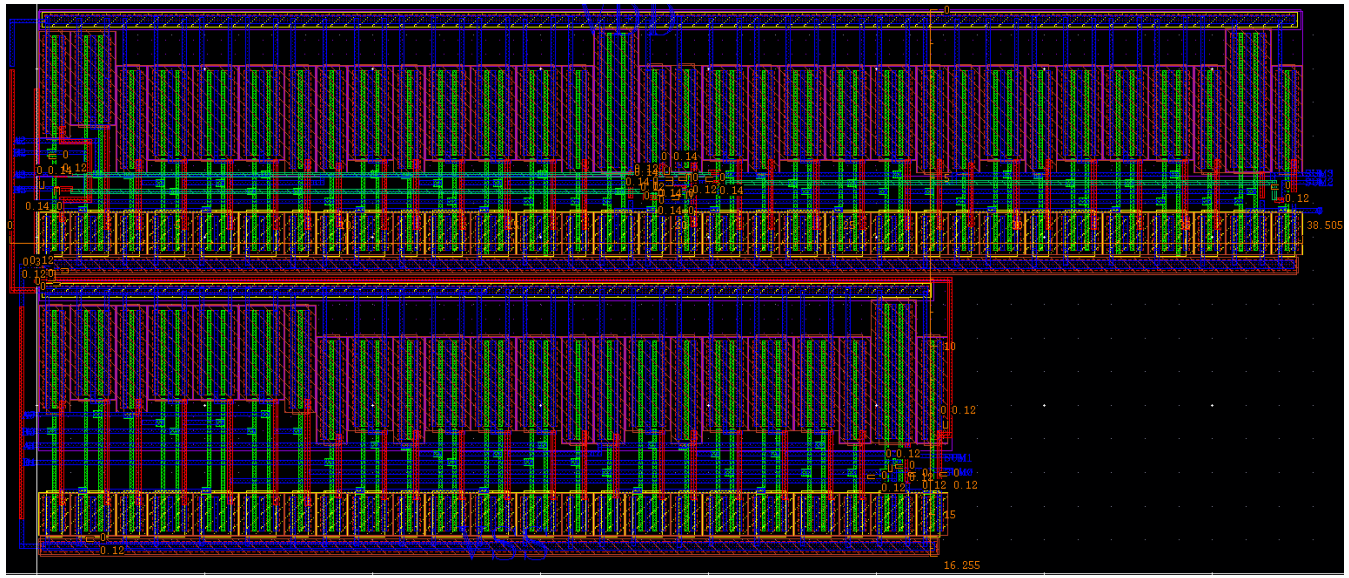
[Full Adder]

Simulation



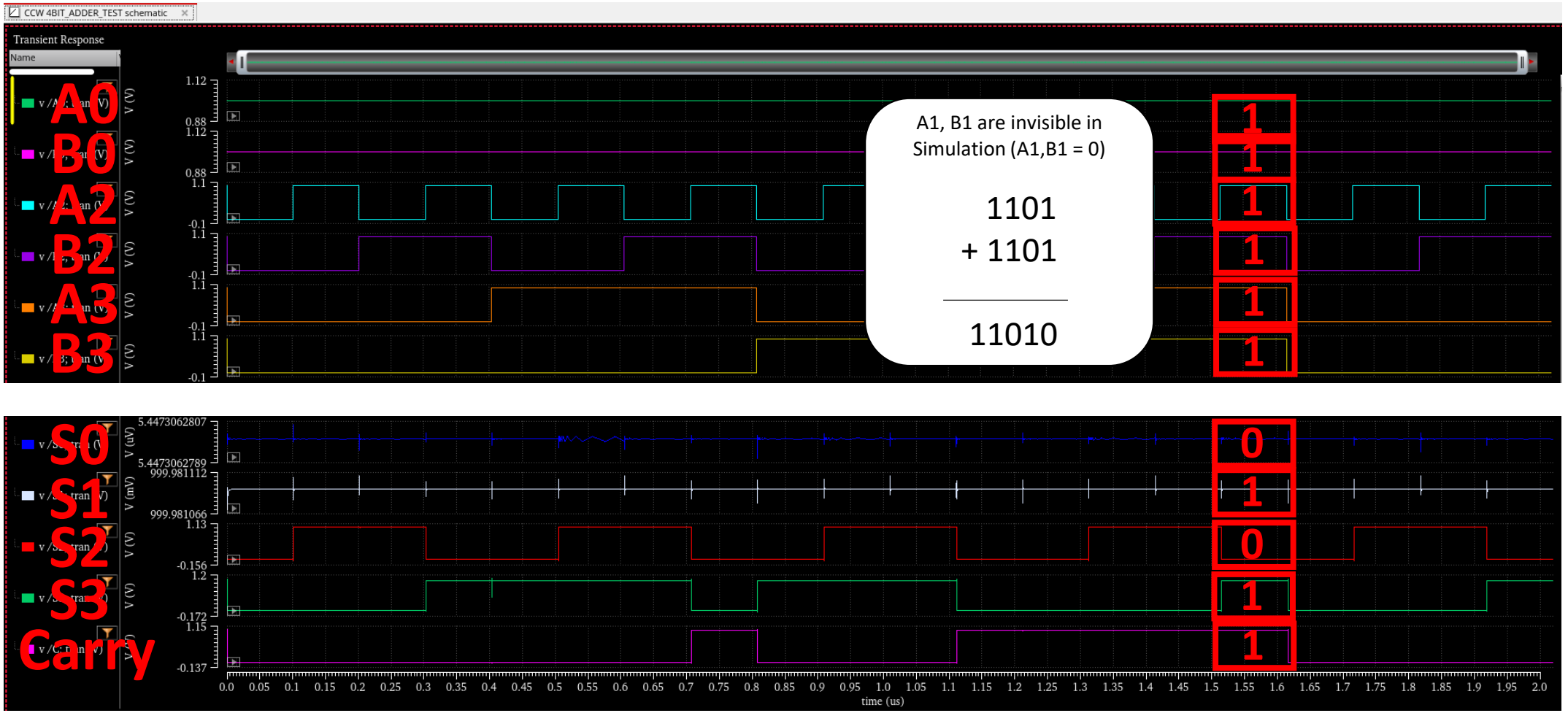
4-Bit Adder


A0
B0
VINA
VINB
HA
VDD
VSS
S
C
SUM0
A1
B1
VINA
VINB
CIN
FA
SUM1
A2
B2
SUM2
A3
B3
SUM3
A0 B0 VDD SUM0
A1 B1 VSS SUM1
A2 B2 SUM2
A3 B3 C SUM3

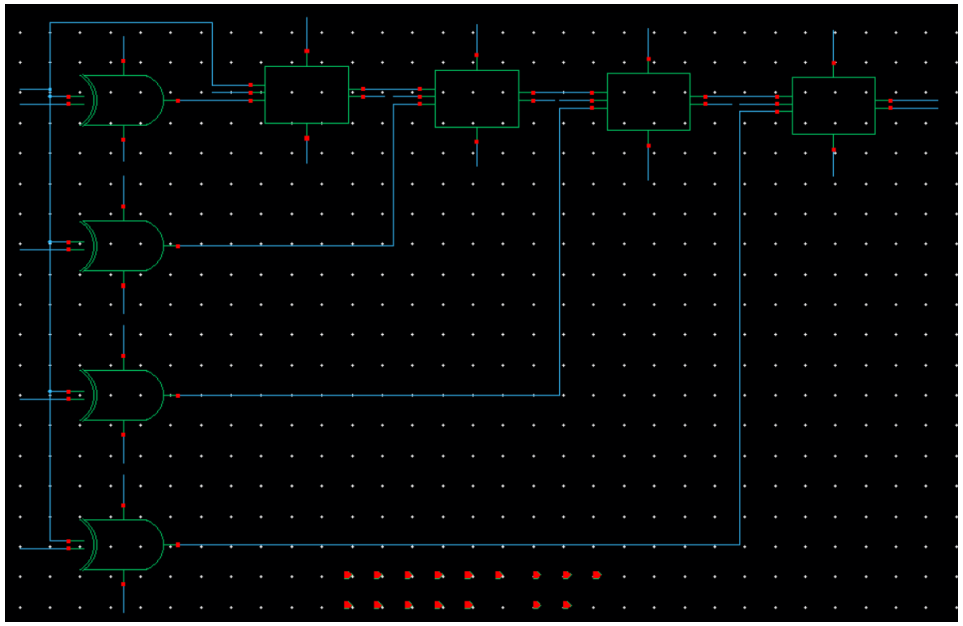


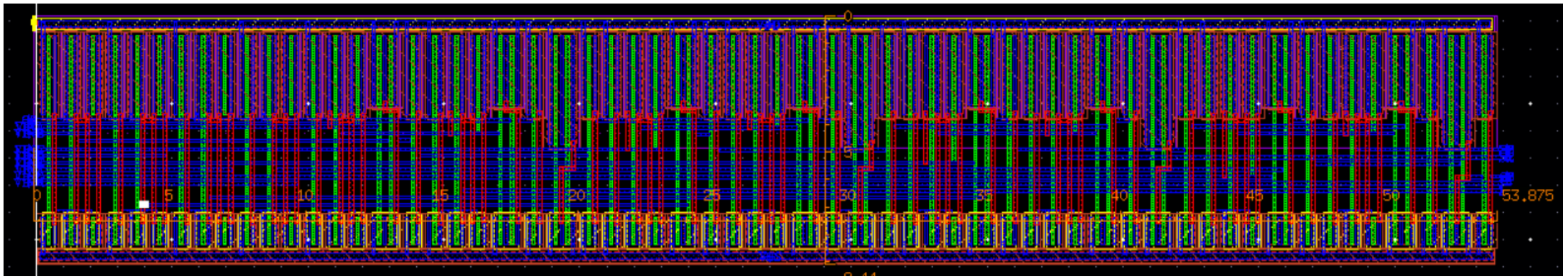
[4-Bit Adder]

Simulation



4Bit Adder-Subtractor



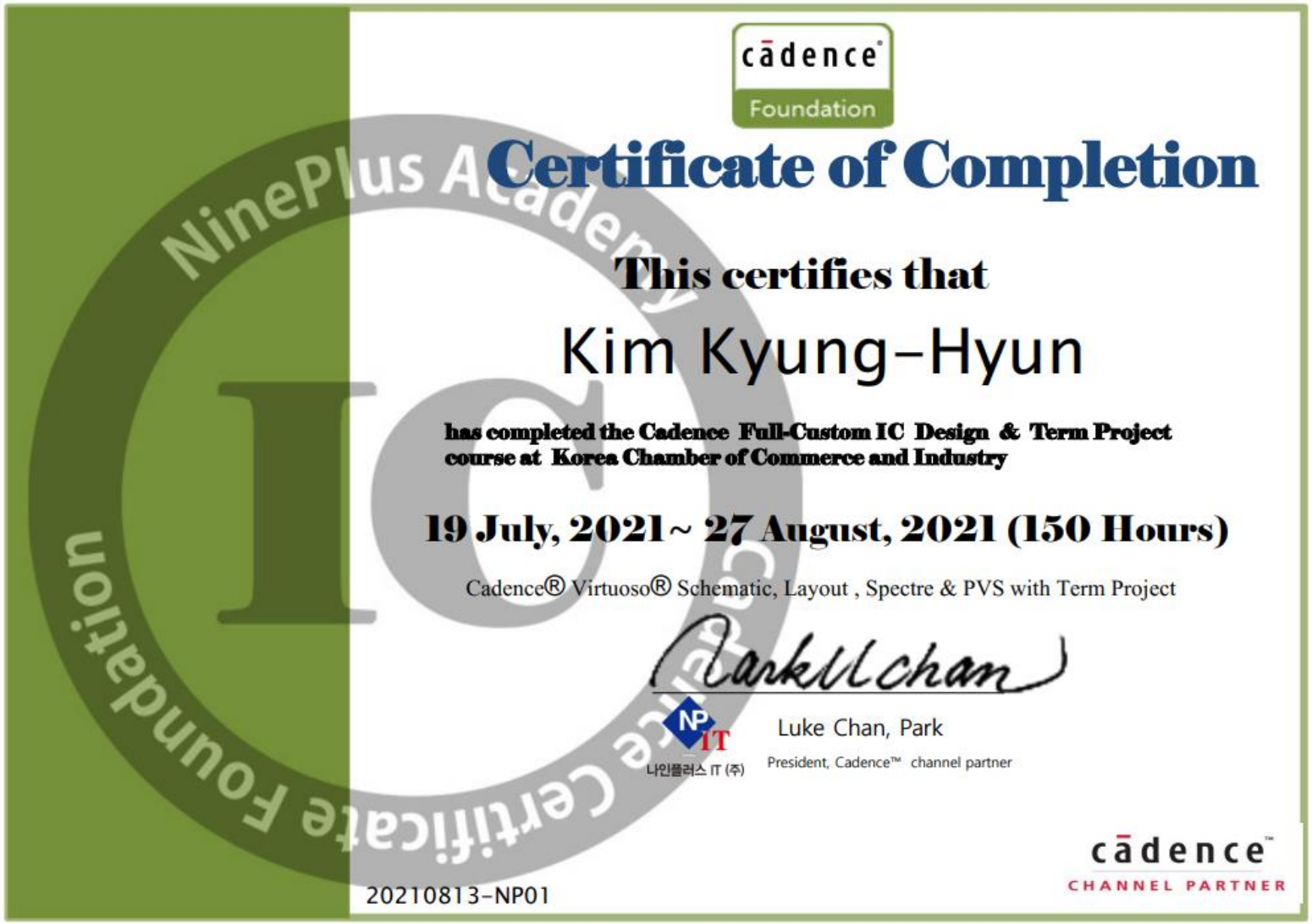


Adder

[4Bit Adder-Subtractor]

Simulation

A certificate of completion



Contact

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