

FULL_ADDER

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순서

- Full_Adder
- Circuit design
- Schematic
- Circuit simulation
- Layout
- DRC, LVS

Full Adder

- 덧셈을 수행하는 연산 장치이자 디지털 회로
- 2 개의 반가산기와 OR GATE로 구성

$$S = A \oplus B \oplus C_{in}, C_{out} = (A \cdot B) + C_{in}(A \oplus B)$$

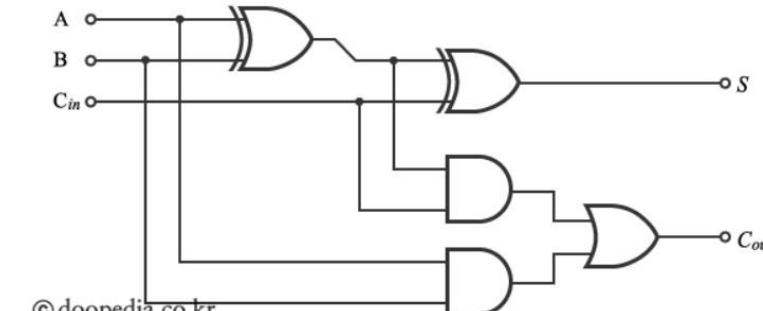
전가산기 진리표

입 력			출 력	
A	B	C_{in}	합 S	자리 올림 C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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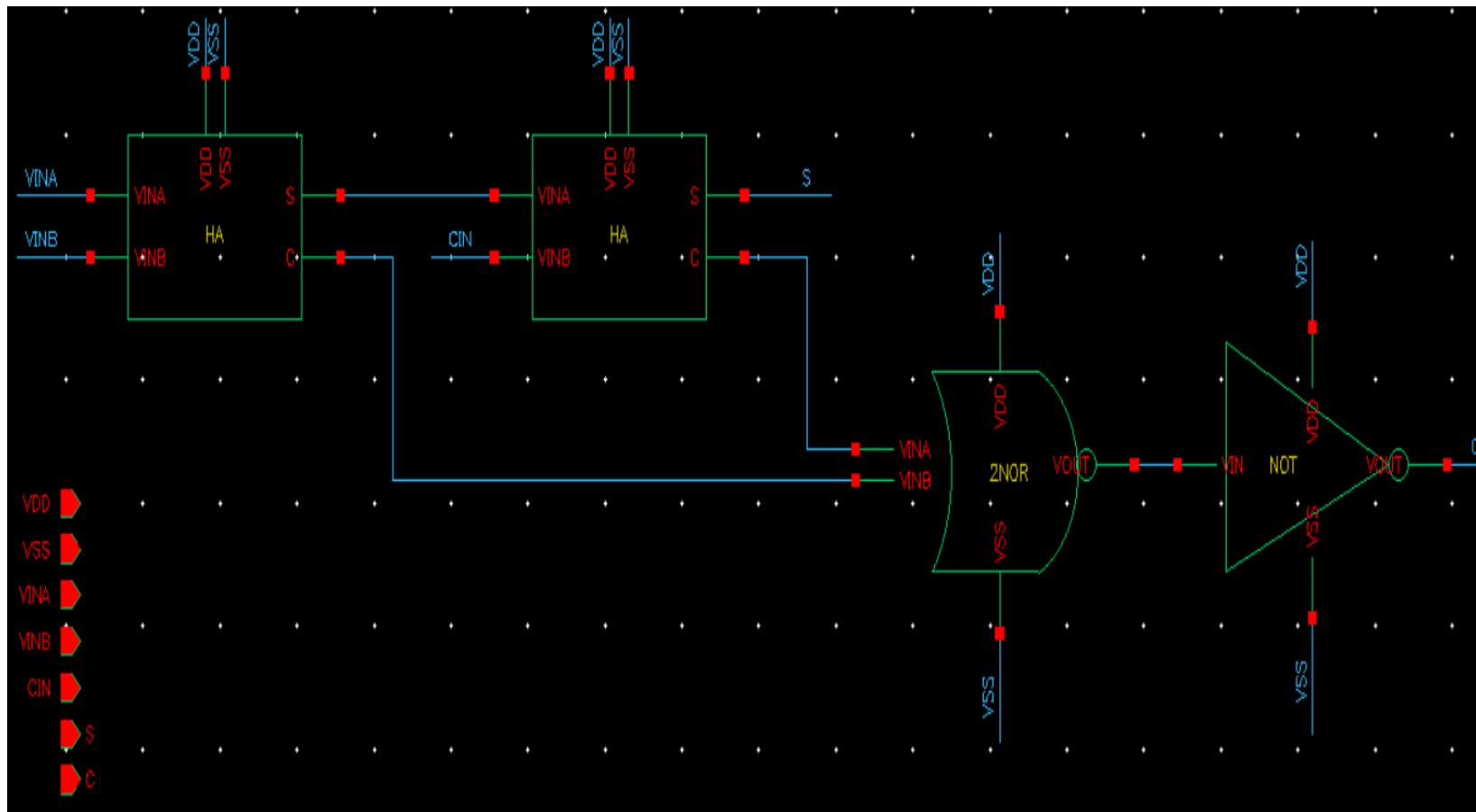


전가산기 논리 회로

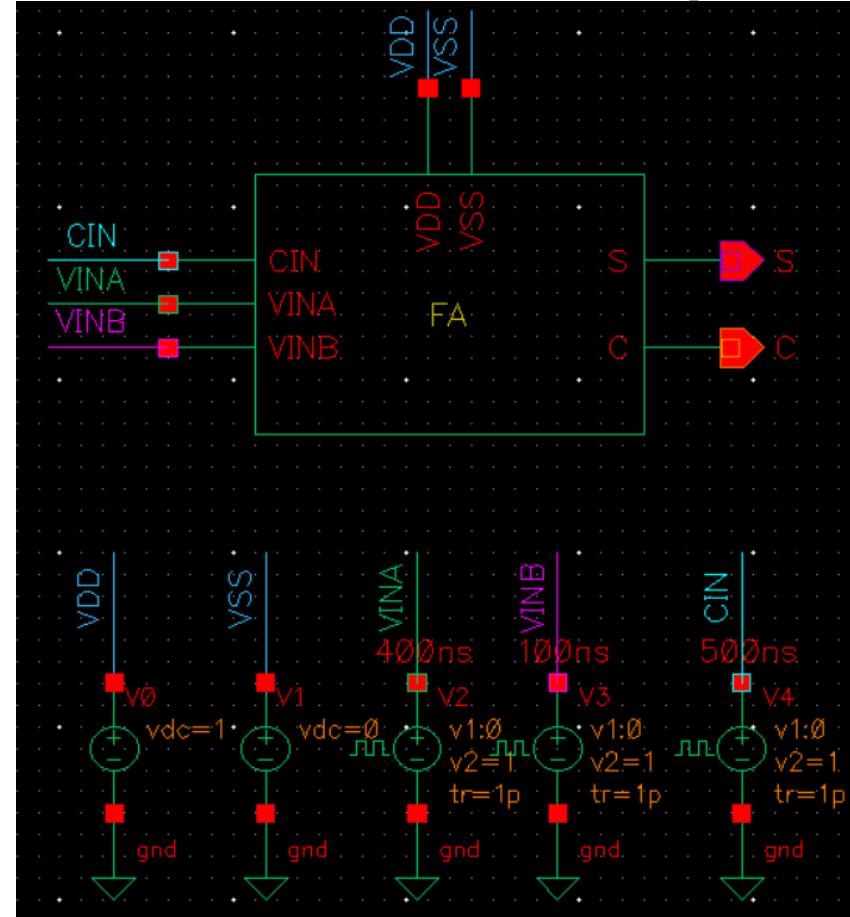


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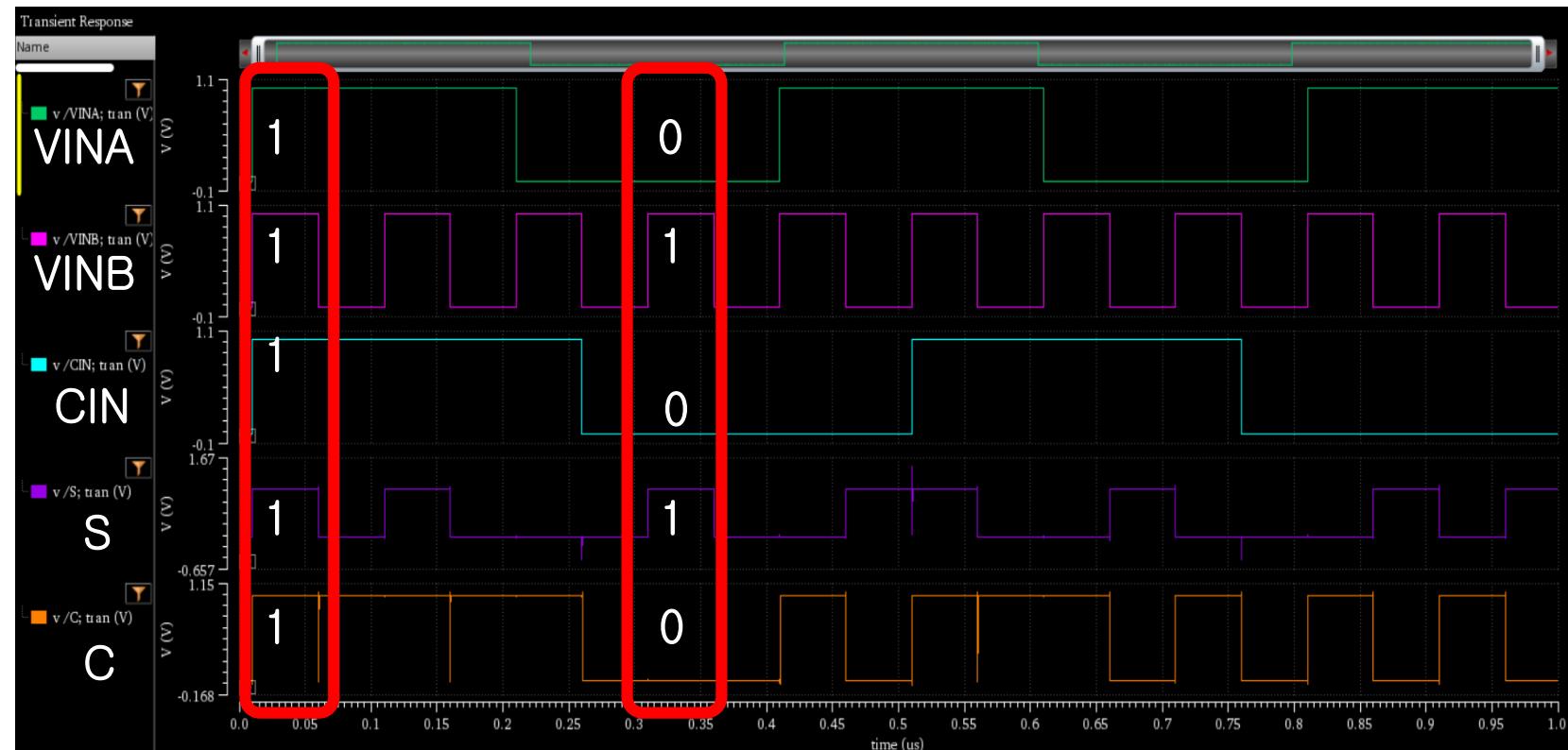
Schematic(Logic gate)



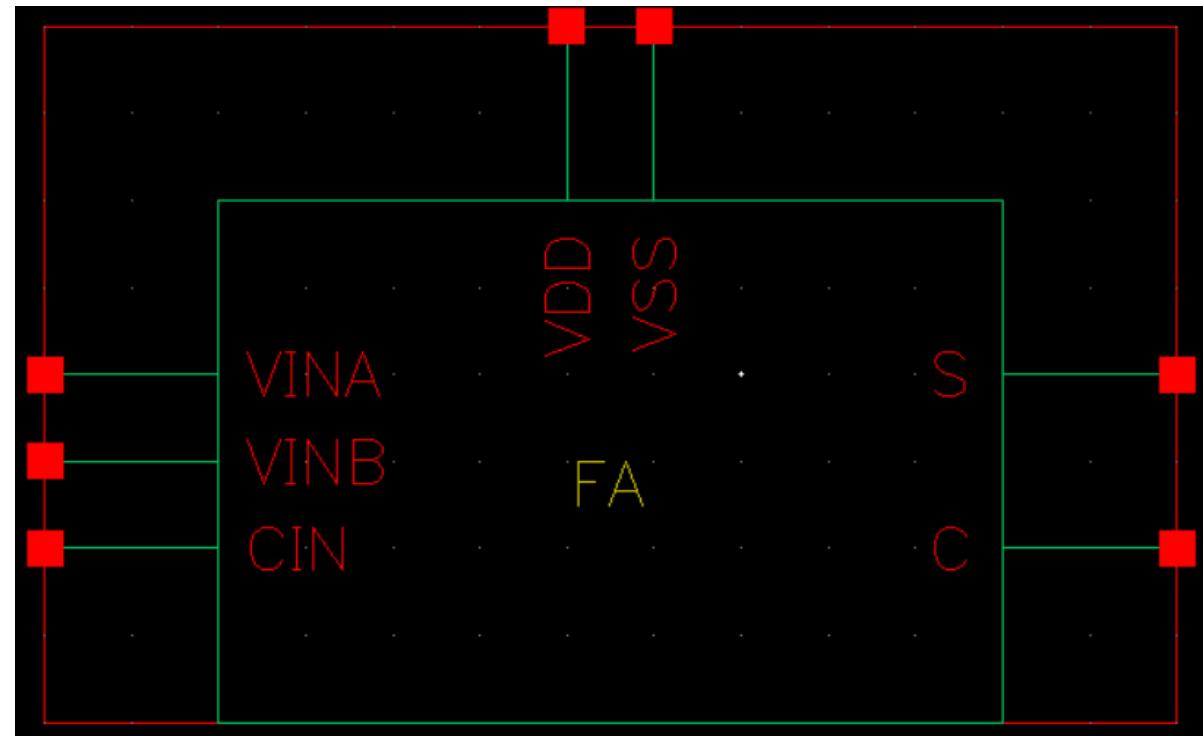
Full Adder simulation setup



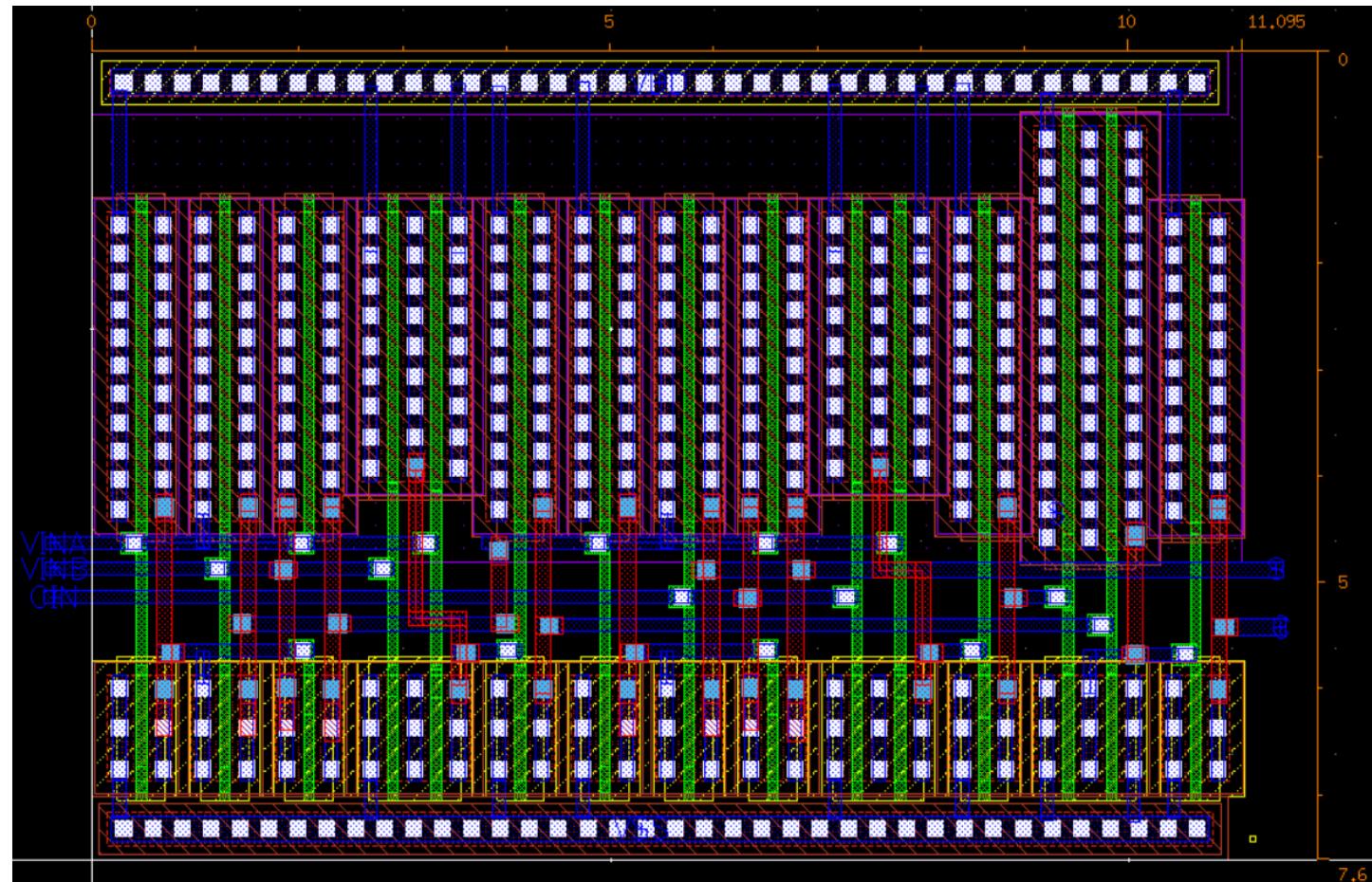
Wave Form



Full Adder 블록 외부 PORT

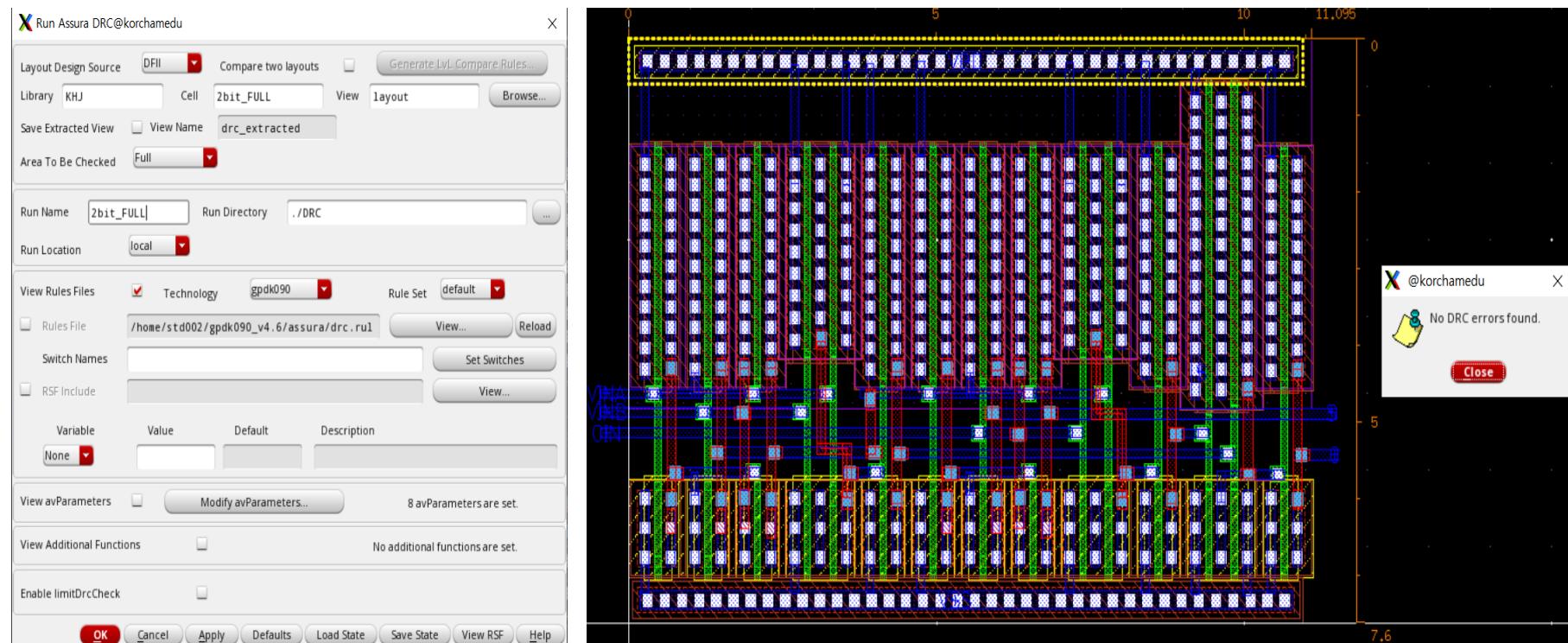


Full Adder (Layout)



$$\text{Area} : 11.095 \times 7.6 = 84.322 \mu\text{m}^2$$

Full Adder (DRC)



Full Adder (LVS)

LVS Debug - 2bit_FULL@korchamedu

File View Options Tools Help

Cell List (sch || lay) Extract Compare Summary (sch || lay)

*** Schematic and Layout Match

Open Schematic Cell... Open Layout Cell... Open Tool...

Run Assura LVS@korchamedu

Schematic Design Source DFII Use Existing Netlist Netlisting Options...
Library KHJ Cell 2bit_FULL View schematic Browse...

Layout Design Source DFII Use Existing Extracted Netlist
Library KHJ Cell 2bit_FULL View layout Browse...

Run Name 2bit_FULL Run Directory ./LVS
Run Location local

View Rules Files Technology -undefined- Rule Set default
Extract Rules ./assura/extract.rul View... Edit... Reload
Compare Rules View... Edit...
Switch Names Set Switches
Binding File(s) View... Edit...
RSF Include View... Edit...
Variable Value Default Description None
View avParameters Modify avParameters... 1 avParameter is set.
View avCompareRules Modify avCompareRules... No avCompare rules are set.
View Additional Functions No additional functions are set.

OK Cancel Apply Defaults Load State Save State View RSP Help

Run: "2bit_FULL" @korchamedu

Run: "2bit_FULL" from /home/std002/gdk090_v4.6/LVS

Schematic and Layout Match
You currently have an open run (project).

Do you want to close current project and view the results of new run?

Summary of LVS Issues

Extraction Information:

- 0 cells have 0 mal-formed device problems
- 0 cells have 0 label short problems
- 0 cells have 0 label open problems

Comparison Information:

- 0 cells have 0 Net mismatches
- 0 cells have 0 Device mismatches
- 0 cells have 0 Pin mismatches
- 0 cells have 0 Parameter mismatches

ELW Information:

- Total DRC violations: 0

Yes No Help