

Cadence
PCB Design for CCS

Distance Measurement Circuit using by Ultrasonic Sensor

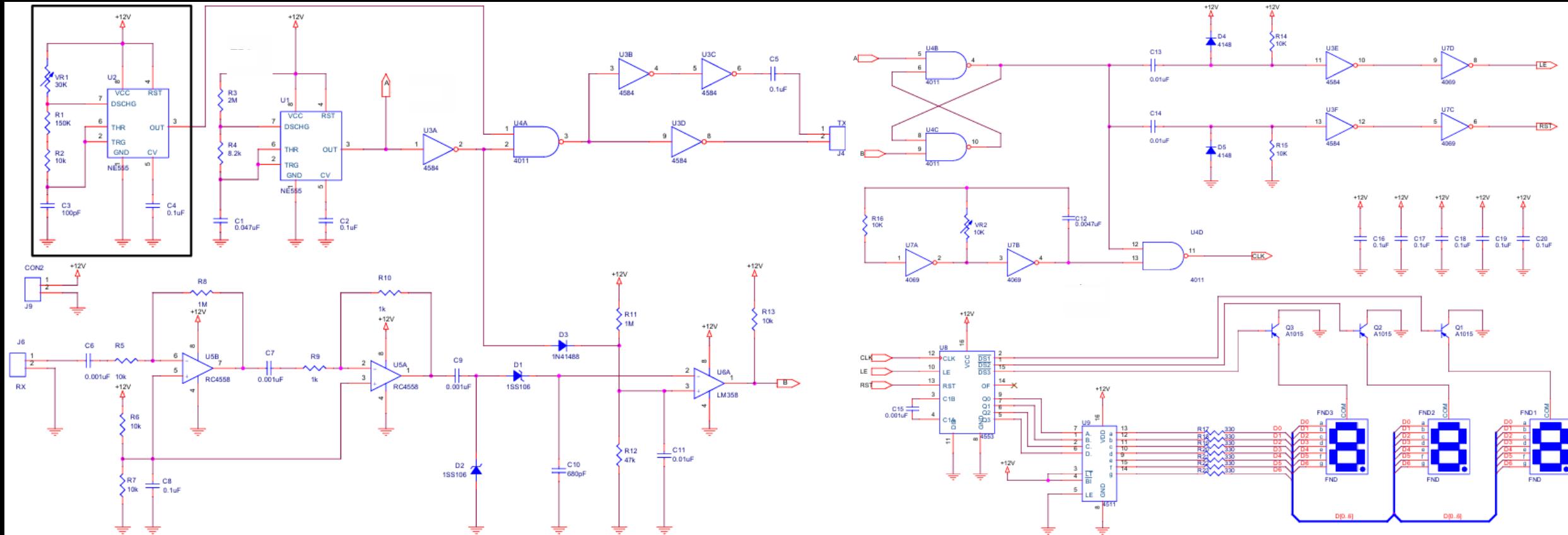
SHIN HONG MIN

Contents

- Summary
- Introduction
- Capture CIS user's guide
- Circuit Design & Measurement
- Conclusions
- Schematic
- Procedure of PCB Design

Summary

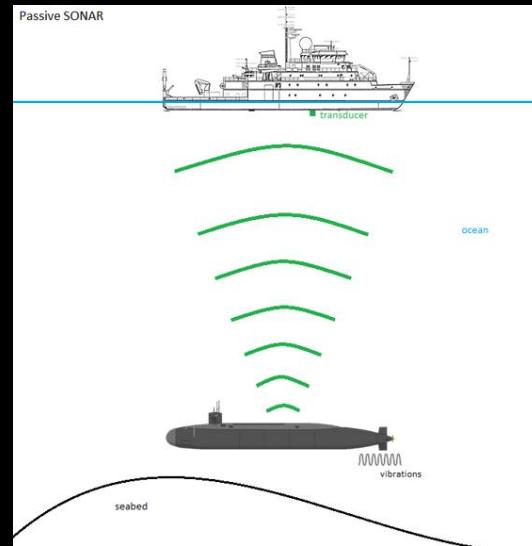
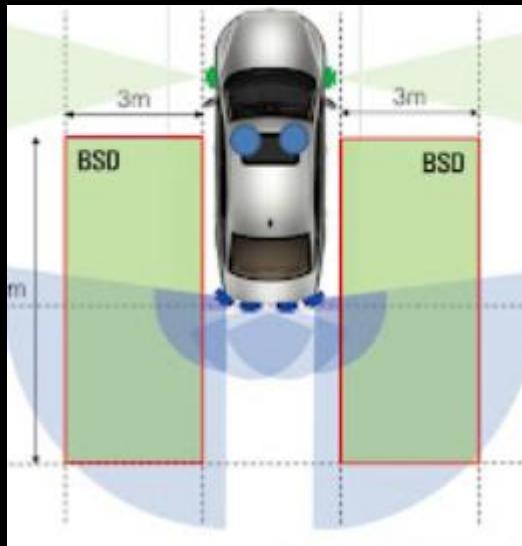
1. Full Circuit Diagram



Introduction

1. Background of Project

- 1) Developing a multi-purpose ultrasonic sensor distance measurement circuit
- 2) Understanding and researching the circuit
- 3) Identifying and addressing issues



Introduction

2. Project Goal

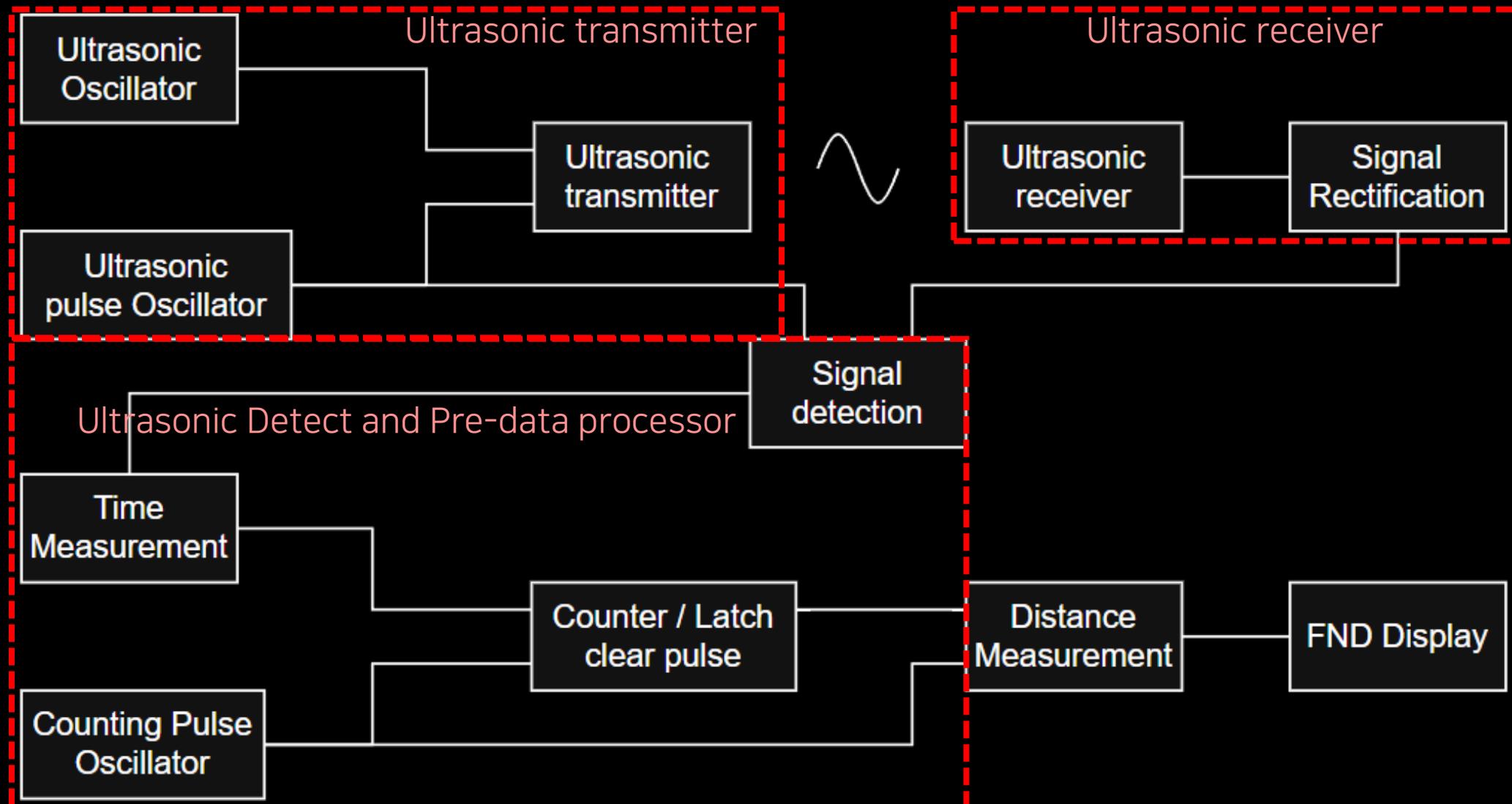
Distance Measurement Circuit using by Ultrasonic Sensor

1. Minimum distance : 30cm
2. Maximum distance : 1m
3. Measure Unit : [cm]
4. Realtime Measurement

1. Power Supply : 12V
2. Design TP1 frequency to 40kHz by adjusting VR1
3. Design TP2 frequency to 17.2kHz by adjusting VR2
4. FND1 > 1's place, FND2 > 10's place, FND3 > 100's place
5. 100[cm], 50[cm], 30[cm] distance measurement

Introduction

3. Block Diagram



Introduction

4. BOM List

Type	Name	Quantity	Type	Name	Quantity	Type	Name	Quantity
Chip IC	NE555(SMD TYPE)	1	Register	2[MΩ], ¼[W], 1%	1	Ceramic Cap	0.01[μF]	3
IC	NE555	1	Register	8.2[kΩ], ¼[W], 1%	1	Ceramic Cap	0.001[μF]	4
IC	4584	1	Register	1[MΩ], ¼[W], 1%	2	Ceramic Cap	0.0047[μF]	1
IC	4011	1	Register	47[kΩ], ¼[W], 1%	1	Variable Register	47[kΩ]	1
IC	RC4558	1	Register	1[kΩ], ¼[W], 1%	2	Variable Register	10[kΩ]	1
IC	LM358	1	Chip Register	SMD 330[Ω] (2012)	7	Transistor	A1015	3
IC	4069	1	Mylar Cap	0.047[μF]	1	FND	500	3
IC	4553	1	Ceramic Cap	680[pF]	1	Ultrasonic Sensor	SE-400ST160	1
IC	4511	1	Ceramic Cap	100[pF]	1	Ultrasonic Sensor	SE-400SR160	1
IC Socket	8PIN(DIP)	3	Ceramic Cap	0.1[μF]	9	Diode	1SS106	2
IC Socket	14PIN(DIP)	3				Diode	1N4148	3
IC Socket	16PIN(DIP)	2				Connector	Green Conn(2P)	1
Register	150[kΩ], ¼[W], 1%	1						
Register	10[kΩ], ¼[W], 1%	8						

Introduction

5. Used Equipment



OrCAD ver 17.2



Multimeter



Oscilloscope



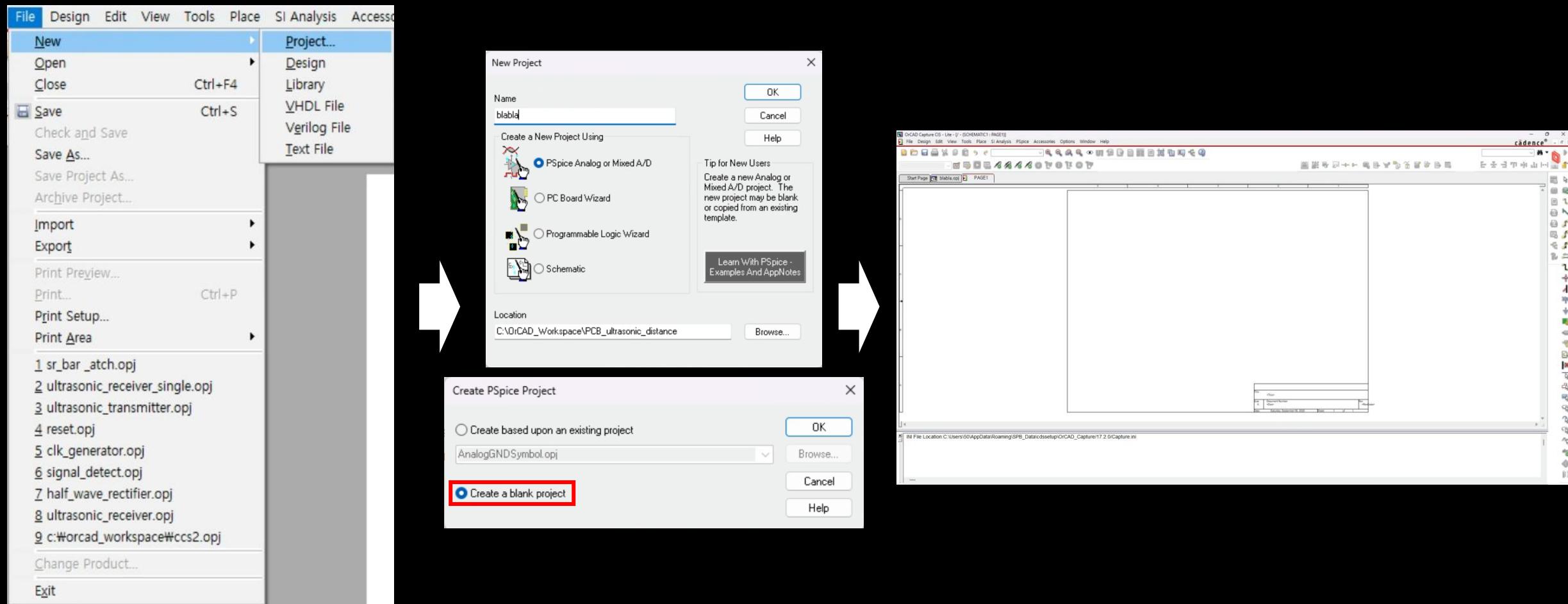
Tool SET



Power Supply

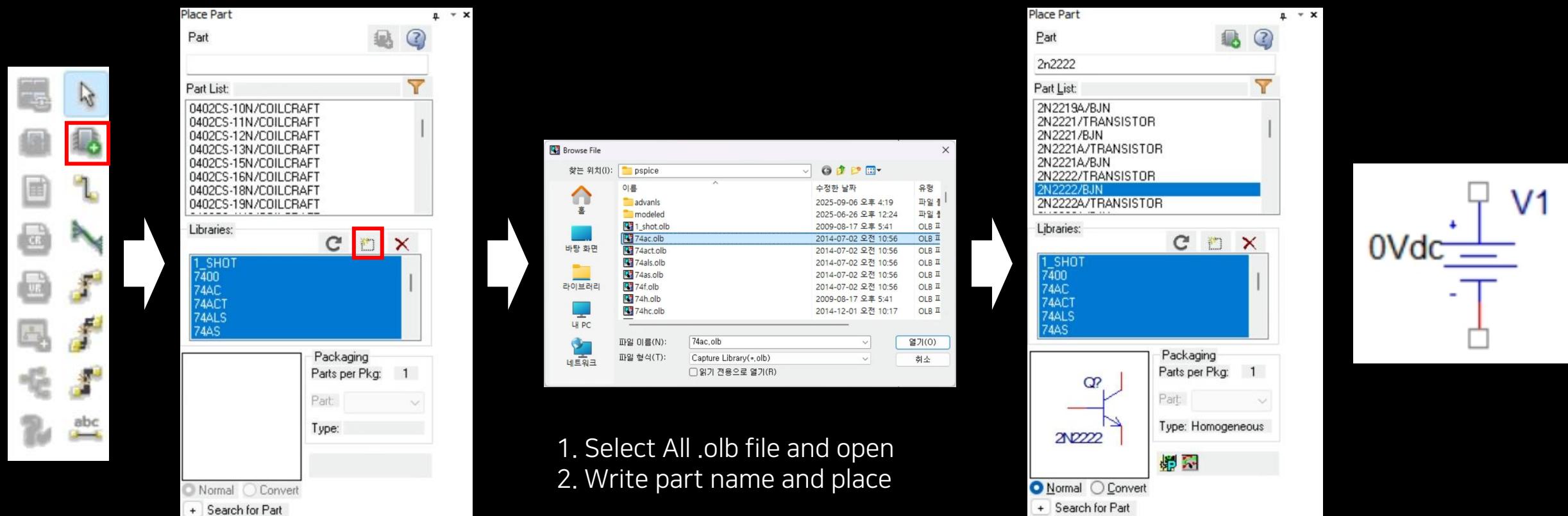
Capture CIS user's guide

1. Create New Project



Capture CIS user's guide

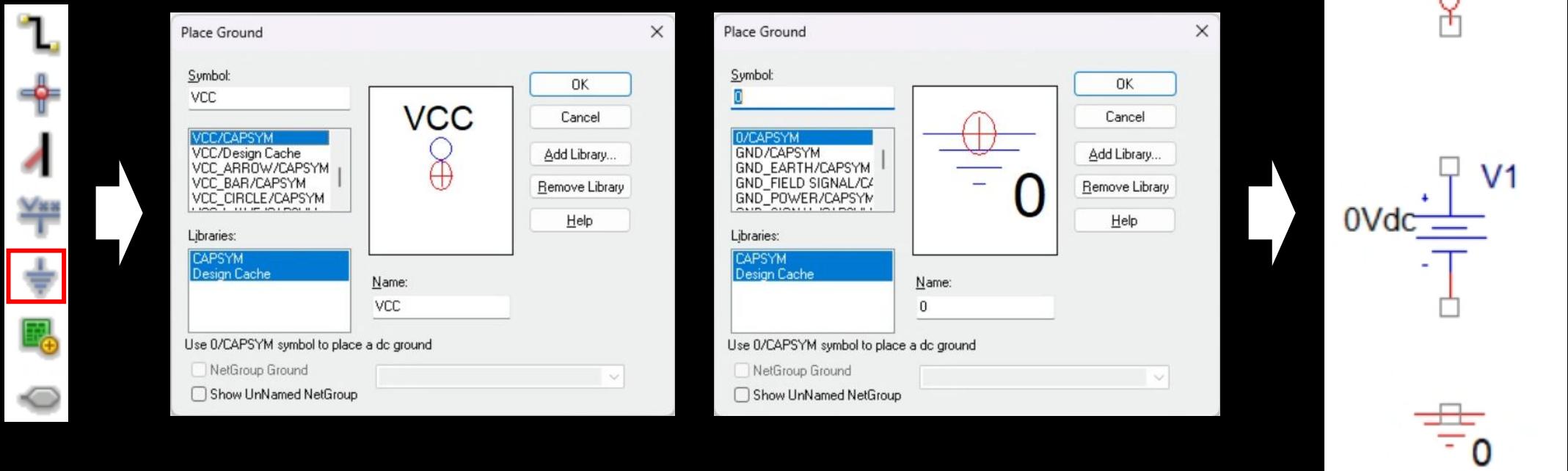
2. Place to parts



1. Select All .olb file and open
2. Write part name and place

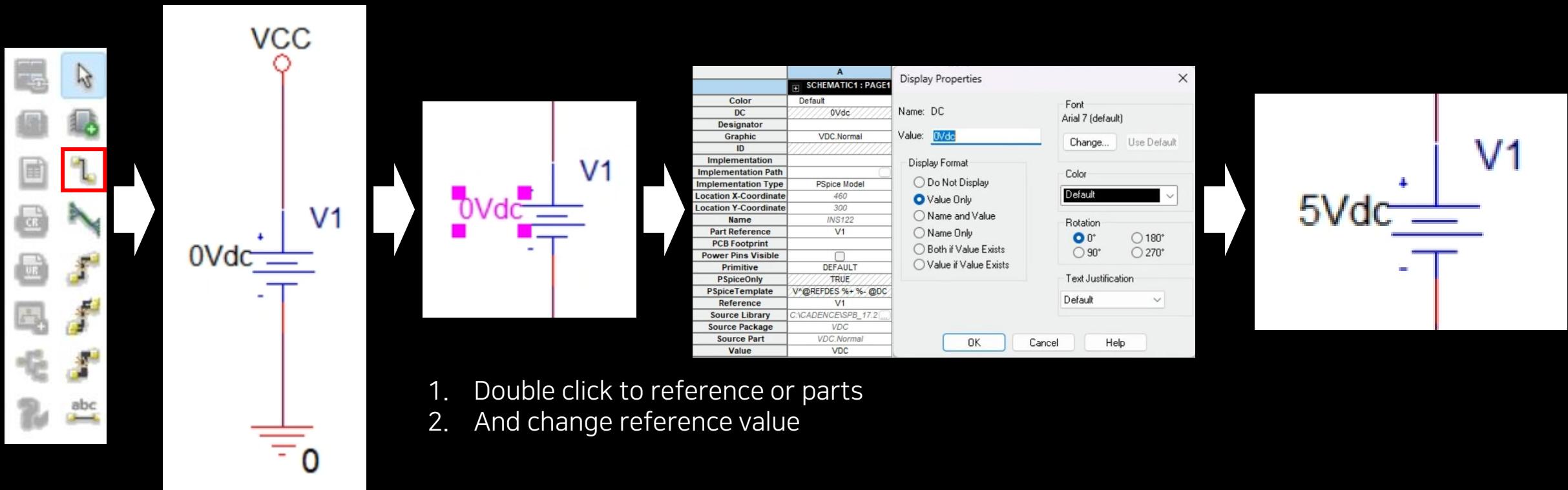
Capture CIS user's guide

3. Place VCC and GND



Capture CIS user's guide

4. Connect to parts and change to reference



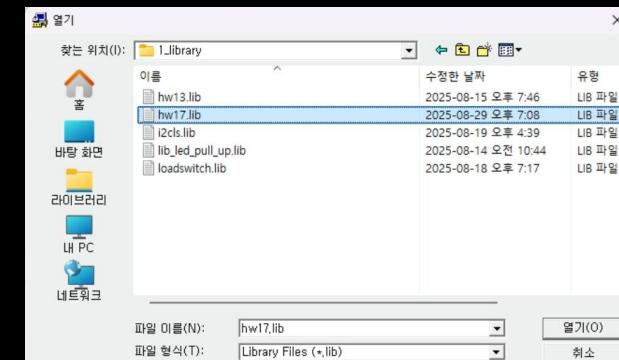
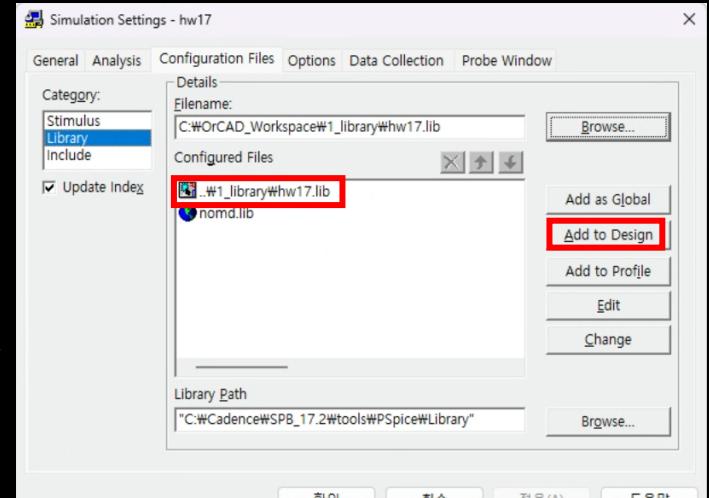
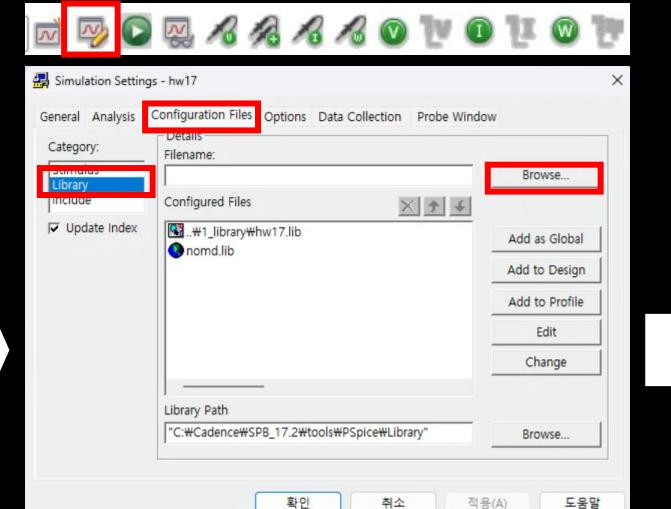
1. Double click to reference or parts
2. And change reference value

Capture CIS user's guide

5. Import library

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* RC4558 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
* CREATED USING PARTS RELEASE 4.01 ON 09/08/89 AT 16:07
* (REV N/A) SUPPLY VOLTAGE: +/-15V
* CONNECTIONS: NON-INVERTING INPUT
*   | INVERTING INPUT
*   || POSITIVE POWER SUPPLY
*   ||| NEGATIVE POWER SUPPLY
*   ||| OUTPUT
*   |||
.SUBCKT RC4558 1 2 3 4 5
*
C1 11 12 2.664E-12
C2 6 7 20.00E-12
DC 5 53 DX
DE 54 5 DX
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EGND 99 0 POLY(2) (3.0) (4.0) 0 .5 .
FB 7 99 POLY(5) VB VC VE VLP VLN 0 6.365E6 -6E6 6E6 6E6 -6E6
GA 6 0 11 12 418.0E-6
GCM 0 6 10 99 6.705E-9
IEE 3 10 DC 34.28E-6
HLM 90 0 VLIM 1K
Q1 11 2 13 QX
Q2 12 1 14 QX
R2 6 9 100.0E3
RC1 4 11 2.652E3
RC2 4 12 2.652E3
RE1 13 10 1.122E3
RE2 14 10 1.122E3
REE 10 99 5.834E6
RO1 8 5 125
RO2 7 99 125
RP 3 4 24.67E3
VB 9 0 DC 0
VC 3 53 DC 2.600
VE 54 4 DC 2.600
VLIM 7 8 DC 0
VLP 91 0 DC 25
VLN 0 92 DC 25
.MODEL DX D(IIS=800.0E-18)
.MODEL QX PNP(IIS=800.0E-18 BF=121.4)
.ENDS
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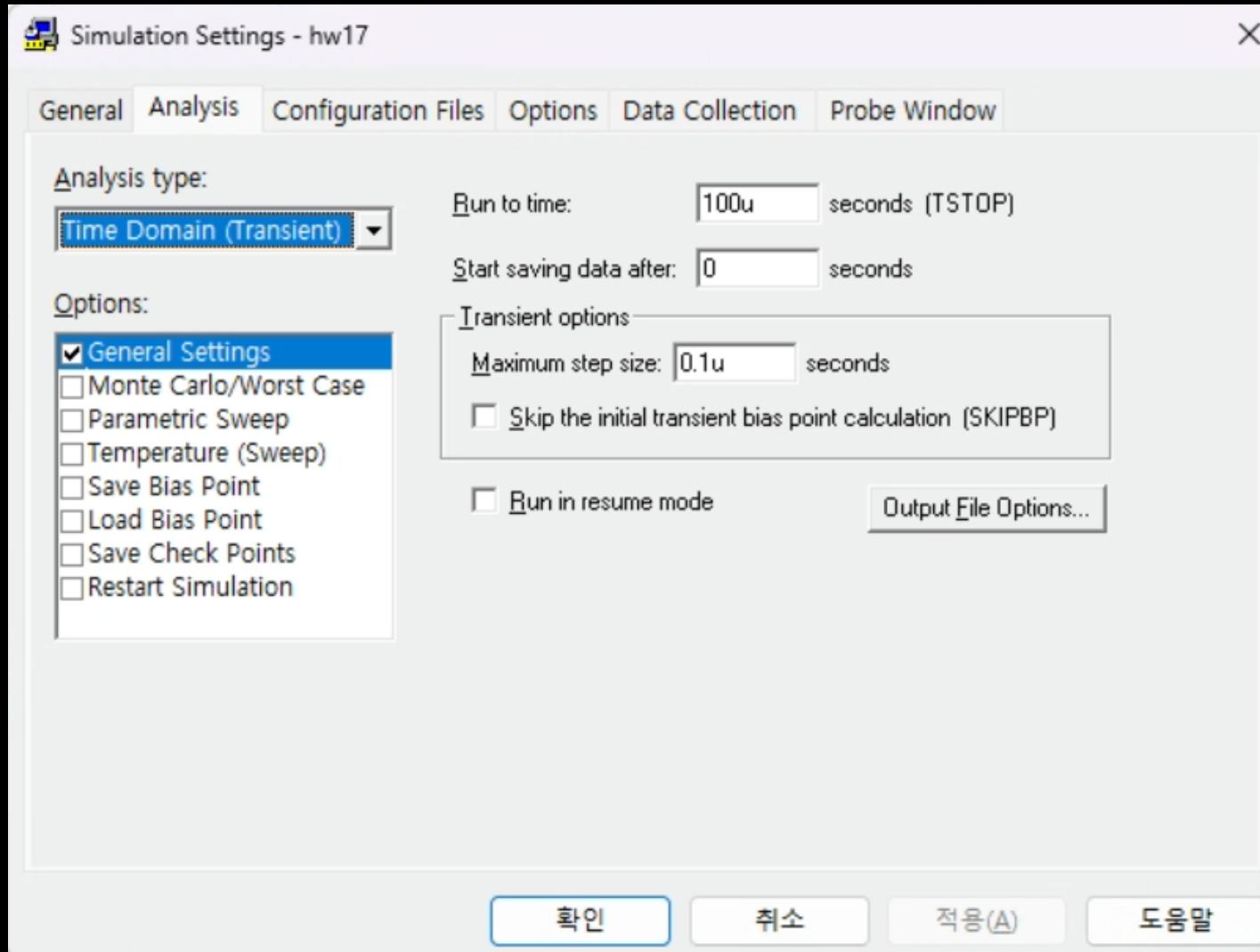
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*****
* proj name : hw17
* supervisor : HONGMIN
* manager : HONGMIN
* start day : 2025-08-21
* final modified day/manager : 2025-08-21/HONGMIN
*****
* RC4558 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
* CREATED USING PARTS RELEASE 4.01 ON 09/08/89 AT 16:07
* (REV N/A) SUPPLY VOLTAGE: +/-15V
* CONNECTIONS: NON-INVERTING INPUT
*   | INVERTING INPUT
*   || POSITIVE POWER SUPPLY
*   ||| NEGATIVE POWER SUPPLY
*   ||| OUTPUT
*   |||
.SUBCKT RC4558 1 2 3 4 5
*
C1 11 12 2.664E-12
C2 6 7 20.00E-12
DC 5 53 DX
DE 54 5 DX
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EGND 99 0 POLY(2) (3.0) (4.0) 0 .5 .
FB 7 99 POLY(5) VB VC VE VLP VLN 0 6.365E6 -6E6 6E6 6E6 -6E6
GA 6 0 11 12 418.0E-6
GCM 0 6 10 99 6.705E-9
IEE 3 10 DC 34.28E-6
HLM 90 0 VLIM 1K
Q1 11 2 13 QX
Q2 12 1 14 QX
R2 6 9 100.0E3
RC1 4 11 2.652E3
RC2 4 12 2.652E3
RE1 13 10 1.122E3
RE2 14 10 1.122E3
REE 10 99 5.834E6
RO1 8 5 125
RO2 7 99 125
RP 3 4 24.67E3
VB 9 0 DC 0
VC 3 53 DC 2.600
VE 54 4 DC 2.600
VLIM 7 8 DC 0
VLP 91 0 DC 25
VLN 0 92 DC 25
.MODEL DX D(IIS=800.0E-18)
.MODEL QX PNP(IIS=800.0E-18 BF=121.4)
.ENDS
```



1. Select what I want to place parts in schematic and go to parts manufactory website
2. Download orcad library(pspice) file
3. Make a new library file and copy to pspice code -> save file to .lib
4. Add to lib file in Simulation setting

Capture CIS user's guide

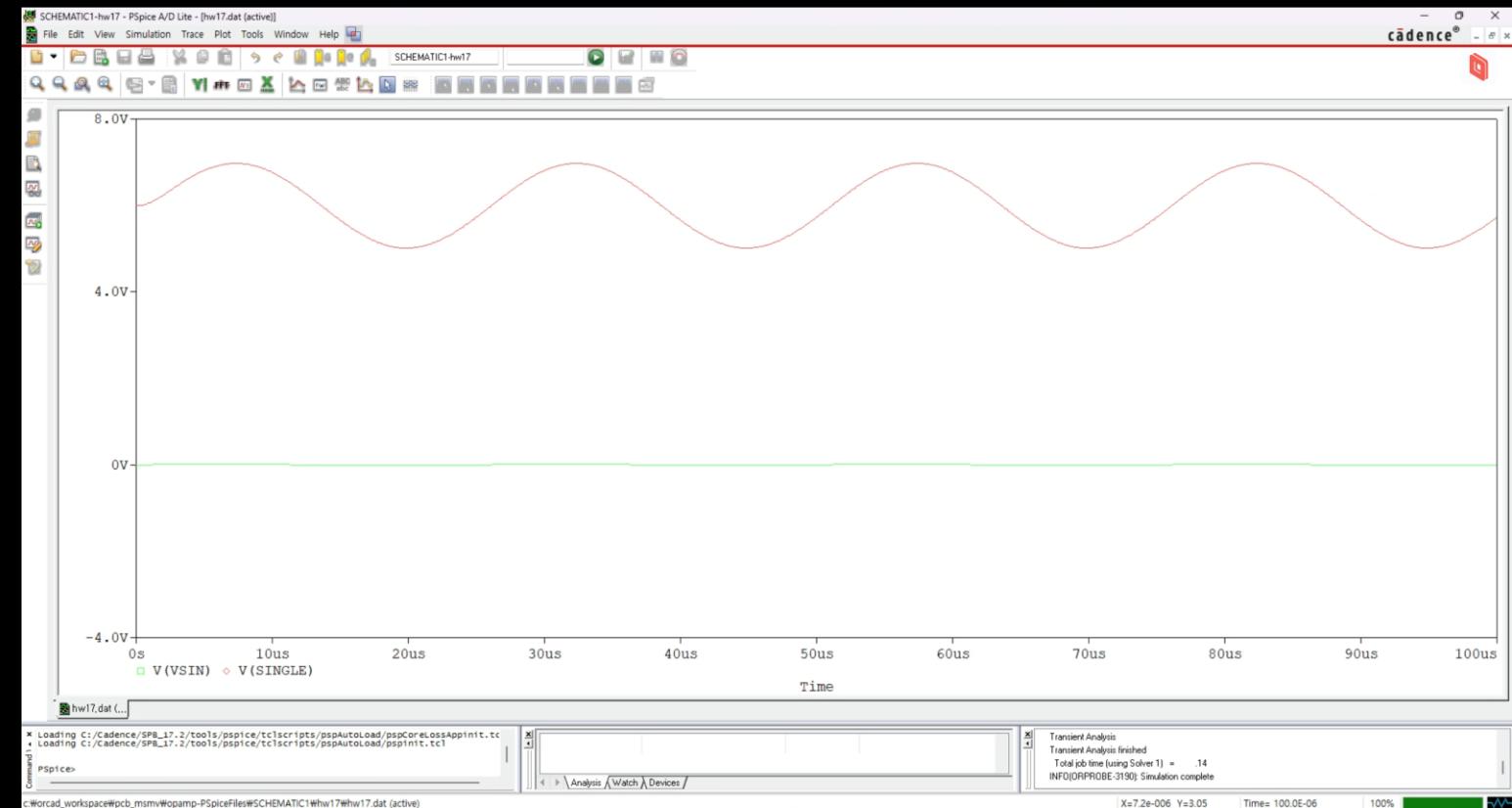
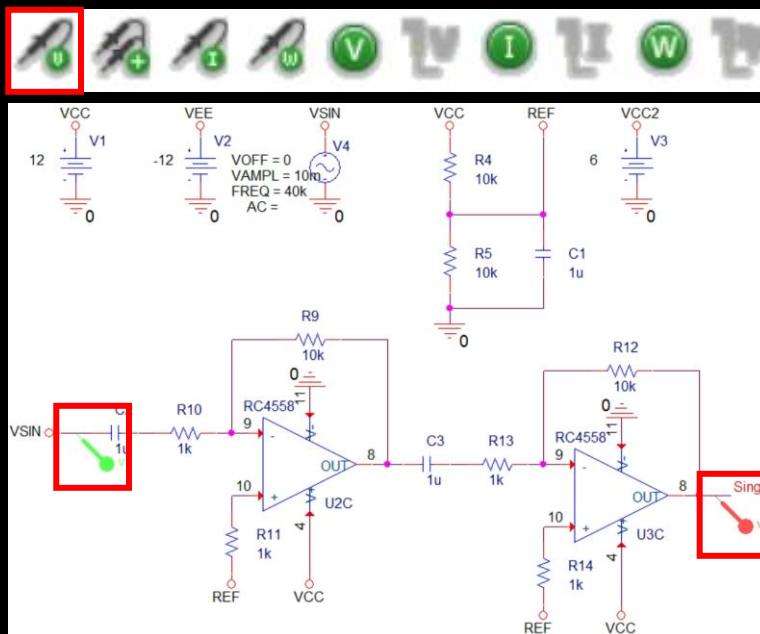
6. Simulation setting



1. Setting to run to time and maximum step size

Capture CIS user's guide

7. Check to simulation result



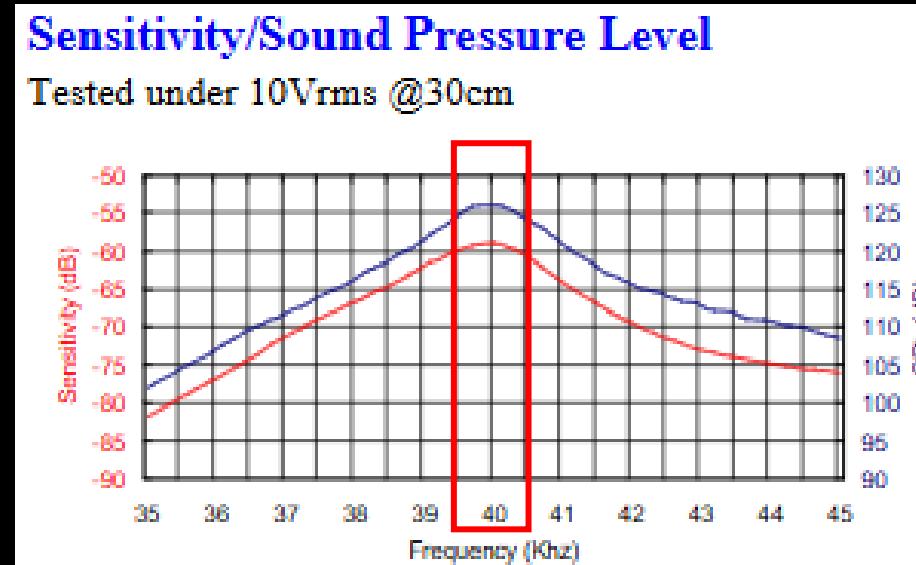
Circuit Design & Measurement

1. Ultrasonic Oscillation

Design Process



Specification	
400ST160	Transmitter
400SR160	Receiver
Center Frequency	$40.0 \pm 1.0 \text{ KHz}$
Bandwidth (-6dB)	400ST160: 2.0Khz 400SR160: 2.5Khz
Transmitting Sound Pressure Level	120dB min. at 40.0Khz; 0dB re 0.0002 \times bar per 10Vrms at 30cm
Receiving Sensitivity	-65dB min. at 40.0Khz 0dB = 1 volt/ \times bar
Capacitance at 1Khz	$\pm 20\%$
Max. Driving Voltage (cont.)	20Vrms
Total Beam Angle -6dB	55° typical
Operation Temperature	-30 to 80°C
Storage Temperature	-40 to 85°C



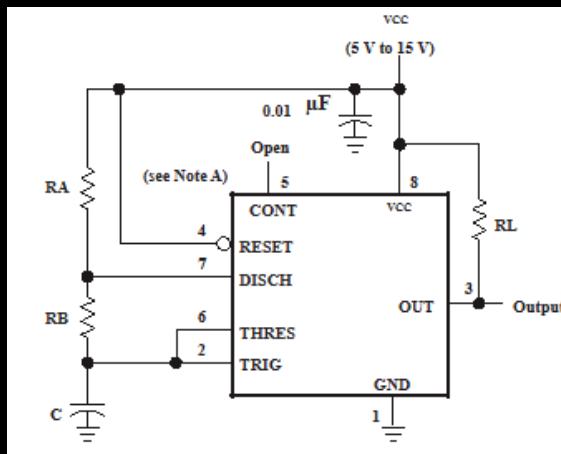
< Design Process >

1. Tx Frequency = 40kHz
2. Input Voltage < 20V

Circuit Design & Measurement

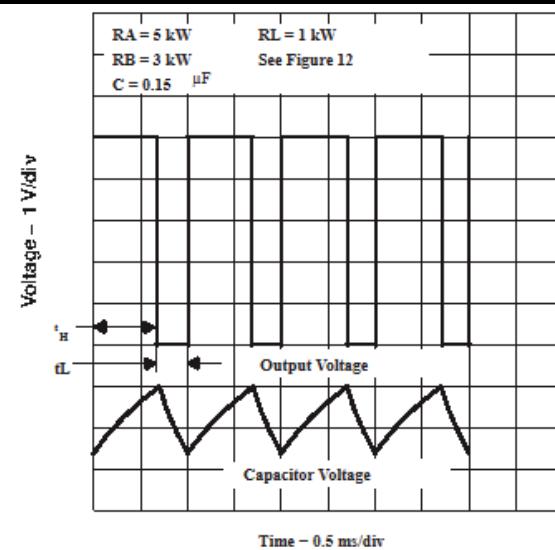
1. Ultrasonic Oscillator

Design Process



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.



for 40kHz oscillation

($RA = 30k\Omega$, $RB = 160k\Omega$, $C = 100pF$),

$$\begin{aligned} TH &= 0.693 \times (RA + RB) \times C \\ &= 0.693 \times 190k \times 100p \\ &13\mu s \end{aligned}$$

$$\begin{aligned} TL &= 0.693 \times RB \times C \\ &= 0.693 \times 160k \times 100p \\ &11\mu s \end{aligned}$$

$$f = 1 / (TH + TL)$$
$$41\text{kHz}$$

> 40kHz Frequency generate

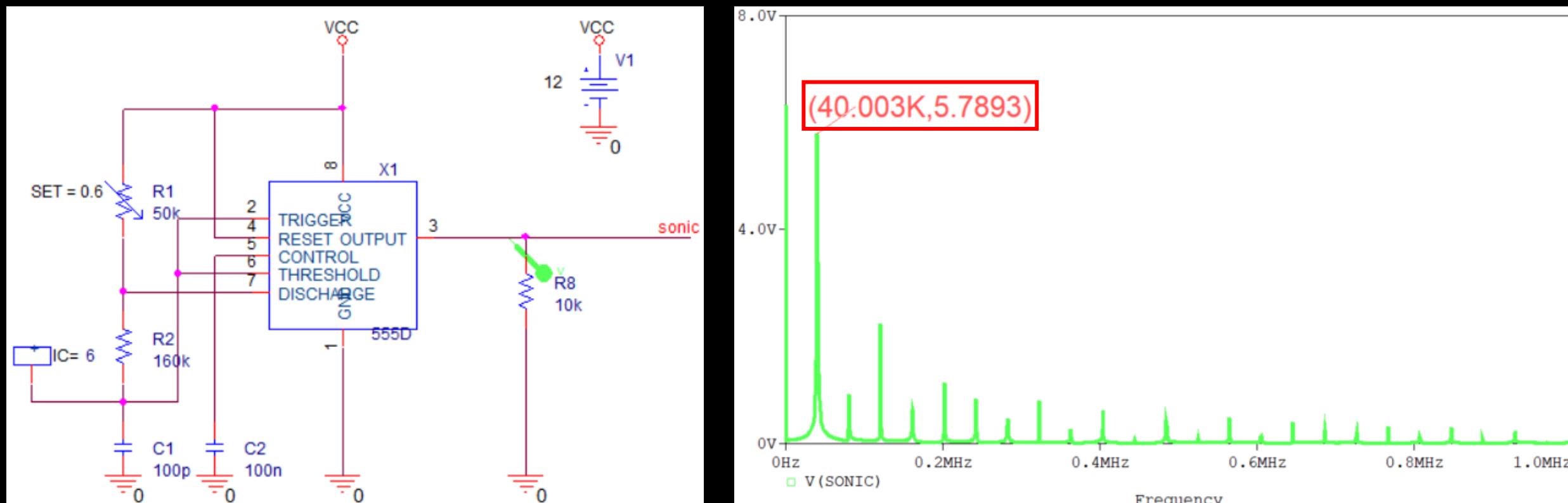
$$t_H = 0.693(R_A + R_B)C$$

$$t_L = 0.693(R_B)C$$

Circuit Design & Measurement

1. Ultrasonic Oscillator

Design Process



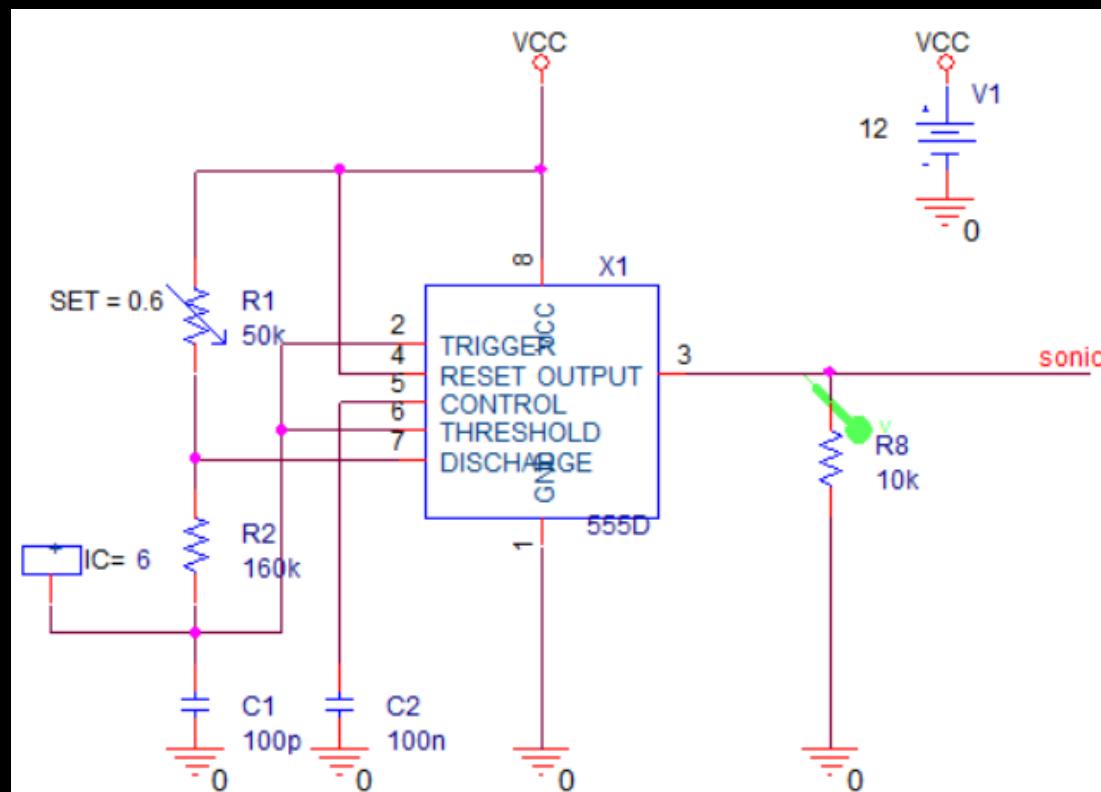
RA=30k Ω , RB=160k Ω , C=100pF

> 40kHz Oscillator

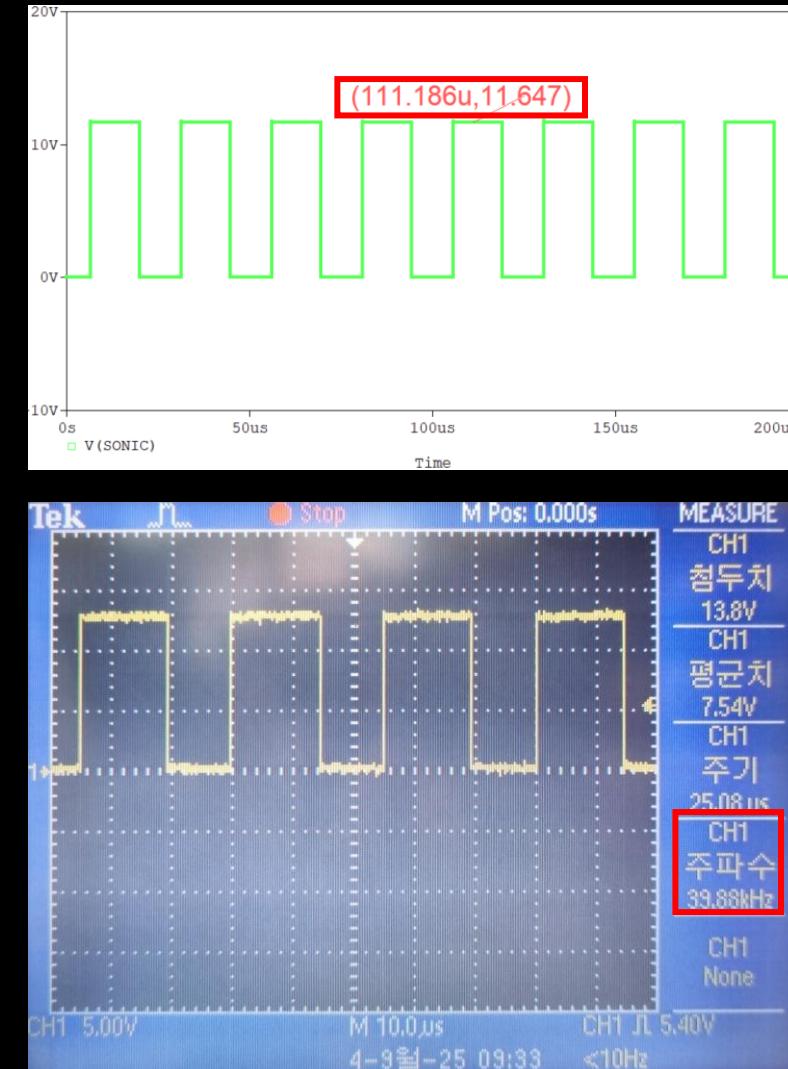
Circuit Design & Measurement

1. Ultrasonic Oscillation

Result



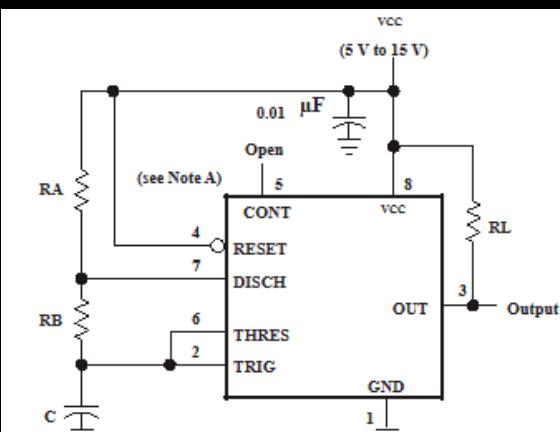
> 40kHz Frequency generate



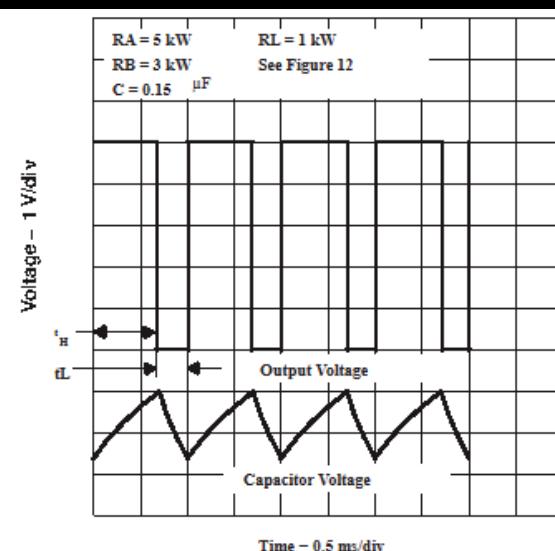
Circuit Design & Measurement

2. Ultrasonic Pulse Oscillator

Design Process



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.



$$t_H = 0.693(R_A + R_B)C$$
$$t_L = 0.693(R_B)C$$

1. Frequency Transmission Timing Control
→ $t_H = 65\text{m(s)}$, $t_L = 0.3\text{m(s)}$
→ 65.3ms pulse generate

For $t_H = 65\text{m(s)}$, $t_L = 0.3\text{m(s)}$ oscillation
($R_A = 2\text{M}\Omega$, $R_B = 8.2\text{k}\Omega$, $C = 47\text{nF}$)

$$\begin{aligned} t_H &= 0.693 \times (R_A + R_B) \times C \\ &= 0.693 \times 2008.2\text{k} \times 47\text{n} \\ &\approx 65.4\text{m(s)} \end{aligned}$$

$$\begin{aligned} t_L &= 0.693 \times R_B \times C \\ &= 0.693 \times 8.2\text{k} \times 47\text{n} \\ &\approx 0.267\text{m(s)} \end{aligned}$$

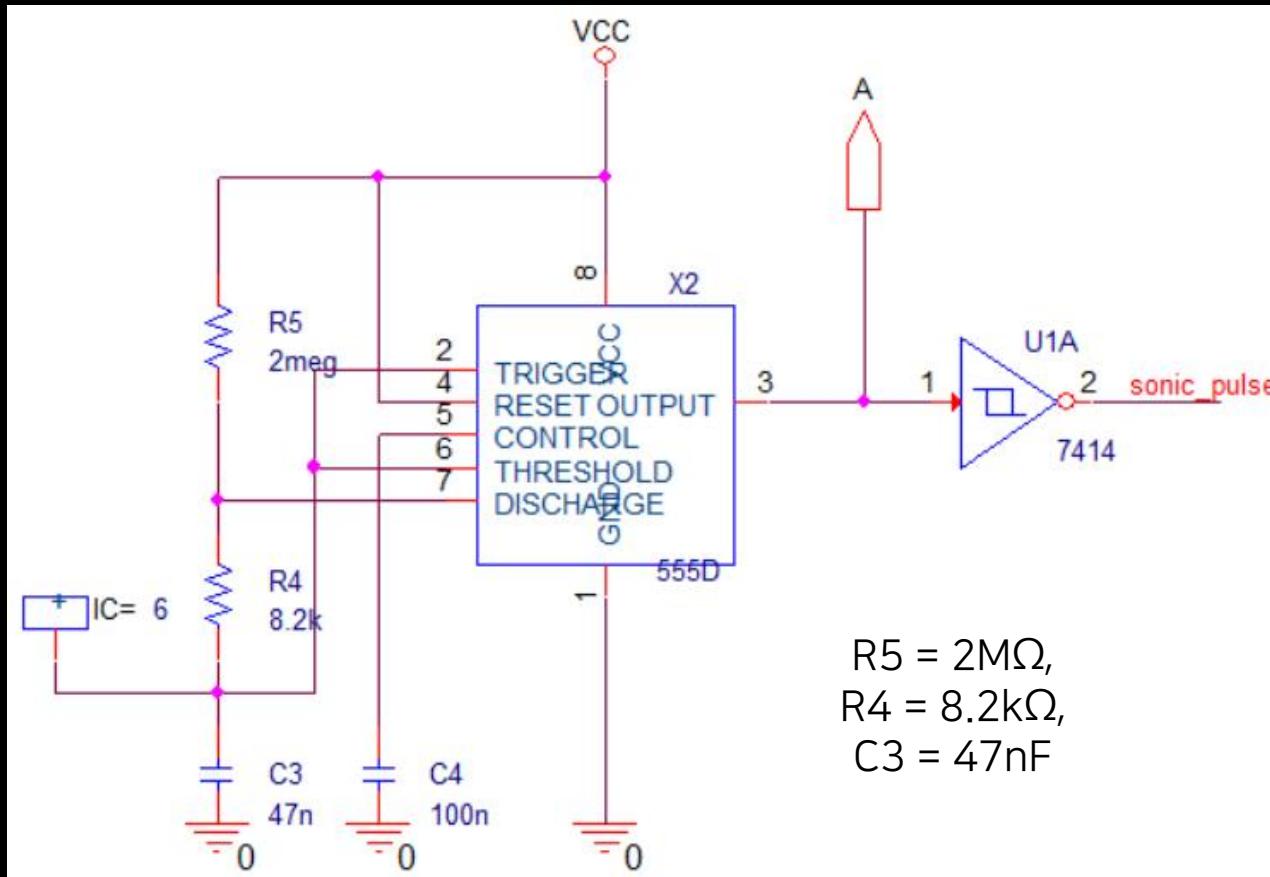
$$T = t_H + t_L \approx 65.66\text{m(s)}$$

⇒ 15.2Hz 주파수 발생

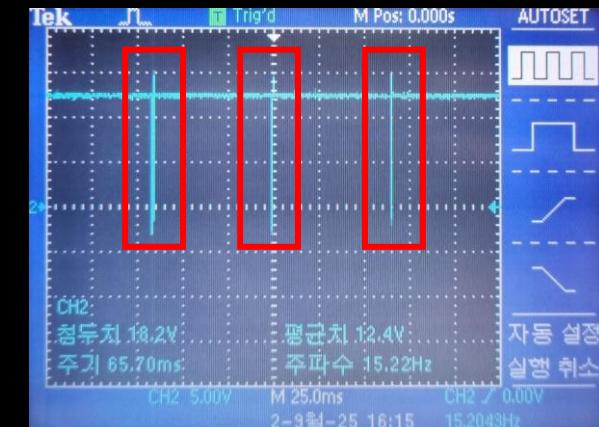
Circuit Design & Measurement

2. Ultrasonic Pulse Oscillator

Design Process & Result



→ T=66ms, 15.15Hz
Pulse Oscillator

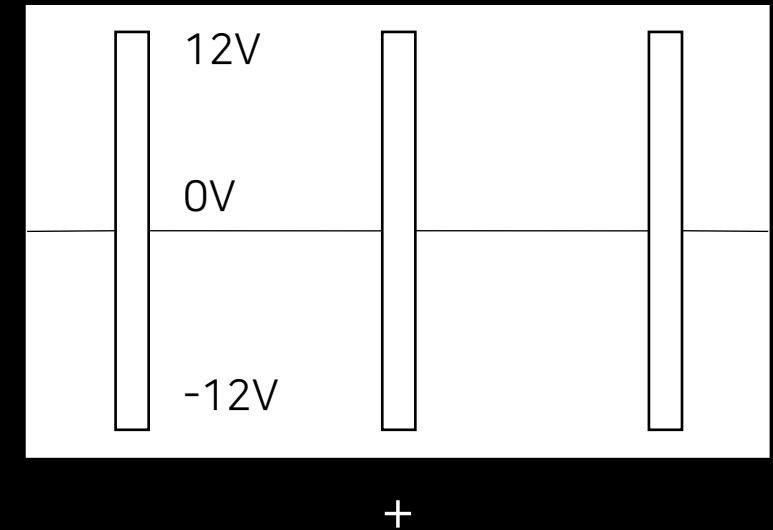
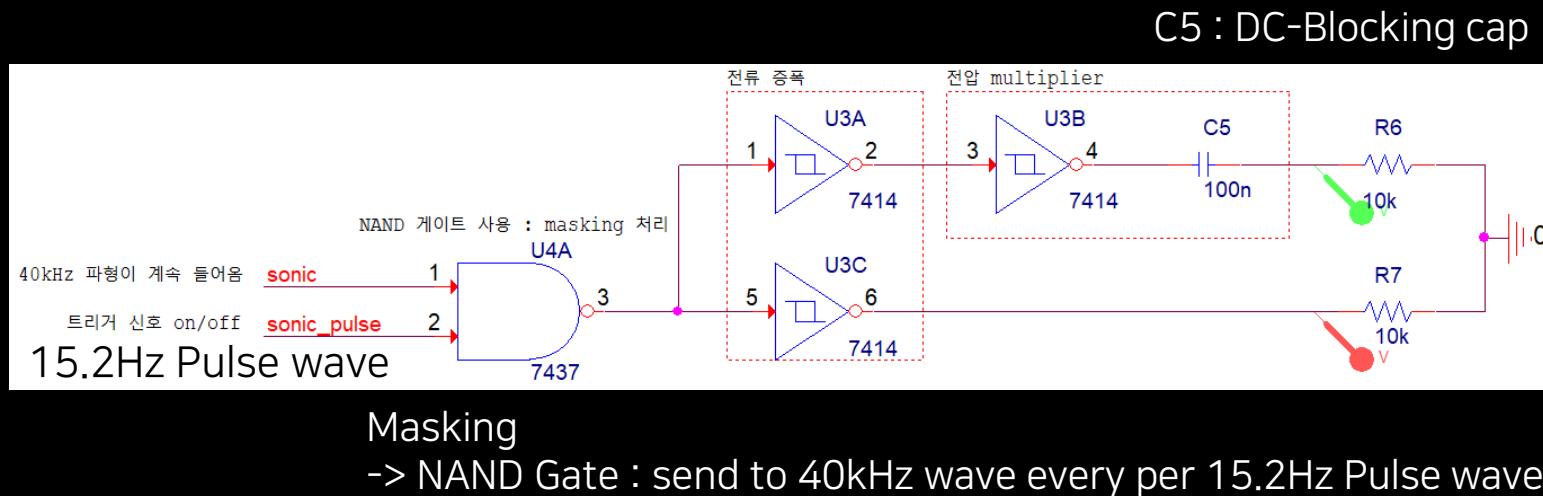


→ T=65.7ms, 15.22Hz
Pulse Oscillator

Circuit Design & Measurement

3. Ultrasonic Transmitter

Design Process



Buffer : Current AMP

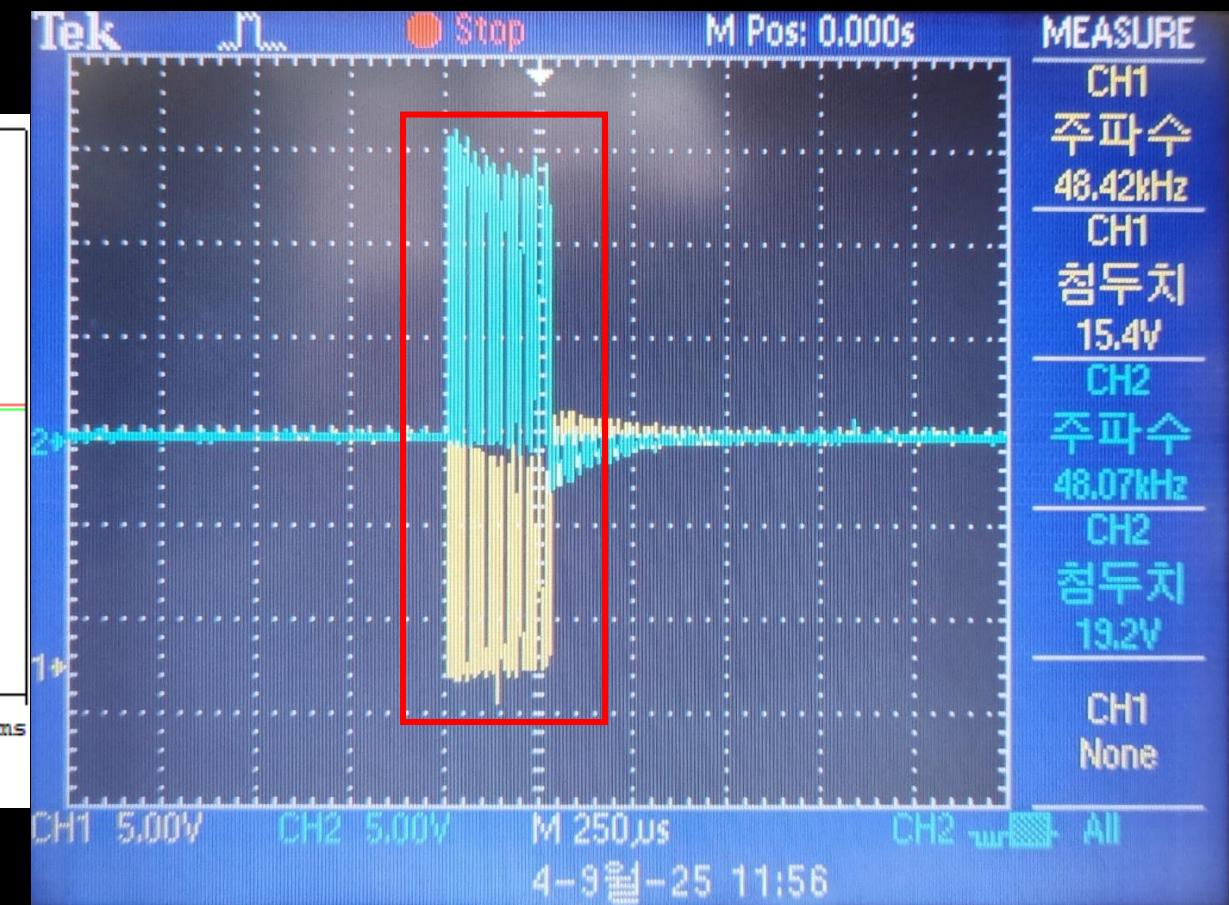
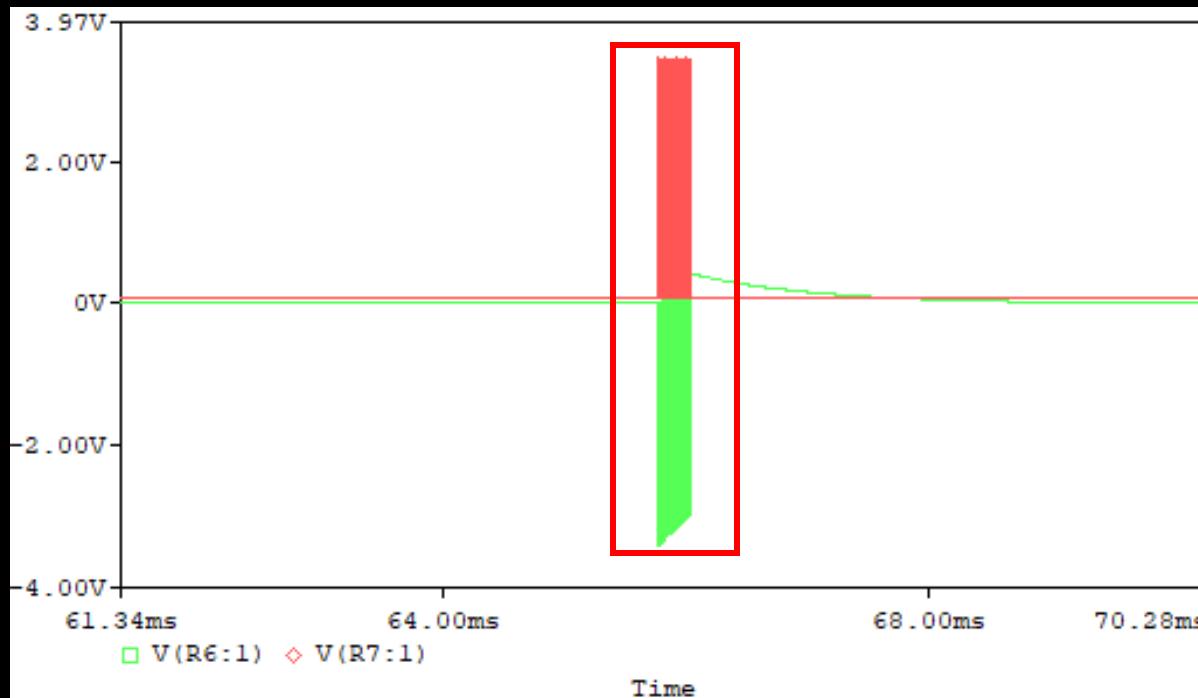


Power AMP

Circuit Design & Measurement

3. Ultrasonic Transmitter

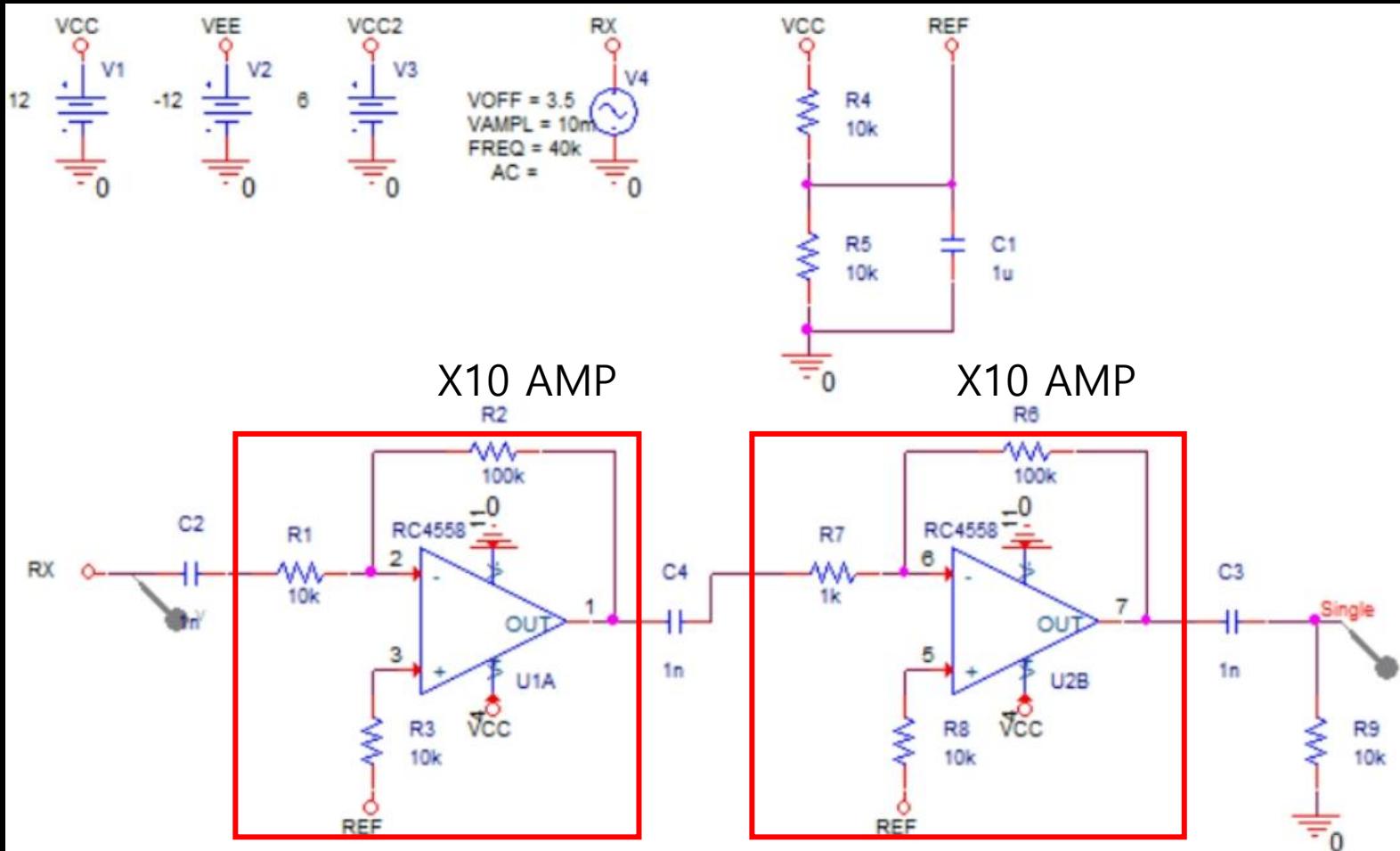
Result



Circuit Design & Measurement

4. Ultrasonic Receiver

Design process



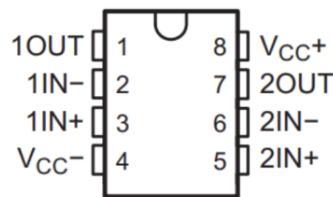
Input: -10 mV ~ 10 mV
Output: -1 V ~ 1 V
→ x100 Amplification
Capacitor (C2, C3): DC-Blocking Cap

Do not work to x100/x1 amplifier

Circuit Design & Measurement

4. Ultrasonic Receiver

Design process & Result



PARAMETER	TEST CONDITIONS ⁽¹⁾	T _A ⁽²⁾	MIN	TYP	MAX	UNIT	
V _{IO}	V _O = 0	25°C	0.5	6	7.5	mV	
		Full range					
I _{IO}	V _O = 0	25°C	5	200	300	nA	
		Full range					
I _{IB}	V _O = 0	25°C	150	500	800	nA	
		Full range					
V _{ICR}	Common-mode input voltage range	25°C	±12	±14		V	
V _{OM}	R _L = 10 kΩ	25°C	±12	±14			
		25°C	±10	±13			
A _{VD}	R _L ≥ 2 kΩ, V _O = ±10 V	25°C	20	300		V/mV	
		Full range	-15				
B ₄	Unity-gain bandwidth	25°C	3		5	MHz	
r _i	Input resistance	25°C	0.3	5	6.6	MΩ	
CMRR	Common-mode rejection ratio	25°C	70	90		dB	
k _{VSV}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V _{CC} = ±15 V to ±9 V	25°C	30	150	µV/V	
V _n	Equivalent input noise voltage (closed loop)	A _{VD} = 100, R _S = 100 Ω, f = 1 kHz, BW = 1 Hz	25°C	8		nV/√Hz	
I _{CC}	Supply current (both amplifiers)		25°C	2.5	5.6		
			T _A min	3	6.6		
			T _A max	2.3	5		
P _D	Total power dissipation (both amplifiers)	V _O = 0, No load	25°C	75	170		
			T _A min	90	200	mW	
			T _A max	70	150		
V _{O1} /V _{O2}	Crosstalk attenuation	Open loop	R _S = 1 kΩ, f = 10 kHz	25°C	85		
		A _{VD} = 100			105	dB	

[Design Goal]

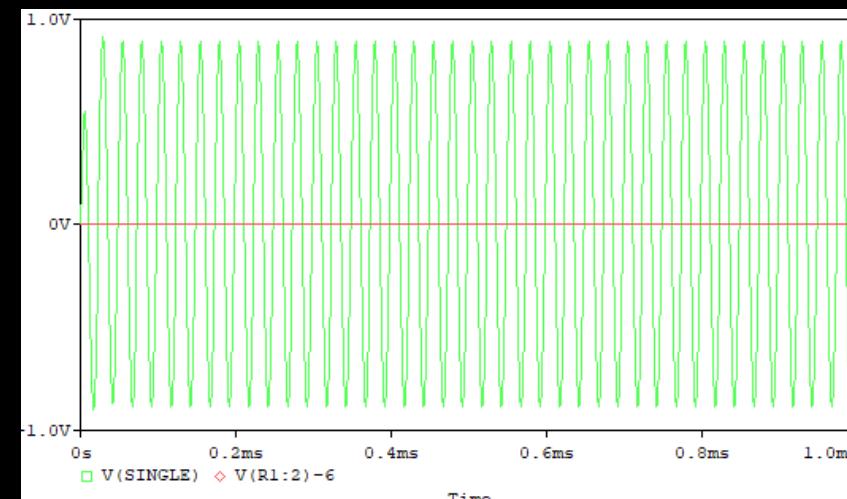
1. Amplify received signal by 100 times
→ Using OP-Amp

RC4558 GBW (Unity Gain Bandwidth) = 3 MHz
@ 40kHz Gain = GBW / Bandwidth

$$= 3 \text{ MHz} / 40 \text{ kHz}$$

$$= 75$$

- With RC4558, maximum gain = 75
- Using two RC4558, achieve 100x amplification (x10, x10)



Circuit Design & Measurement

5. Signal Rectification

Design process

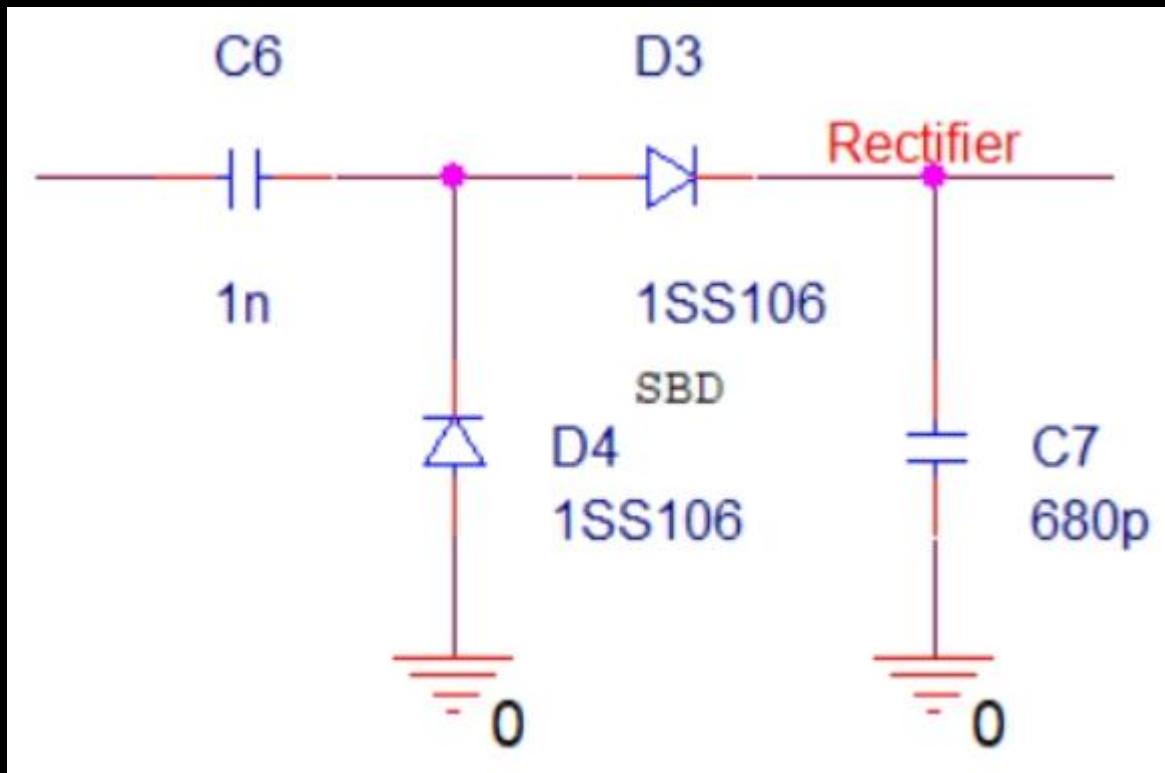
[Design Goal]

1. Rectification of amplified signal
 - Use diode and smoothing capacitor
2. Diode suitable for small signals
 - Use SBD (Schottky Barrier Diode) with low forward voltage

Circuit Design & Measurement

5. Signal Rectification

Design process



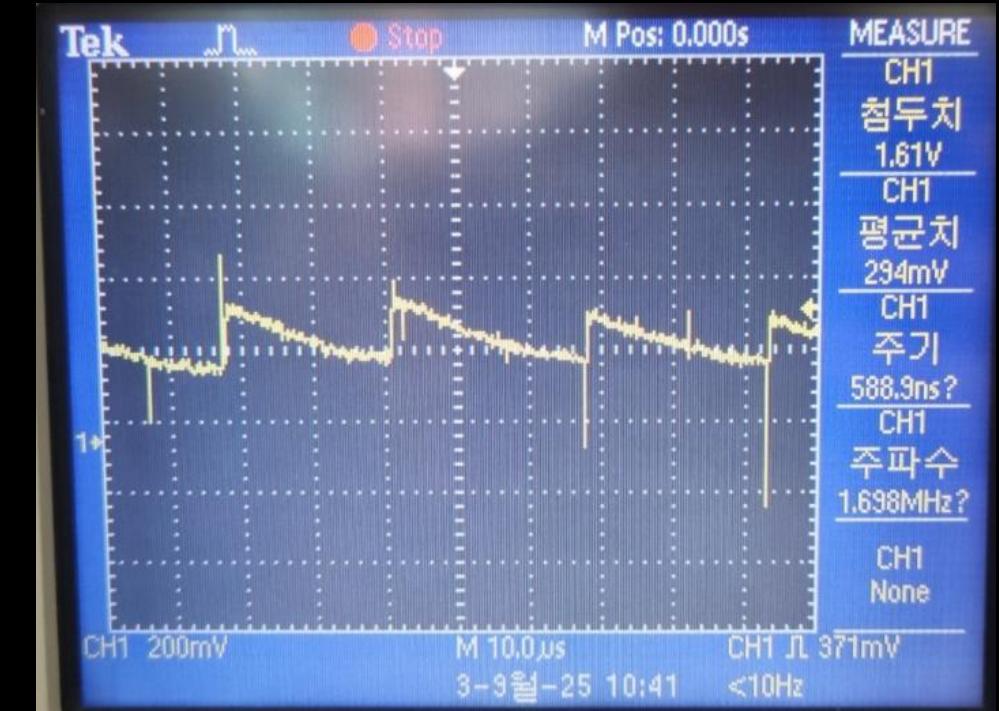
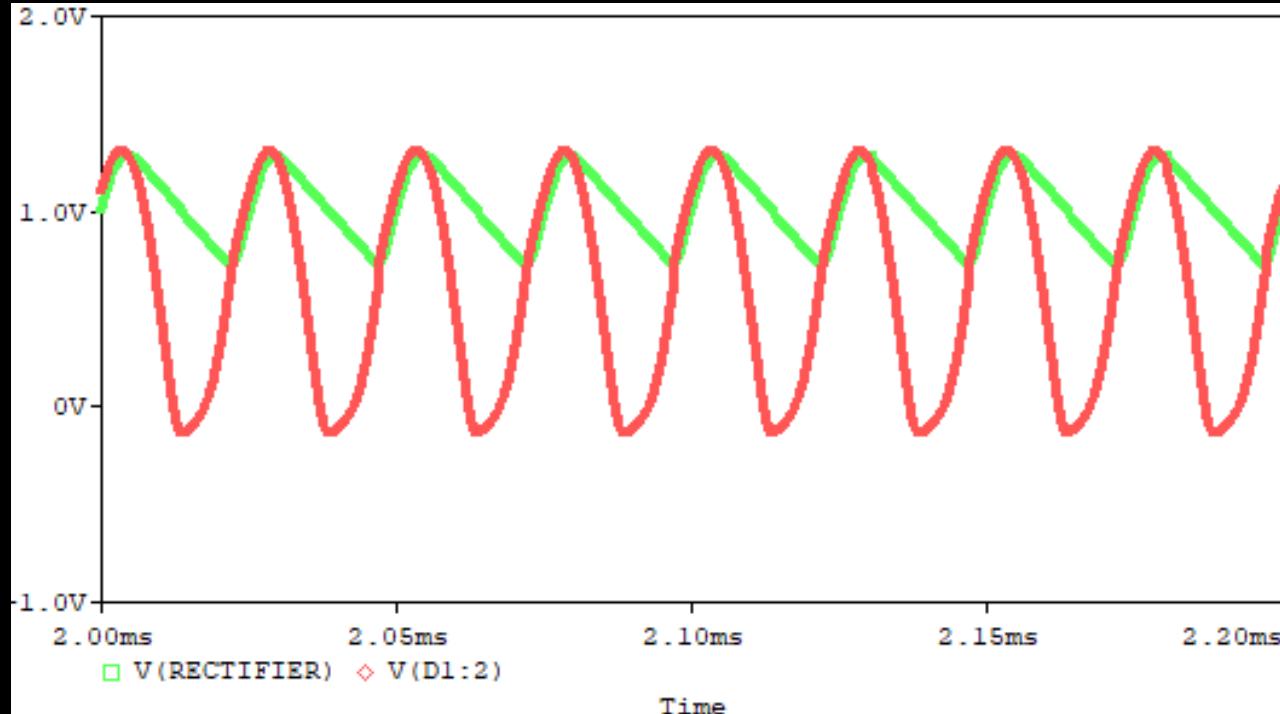
<Signal Rectification>

- Diode, Capacitor: Half-wave rectifier
- C7 Capacitor: Smoothing Cap

Circuit Design & Measurement

5. Signal Rectification

Result



Simulation

Measurement

Rectification -> Same Result

Circuit Design & Measurement

6. Signal Detection

Design process

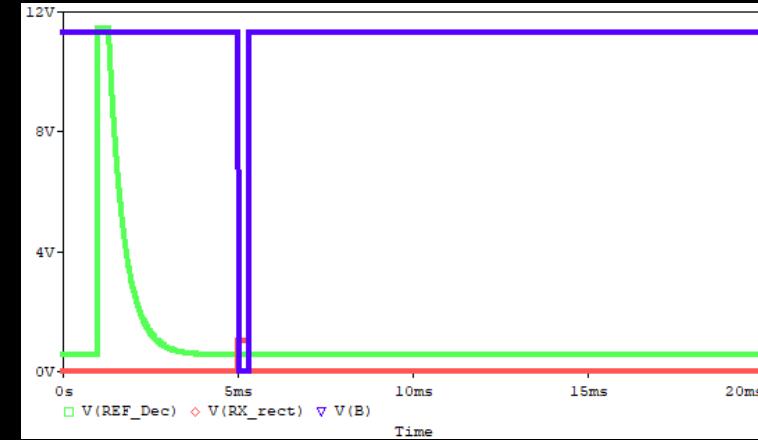
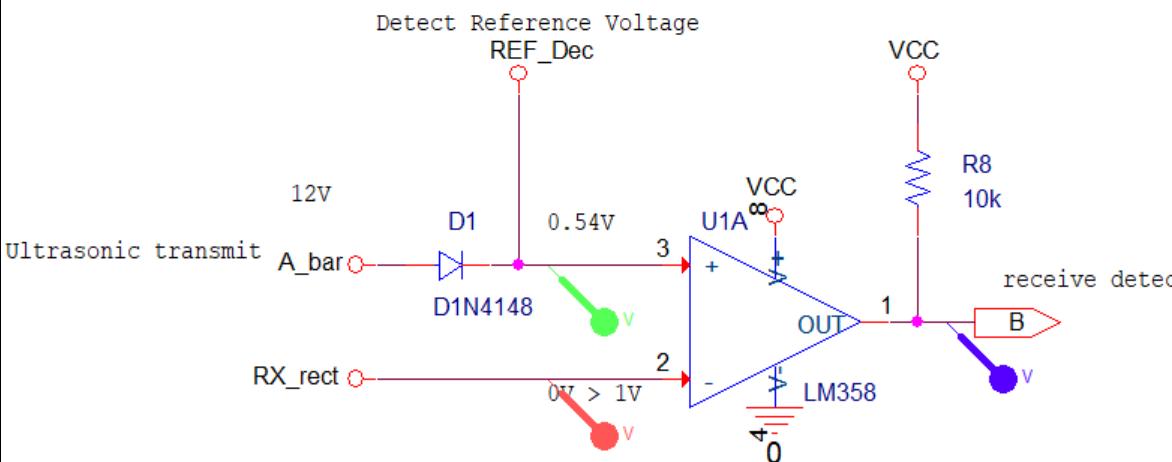
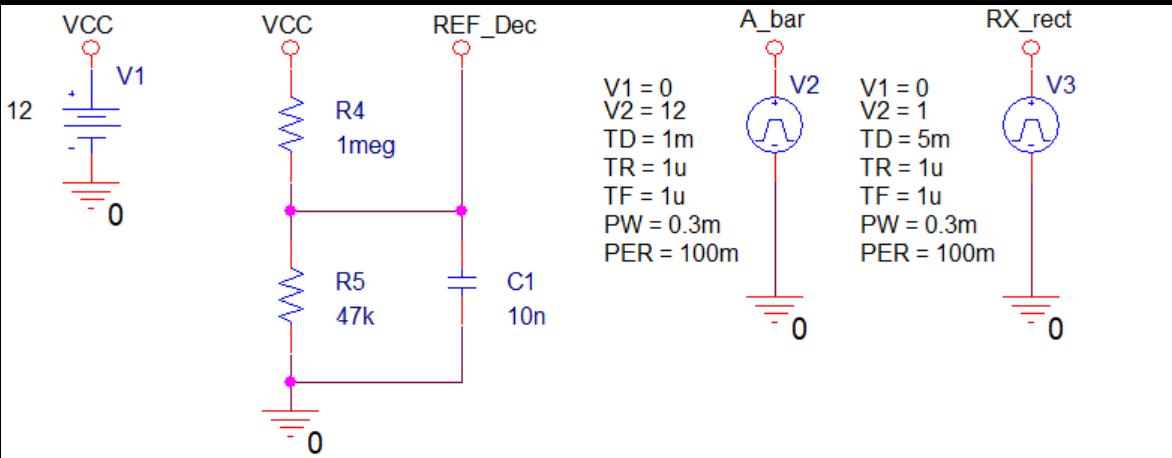
[Design Goal]

- Detection of Received Signal
 - Use OP-Amp Comparator, designed as Low Active
- Blocking of Reverse Signal
 - Use Diode
- Noise Blocking
 - Detect only signals above 0.54V as valid received signals

Circuit Design & Measurement

6. Signal Detection

Design process

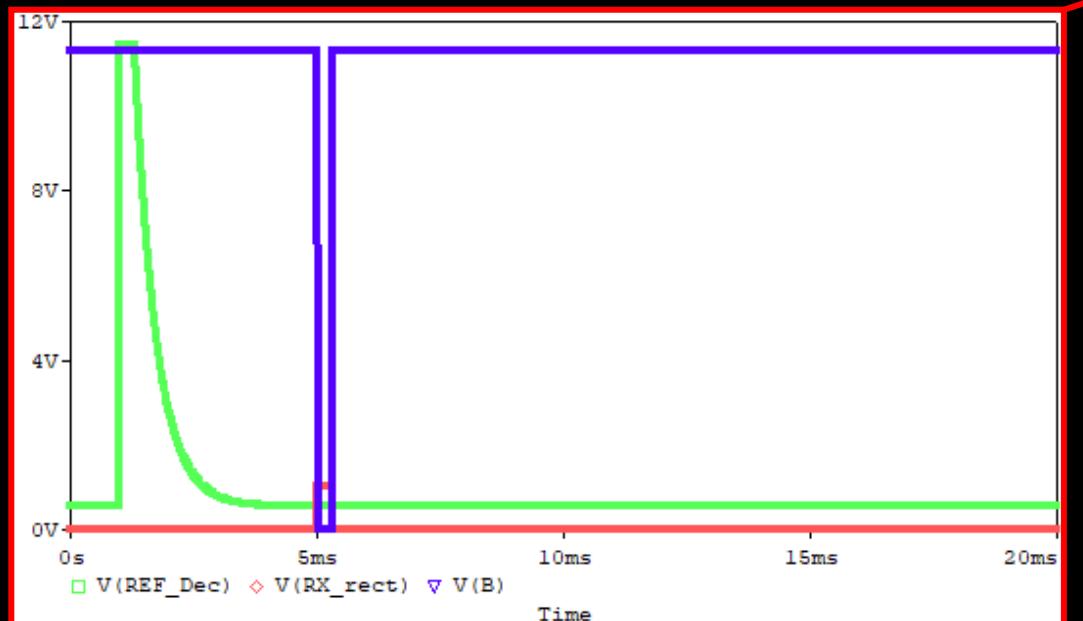


- OP-Amp Comparator: Slow but ensures stability
 - ① $V_+ > V_-$: VCC output, $V_+ < V_-$: GND output
 - ② Signal detection \rightarrow GND output \rightarrow Low Active
- REF_Dec: Noise Blocking
 \rightarrow Detect only signals above 0.54V
- D1 Diode: Reverse Signal Blocking
 - ① Timing pulse \rightarrow V_+ input
 - ② Use Capacitor delay \rightarrow Detection time delay
 - ③ Ignore signals entering during this period (reverse signals)

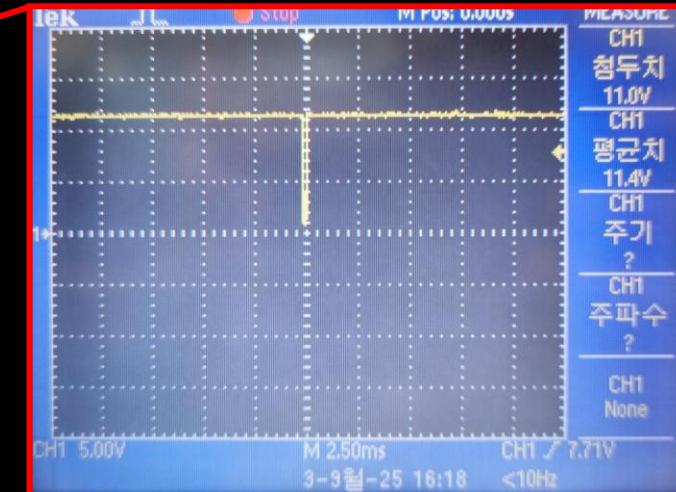
Circuit Design & Measurement

6. Signal Detection

Result



V(B)



Simulation

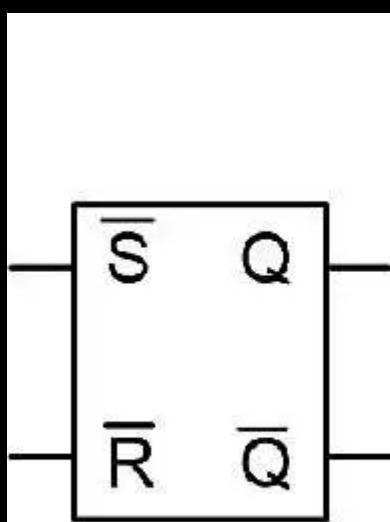
Measurement

Same Result

Circuit Design & Measurement

7. Time Measurement

Design process



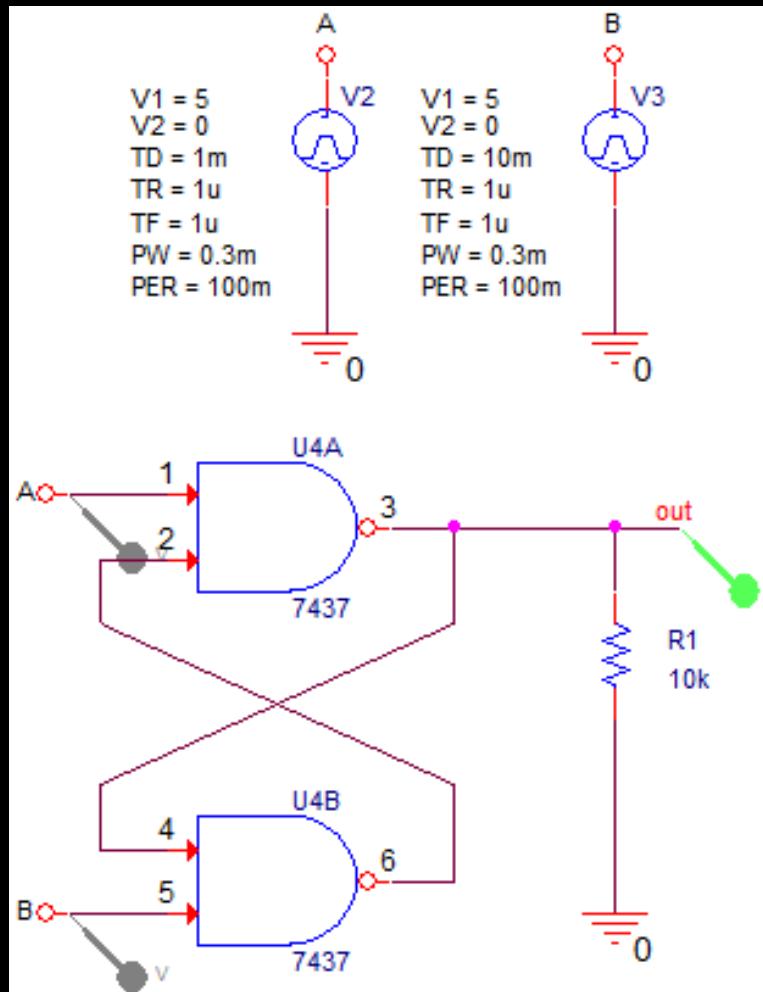
\bar{S}	\bar{R}	Q	\bar{Q}
1	1	Q	\bar{Q}
0	1	1	0
1	0	0	1
0	0	X	X

- Measurement of Ultrasonic Transmission Time
 - Calculate the time difference between transmission timing pulse & received signal detection
 - Use SR Latch

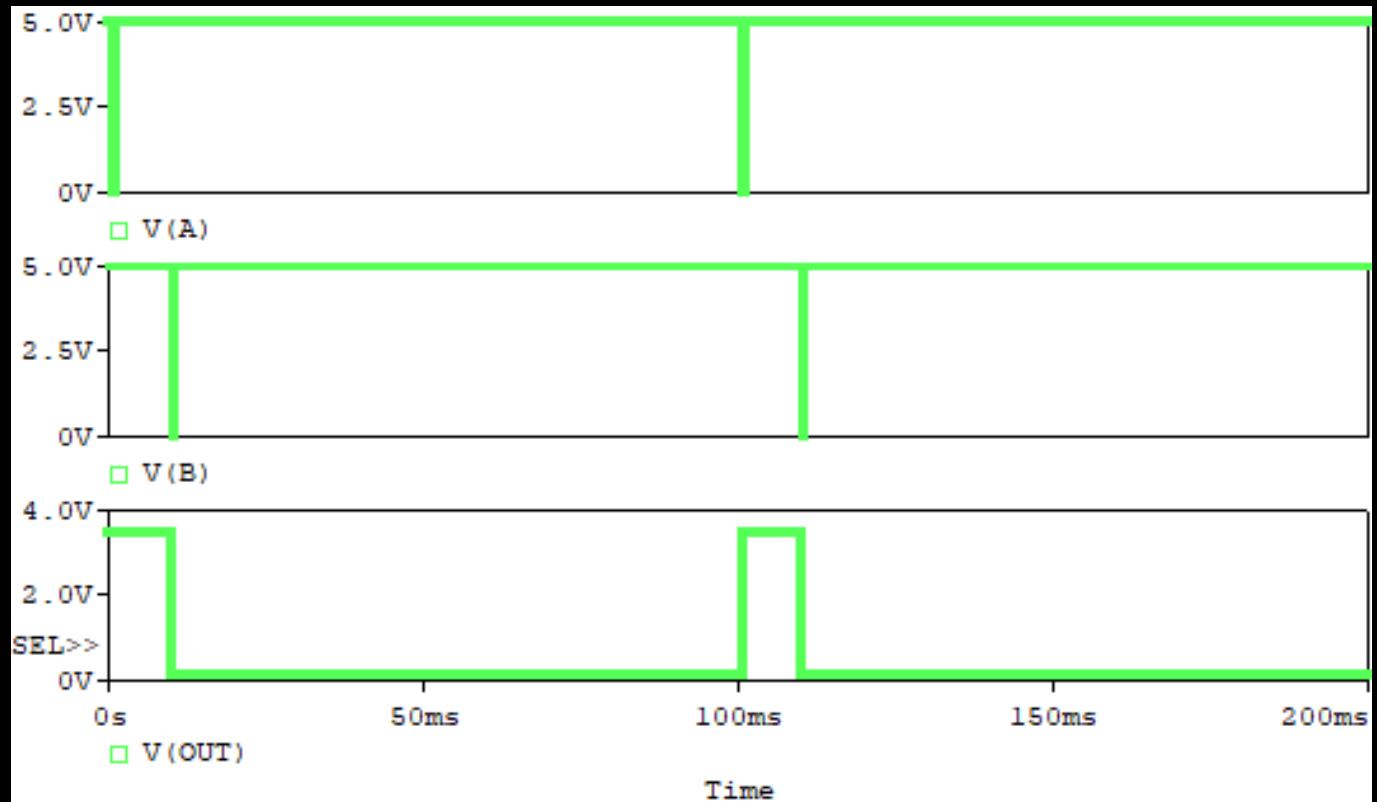
Circuit Design & Measurement

7. Time Measurement

Result



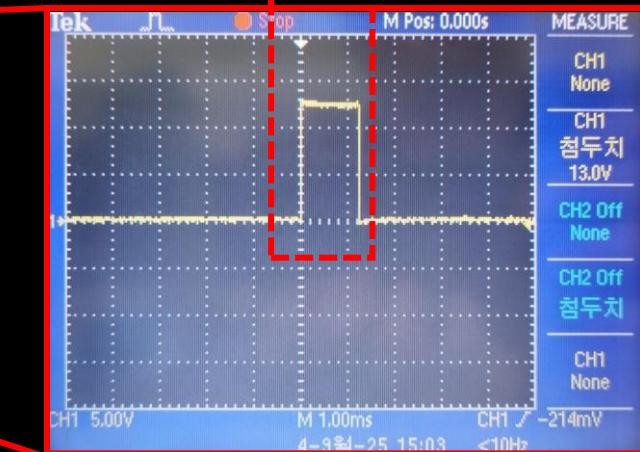
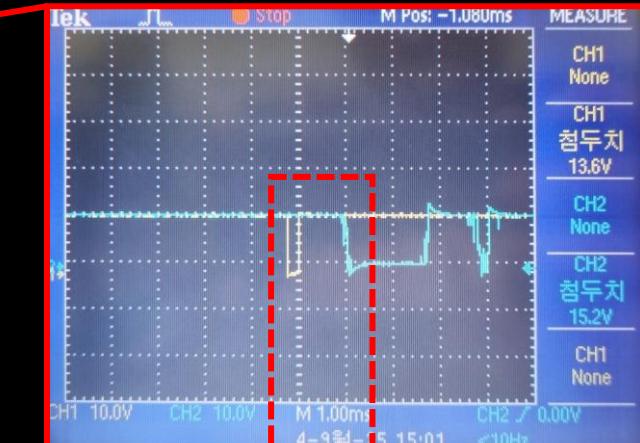
SR Latch Output :
High \rightarrow transmit \sim receive time



Circuit Design & Measurement

7. Time Measurement

Result

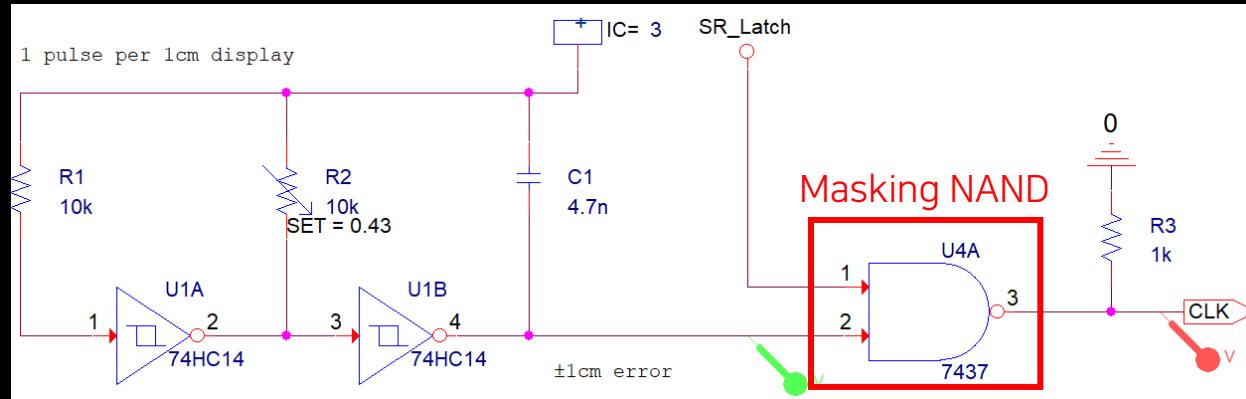


Simulation	Measurement
Same Result	

Circuit Design & Measurement

8. Counting Pulse Oscillator

Design process



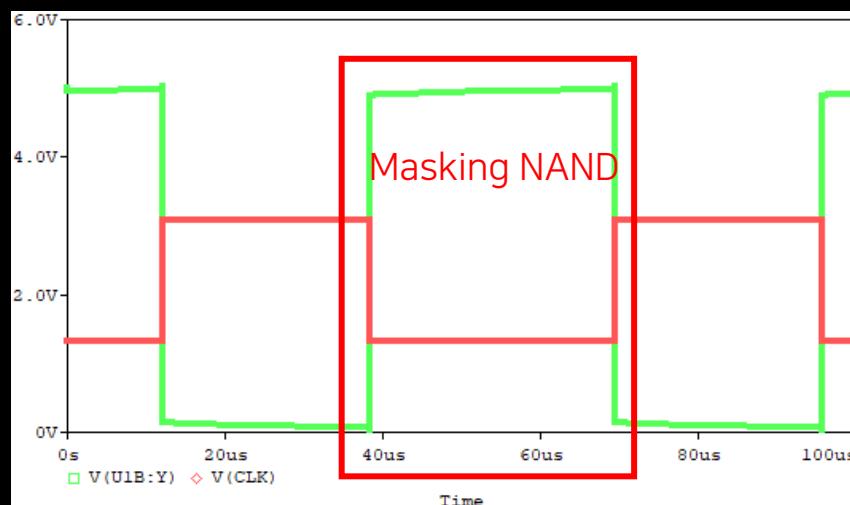
1. Object Distance Measurement

- ① Design a counting pulse that can count during ultrasonic transmission time
- ② Use NAND Gate for masking
- ③ Standard: 100 cm → 100 pulses → 17.18 kHz pulse generation

$$\begin{aligned} T(\text{round trip } 100 \text{ cm}) &= \text{Round distance} / \text{Speed of Ultrasonic} \\ &= 2 [\text{m}] / 343.5 [\text{m/s}] = 5.82 \text{ ms} \end{aligned}$$

$$\begin{aligned} \text{distance} &= 100 \text{ cm} \rightarrow 100 \text{ pulses occur} \\ f &= 100 / T = 100 / 5.82 \text{ ms} = 17.18 \text{ kHz} \end{aligned}$$

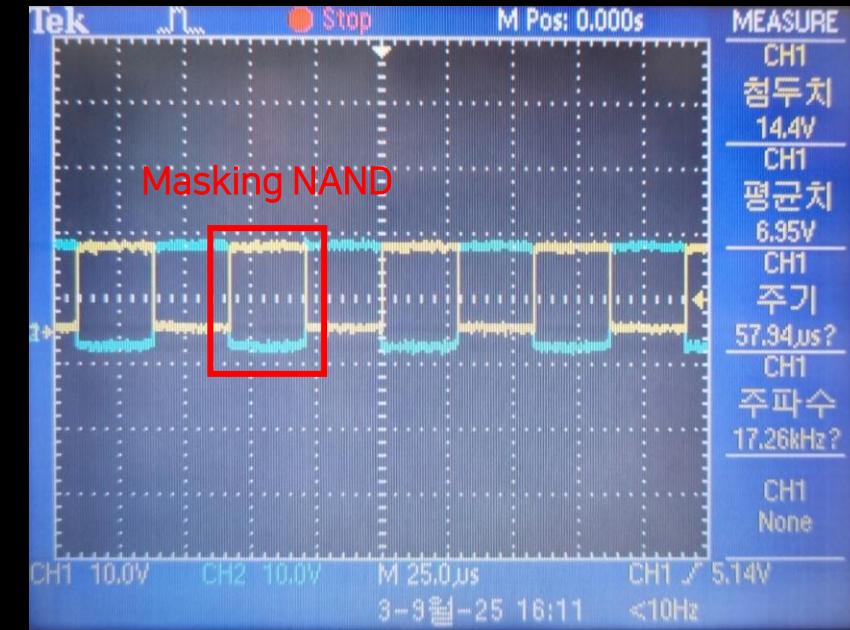
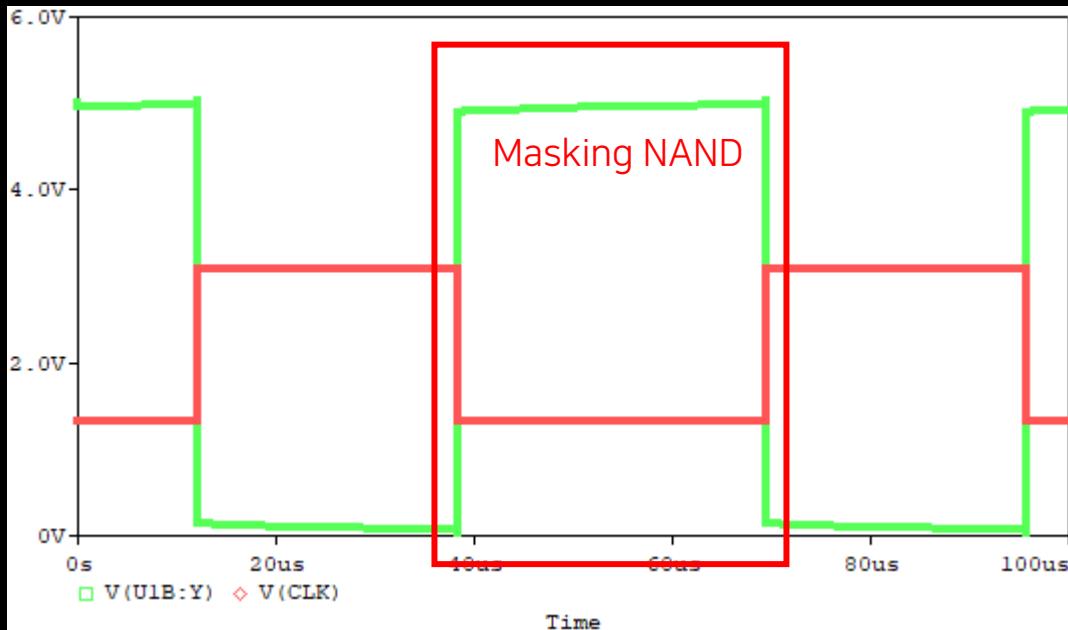
→ 1 cm = 1 pulse, 100 cm = 100 pulses



Circuit Design & Measurement

8. Counting Pulse Oscillator

Result



Simulation	Measurement
Same Result	

Circuit Design & Measurement

9. Counter/Latch clear pulse

Design process

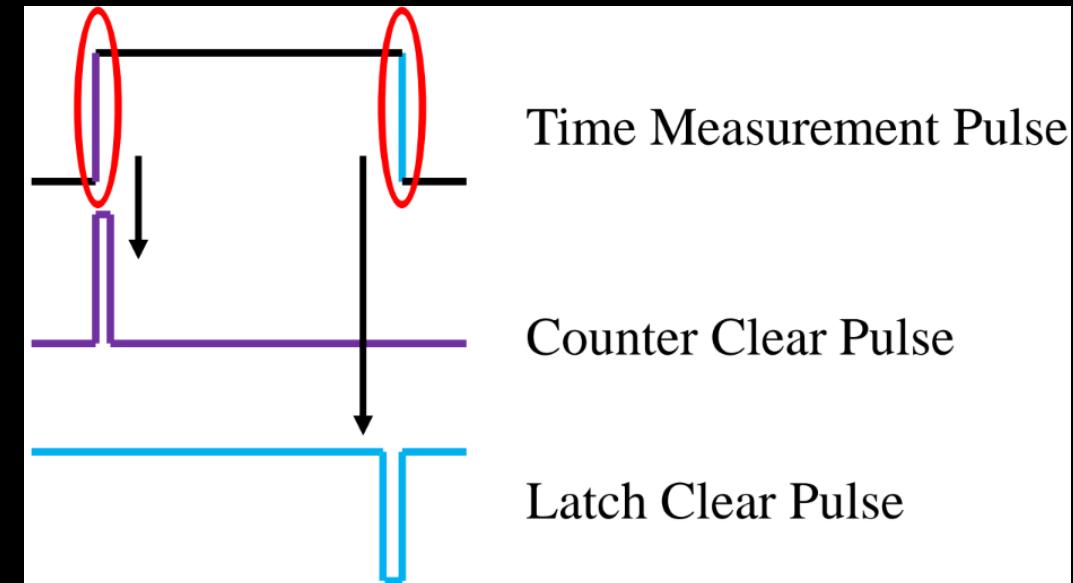
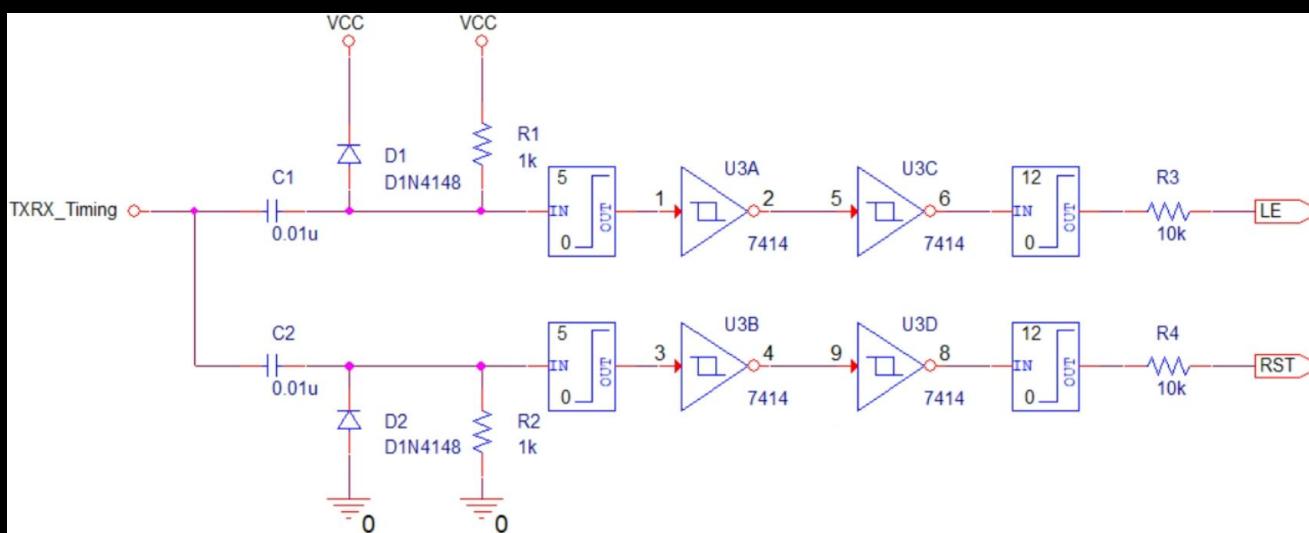
[Design Goal]

1. Ultrasonic Reception → Generate signal pulse to clear latch
 - Remove transmission information from SR Latch signal
 - Use Buffer for current amplification
2. Ultrasonic Transmission → Generate signal pulse to clear counter
 - Remove reception information from SR Latch signal
 - Use Buffer for current amplification

Circuit Design & Measurement

9. Counter/Latch clear pulse

Design process



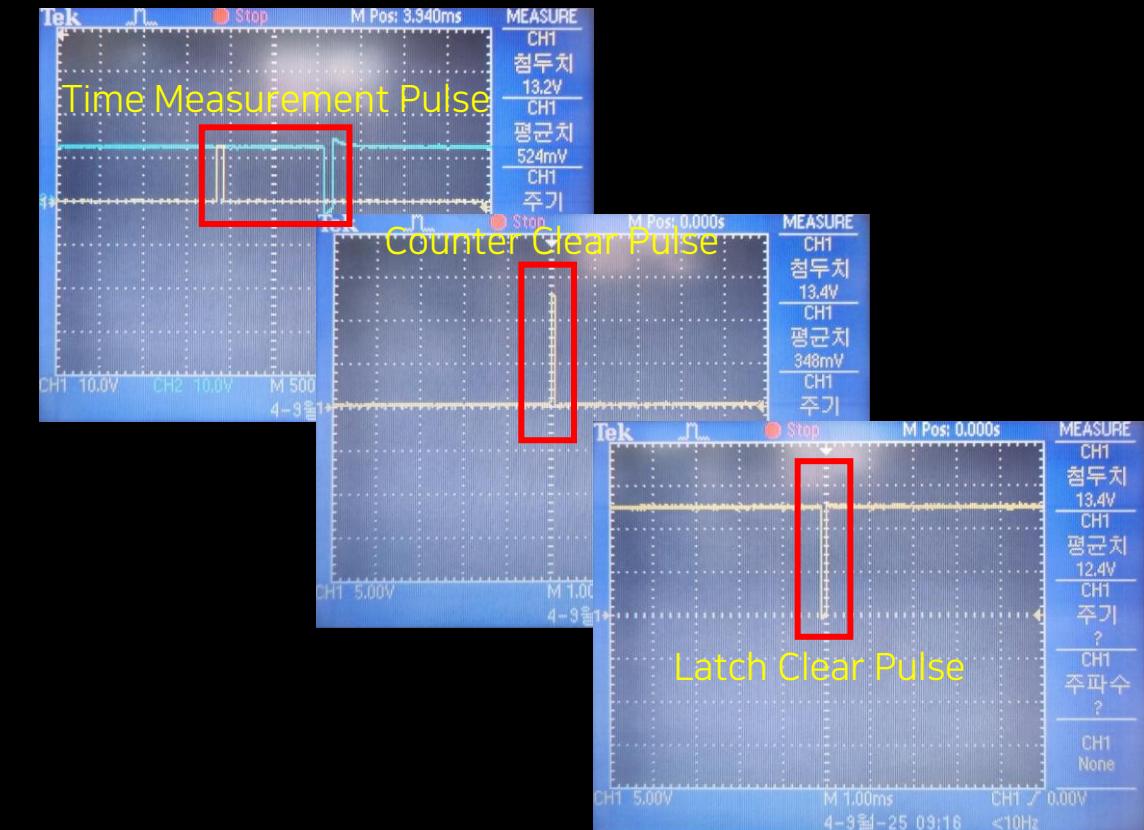
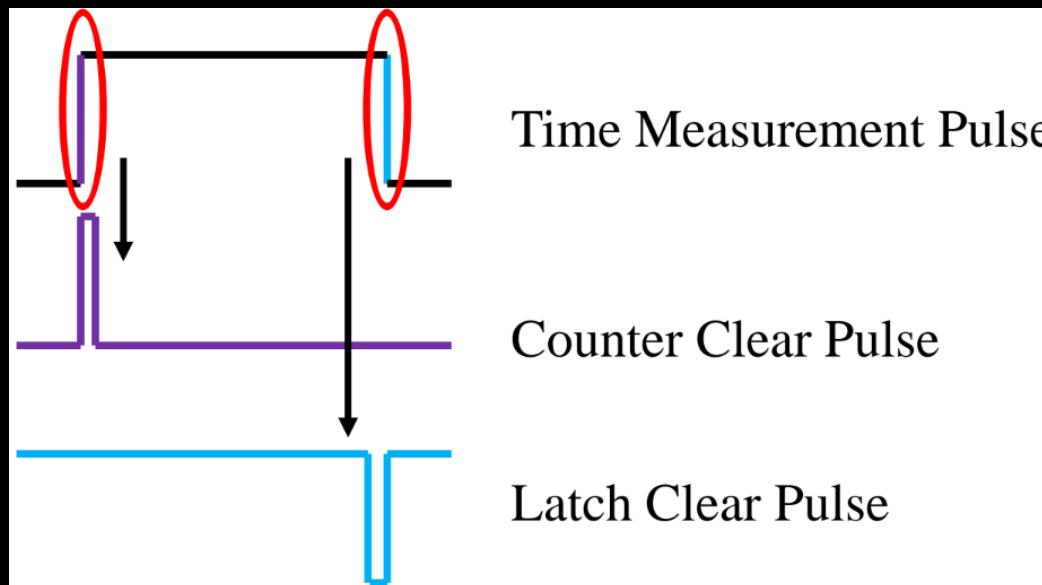
- C4, C5 Capacitor: DC-Blocking Cap
- D2, D3 Diode: Clamping Diode
- R1, R2 Resistor: Pull Up/Down R
- Buffer: Current Amplification

- Latch Clear Pulse = Reception Signal
- Counter Clear Pulse = Transmission Signal

Circuit Design & Measurement

9. Counter/Latch clear pulse

Result



Simulation

Measurement

Same Result

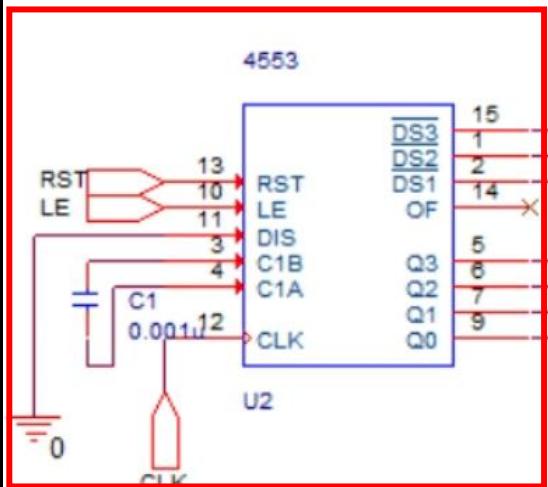
Circuit Design & Measurement

10. Distance Measurement & FND Display

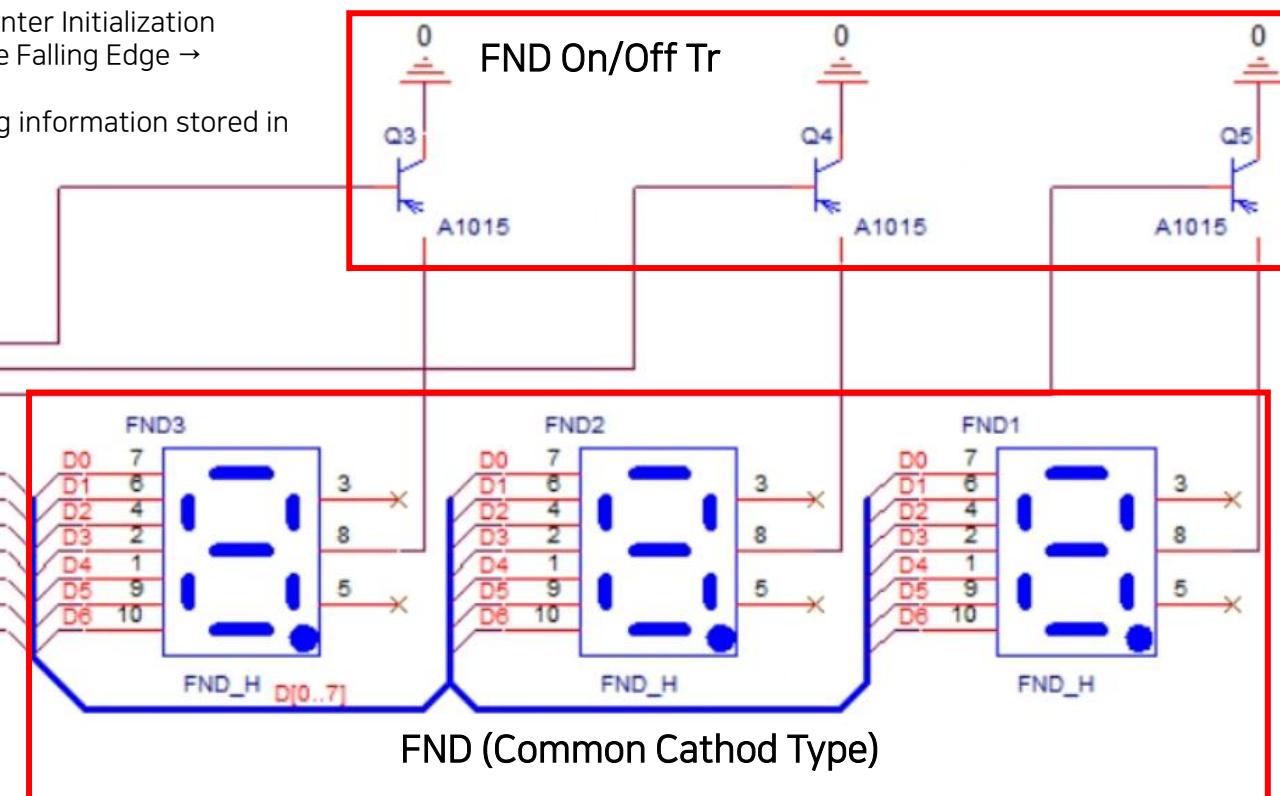
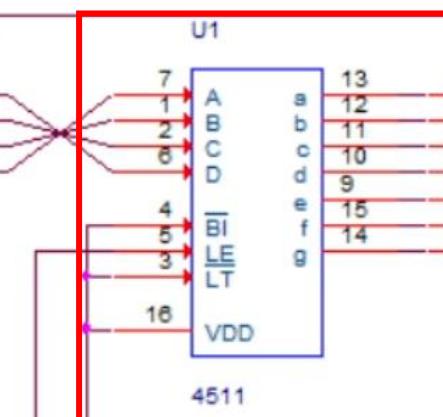
Design process

- Transmit → Counter Clear Pulse: High → Counter Initialization
- Counting Pulse (Measurement Pulse) → Pulse Falling Edge → Counter UP
- Receive → Latch Clear Pulse: Low → Counting information stored in Latch Register

BCD Counter



BCD Decoder (FND Driver)



Circuit Design & Measurement

10. Distance Measurement & FND Display

Result



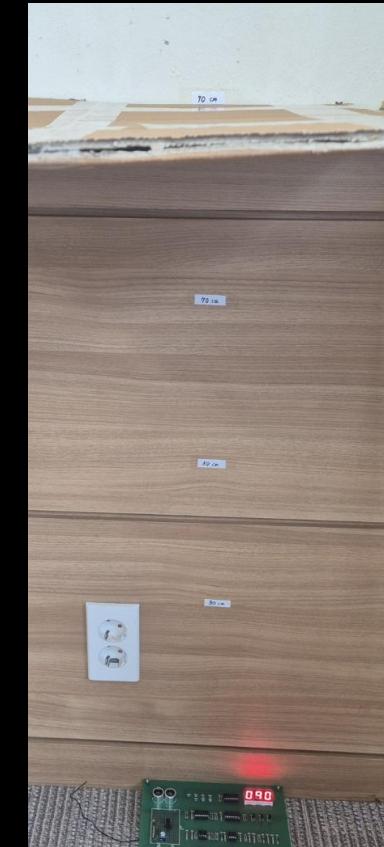
Distance : 30cm
Measurement : 31cm



Distance : 50cm
Measurement : 51cm



Distance : 70cm
Measurement : 70cm



Distance : 90cm
Measurement : 90cm



Distance : 110cm
Measurement : 110cm

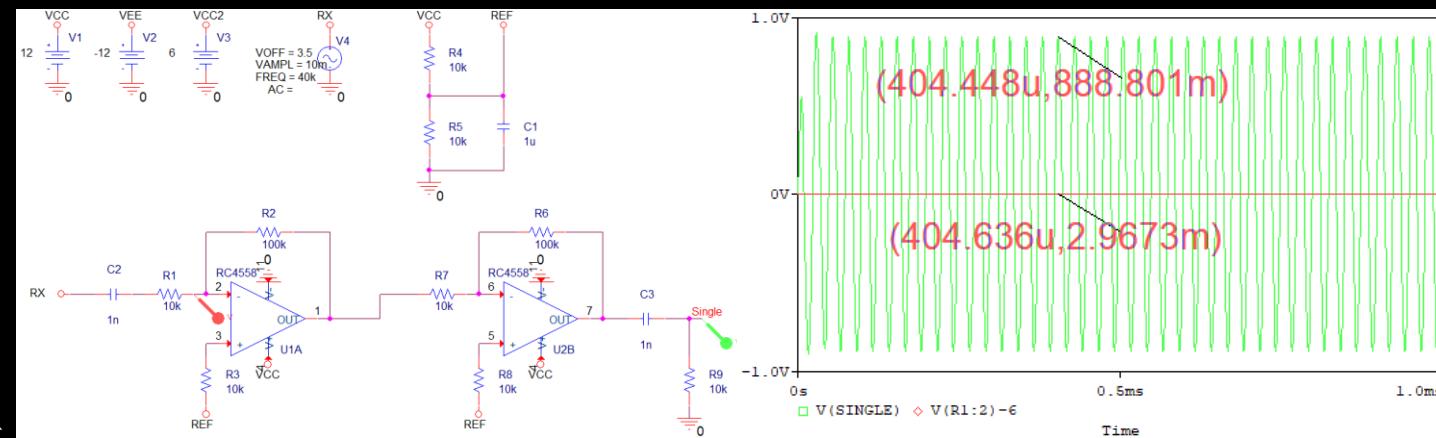
Conclusions

1. Problem

- 1) 100 times AMP X → x100 & x1 is can not Amplified to 100 times
- 2) Don't need C7 → Cost ↑
- 3) ±1cm Error occur
- 4) Save to bias current pass
- 5) ESD Protection circuit need to nearby power port
- 6) Use to much FND register
- 7) NE555 timer remove
- 8) Need to FND COM port PNP base register
- 9) Need to power & gnd divide (Power and Signal line)
- 10) R1, R2 Value is very high

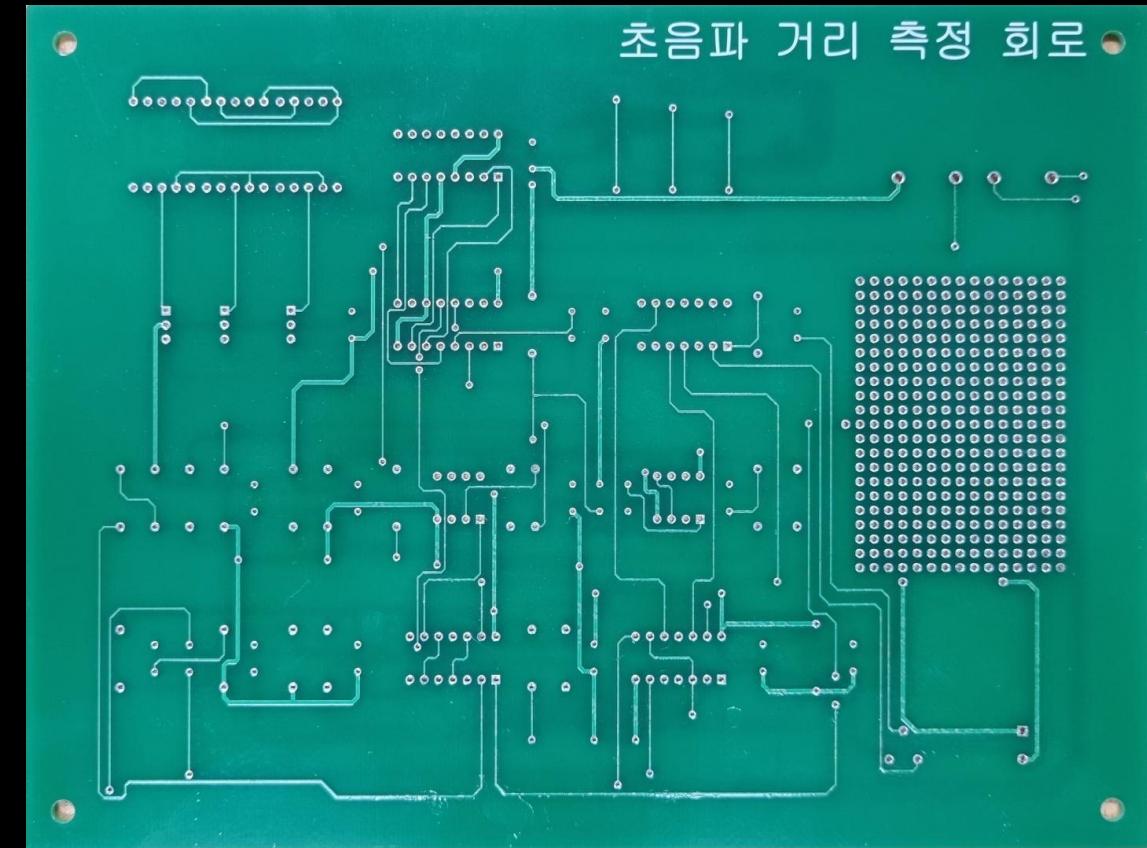
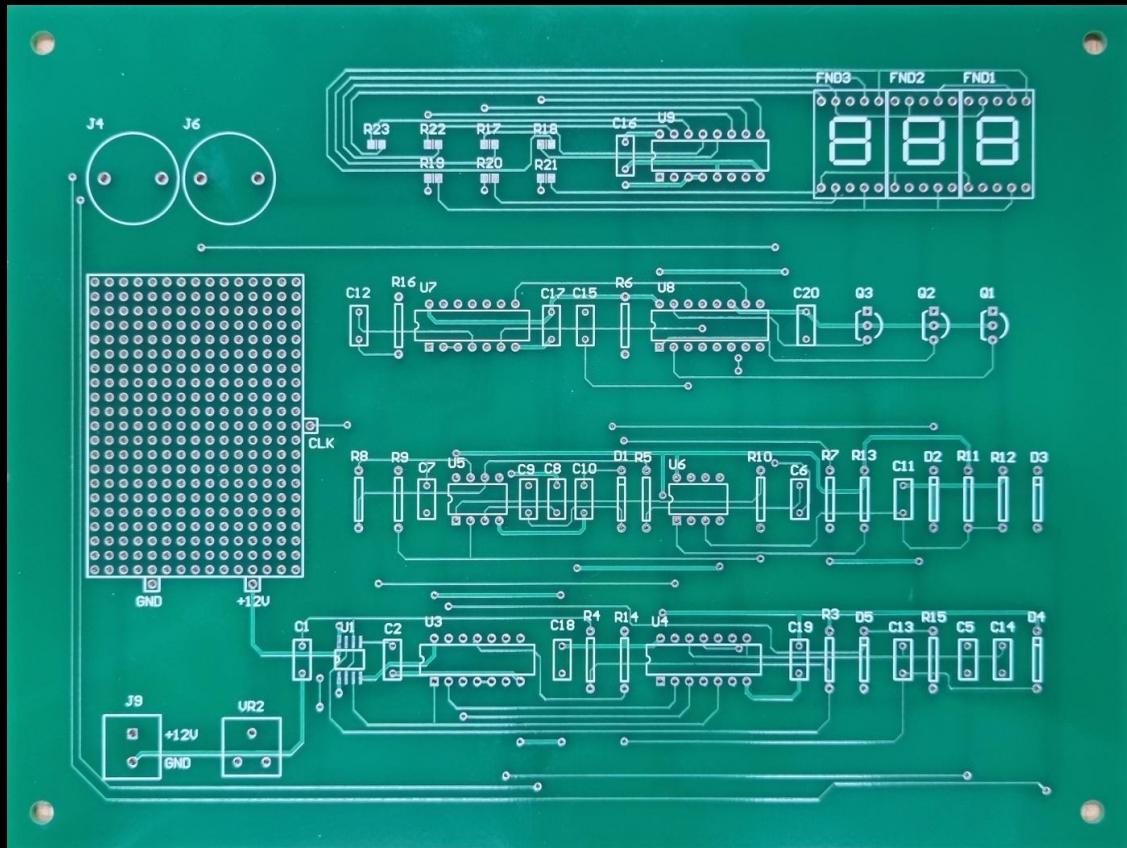
2. Solution

- 1) x10 & x10 is can Amplified to 100 times
- 2) C7 Remove & short → Cost ↓
- 3) Rising for resolution to over sampling → Meta stability ↑
- 4) Need to OPAMP Pull-down register (Save to bias current pass)
- 5) Place to Varistor nearby power port → PI & SI ↑
- 6) Use to FND Array register (Cost ↓)
- 7) Change to Xtal (Crystal Oscillator) → Cost ↓ & make circuit more simply
- 8) Place to PNP base Array register (Protect for over-current)
- 9) Separate to power & gnd (Power and Signal line)
- 10) Rewiring for R1(short), R2(114kΩ)



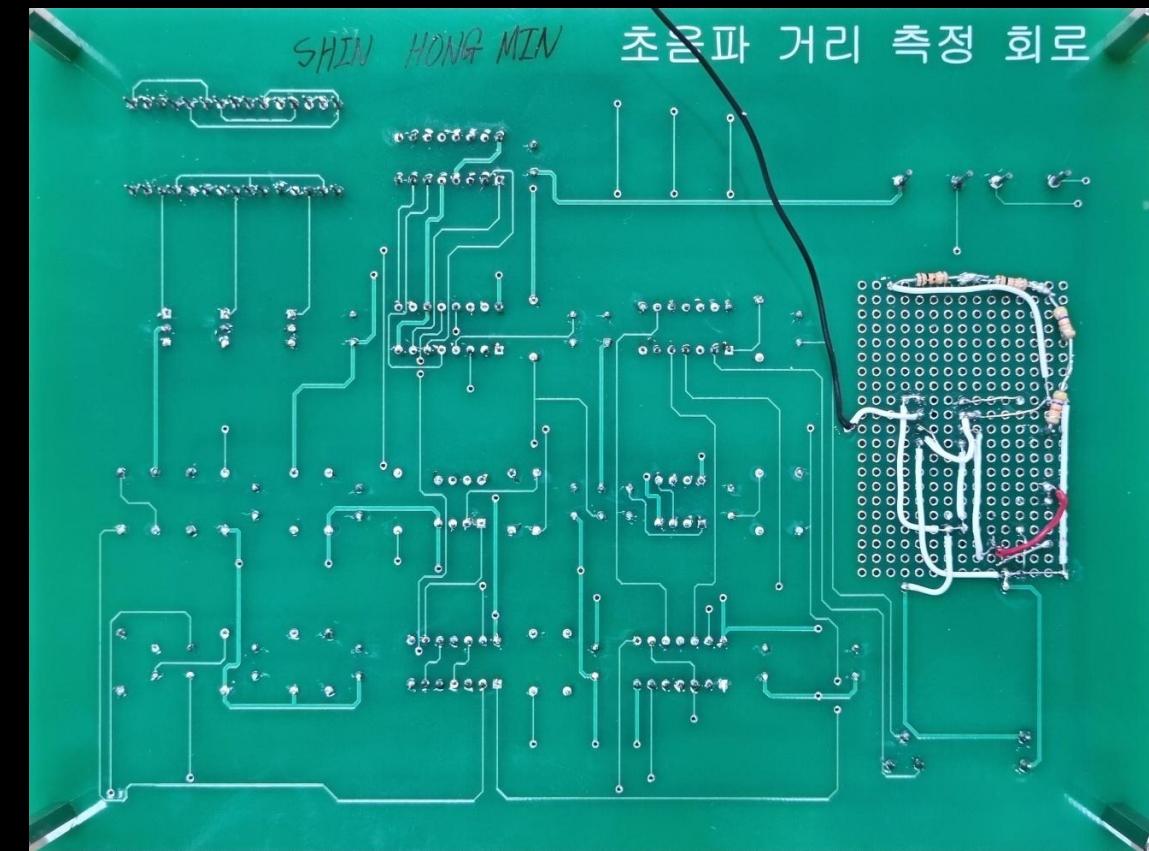
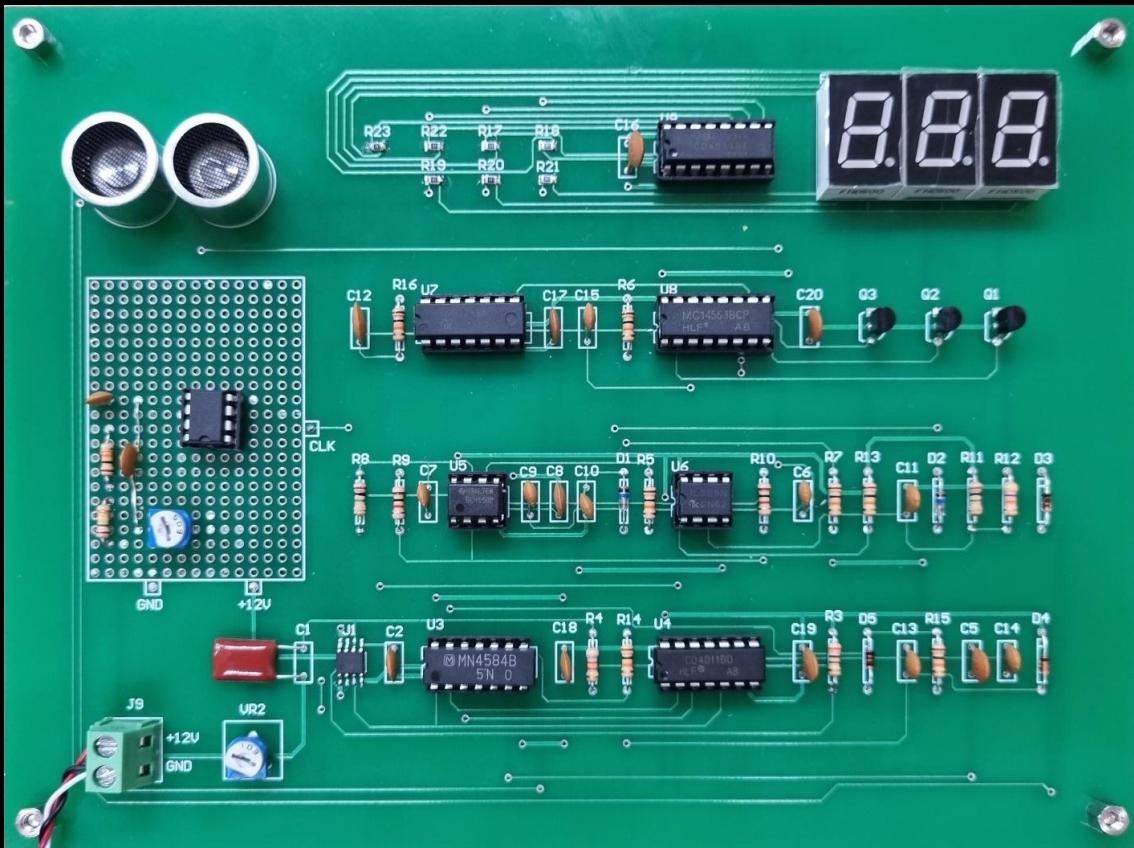
Conclusions

3. PCB (Before Soldering)

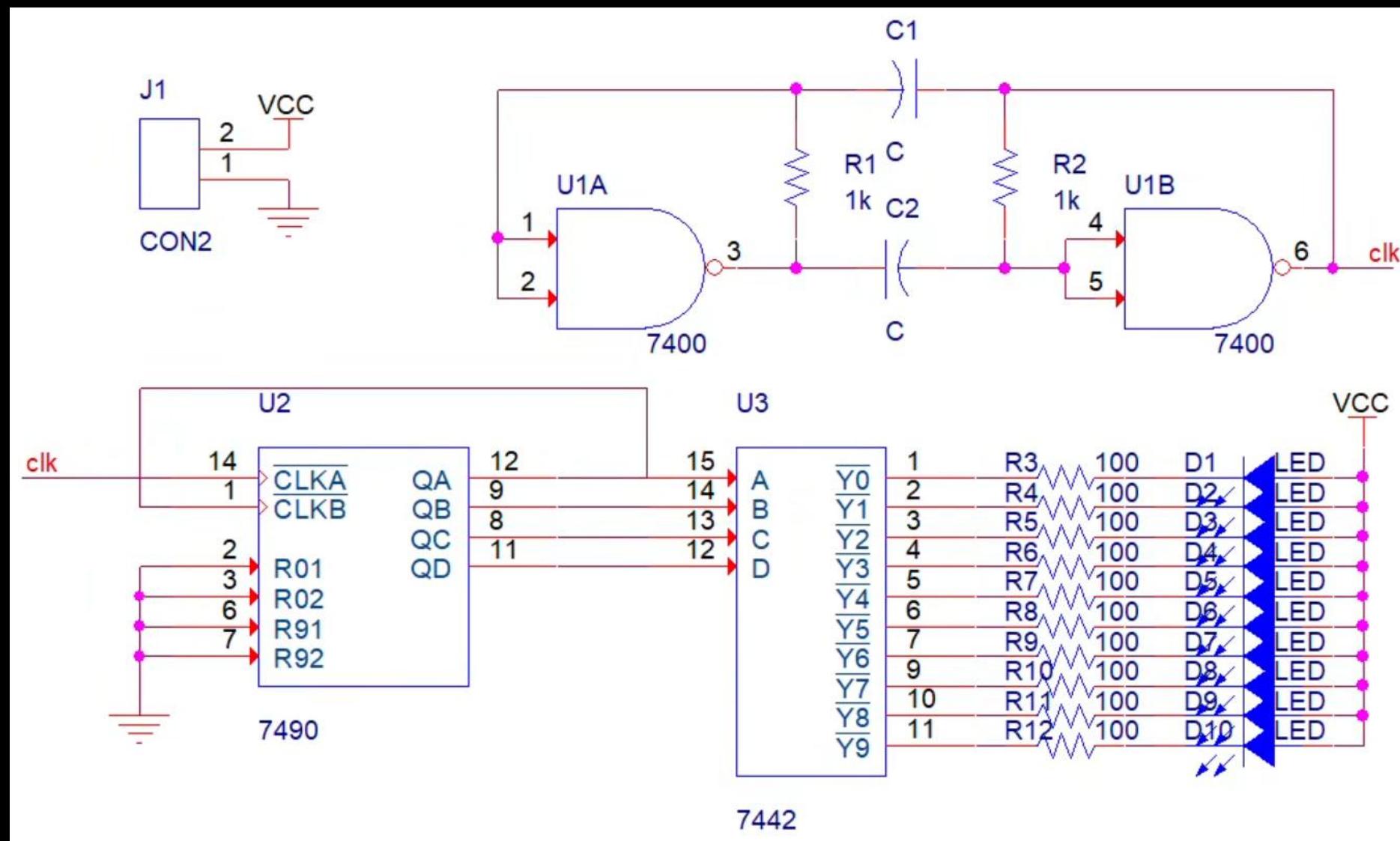


Conclusions

4. PCB (After Soldering)

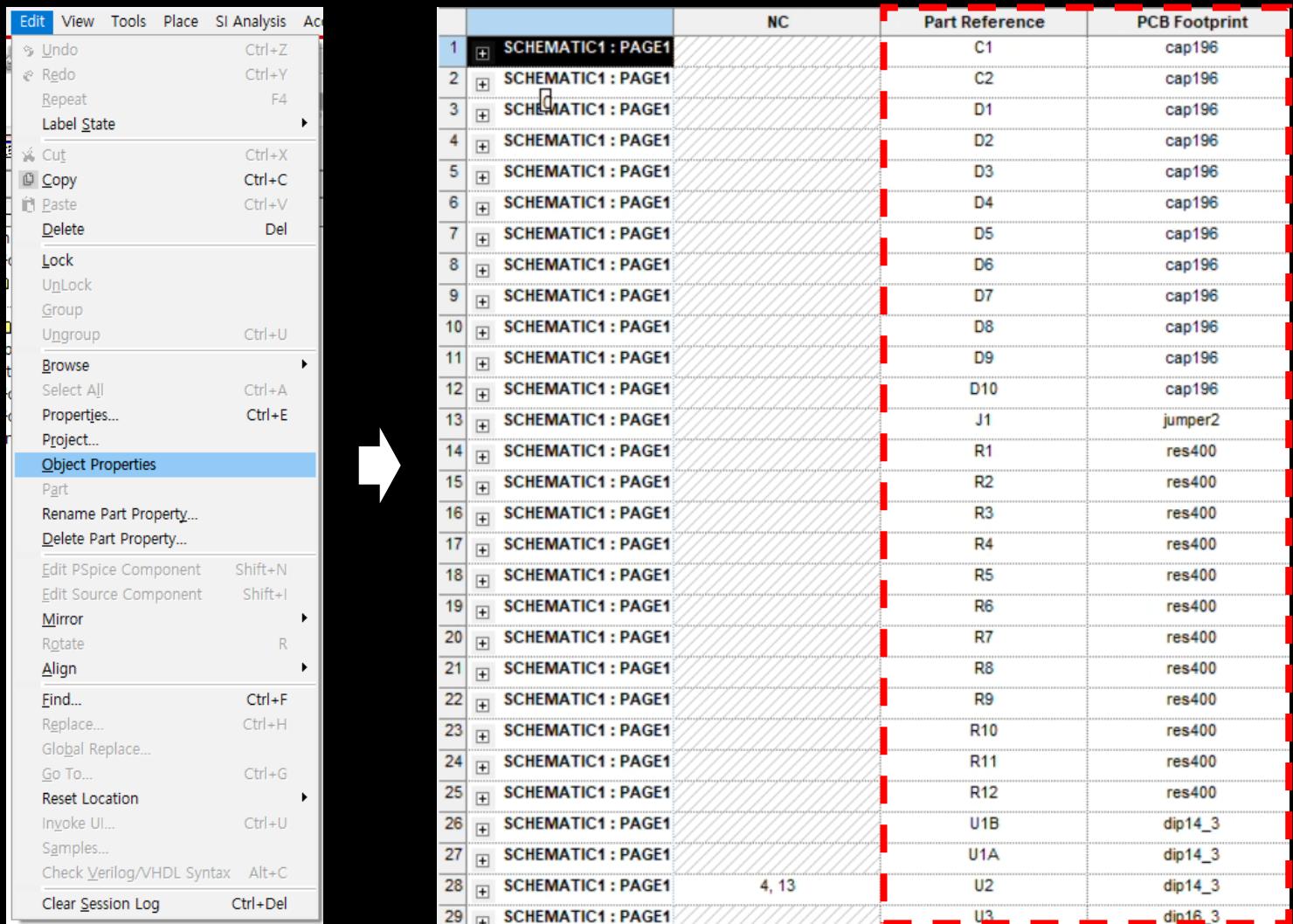


Schematic



Procedure of PCB Design

Setting for Footprint



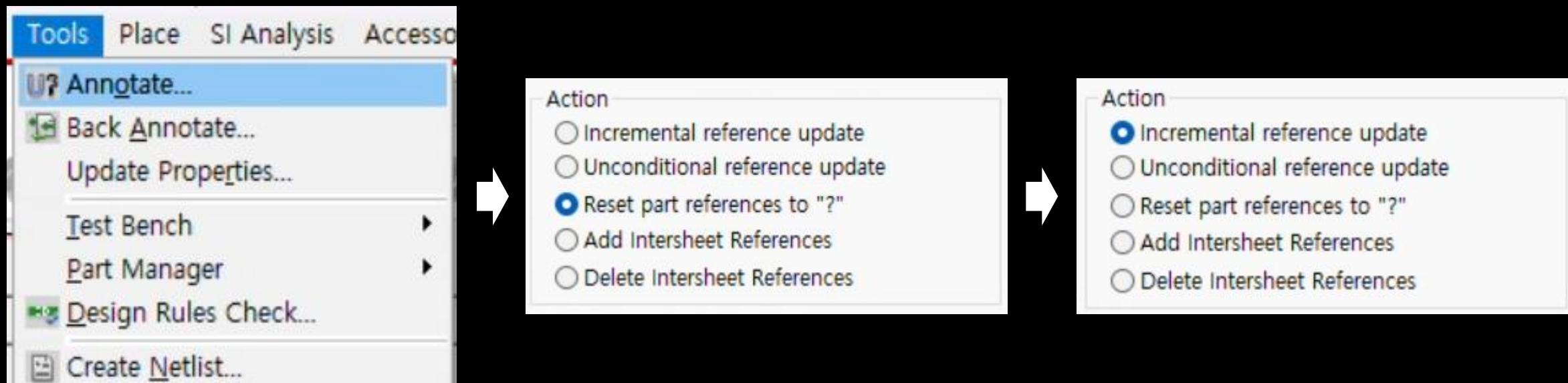
The screenshot shows a software interface for PCB design. On the left, a vertical menu bar lists various tools and functions. A large white arrow points from the 'Object Properties' section of this menu towards a table on the right. The table is titled 'Part Reference' and 'PCB Footprint'. It contains 29 rows, each corresponding to a component in the schematic. The columns are labeled 'NC', 'Part Reference', and 'PCB Footprint'. The data in the table is as follows:

	NC	Part Reference	PCB Footprint
1	SCHEMATIC1 : PAGE1	C1	cap196
2	SCHEMATIC1 : PAGE1	C2	cap196
3	SCHEMATIC1 : PAGE1	D1	cap196
4	SCHEMATIC1 : PAGE1	D2	cap196
5	SCHEMATIC1 : PAGE1	D3	cap196
6	SCHEMATIC1 : PAGE1	D4	cap196
7	SCHEMATIC1 : PAGE1	D5	cap196
8	SCHEMATIC1 : PAGE1	D6	cap196
9	SCHEMATIC1 : PAGE1	D7	cap196
10	SCHEMATIC1 : PAGE1	D8	cap196
11	SCHEMATIC1 : PAGE1	D9	cap196
12	SCHEMATIC1 : PAGE1	D10	cap196
13	SCHEMATIC1 : PAGE1	J1	jumper2
14	SCHEMATIC1 : PAGE1	R1	res400
15	SCHEMATIC1 : PAGE1	R2	res400
16	SCHEMATIC1 : PAGE1	R3	res400
17	SCHEMATIC1 : PAGE1	R4	res400
18	SCHEMATIC1 : PAGE1	R5	res400
19	SCHEMATIC1 : PAGE1	R6	res400
20	SCHEMATIC1 : PAGE1	R7	res400
21	SCHEMATIC1 : PAGE1	R8	res400
22	SCHEMATIC1 : PAGE1	R9	res400
23	SCHEMATIC1 : PAGE1	R10	res400
24	SCHEMATIC1 : PAGE1	R11	res400
25	SCHEMATIC1 : PAGE1	R12	res400
26	SCHEMATIC1 : PAGE1	U1B	dip14_3
27	SCHEMATIC1 : PAGE1	U1A	dip14_3
28	SCHEMATIC1 : PAGE1	U2	dip14_3
29	SCHEMATIC1 : PAGE1	U3	dip16_3

- Setting for Footprint
- C1,2, D1~10 : cap196
- J1 : jumper2
- R1~12 : res400
- U1,2 : dip14_3
- U3 : dip16_3

Procedure of PCB Design

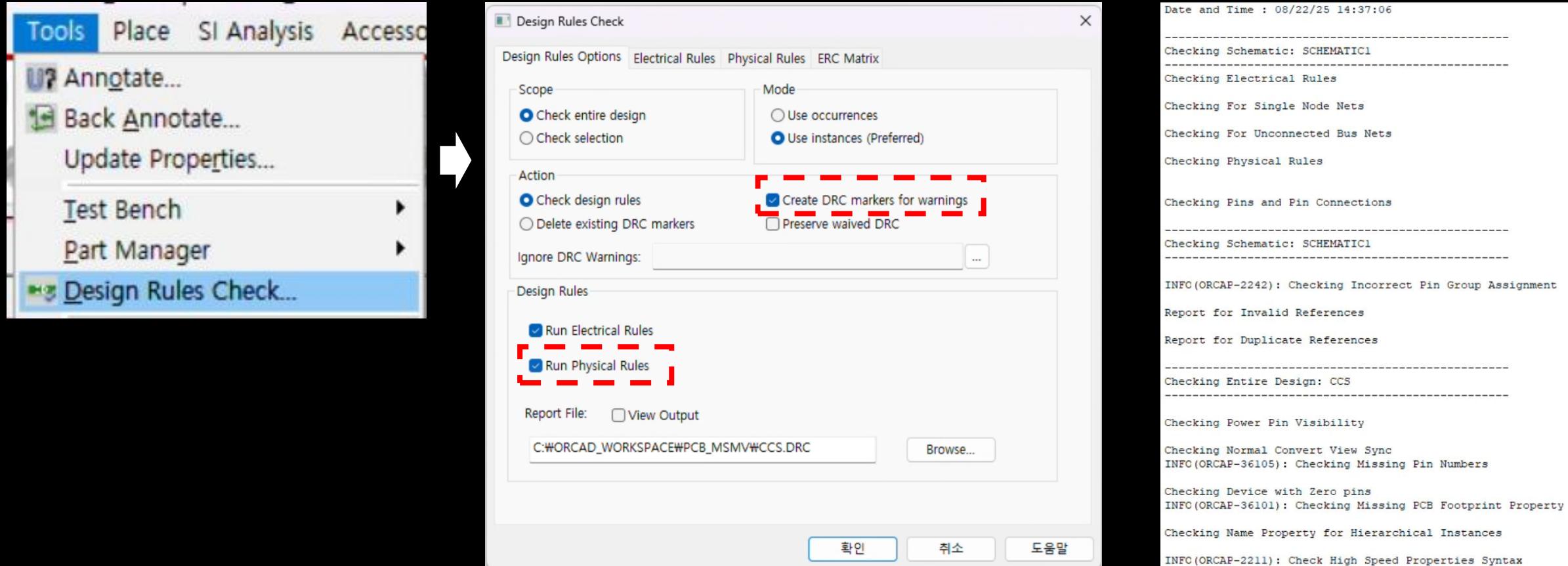
Annotate



1. Tools > Annotate > Action(Reset ref)
2. Tools > Annotate > Action(Incremental ref)

Procedure of PCB Design

Design Rules Check (DRC)



1. Tools > Design Rules Check > Run Physical Rules check

Procedure of PCB Design

Design Rules Check (DRC) Result

INFO(ORCAP-2212): Check Power Ground Mismatch		
Reporting Unused Refdes in multiple part packages		
Part	Quantity	Reference
7400	2	U1: D C

Date and Time : 08/22/25 14:37:06		

Checking Schematic: SCHEMATIC1		

Checking Electrical Rules		
Checking For Single Node Nets		
Checking For Unconnected Bus Nets		
Checking Physical Rules		
Checking Pins and Pin Connections		

Checking Schematic: SCHEMATIC1		

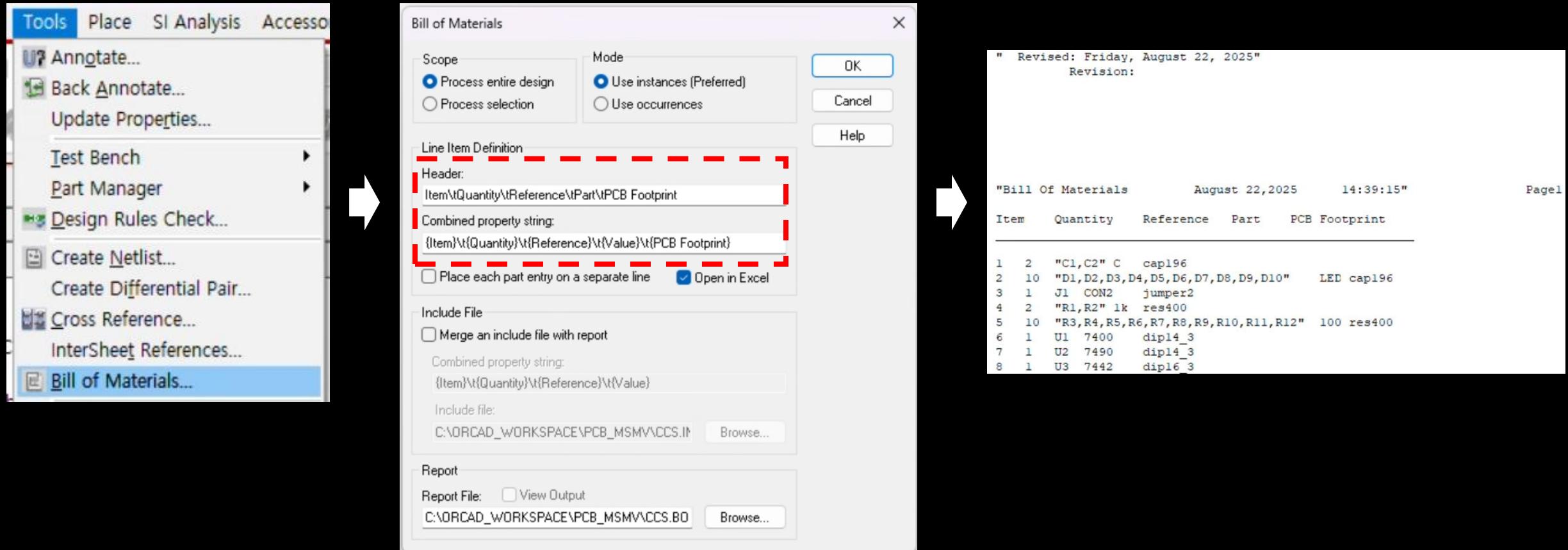
INFO(ORCAP-2242): Checking Incorrect Pin Group Assignment		
Report for Invalid References		
Report for Duplicate References		

Checking Entire Design: CCS		

Checking Power Pin Visibility		
Checking Normal Convert View Sync		
INFO(ORCAP-36105): Checking Missing Pin Numbers		
Checking Device with Zero pins		
INFO(ORCAP-36101): Checking Missing PCB Footprint Property		
Checking Name Property for Hierarchical Instances		
INFO(ORCAP-2211): Check High Speed Properties Syntax		

Procedure of PCB Design

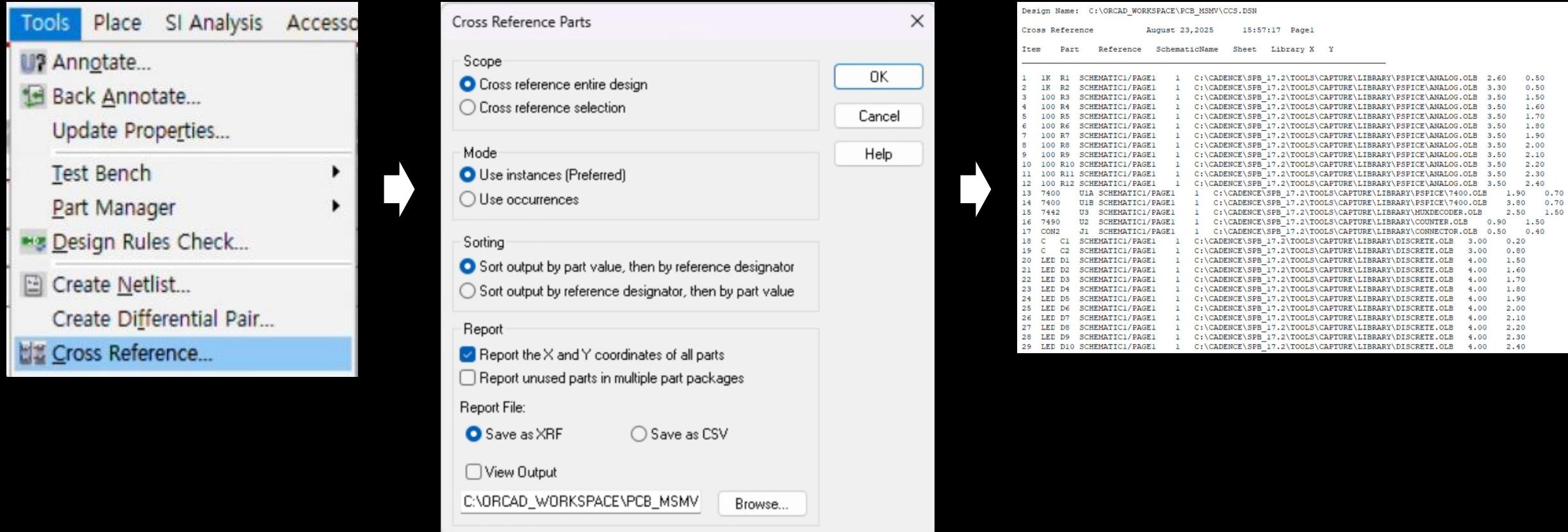
Bill of Materials (BOM)



1. Tools > Bill of Materials > add to Header & Combined property string (tPCB Footprint & t{PCB Footprint})

Procedure of PCB Design

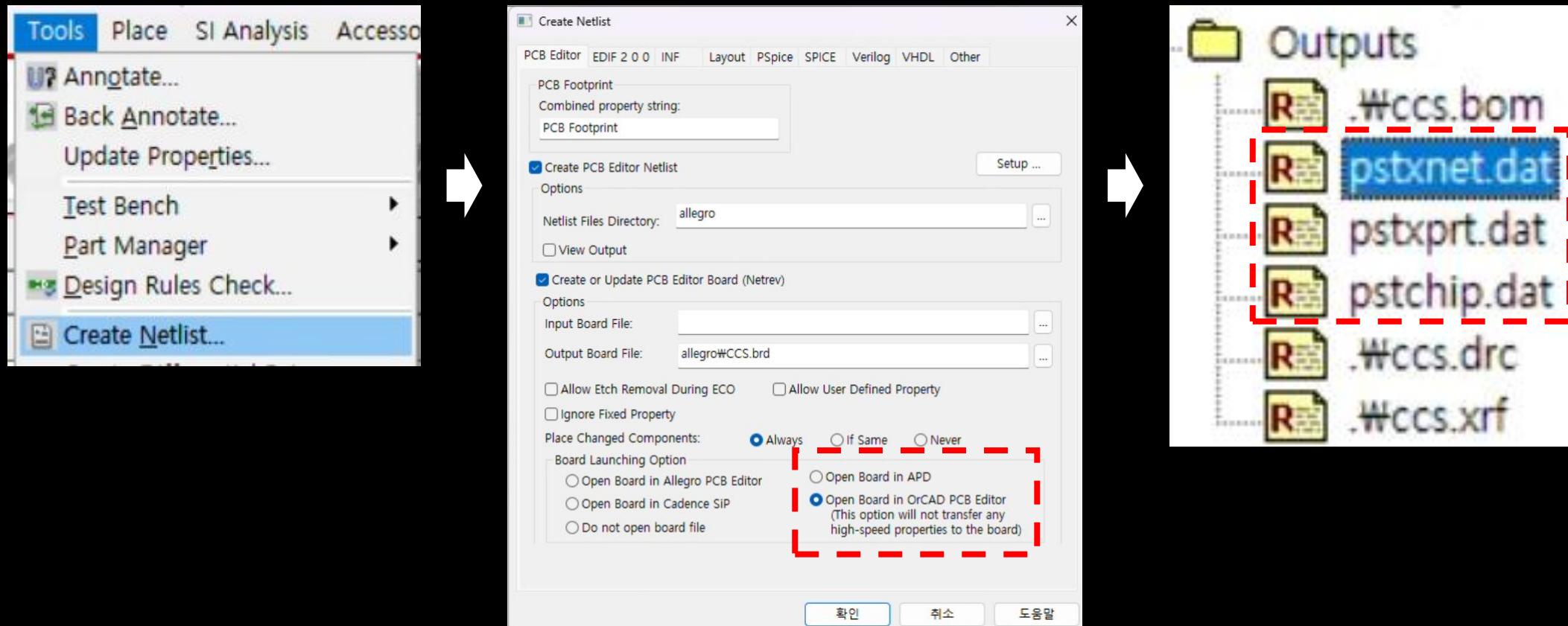
Cross Reference



1. Tools > Cross Reference > Check to .xrf file

Procedure of PCB Design

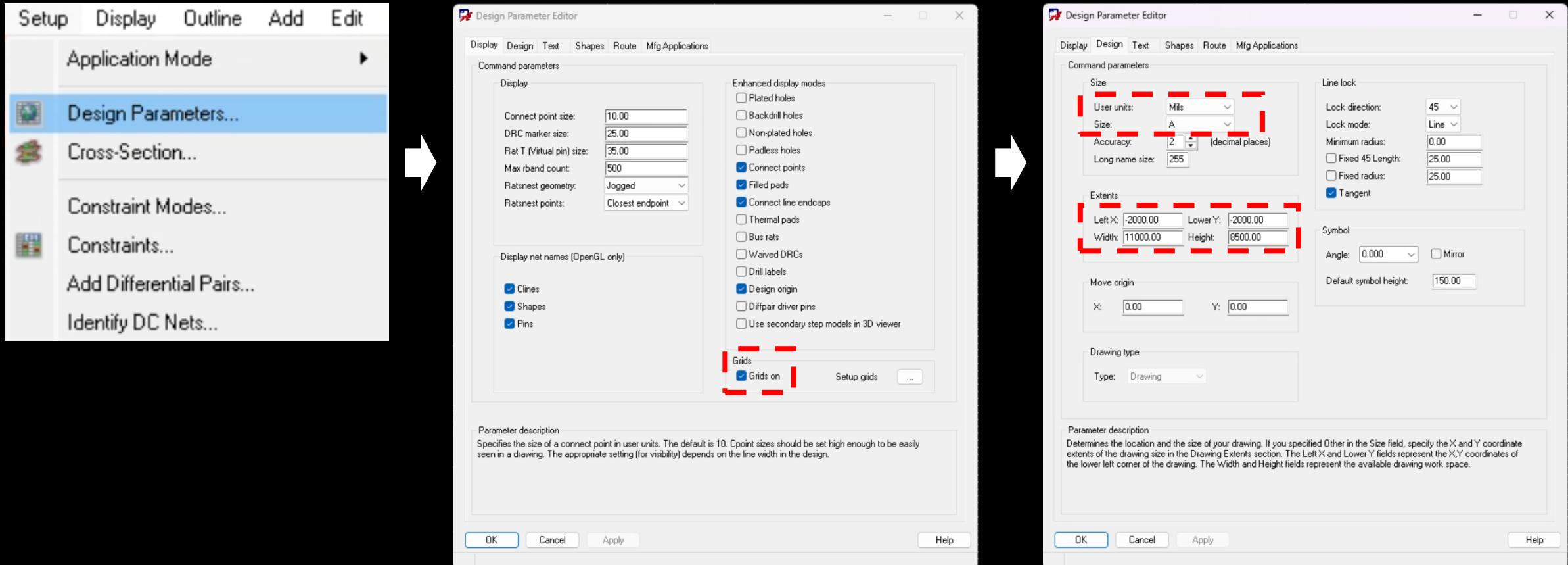
Netlist



1. Tools > Netlist > Check to Open Board in OrCAD PCB Editor > Check to .dat file

Procedure of PCB Design

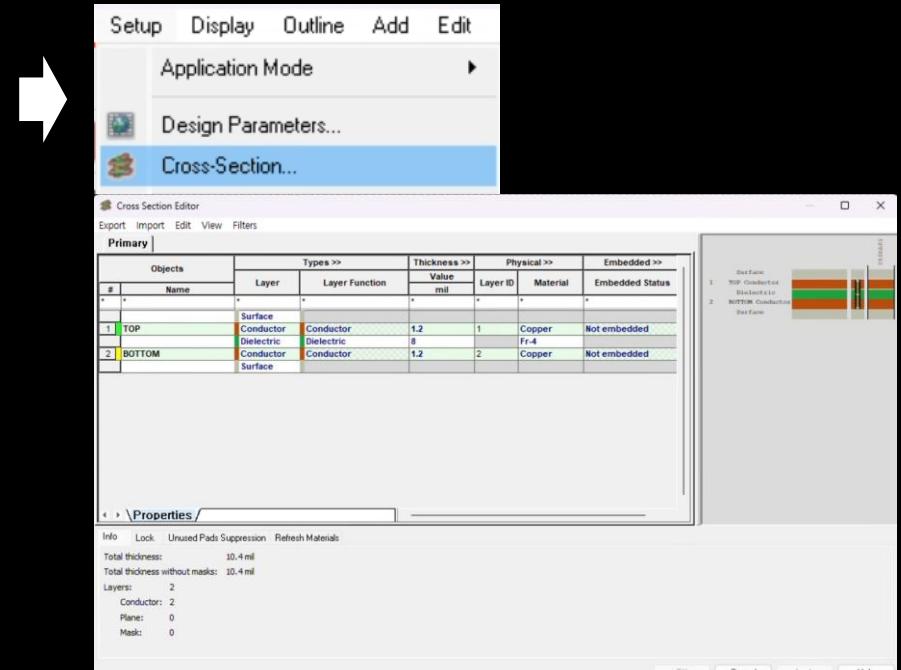
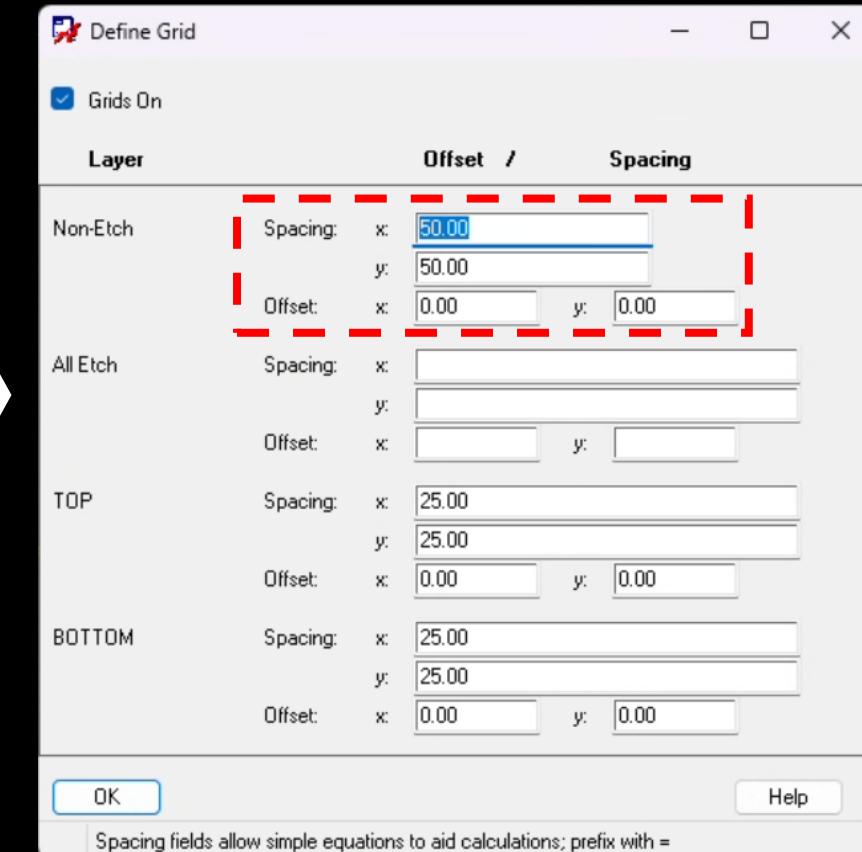
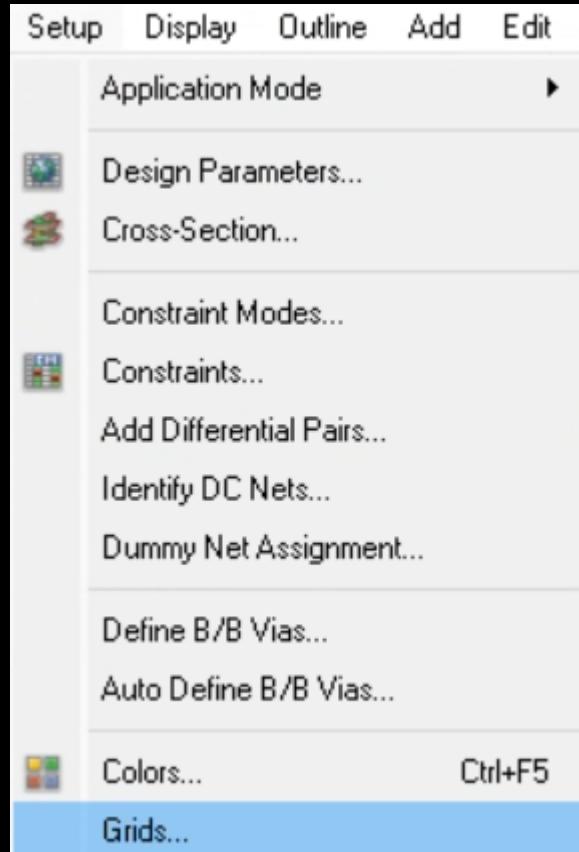
Setting to Orcad PCB Designer Preferences



1. Setup > Design Parameter Editor
2. Display > Grids on check
3. Design > Setting for User units : Mils, Size : A
4. Extents > Setting for Left X, Lower Y : -2000

Procedure of PCB Design

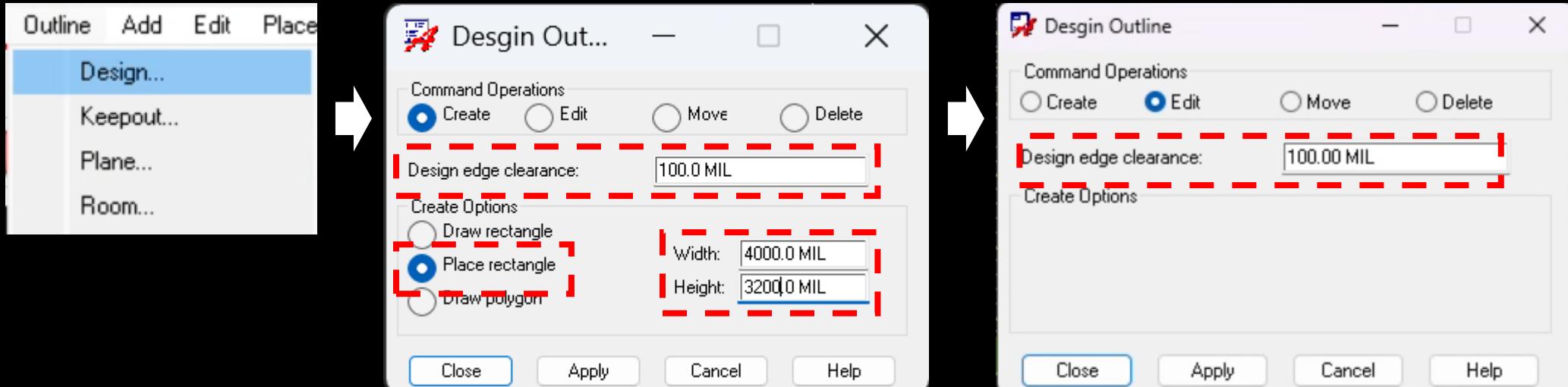
Setting to Orcad PCB Designer Preferences



1. Setup > Grids > Setting for Spacing x, y : 50
2. Check for Cross-Section (2 Layer & FR4)

Procedure of PCB Design

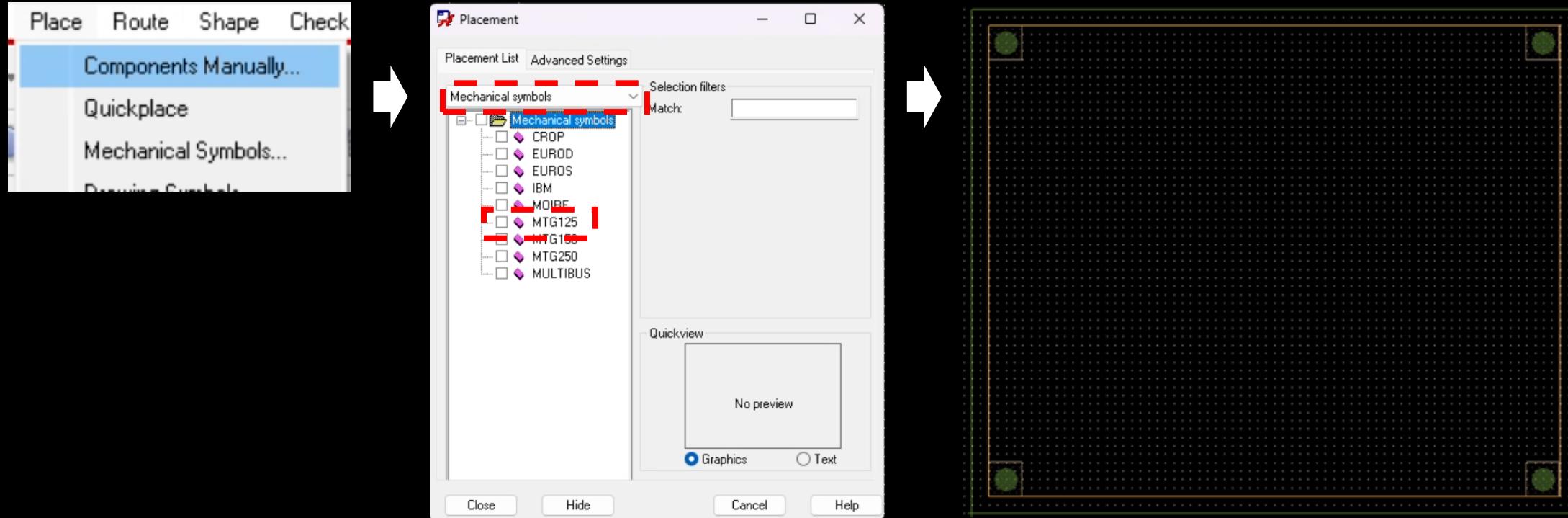
Board Outline



1. Outline > Design > Setting for Design edge clearance :
100 > Create Options : Place rectangle > Width : 4000,
Height : 3200
2. Edit > Design edge clearance : 100
3. Close

Procedure of PCB Design

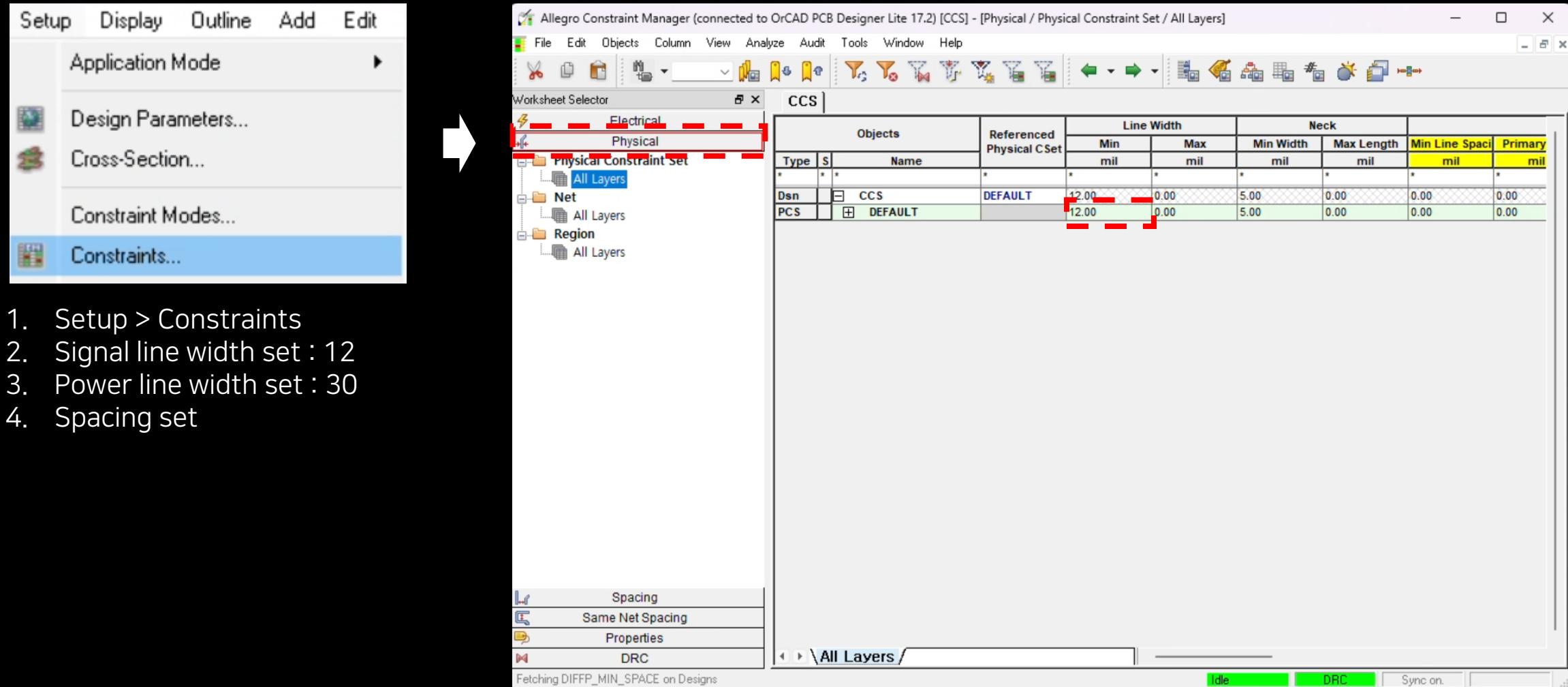
Place Components Manually



1. Place > Components Manually > Mechanical symbols > MTG125 X 4 placing

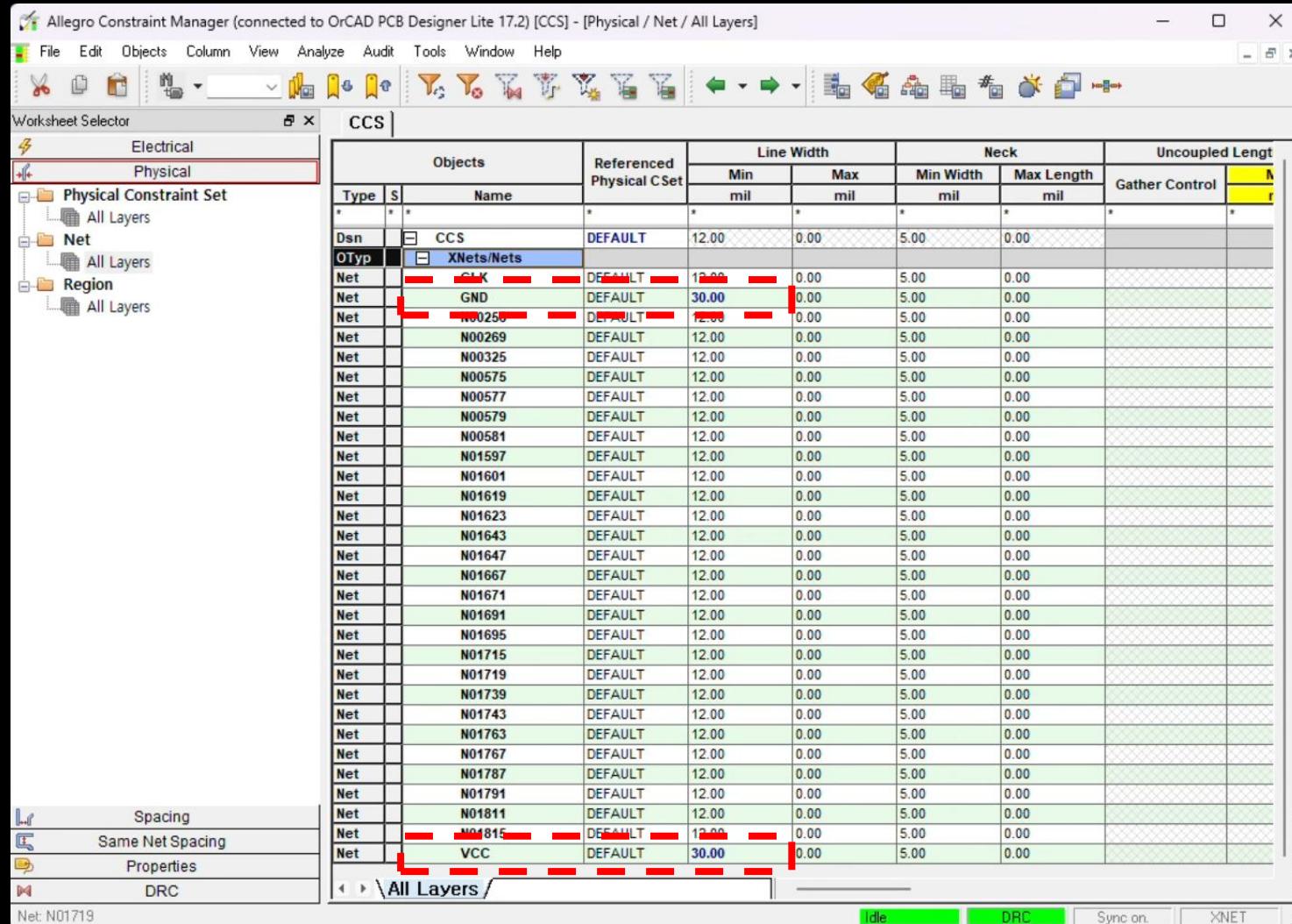
Procedure of PCB Design

Constraints Set



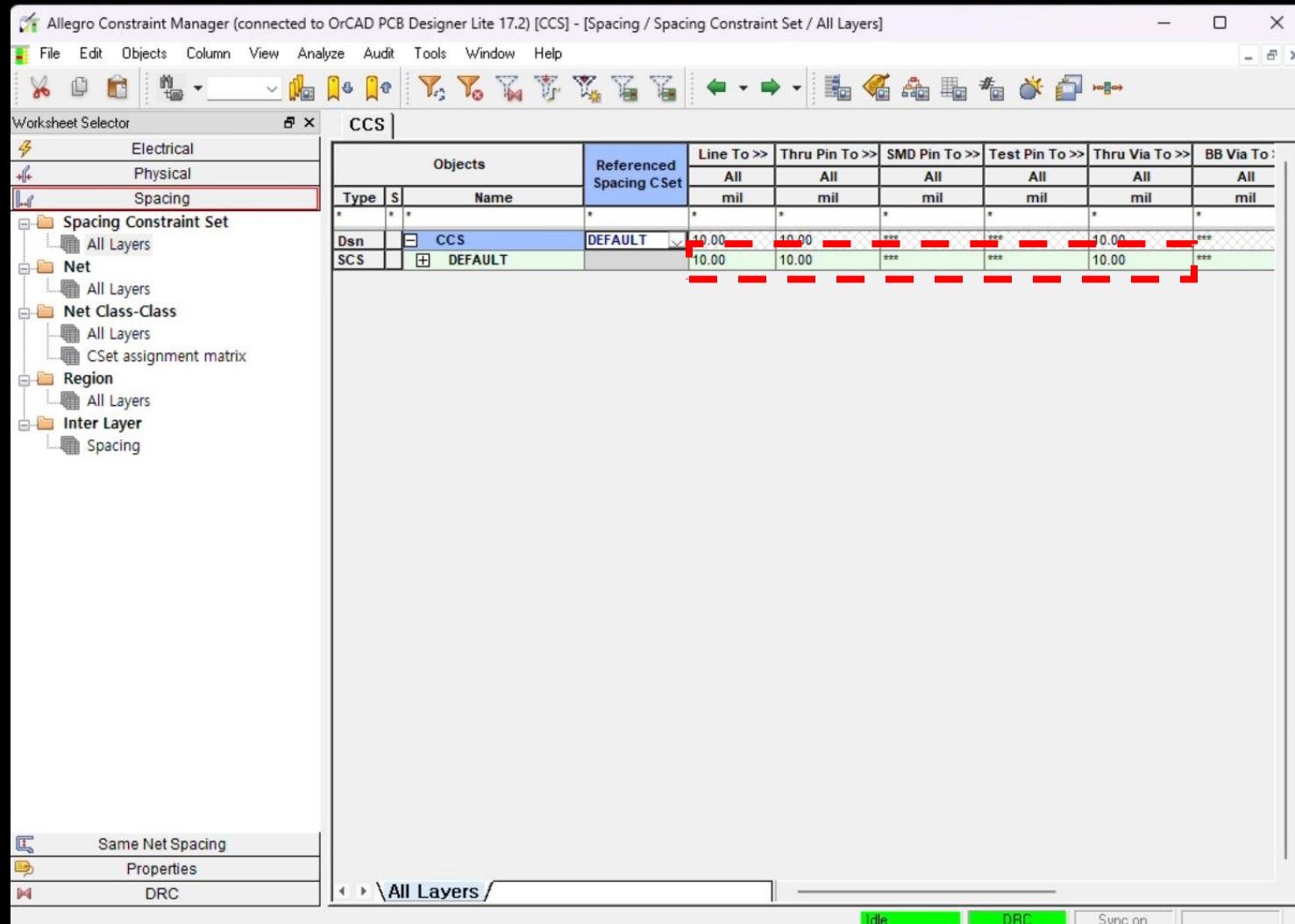
Procedure of PCB Design

Constraints Set



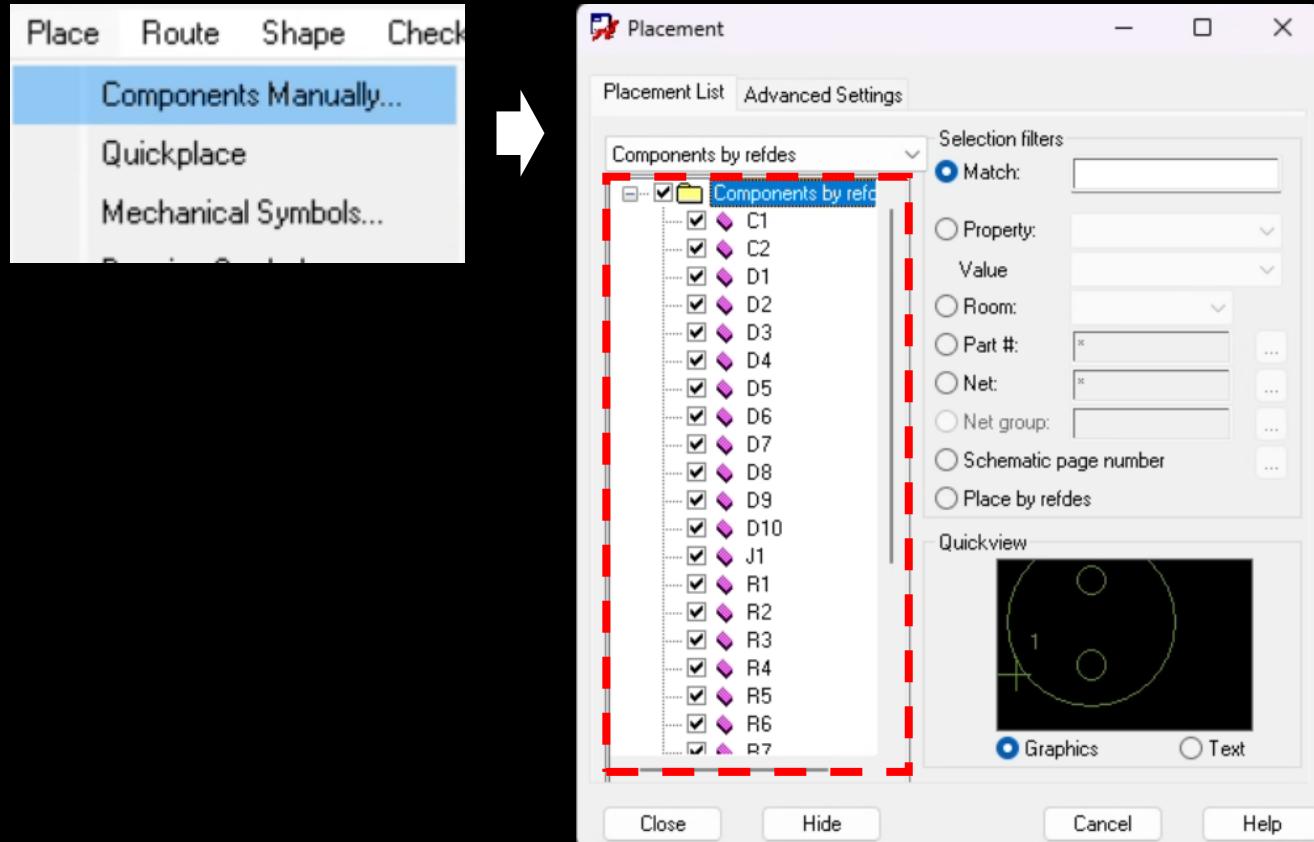
Procedure of PCB Design

Constraints Set

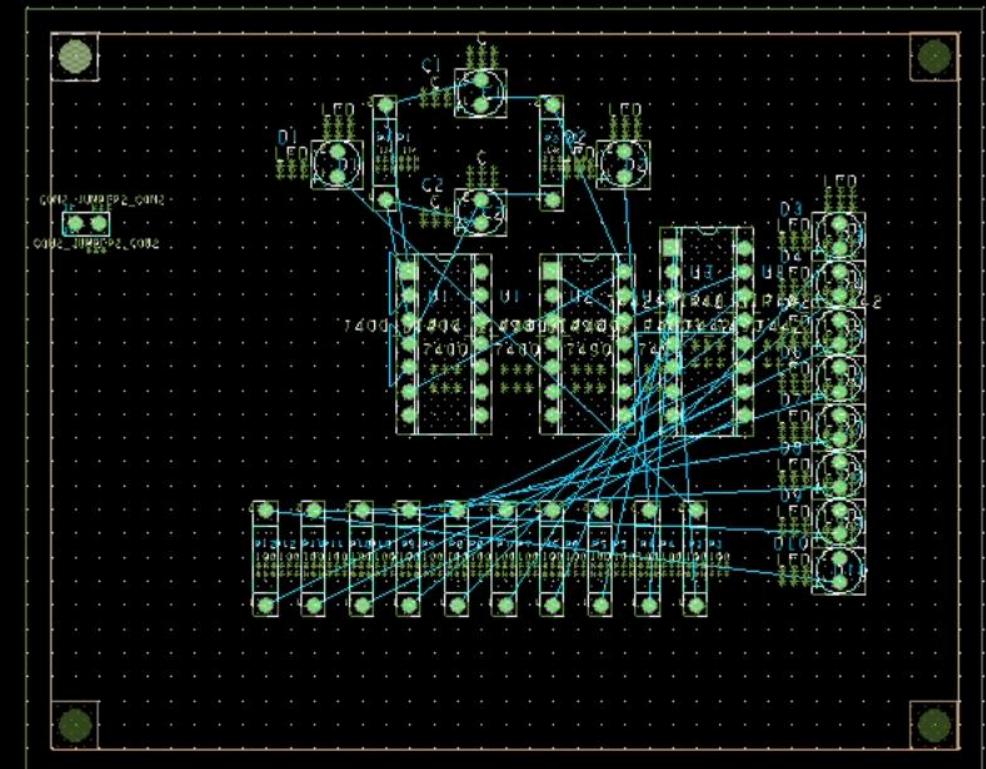


Procedure of PCB Design

Place Components

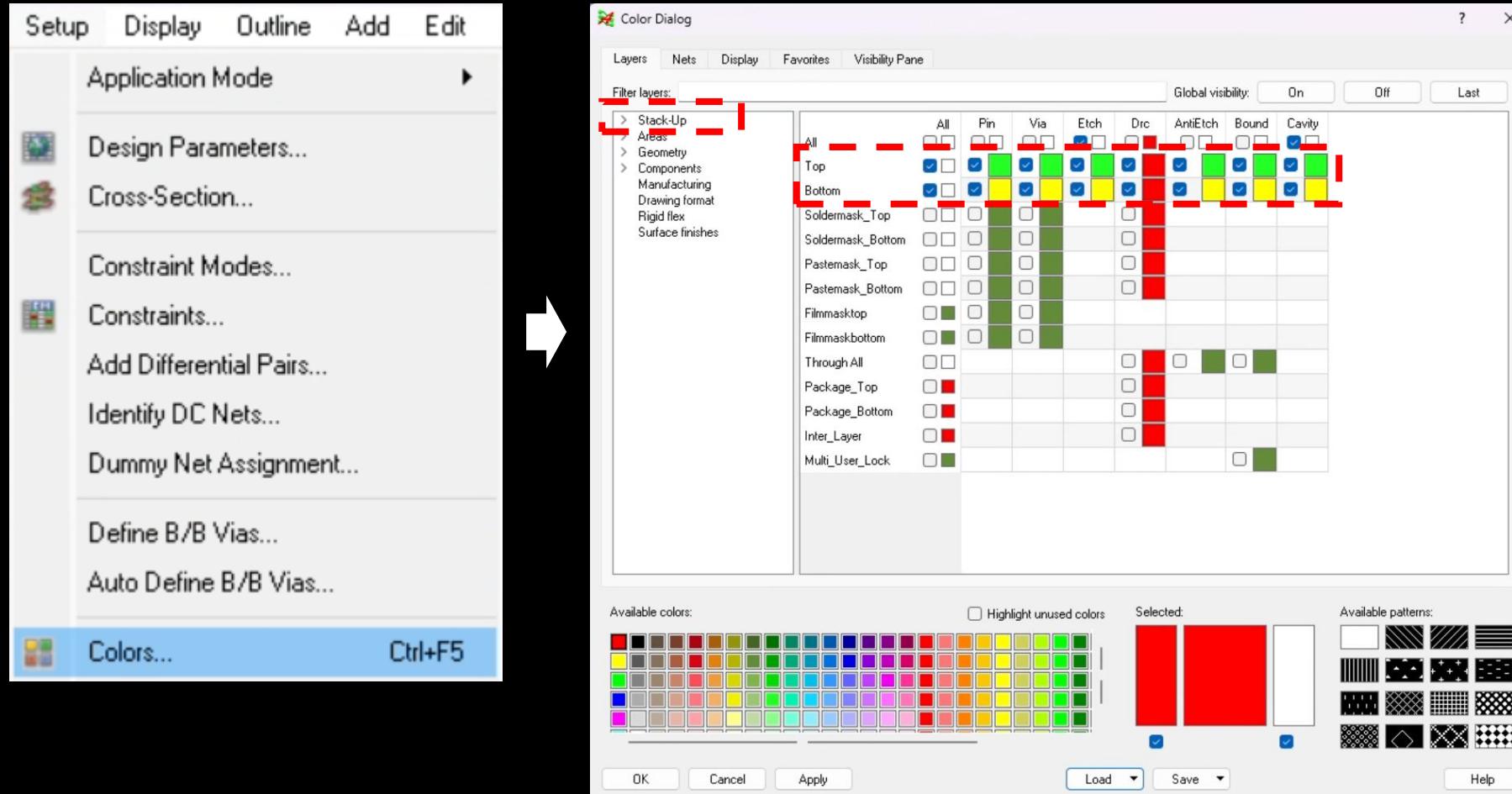


1. All parts check and placing



Procedure of PCB Design

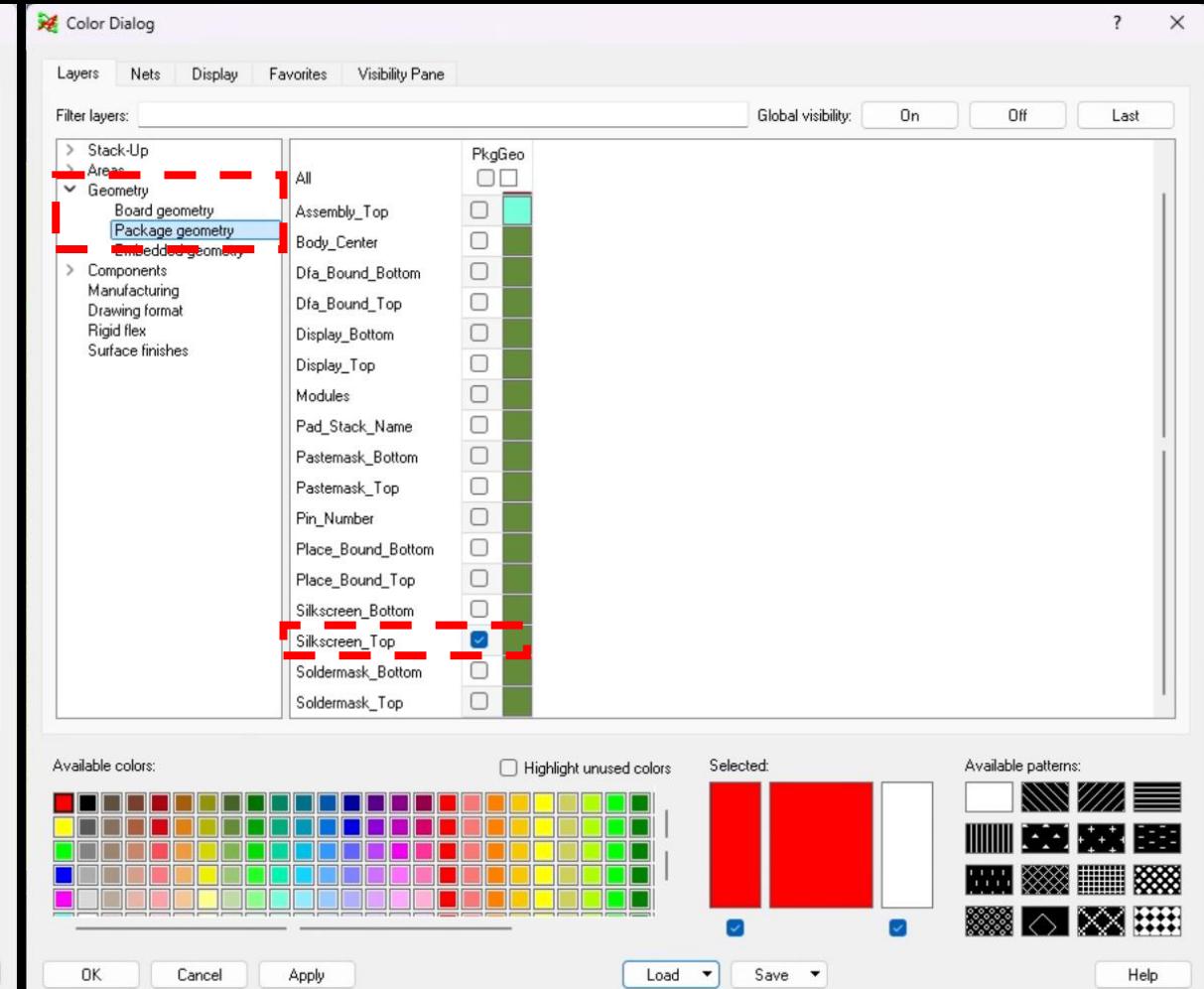
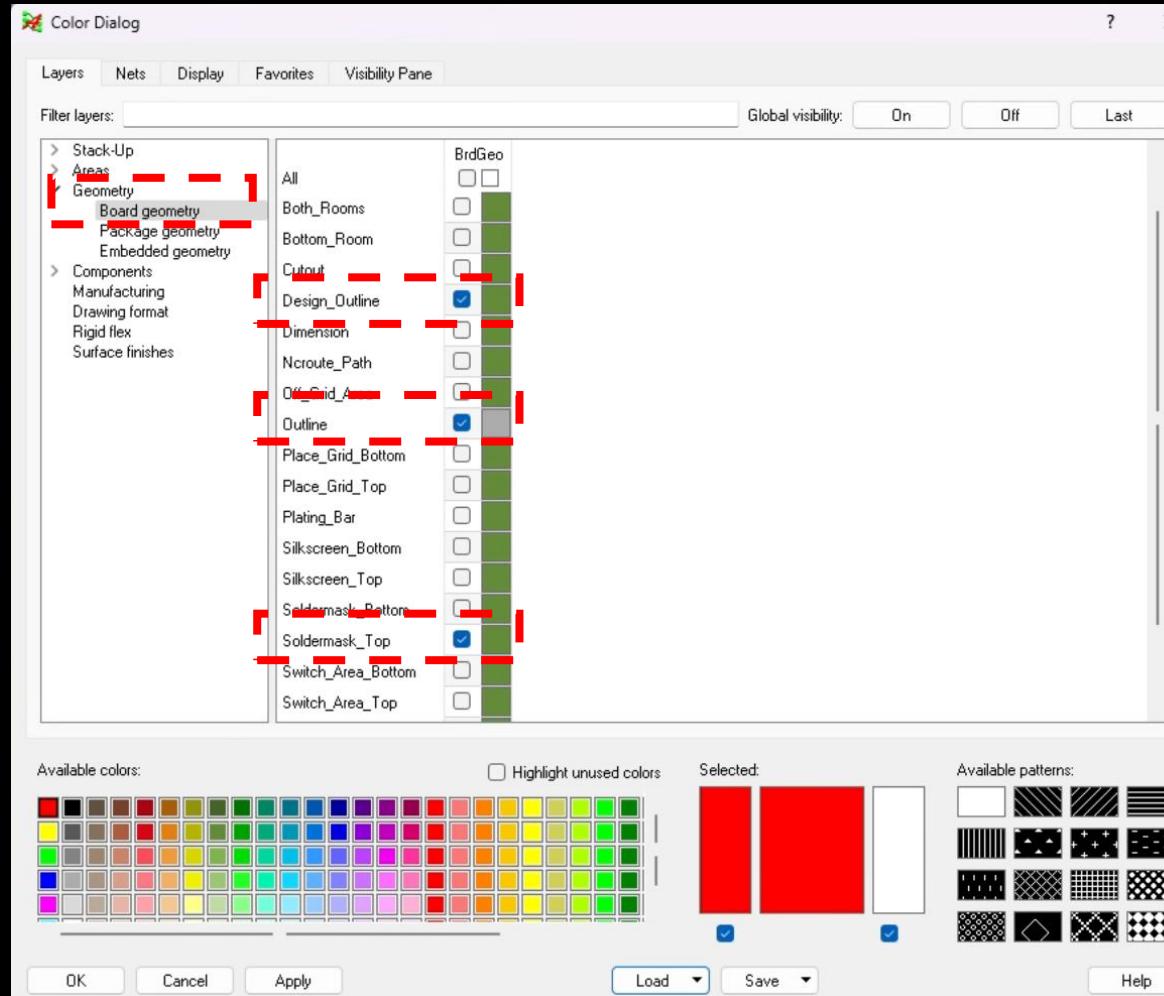
Color Setting



1. Setup > Colors > Stack-up > top, bottom all check

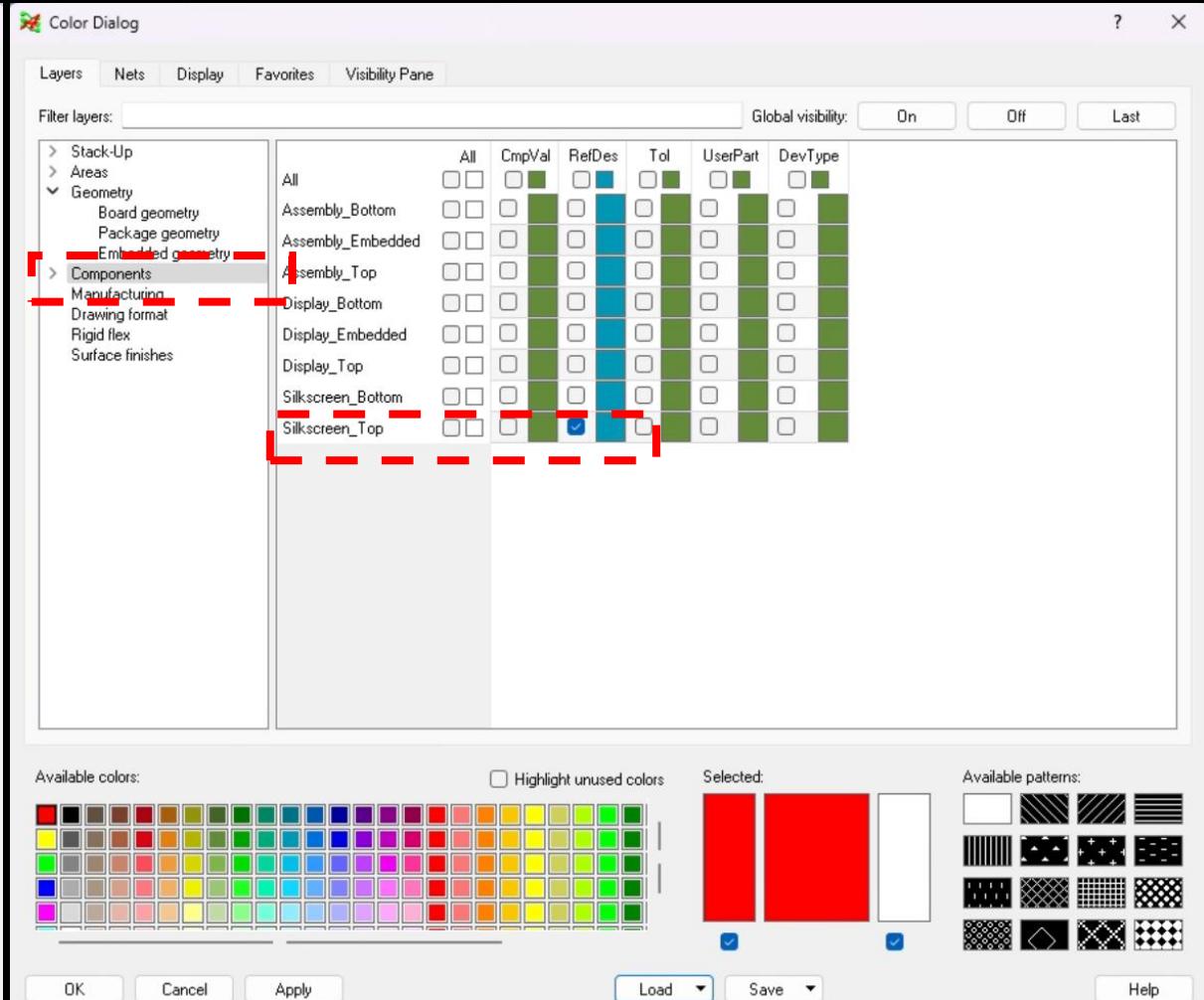
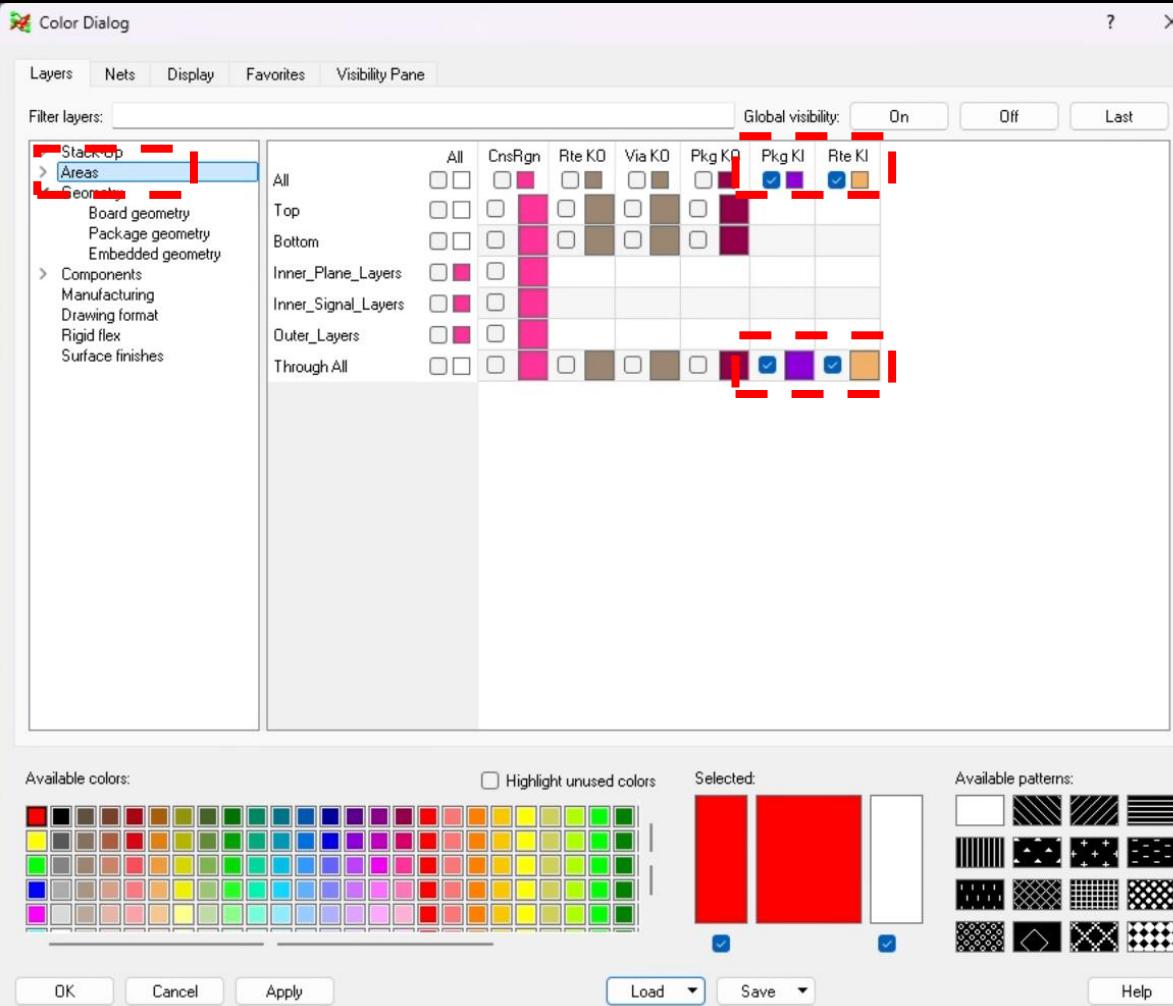
Procedure of PCB Design

Color Setting



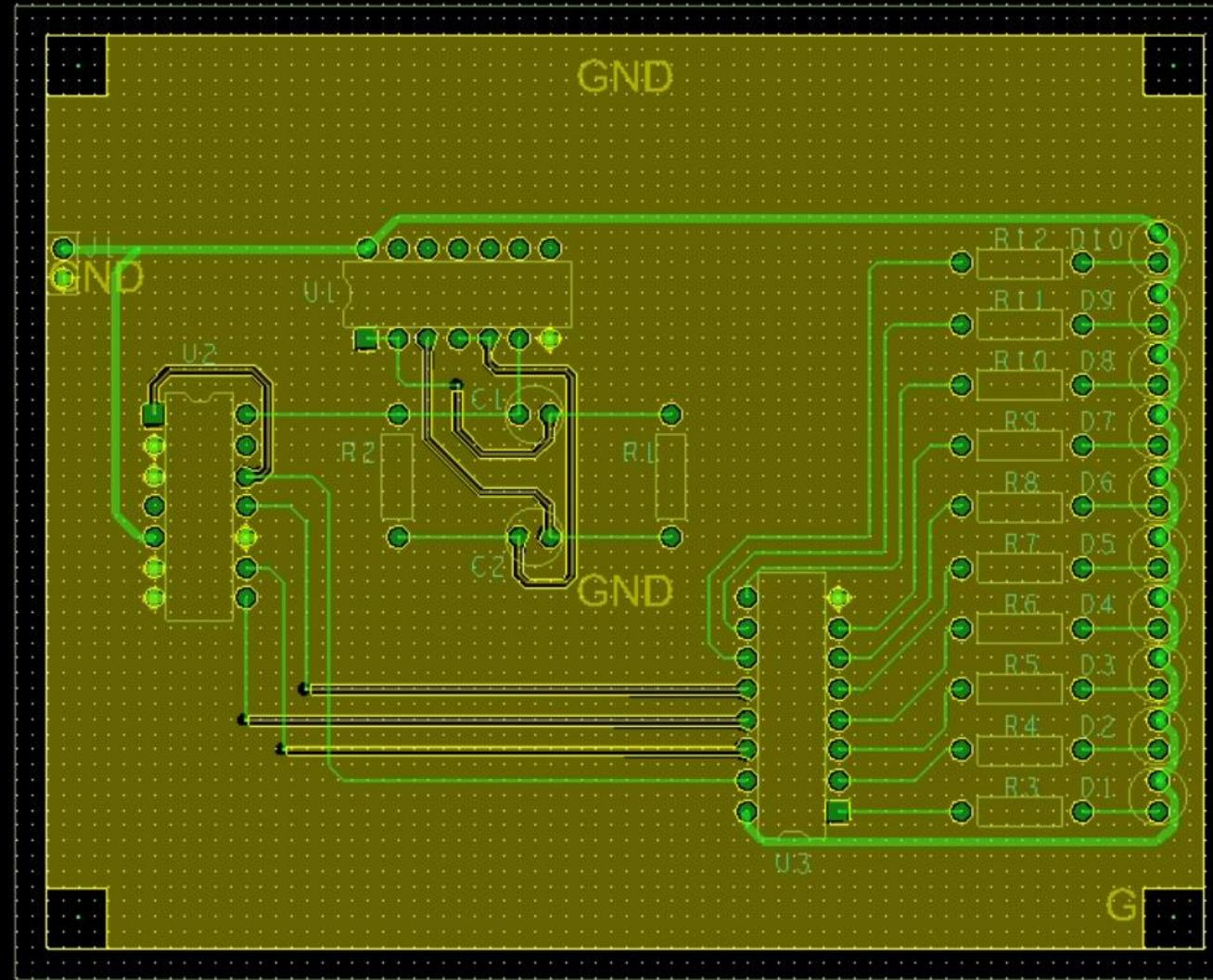
Procedure of PCB Design

Color Setting



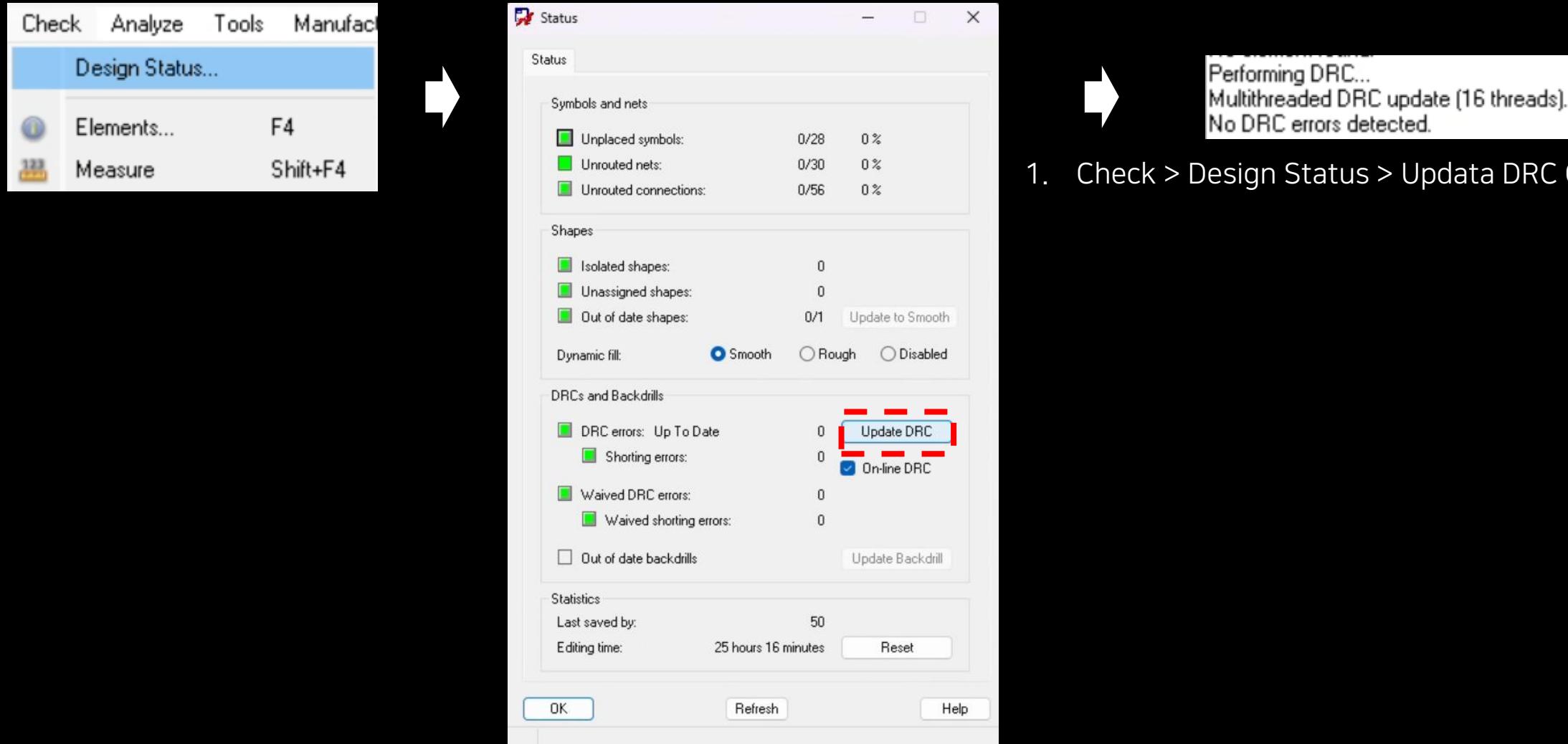
Procedure of PCB Design

Routing



Procedure of PCB Design

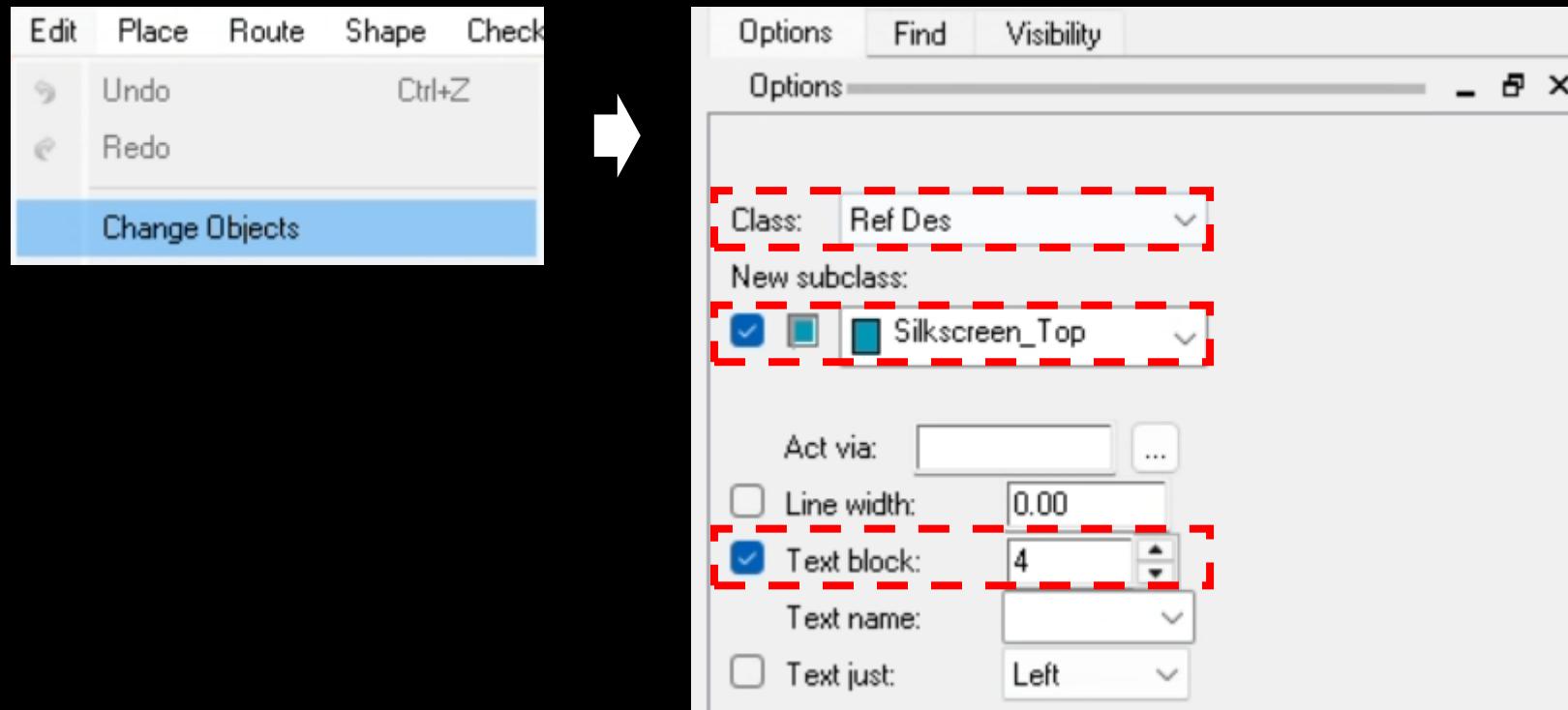
Design Status check



1. Check > Design Status > Update DRC Click

Procedure of PCB Design

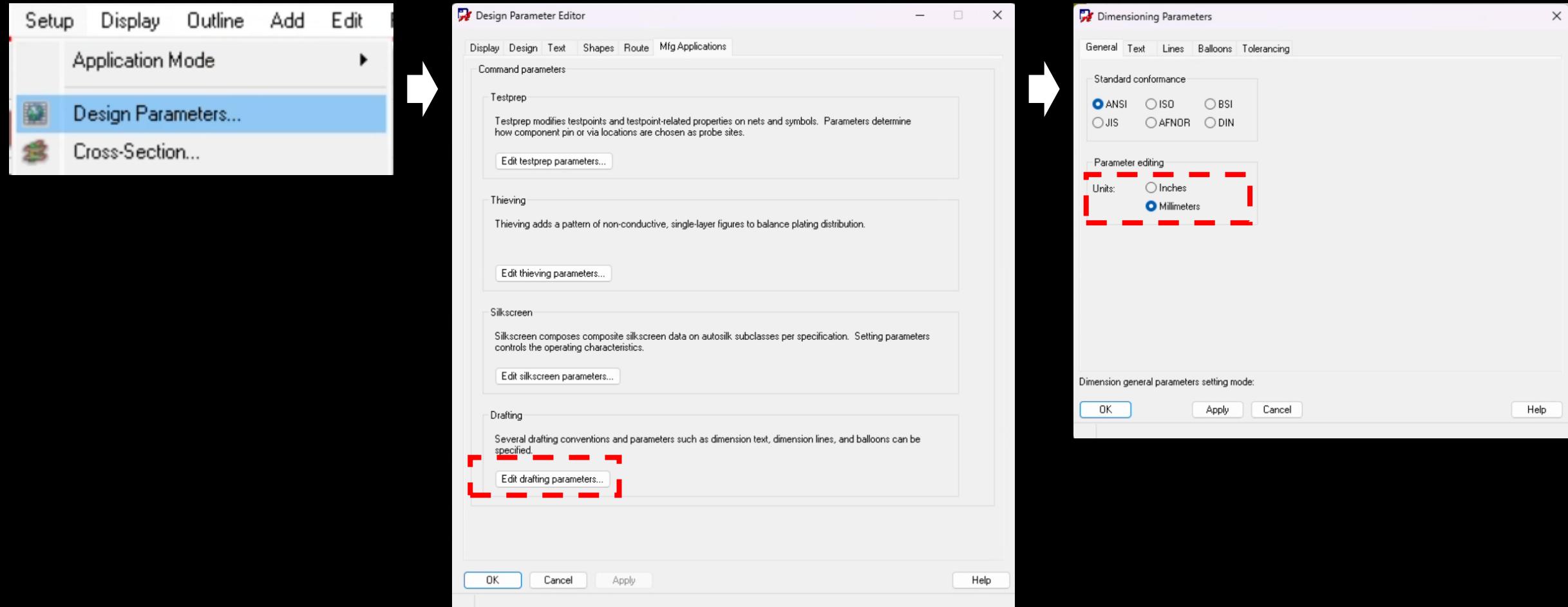
Reference



1. Edit > change objects > class : ref des > new subclass : silkscreen_top > text block : 4

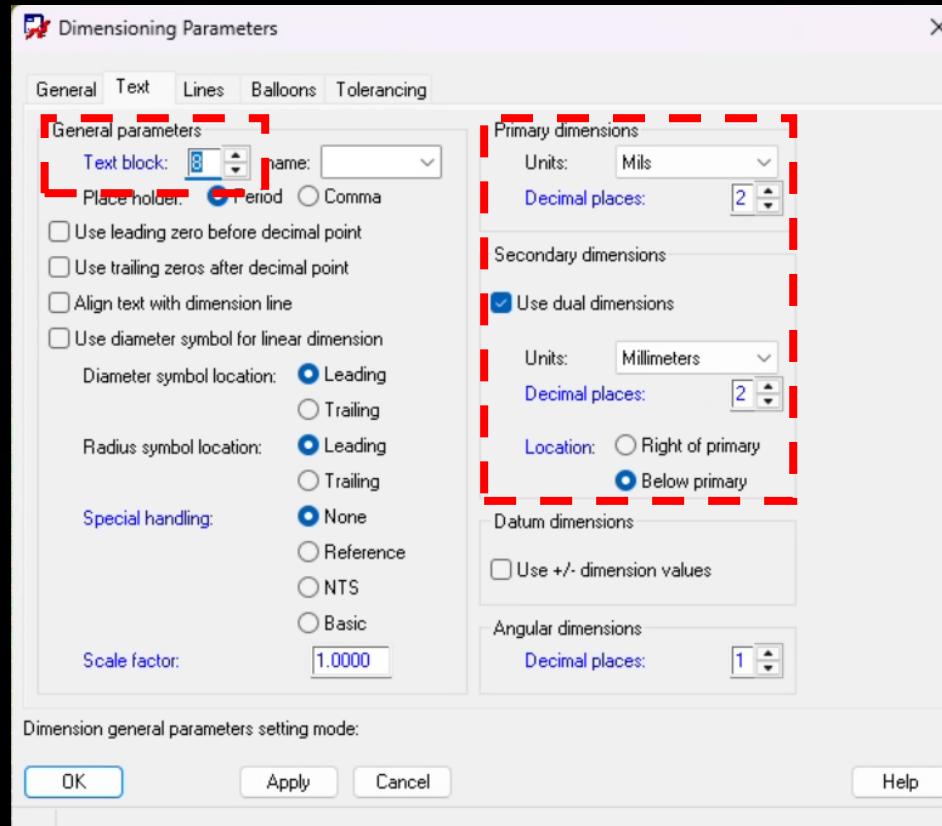
Procedure of PCB Design

Dimensions



Procedure of PCB Design

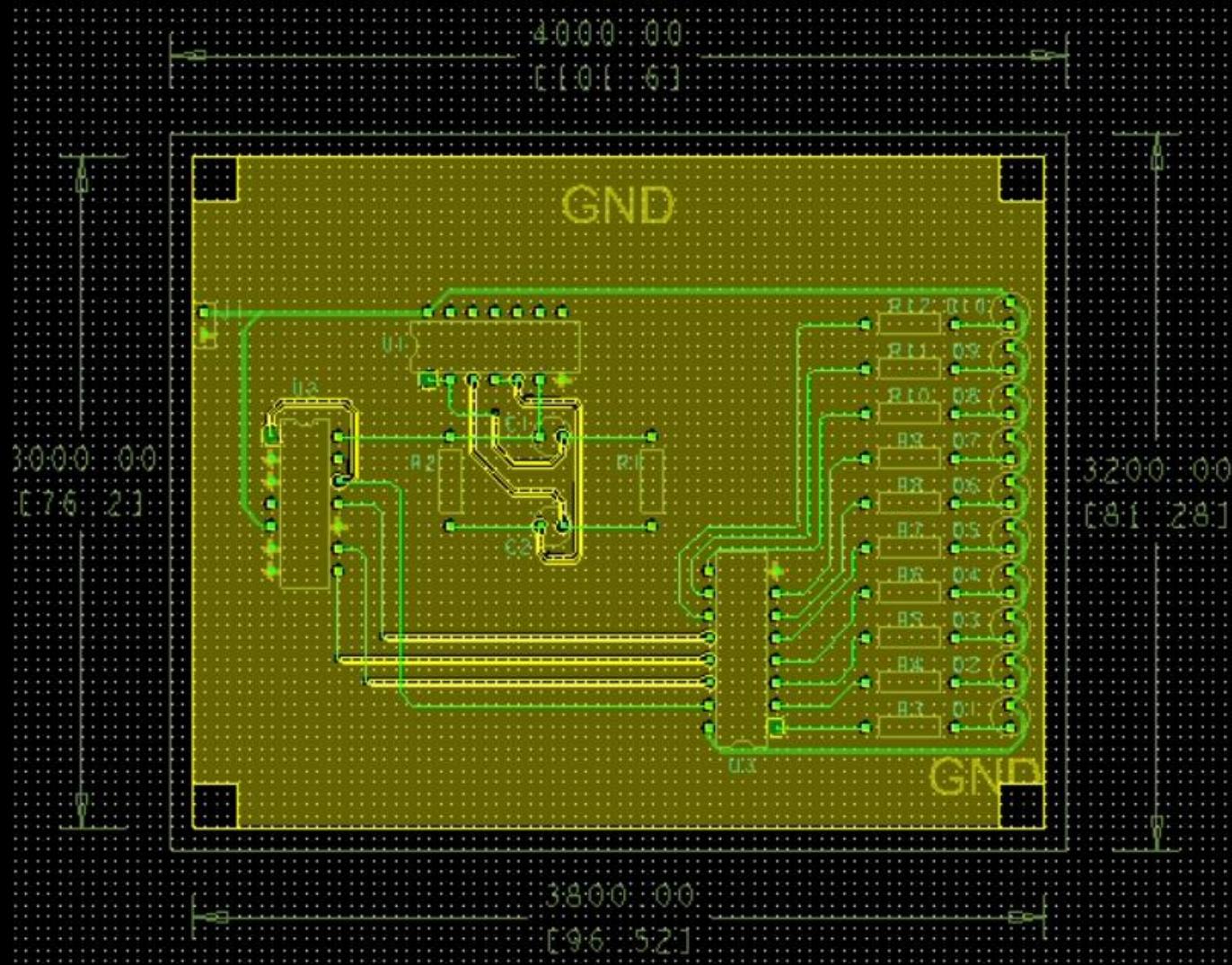
Dimensions



1. Setup > Design Parameter Mfg Applications > drafting
2. General > Parameter editing : millimeters
3. Text > text block 8 > primary : mils > secondary : millimeters

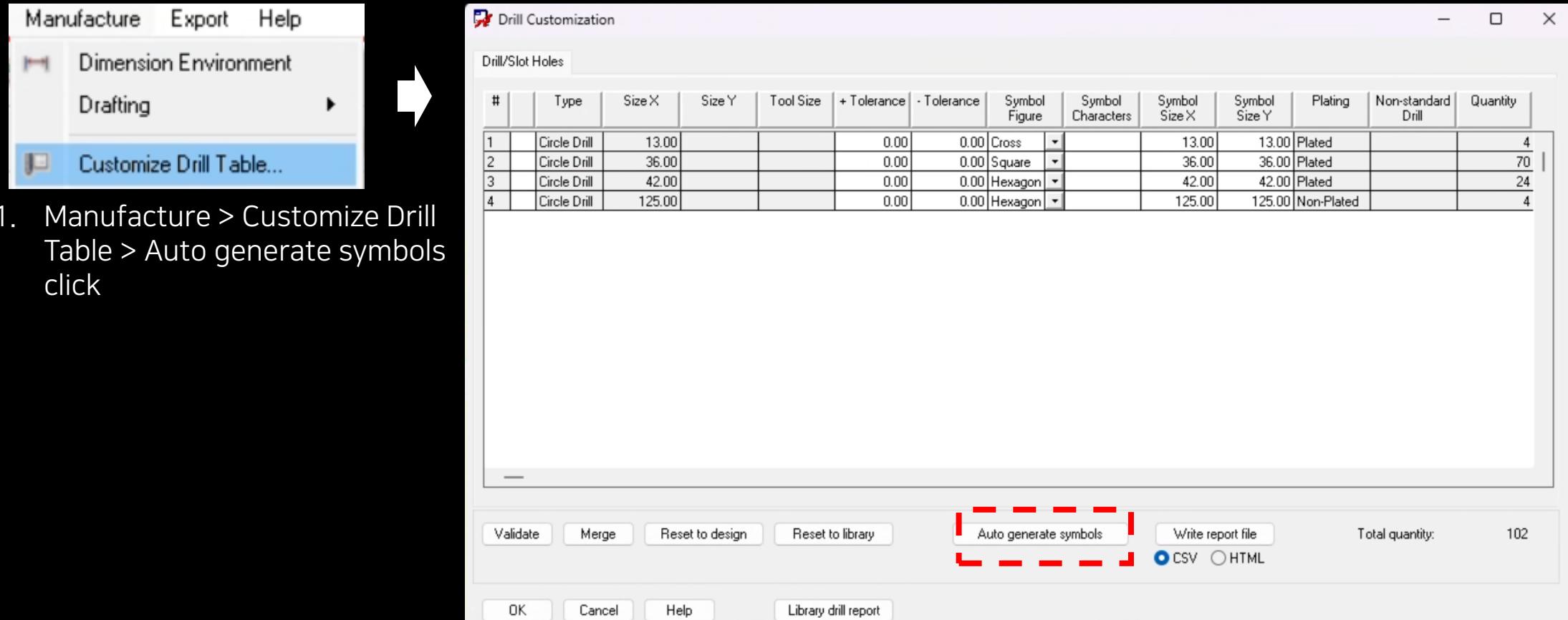
Procedure of PCB Design

Dimensions



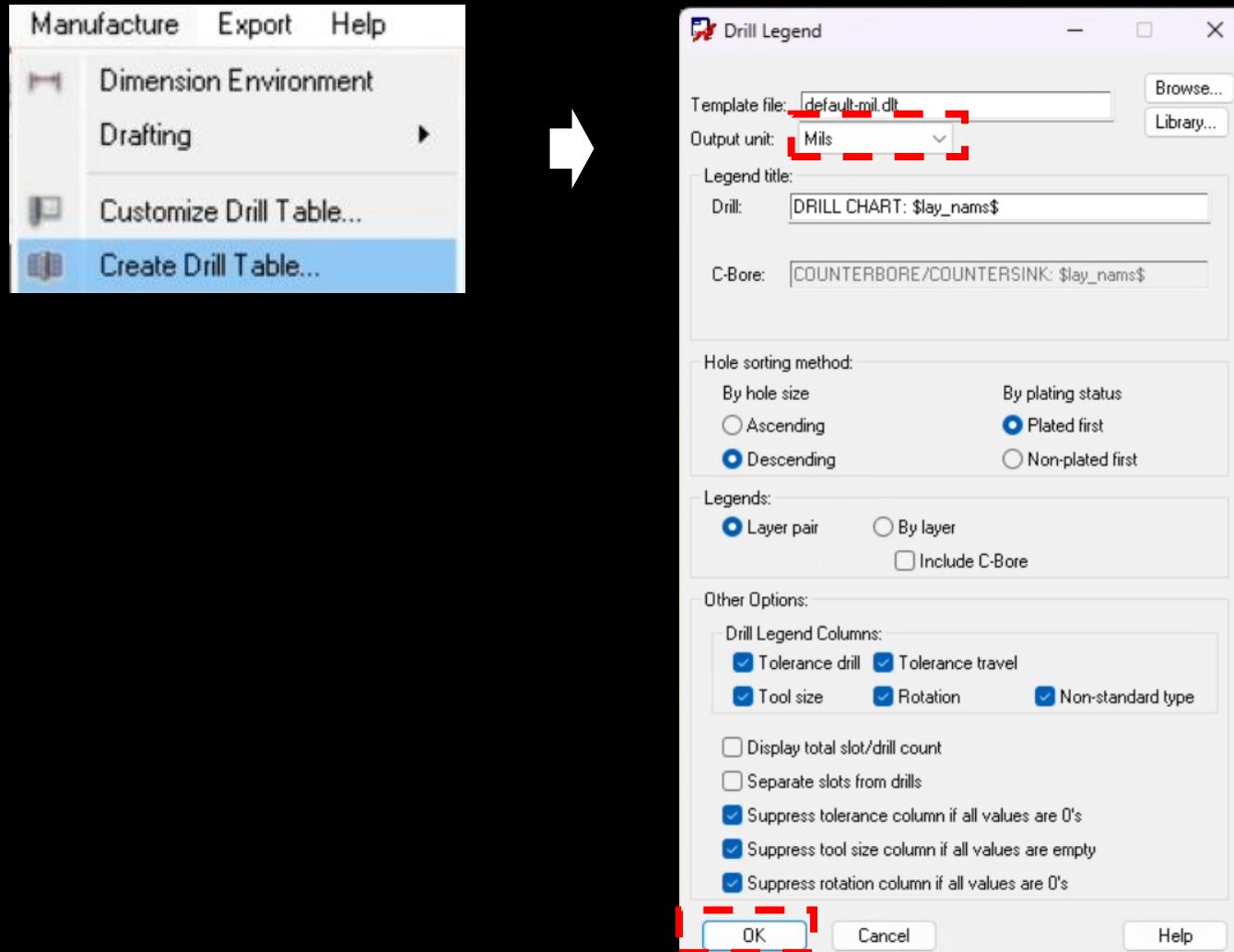
Procedure of PCB Design

Drill Legend

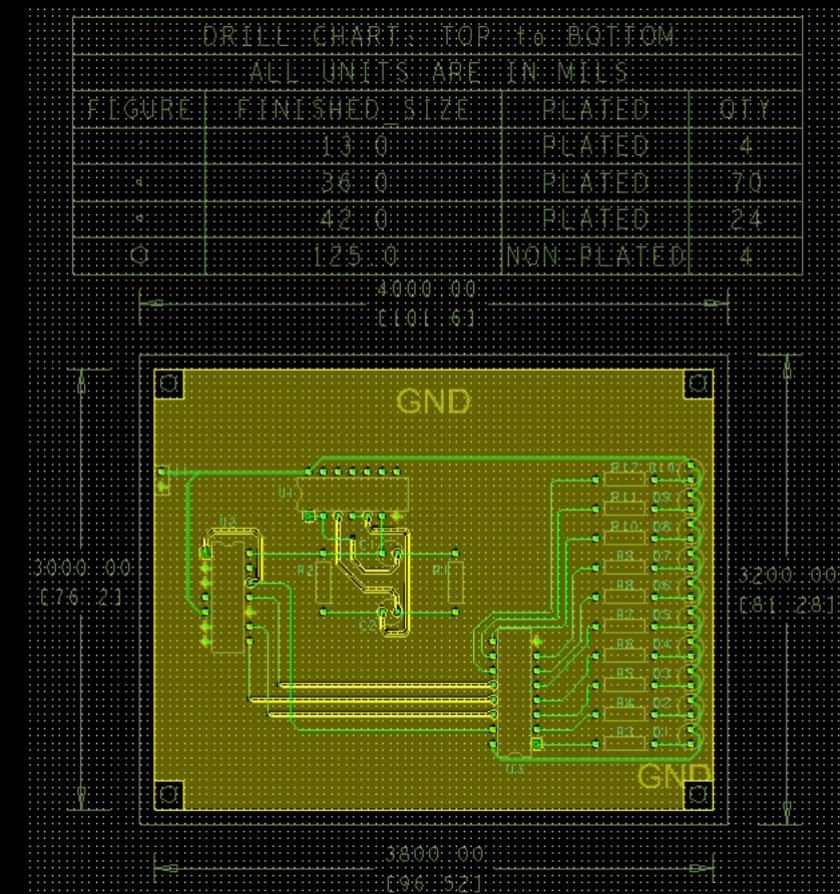


Procedure of PCB Design

Drill Legend

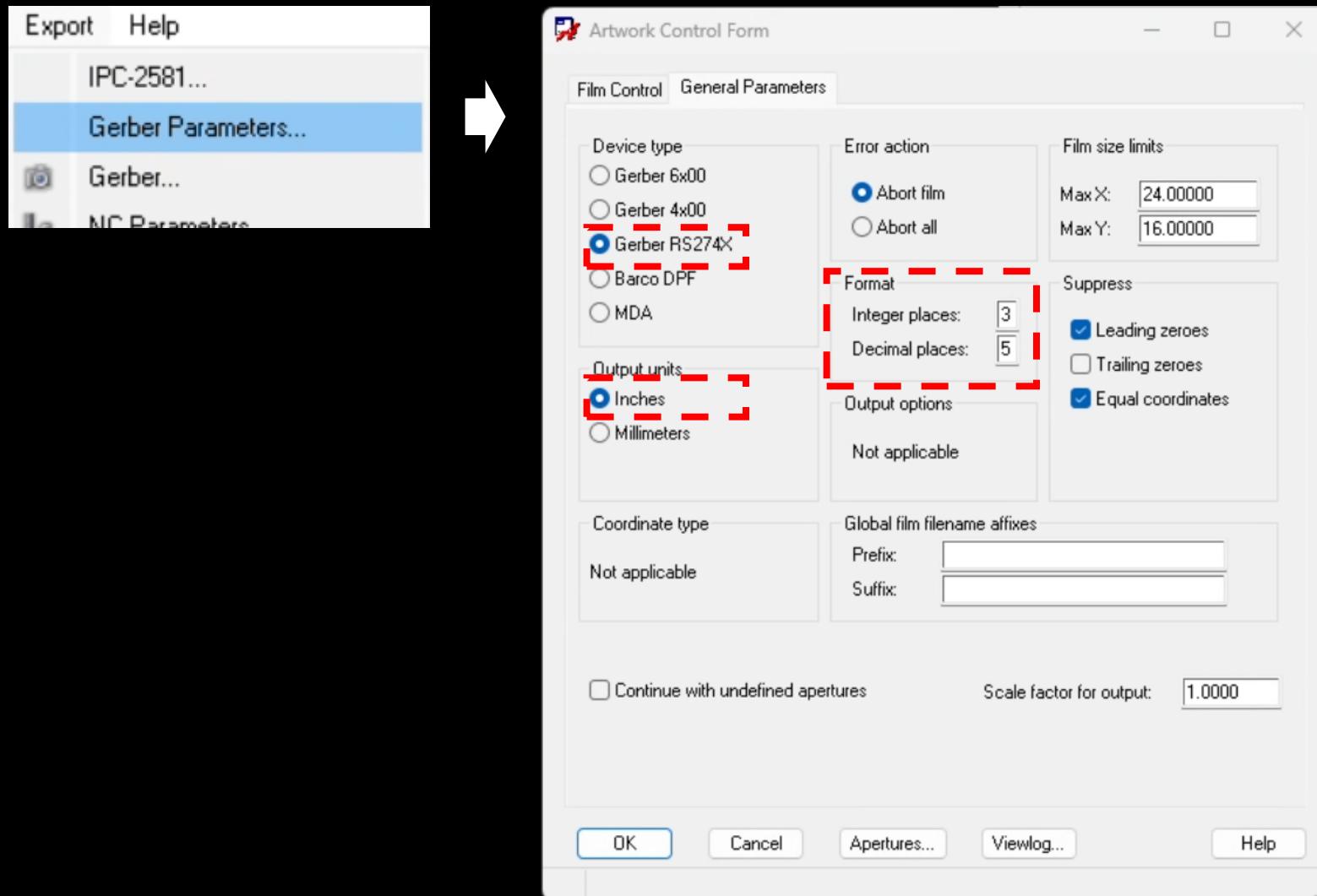


1. Manufacture > Create Drill Table > unit : mils



Procedure of PCB Design

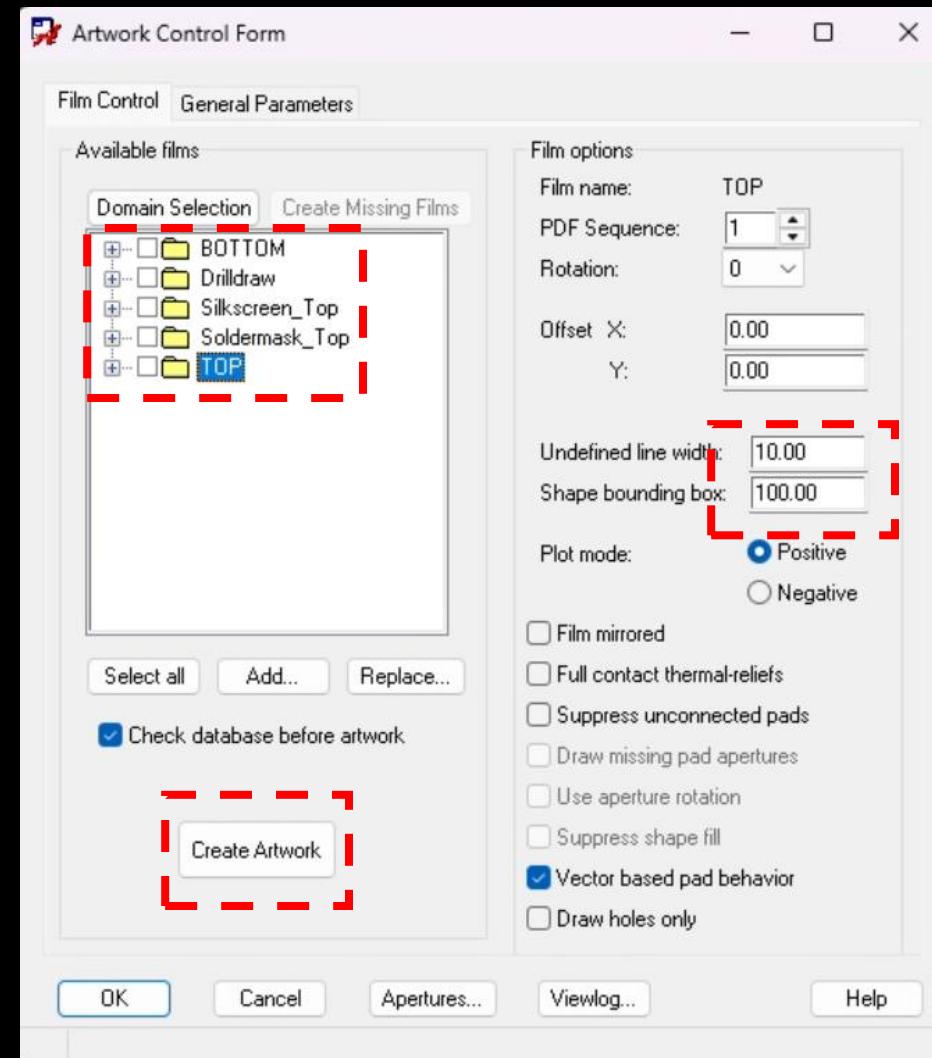
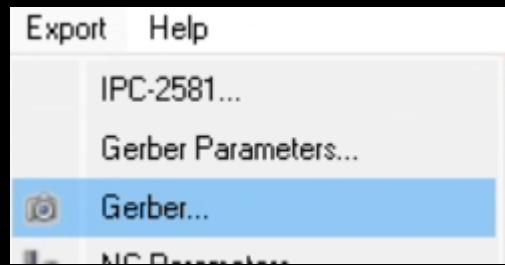
Create Gerber file



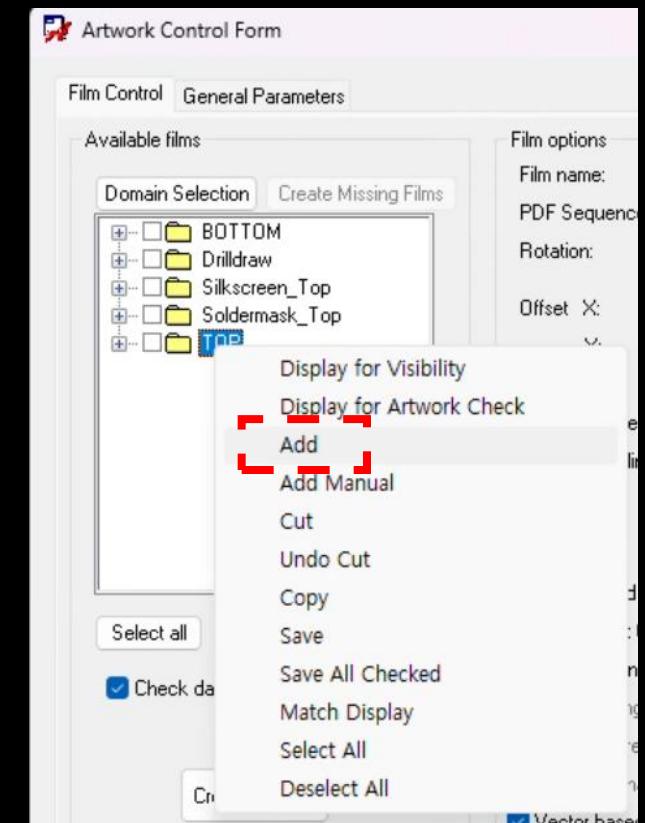
1. Export > Gerber Parameters > format integer places : 3 , decimal places : 5

Procedure of PCB Design

Create Gerber file

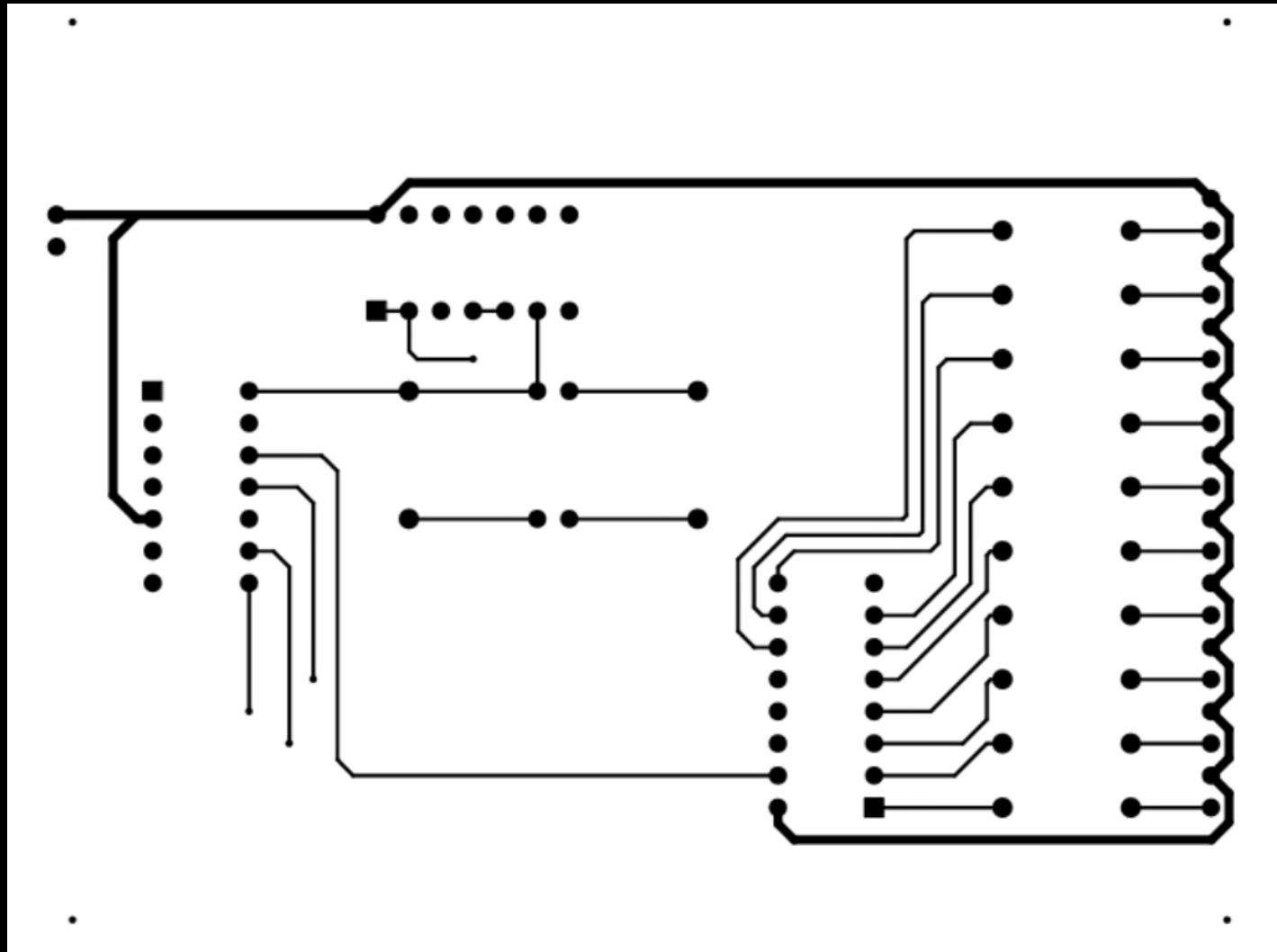


1. Export > Gerber > checking width and bounding box : 10, 100



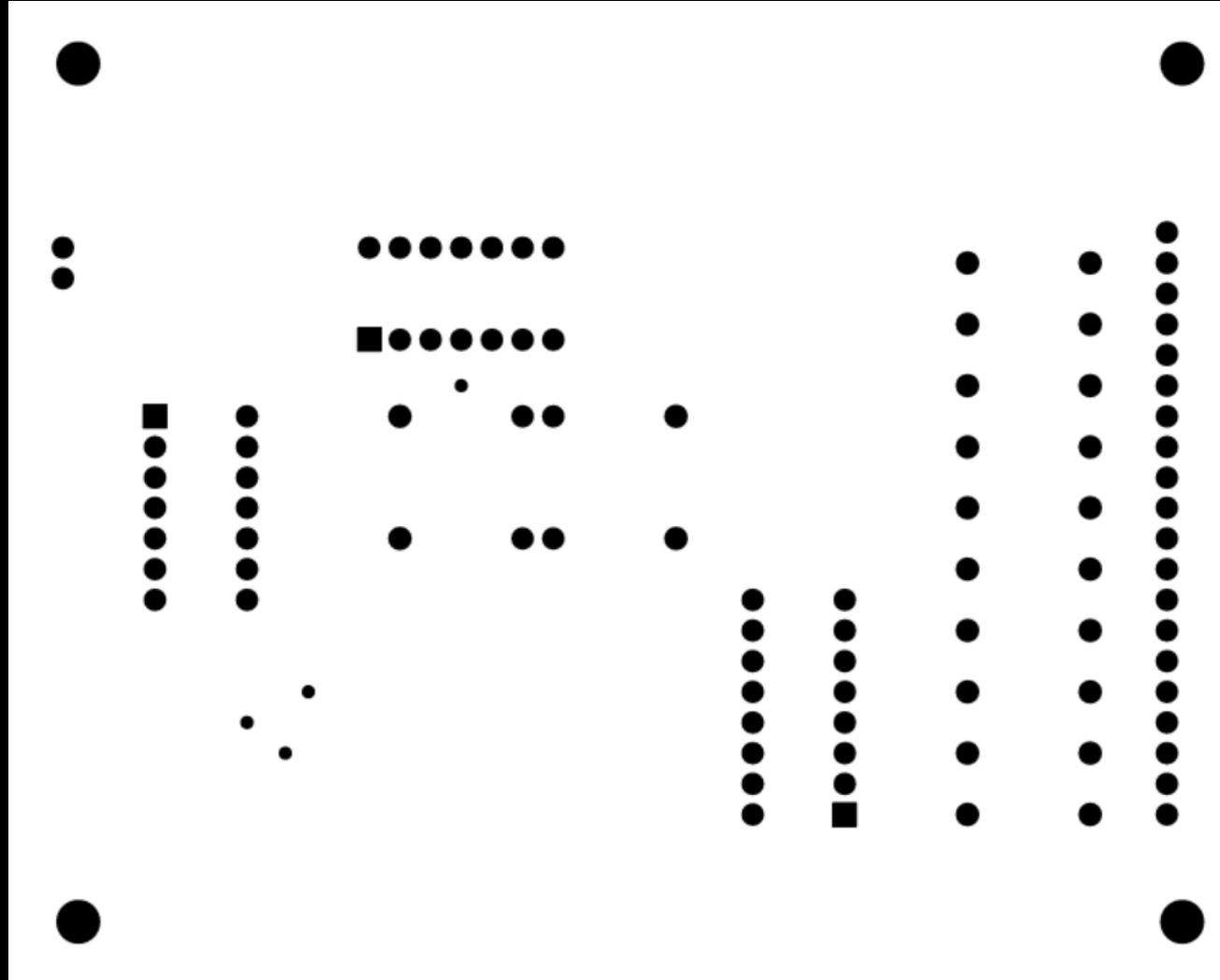
Procedure of PCB Design

Create Gerber file (TOP)



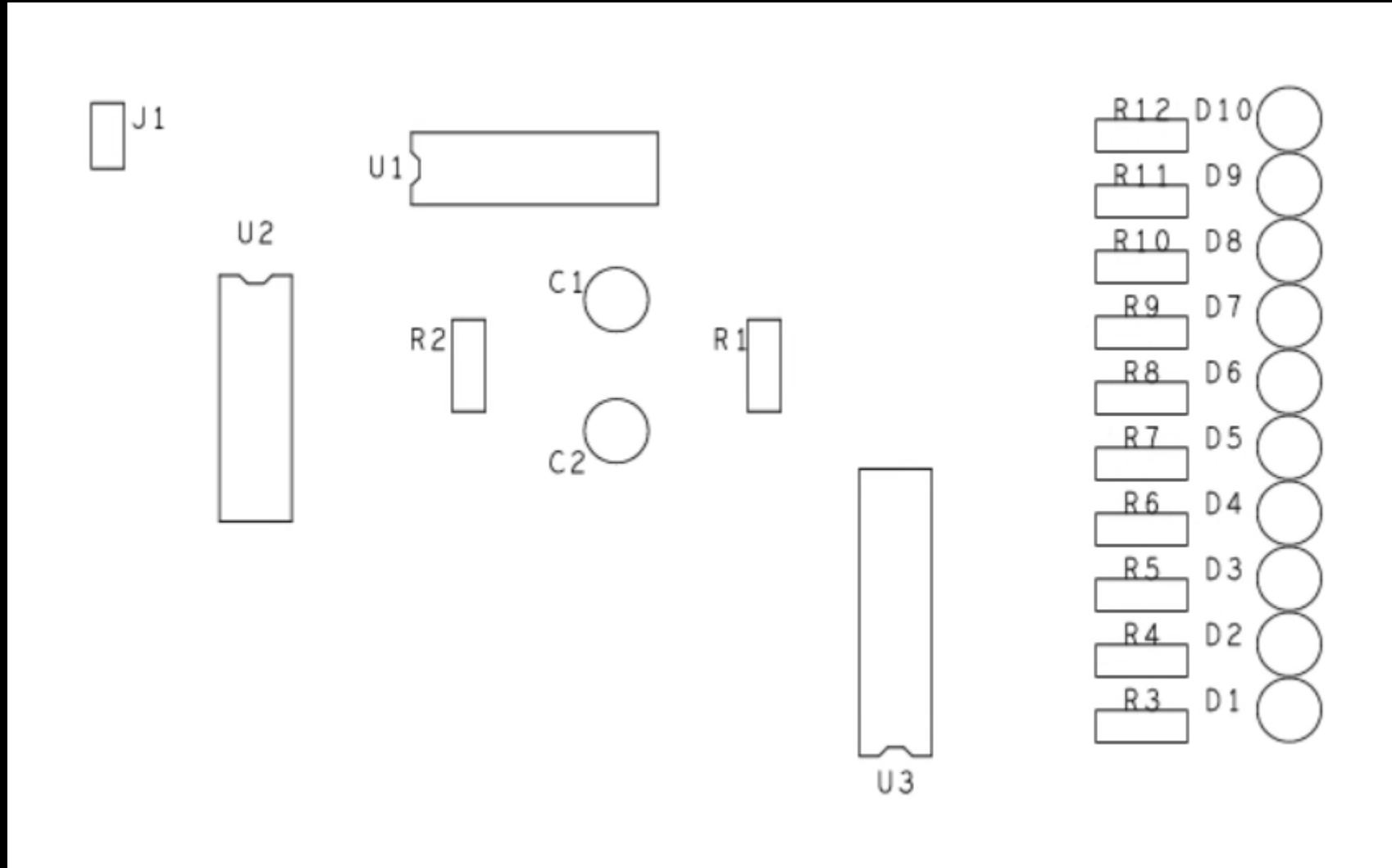
Procedure of PCB Design

Create Gerber file (Soldermask_Top)



Procedure of PCB Design

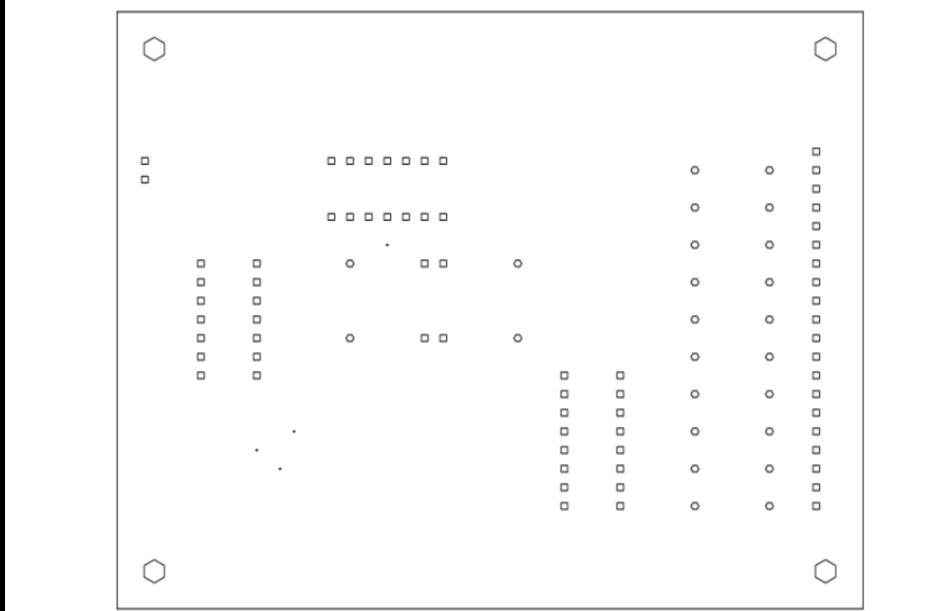
Create Gerber file (Silkscreen_Top)



Procedure of PCB Design

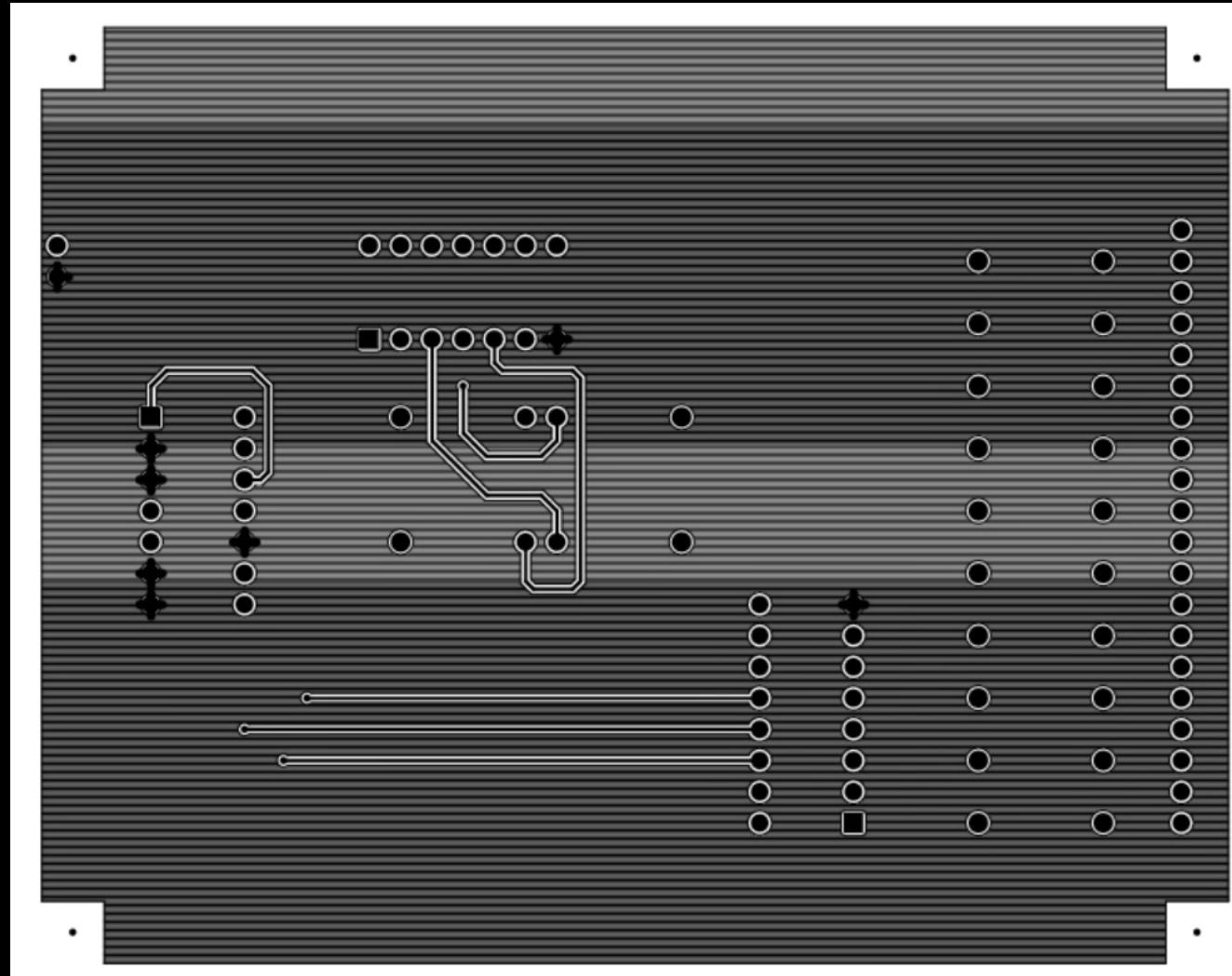
Create Gerber file (Drilldraw)

DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	FINISHED_SIZE	PLATED	QTY
.	13.0	PLATED	4
▫	36.0	PLATED	70
◦	42.0	PLATED	24
◊	125.0	NON-PLATED	4



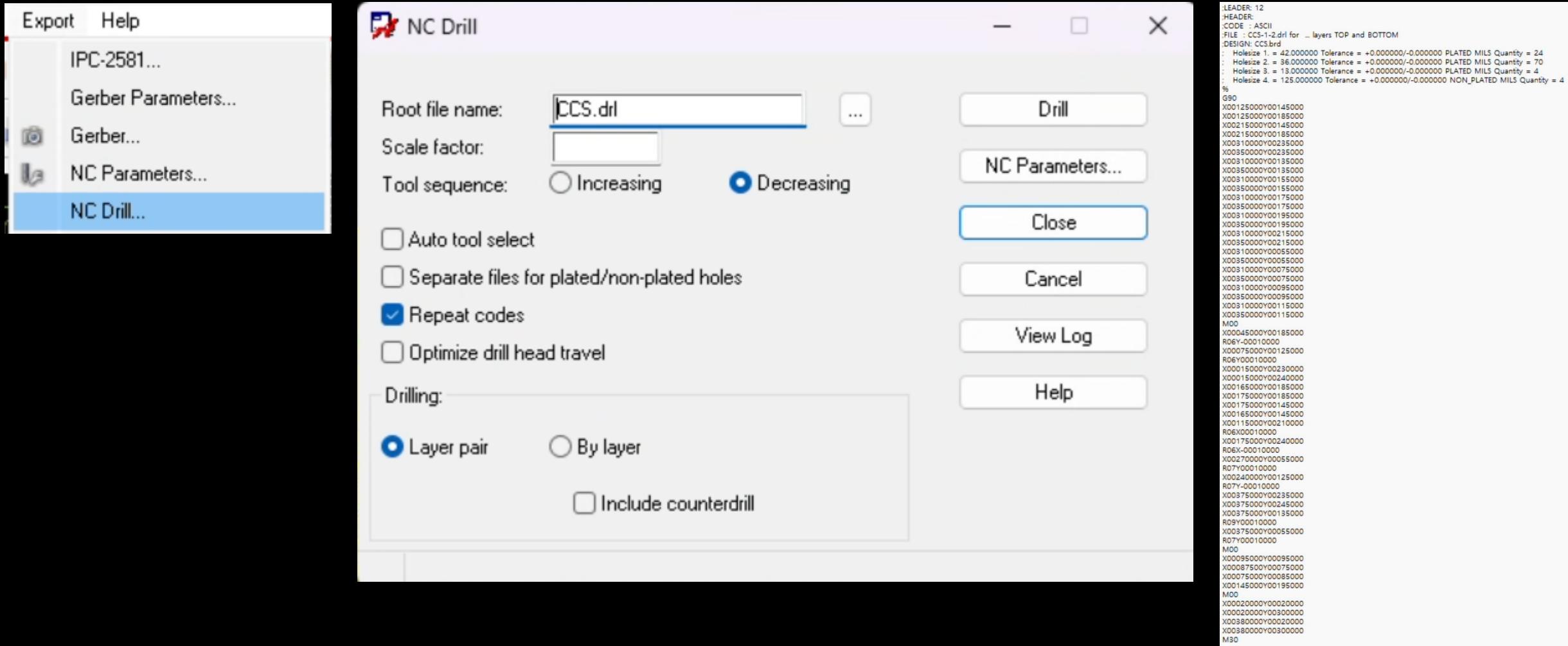
Procedure of PCB Design

Create Gerber file (BOTTOM)



Procedure of PCB Design

Create Gerber file (NC Drill)

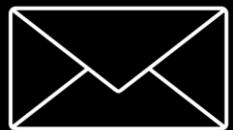


Procedure of PCB Design

Create Gerber file

 BOTTOM.art	2025-08-22 오후 4:55	ART 파일	8KB
 Drilldraw.art	2025-08-22 오후 4:55	ART 파일	4KB
 Silkscreen_Top.art	2025-08-22 오후 4:55	ART 파일	1KB
 Soldermask_Top.art	2025-08-22 오후 4:55	ART 파일	3KB
 TOP.art	2025-08-22 오후 4:55	ART 파일	6KB
 CCS-1-2.drl	2025-08-22 오후 4:56	DRL 파일	2KB
 BOTTOM.pdf	2025-08-22 오후 5:32	Microsoft Edge P...	22KB
 Drilldraw.pdf	2025-08-22 오후 5:33	Microsoft Edge P...	8KB
 Silkscreen_Top.pdf	2025-08-22 오후 5:33	Microsoft Edge P...	4KB
 Soldermask_Top.pdf	2025-08-22 오후 5:33	Microsoft Edge P...	2KB
 TOP.pdf	2025-08-22 오후 5:33	Microsoft Edge P...	4KB

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