

# FULL\_ADDDER

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# 순서

- Full\_Adder
- Circuit design
- Schematic
- Circuit simulation
- Layout
- DRC, LVS

# Full Adder

- 덧셈을 수행하는 연산 장치이자 디지털 회로
- 2개의 반가산기와 OR GATE로 구성

$$S = A \oplus B \oplus C_{in}, C_{out} = (A \cdot B) + C_{in}(A \oplus B)$$

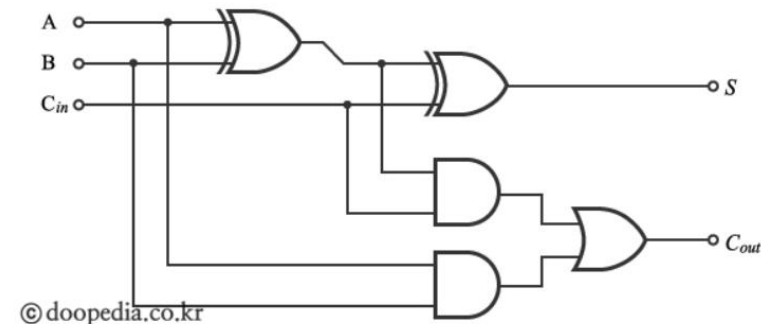
전가산기 진리표

입 력			출 력	
A	B	$C_{in}$	합 S	자리 올림 $C_{out}$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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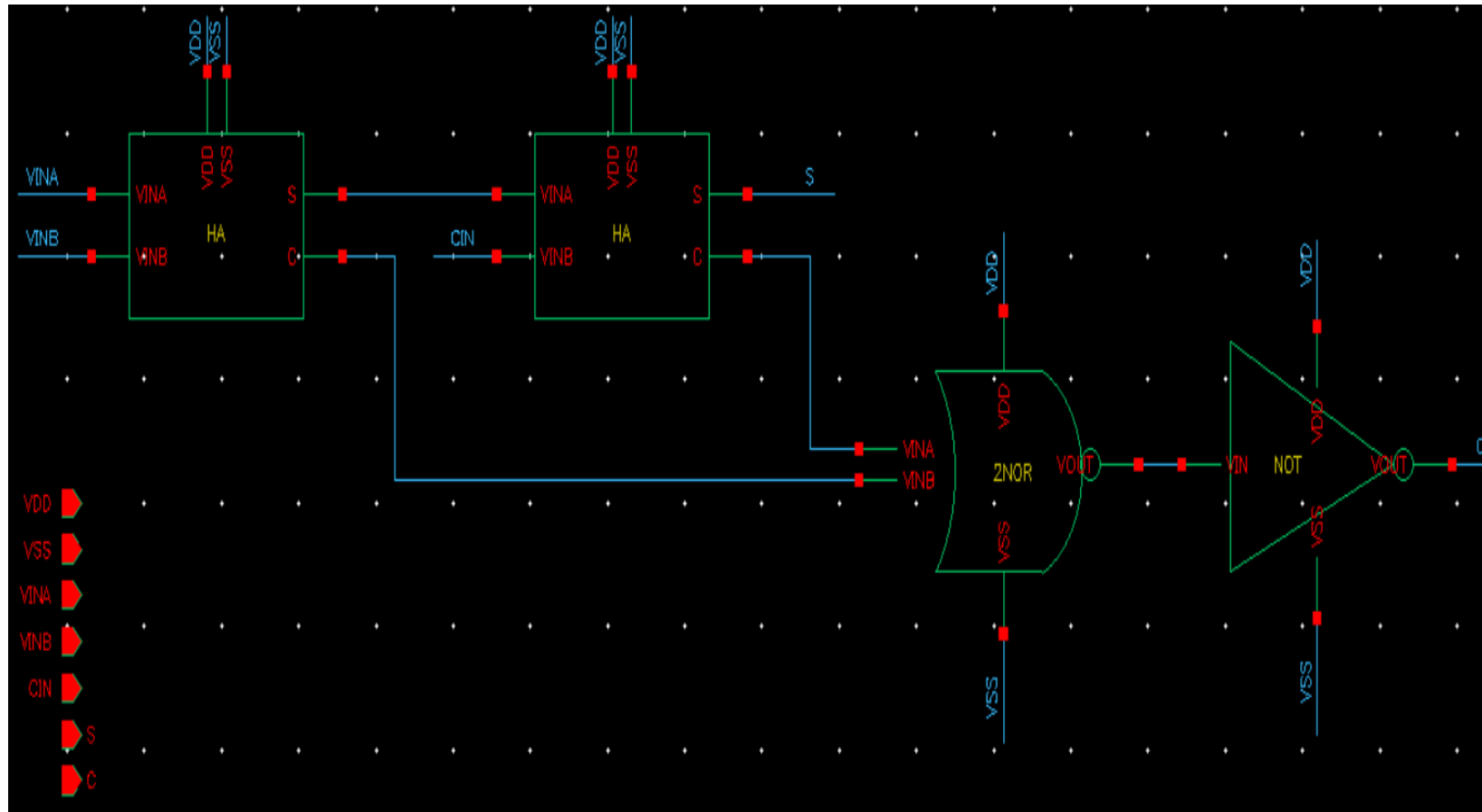


전가산기 논리 회로

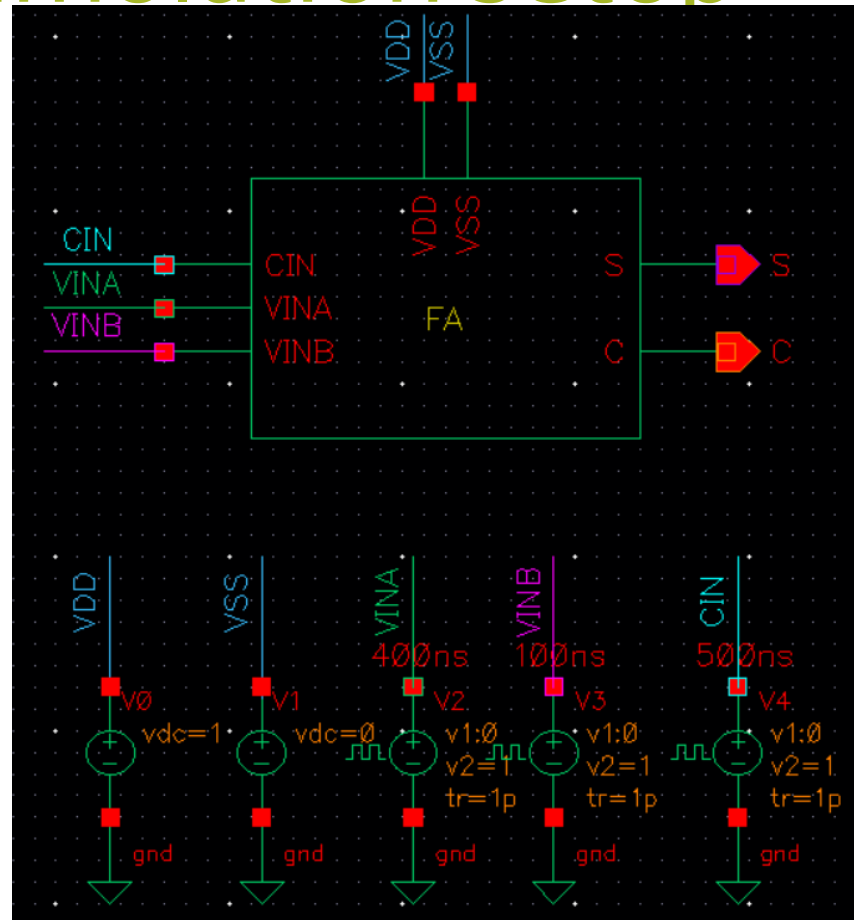


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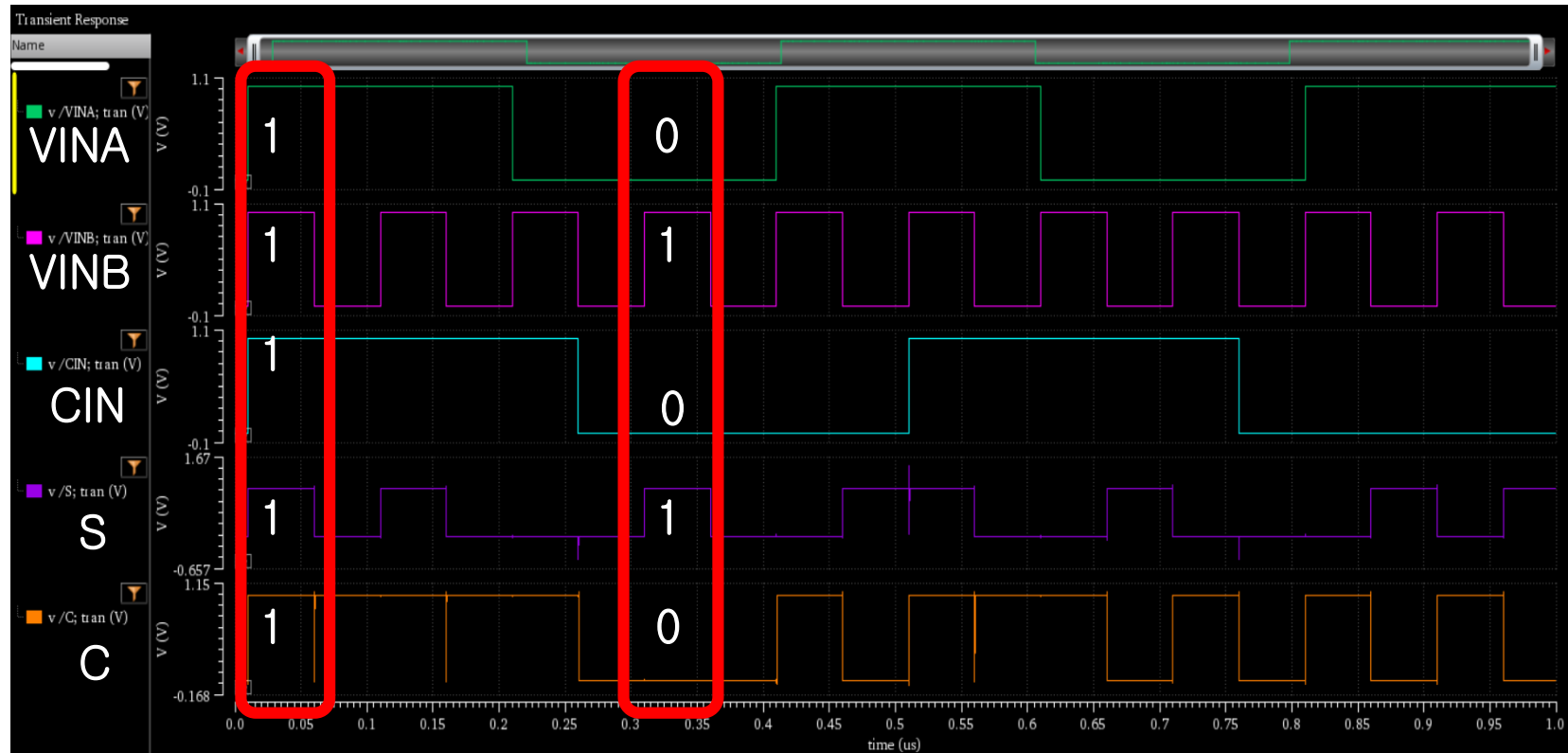
# Schematic(Logic gate)



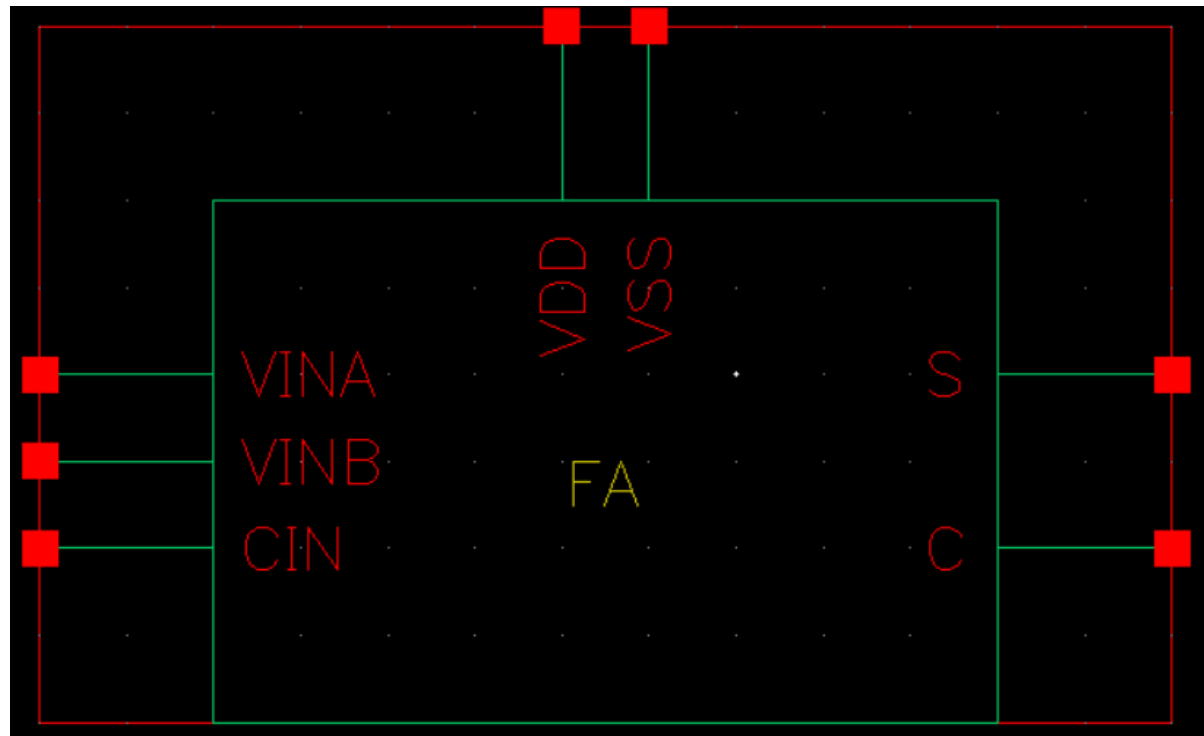
# Full Adder simulation setup



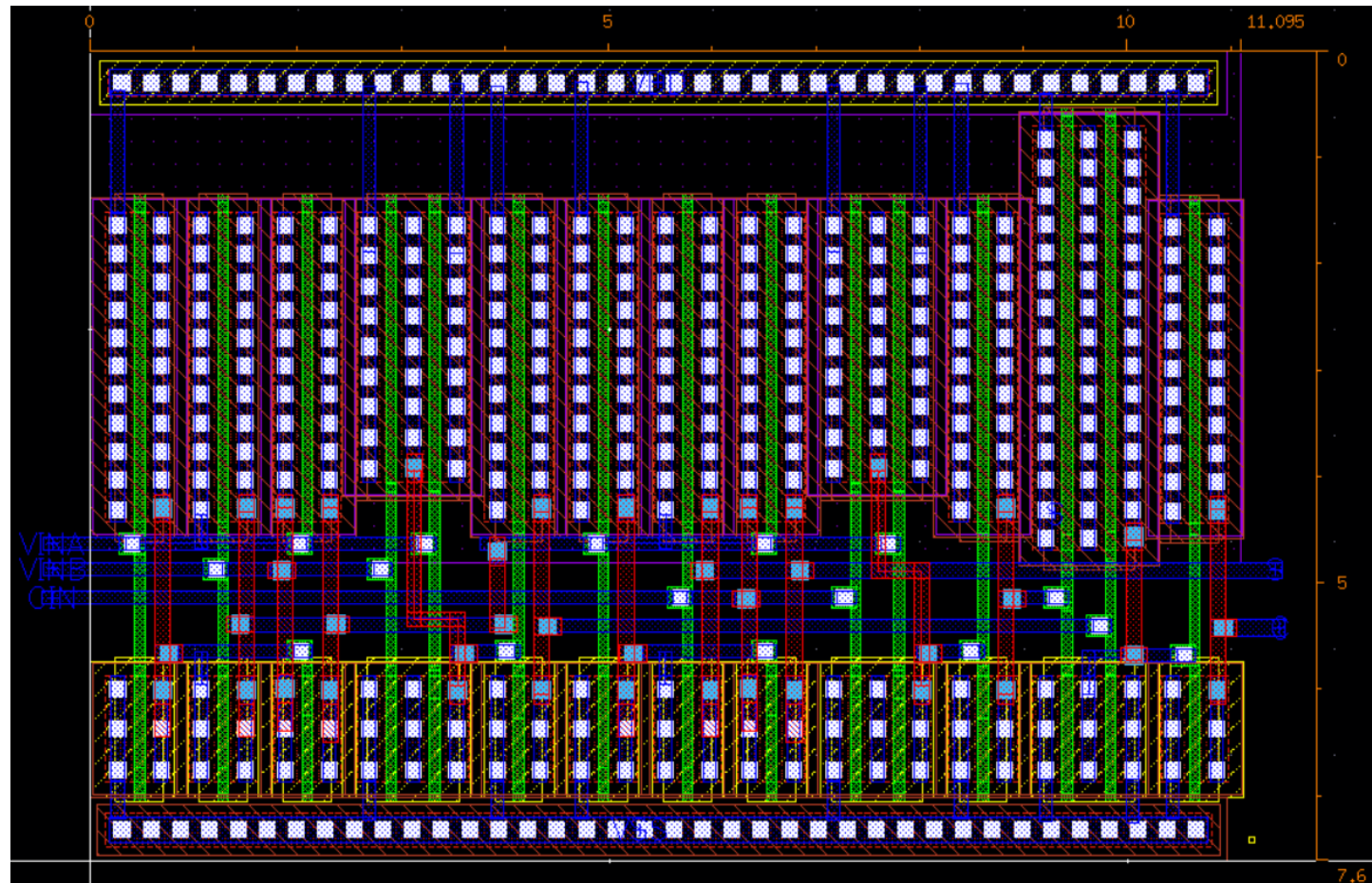
# Wave Form



# Full Adder 블록 외부 PORT



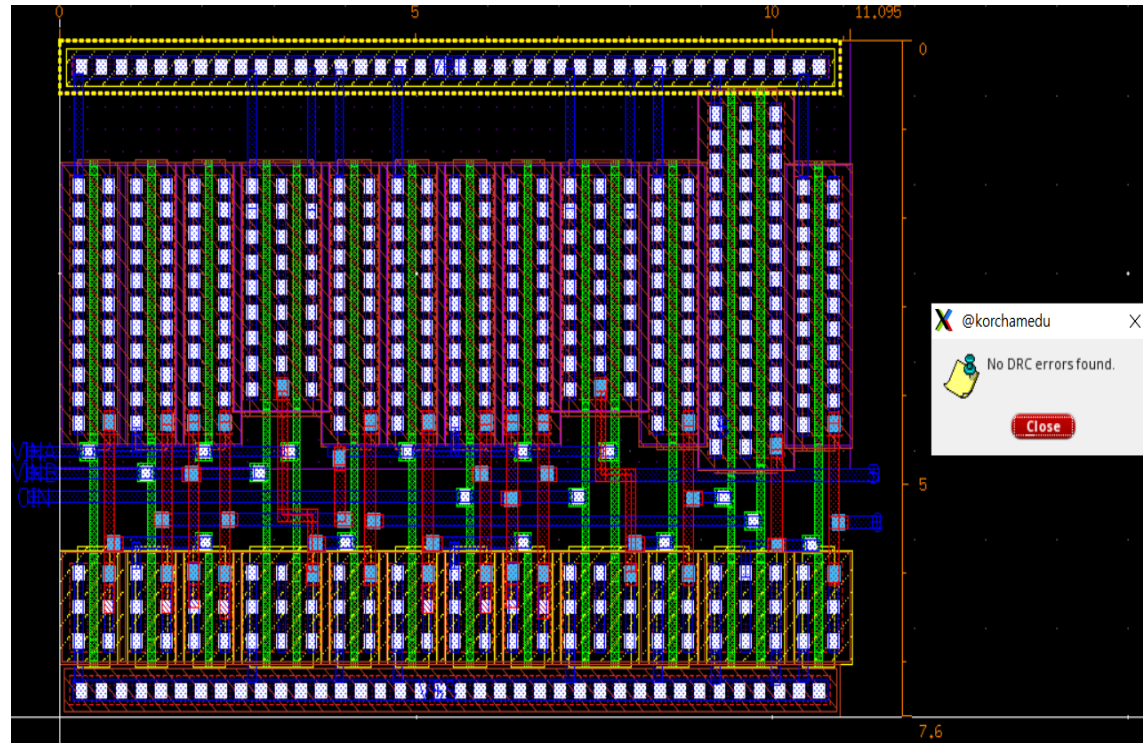
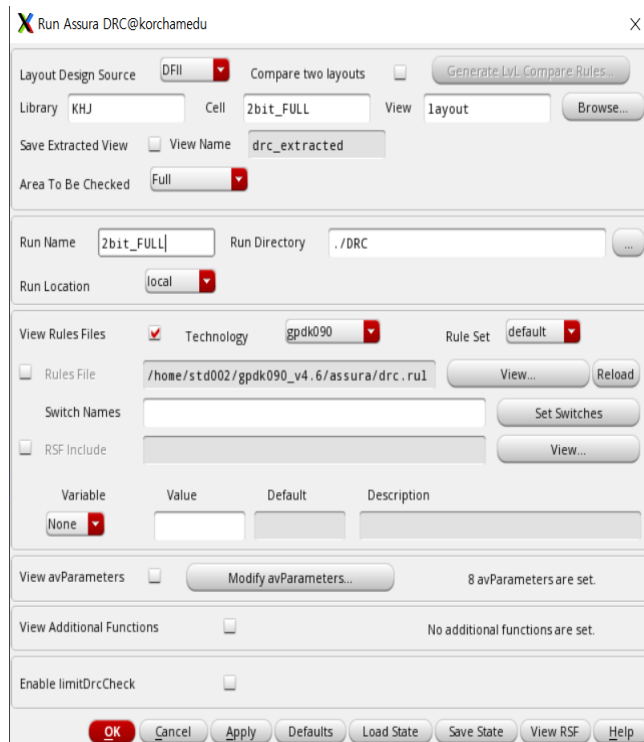
# Full Adder (Layout)



$$\text{Area : } 11.095 \times 7.6 = 84.322 \mu m^2$$



# Full Adder (DRC)



# Full Adder (LVS)

The image displays two windows from the Cadence LVS tool. The top window, titled "LVS Debug - 2bit\_FULL@korchamedu", shows the "Cell List (sch || lay)" tab with the text "\*\*\* Schematic and Layout Match". It includes buttons for "Open Schematic Cell...", "Open Layout Cell...", and "Open Tool...". The bottom window, titled "Run: 2bit\_FULL@korchamedu", shows the "Run" dialog with the following configuration:

- Schematic Design Source: DFI (selected), Use Existing Netlist (checked), Netlisting Options... (button)
- Library: KHJ, Cell: 2bit\_FULL, View: schematic (button)
- Layout Design Source: DFI (selected), Use Existing Extracted Netlist (checked)
- Library: KHJ, Cell: 2bit\_FULL, View: layout (button)
- Run Name: 2bit\_FULL, Run Directory: ./LVS
- Run Location: local (selected)
- View Rules Files: ☒ Technology: undefined- (selected), Rule Set: default (selected)
- Extract Rules: ./assura/extract.rul (button: View..., Edit..., Reload)
- Compare Rules: (button: View..., Edit...)
- Switch Names: (button: Set Switches)
- Binding File(s): (button: View..., Edit...)
- RSF Include: (button: View..., Edit...)
- Variable: None (selected), Value: (empty), Default: (empty), Description: (empty)
- View avParameters: ☐ (button: Modify avParameters...), 1 avParameter is set.
- View avCompareRules: ☐ (button: Modify avCompareRules...), No avCompare rules are set.
- View Additional Functions: ☐ (button: Modify avAdditionalFunctions...), No additional functions are set.
- Buttons: OK, Cancel, Apply, Defaults, Load State, Save State, View RSF, Help

The bottom window also displays a summary of LVS issues and extraction information:

Do you want to close current project and view the results of new run?

Summary of LVS Issues

Extraction Information:

- 0 cells have 0 mal-formed device problems
- 0 cells have 0 label short problems
- 0 cells have 0 label open problems

Comparison Information:

- 0 cells have 0 Net mismatches
- 0 cells have 0 Device mismatches
- 0 cells have 0 Pin mismatches
- 0 cells have 0 Parameter mismatches

ELW Information:

- Total DRC violations: 0

Buttons: Yes, No, Help