FULL_ADDER

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순서

- Full_Adder
- Circuit design
- Schematic
- Circuit simulation
- Layout
- DRC, LVS

Full Adder

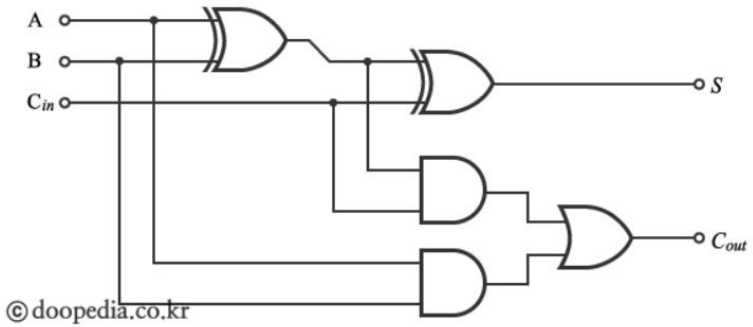
- 덧셈을 수행하는 연산 장치이자 디지털 회로
- 2개의 반가산기와 OR GATE로 구성

$$S = A \oplus B \oplus C_{in},\ C_{out} = (A \cdot B) + C_{in}(A \oplus B)$$

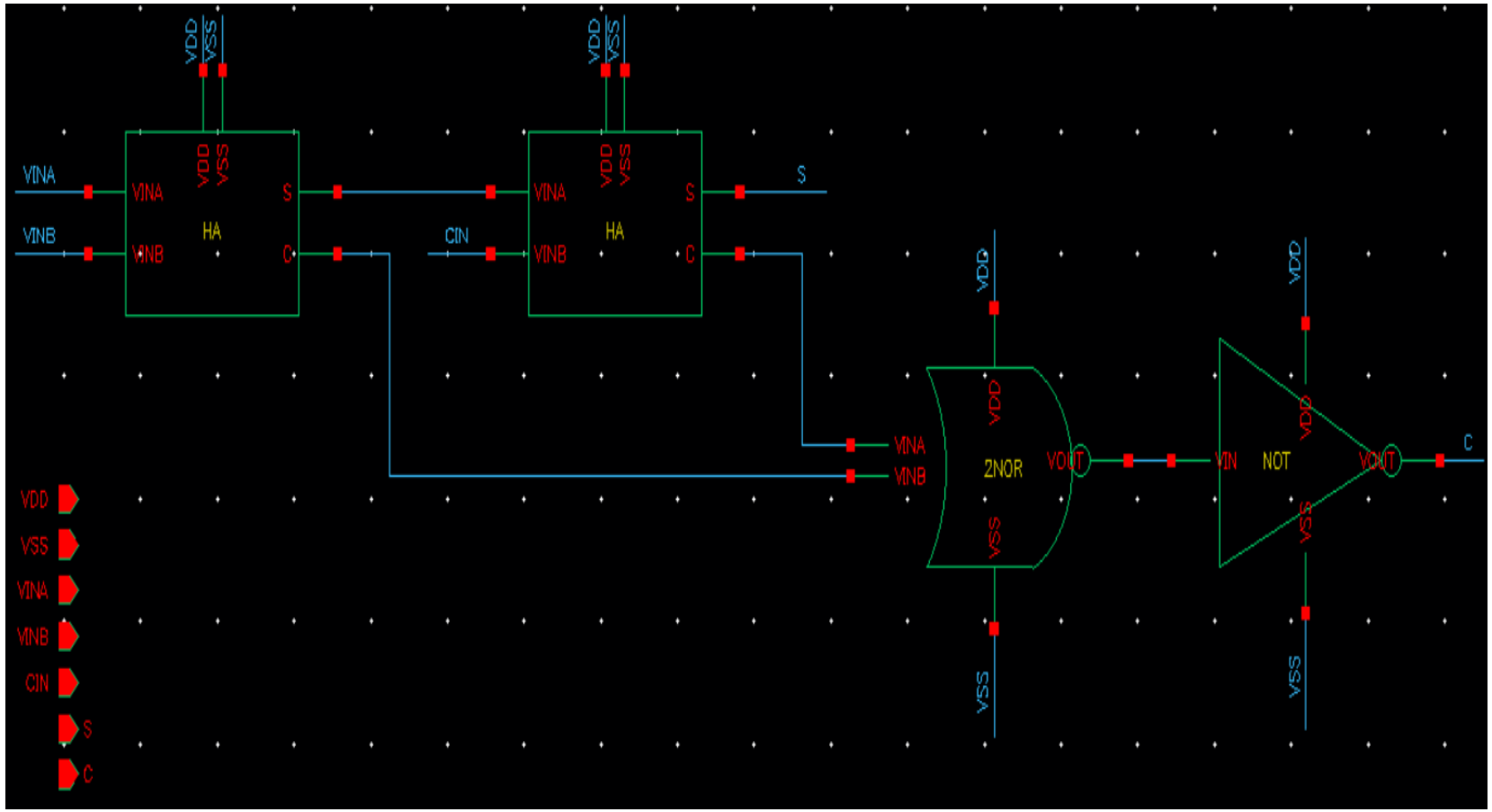
전가산기 진리표

입 력			출 력	
A	B	C_{in}	합 S	자리 올림 C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

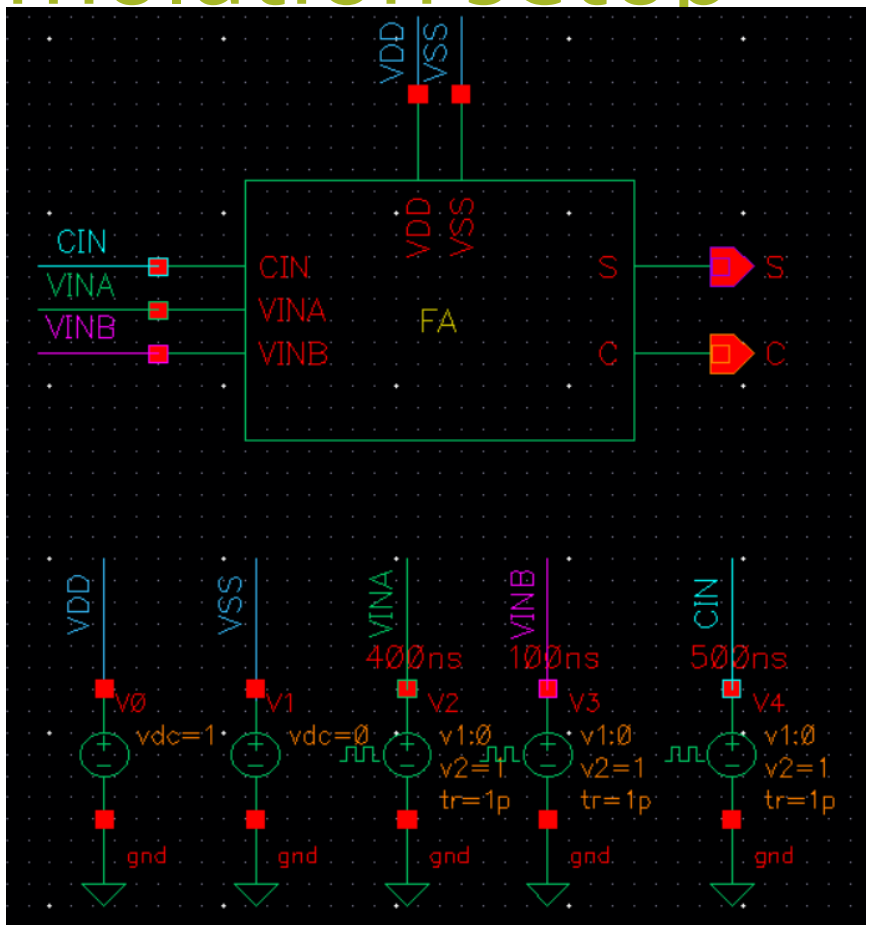
전가산기 논리 회로



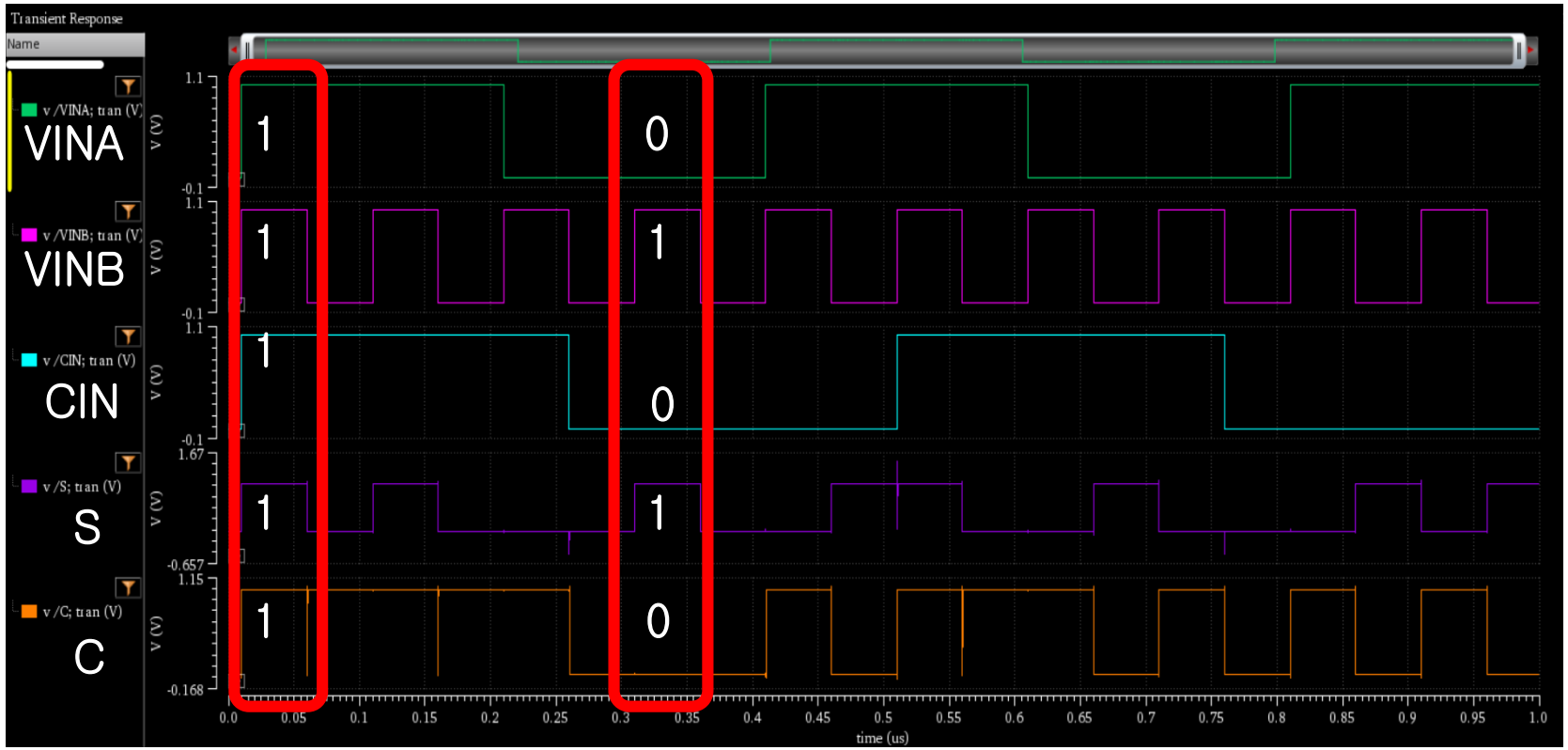
Schematic(Logic gate)



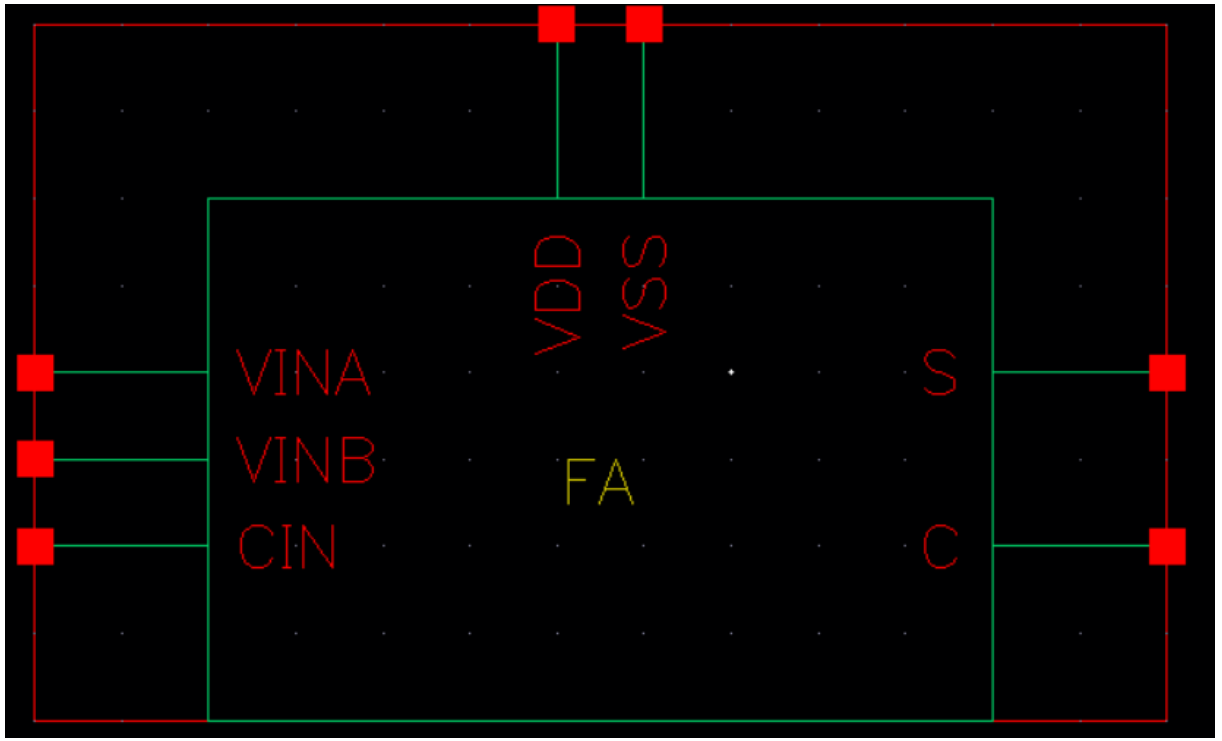
Full Adder simulation setup



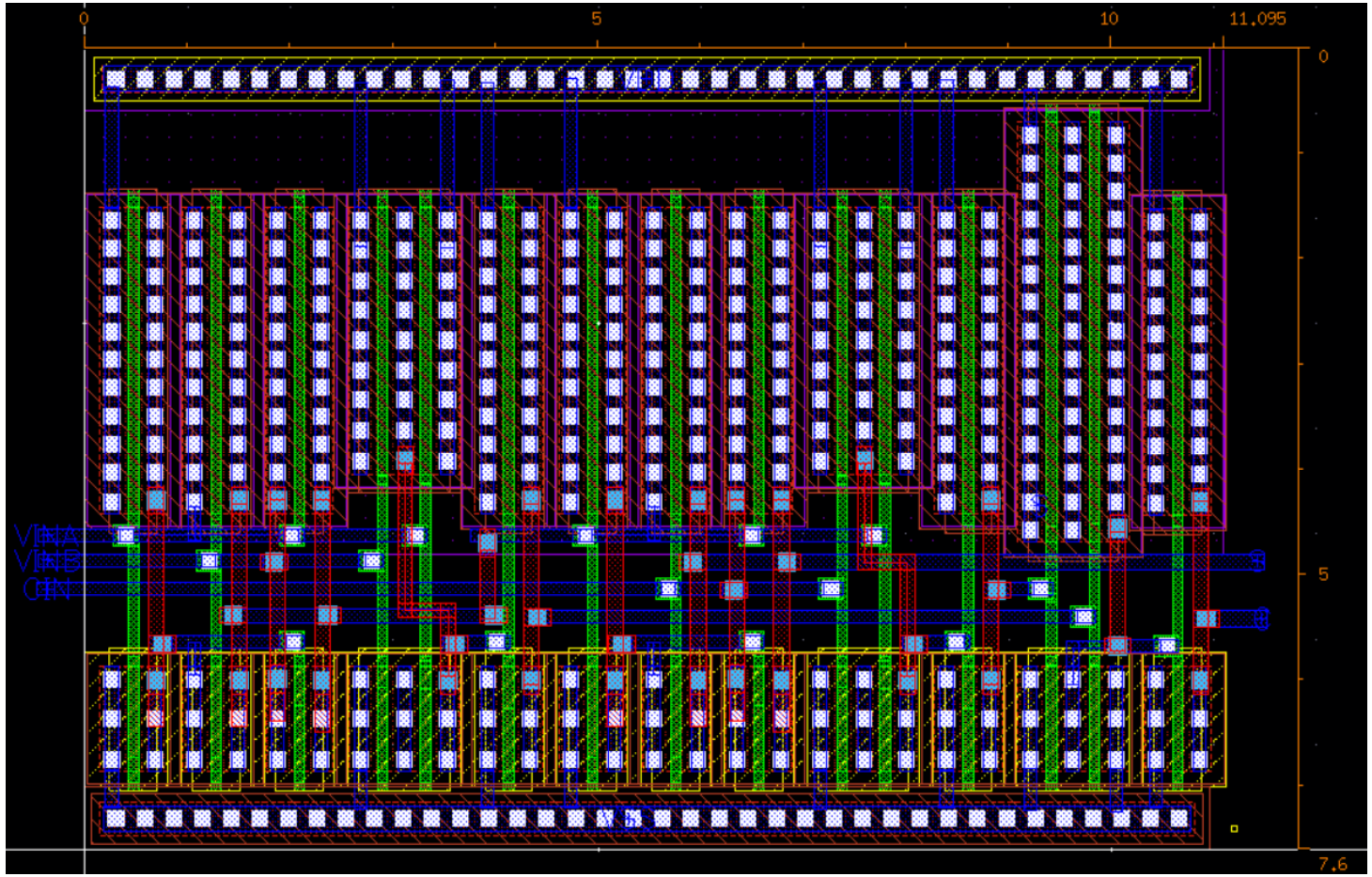
Wave Form


Transient Response
Name
v /VINA; tran (V)
VINA
v /VINB; tran (V)
VINB
v /CIN; tran (V)
CIN
v /S; tran (V)
S
v /C; tran (V)
C
1
0
1
1
1
0
1
1
1
0
time (us)

Full Adder 블록 외부 PORT

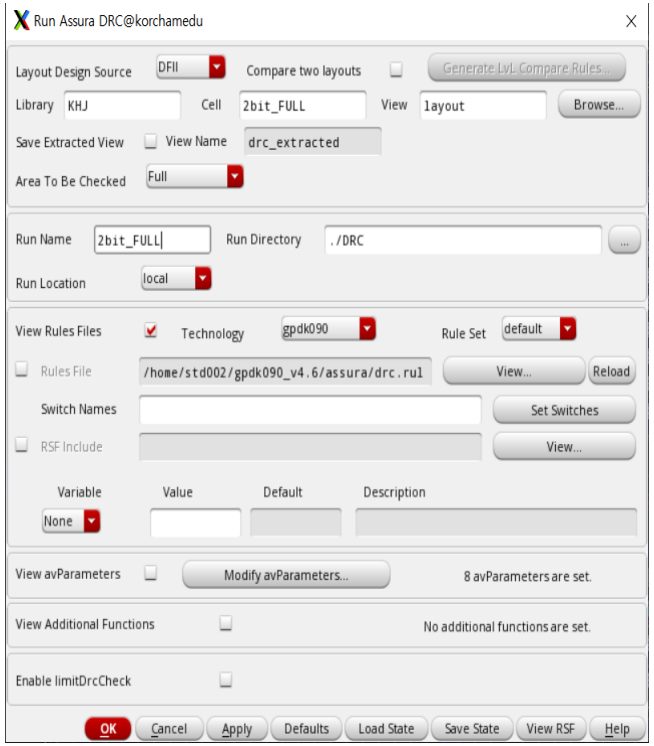


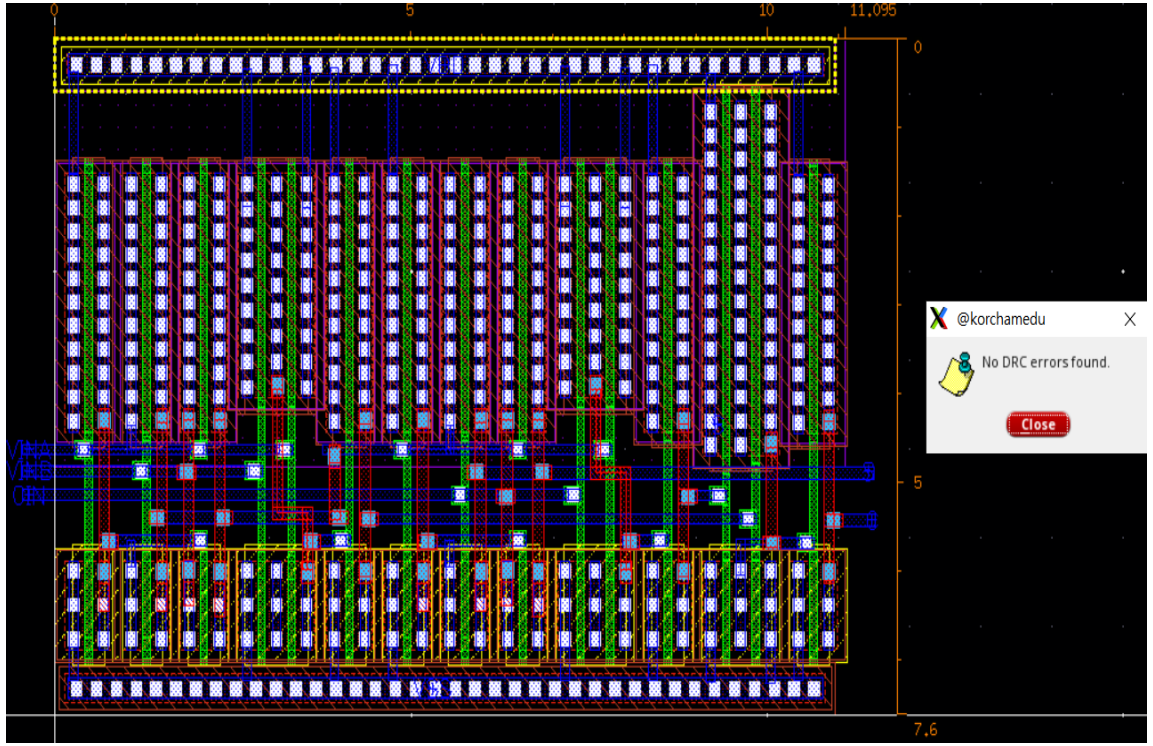
Full Adder (Layout)



Area : 11.095 X 7.6 = 84.322μm^2

Full Adder (DRC)





Full Adder (LVS)