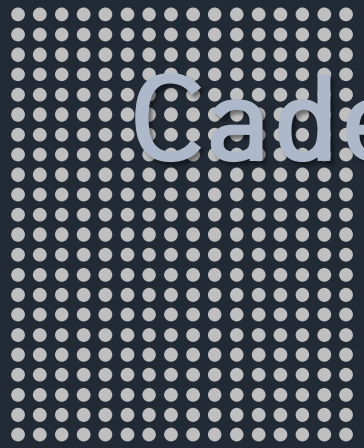

Cadence Full Custom IC

One Chip Design

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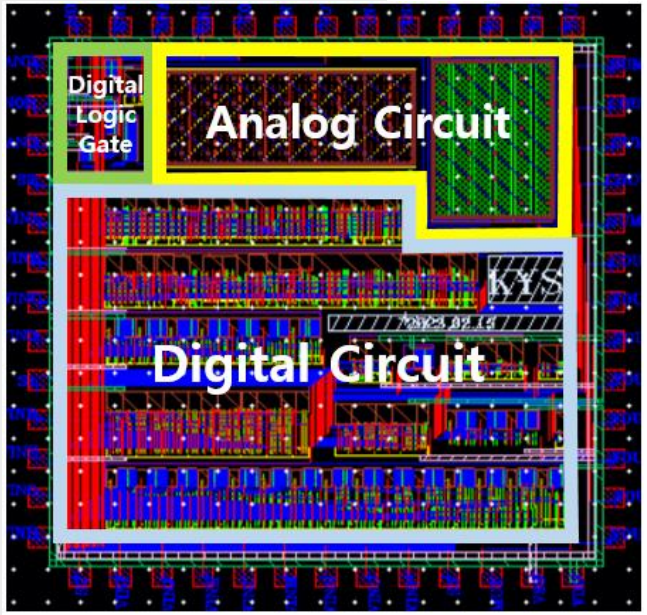
010 2026 3457

INDEX



PROGRAM & TOOLS

- Cadence Virtuoso Schematic Editor / Layout Editor
- Cadence Virtuoso Spectre / ADE
- Assura(DRC & LVS)
- GPDK090

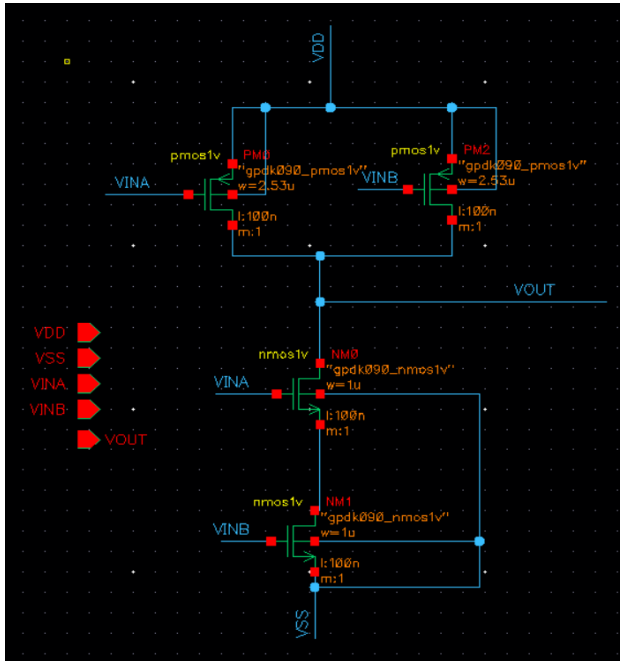
DIGITAL CIRCUITS

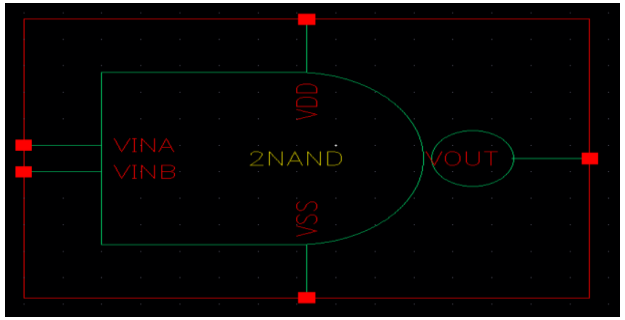
Digital Logic Gates

- NOT / SWITCH / XOR
- 2NAND / 3NAND / 4NAND
- 2NOR / 3NOR / 4NOR

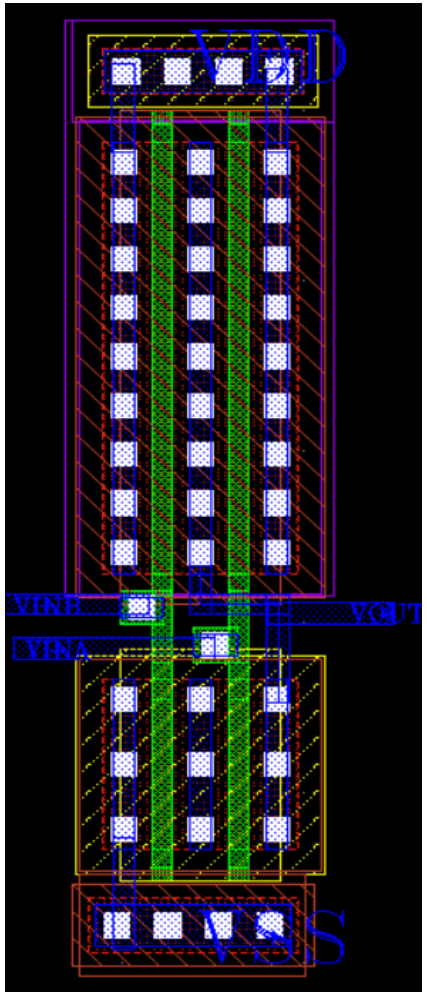
Digital Logic Gate – 2NAND

Schematic & Symbol

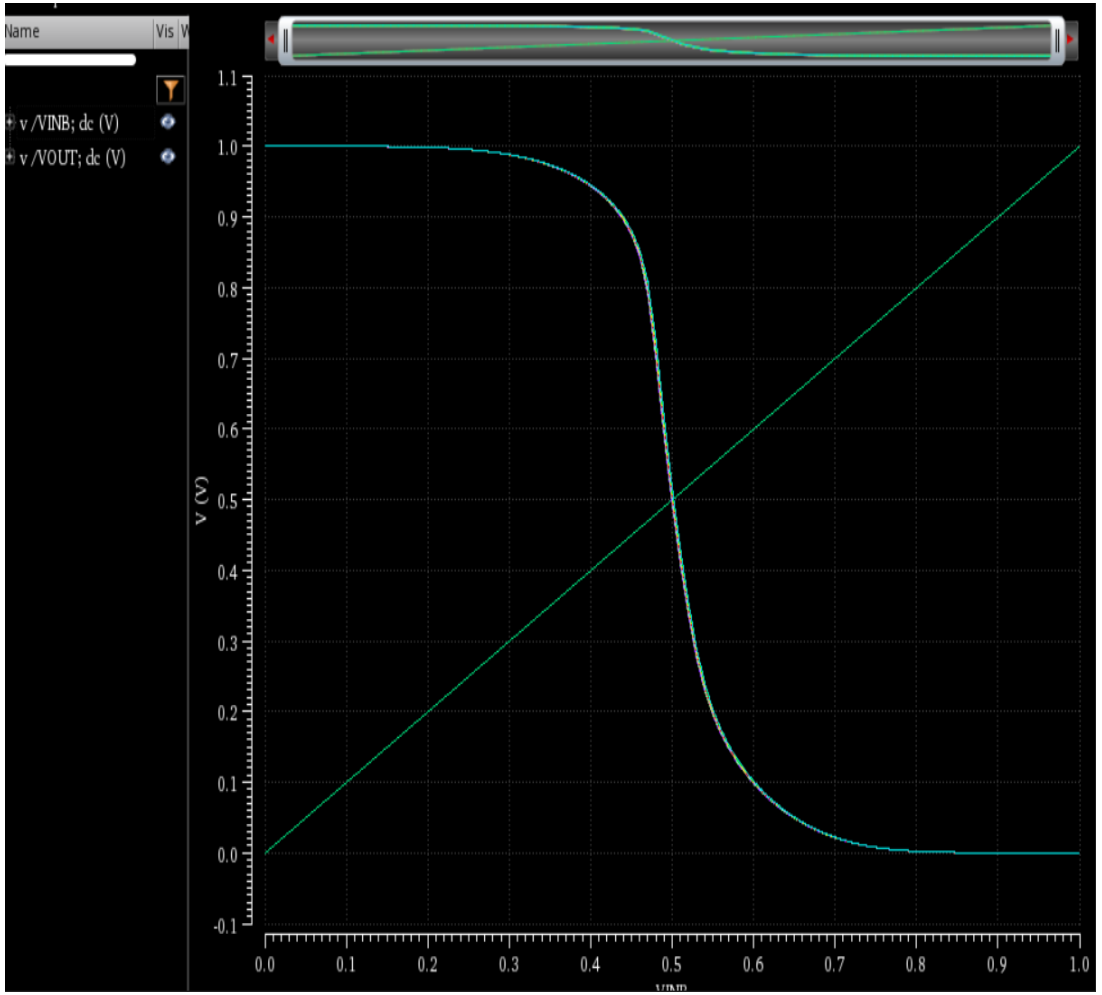




Layout

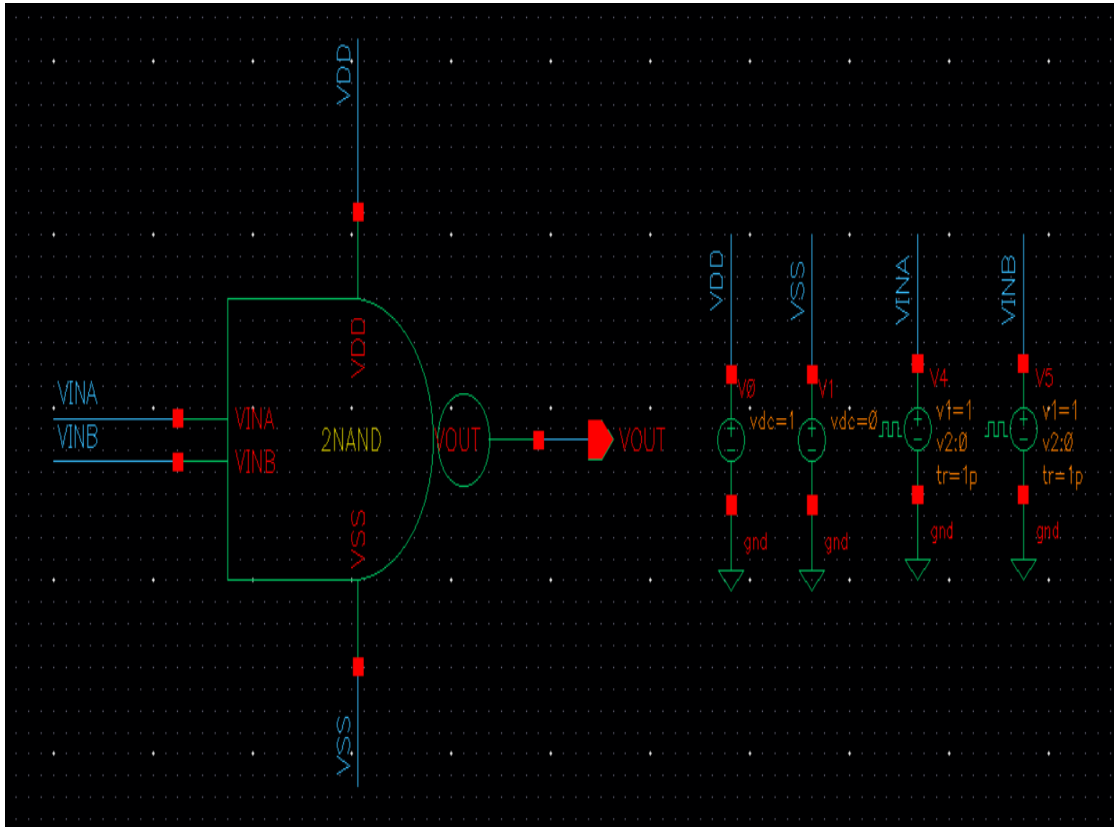


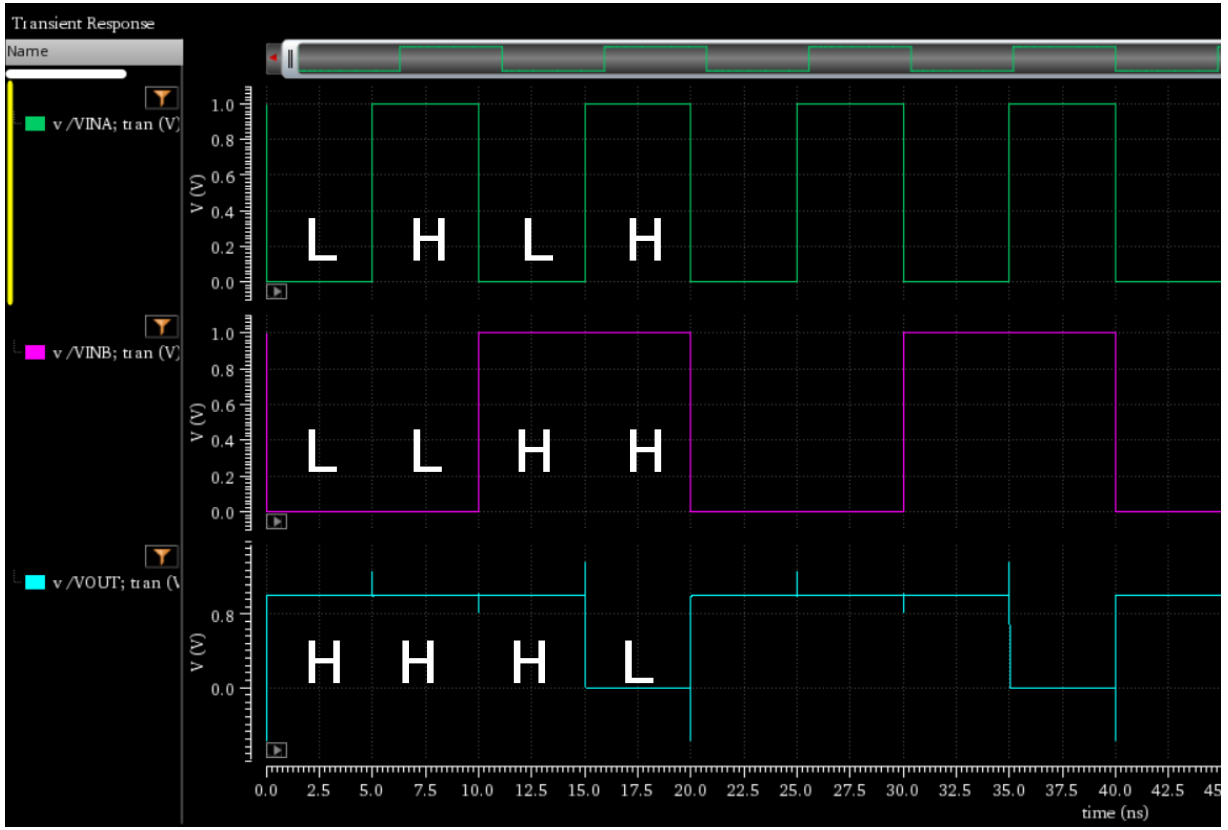
Simulation1



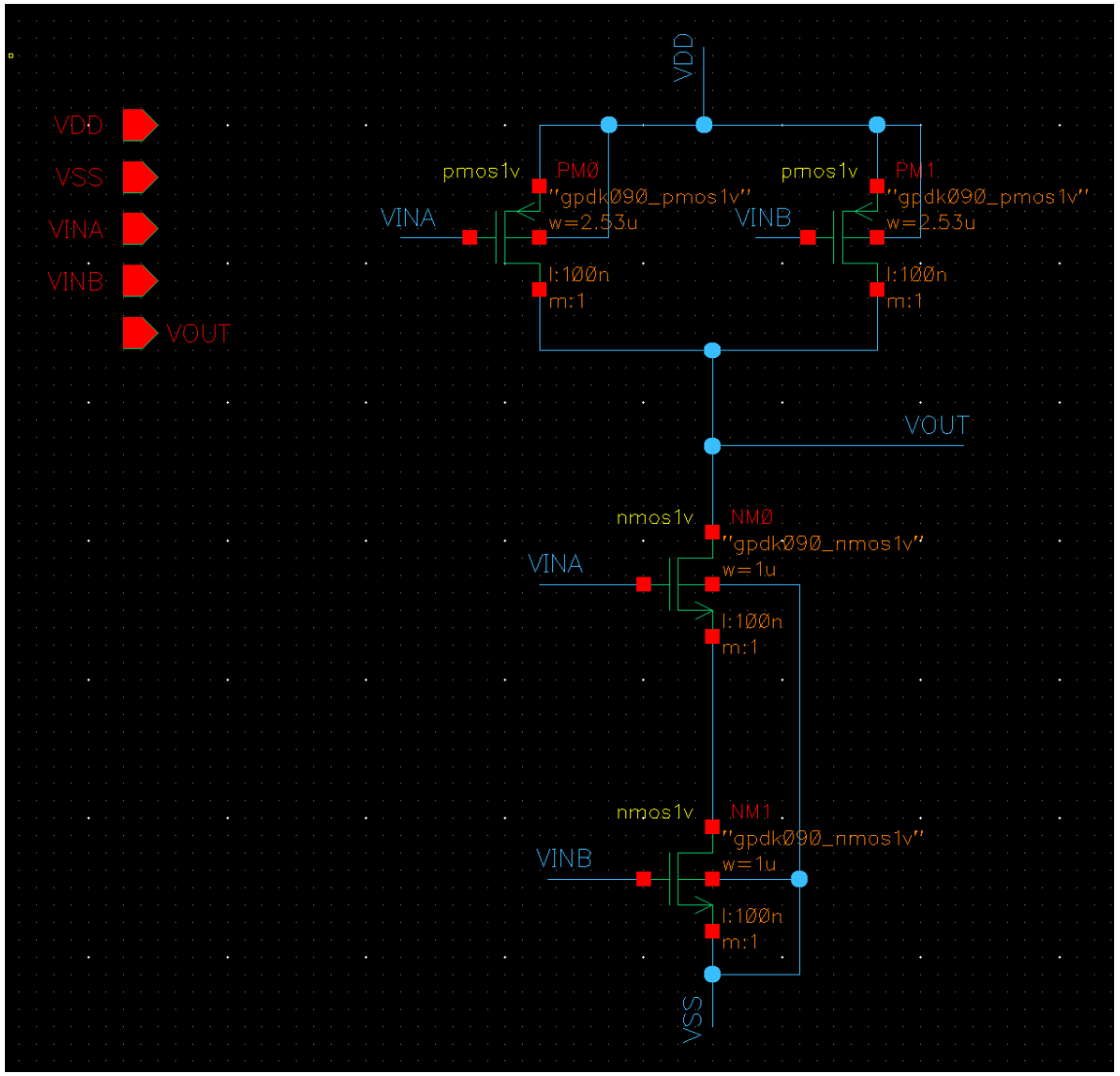
Digital Logic Gate – 2NAND

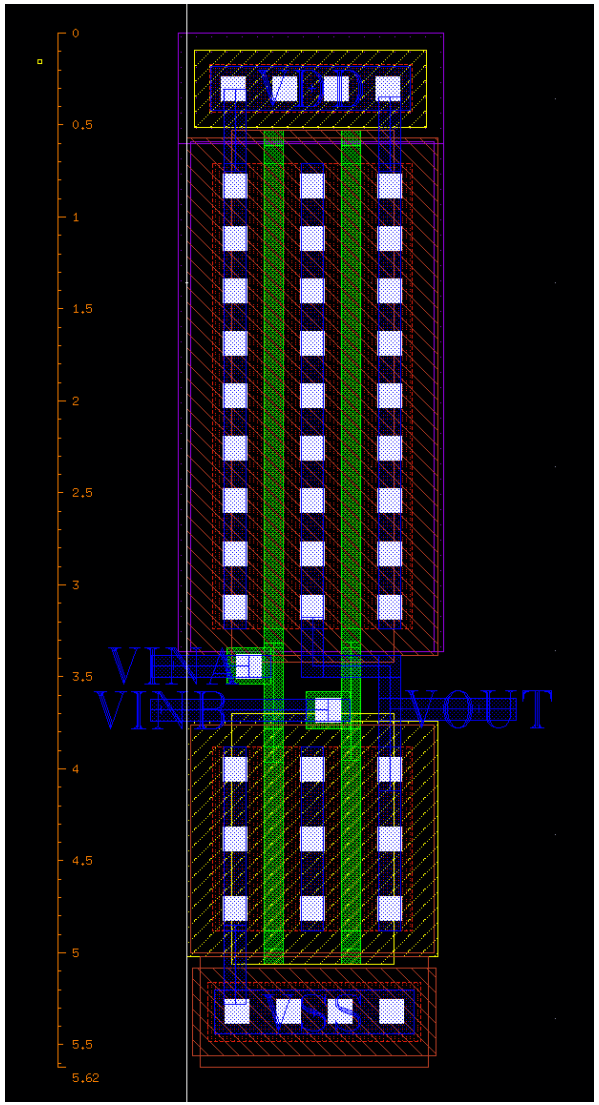
Simulation2





Digital Logic Gate – 2NAND

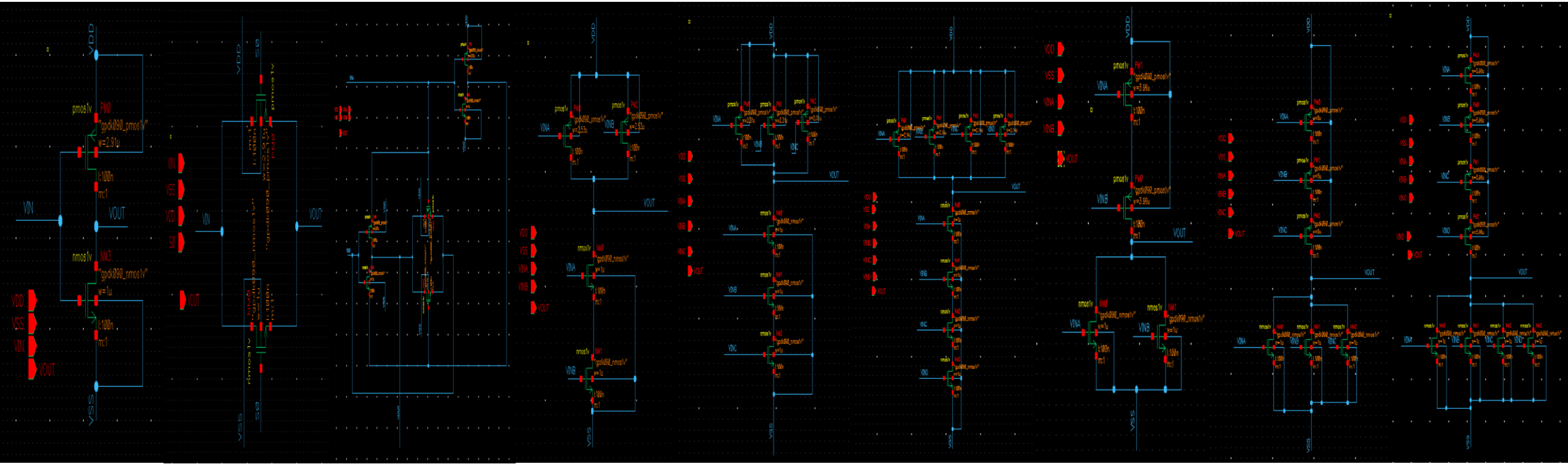




Digital Logic Gate – Schematic

Width	NOT	SWITCH	XOR	2NAND	3NAND	4NAND	2NOR	3NOR	4NOR
nMOS L=100nm	1um	1um	1um	1um	1um	1um	1um	1um	1um
pMOS L=100nm	2.91um	2.91um	2.91um	2.53um	2.31um	2.14um	3.99um	5um	5.96um

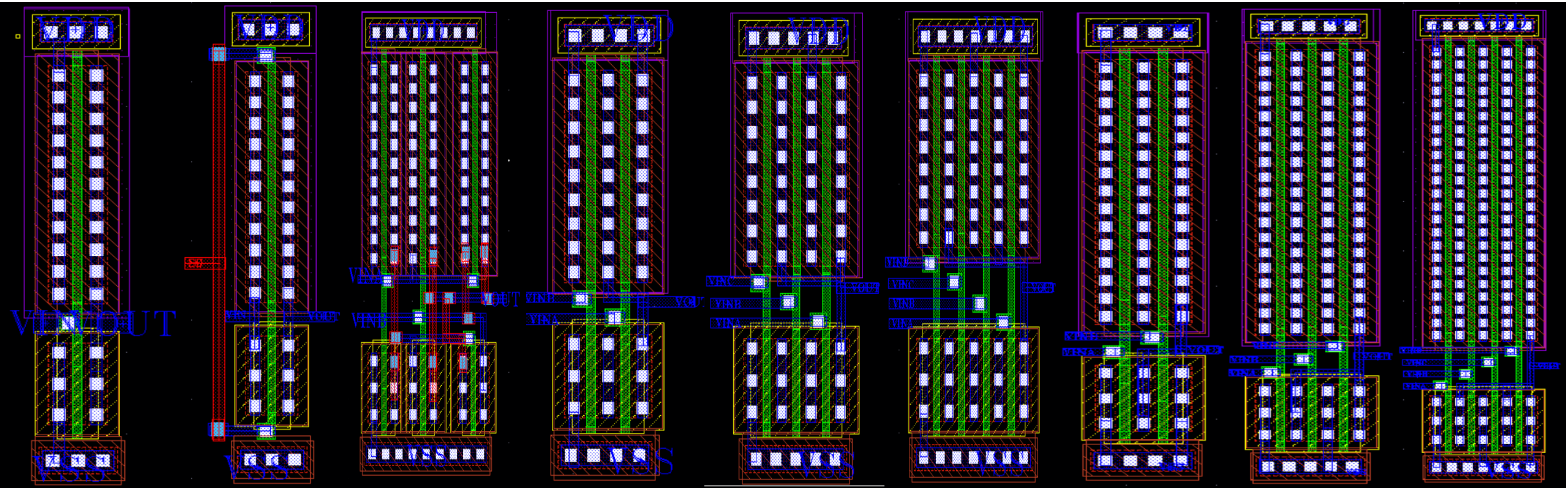
NOT SWITCH XOR 2NAND 3NAND 4NAND 2NOR 3NOR 4NOR



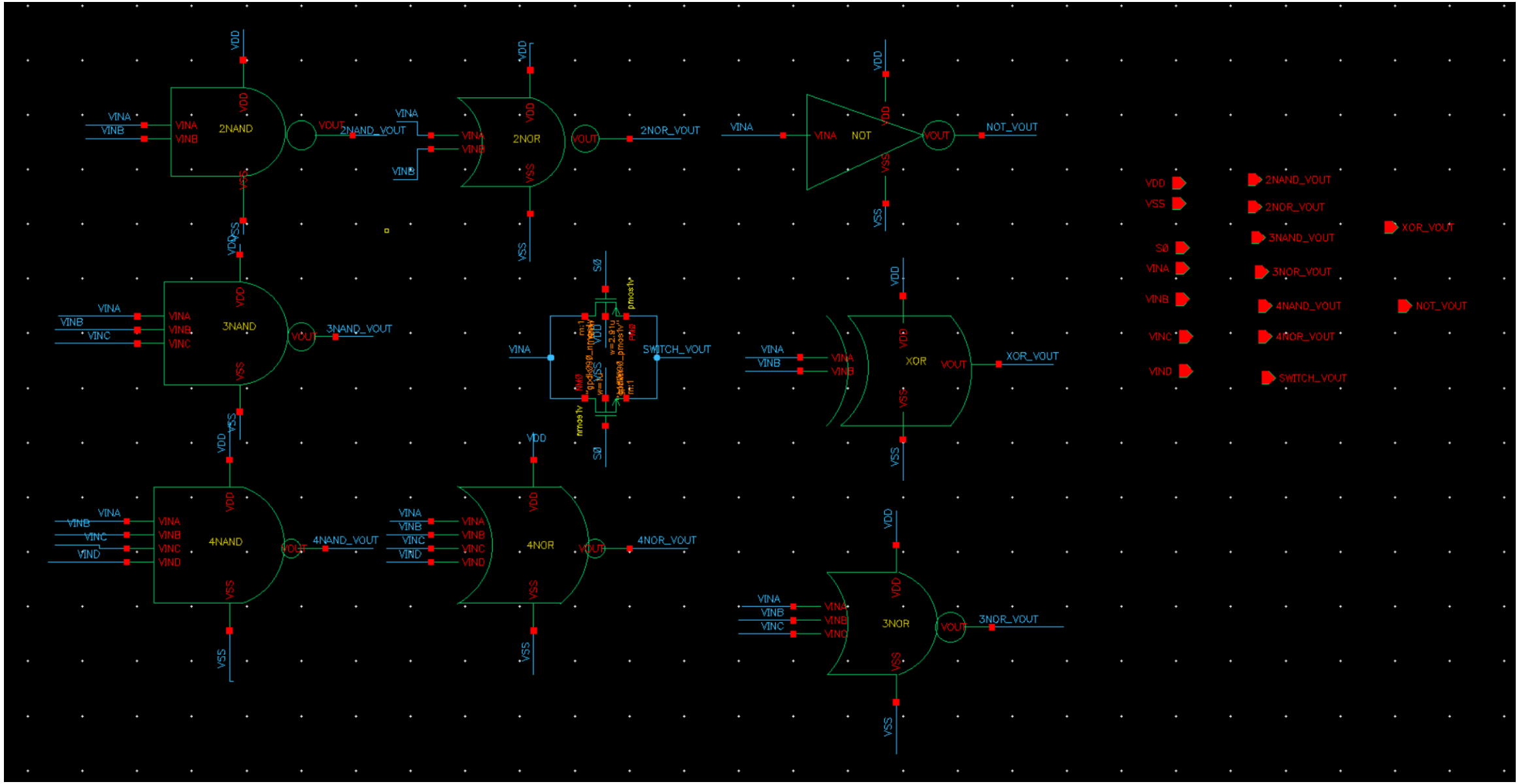
Digital Logic Gate – Layout

	NOT	SWITCH	2NAND	3NAND	4NAND	2NOR	3NOR	4NOR
Area (μm^2)	5.4802	5.6588	7.6160	10.0036	12.5180	9.6016	14.7918	20.9222

NOT SWITCH XOR 2NAND 3NAND 4NAND 2NOR 3NOR 4NOR



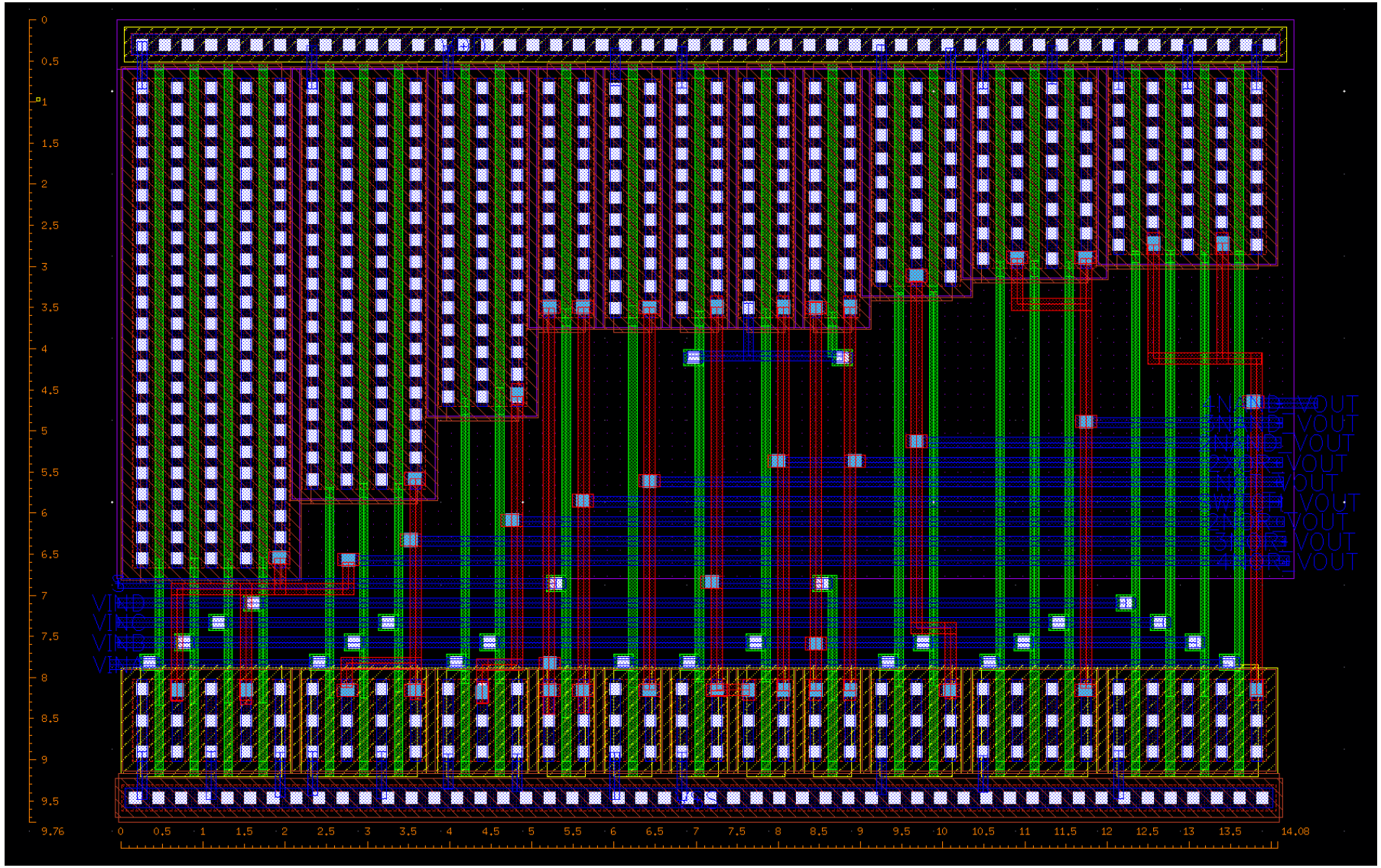
Digital Logic Gates



Digital Logic Gates

Group Layout

SIZE ：137.42um^2



IMPLICATIONS

Price

Speed

Power

THANK YOU.

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