Cadence Full-Custom IC Design

Common-Source Amplifier

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PROGRAM & TOOL

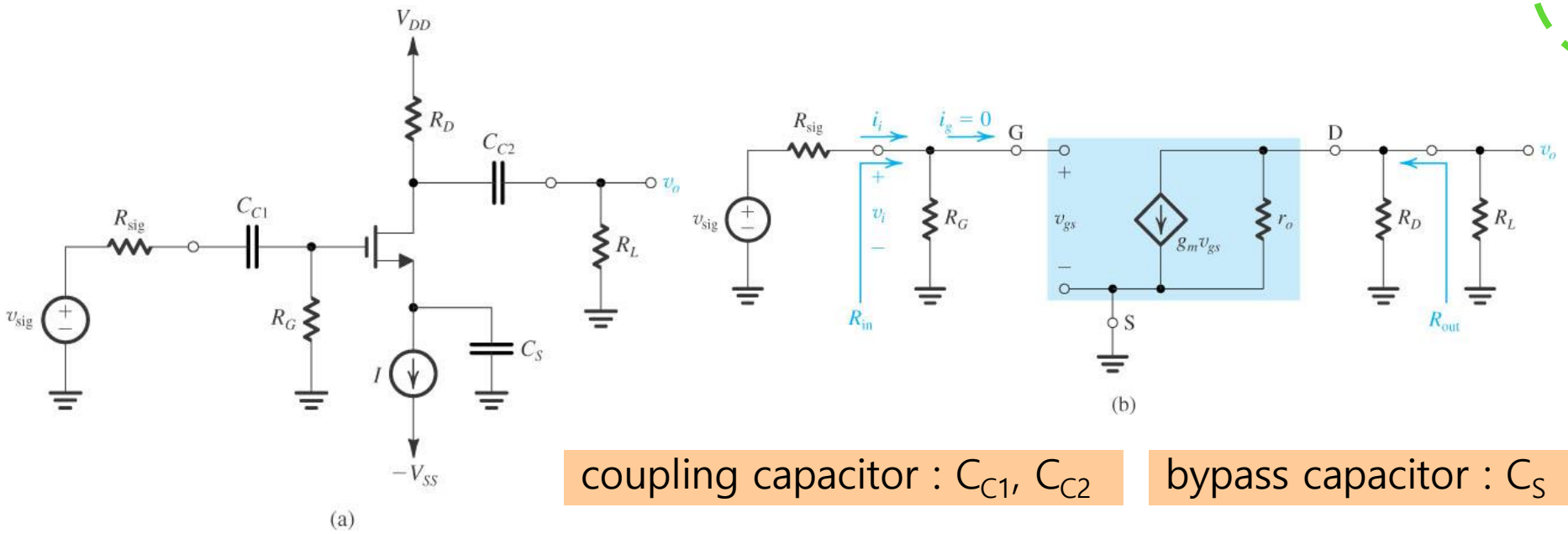
Cadence Virtuoso Schematic Editor/Layout Editor

Cadence Virtuoso Spectre/ADE

Assura(LVS & DRC)

GPDK090

The Common-Source (CS) Amplifier

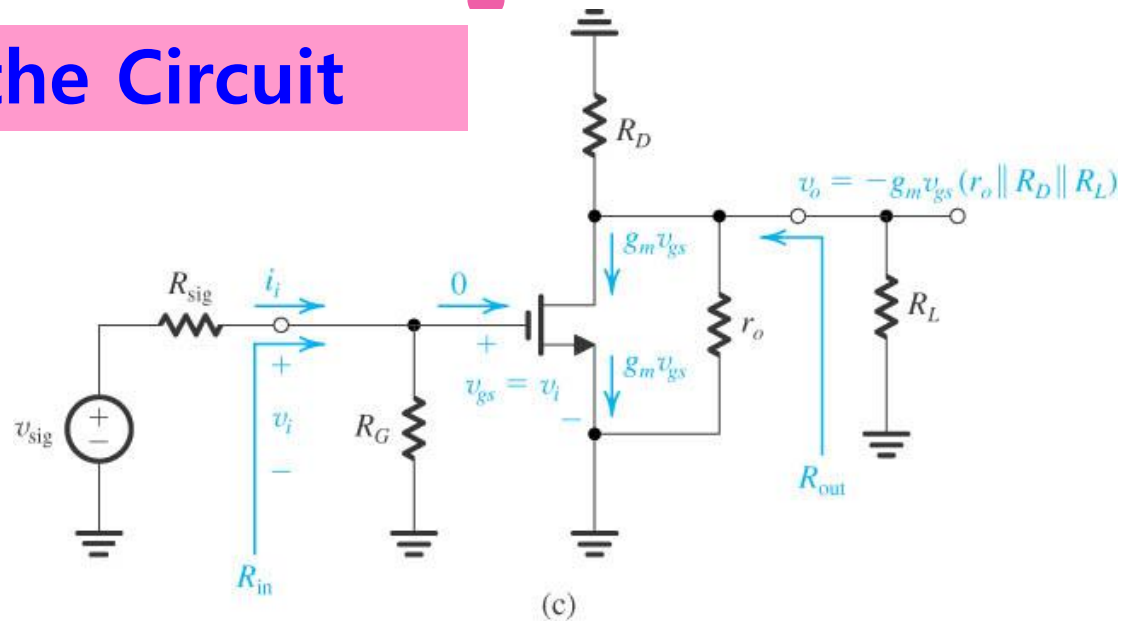


coupling capacitor : C_{C1}, C_{C2}

bypass capacitor : C_S

- input resistance : $R_{in} = R_G$
- output resistance : $R_{out} = r_o \,/\!/\, R_D$
- voltage gain : $A_v = -g_m(r_o \,/\!/\, R_D \,/\!/\, R_L)$
- overall voltage gain : $G_v = -\dfrac{R_G}{R_G + R_{sig}} g_m(r_o \,/\!/\, R_D \,/\!/\, R_L)$
- applications : part of a larger amplifier circuit

Directly on the Circuit



$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{sig} + R_{in}} = \frac{R_G}{R_{sig} + R_G}$$

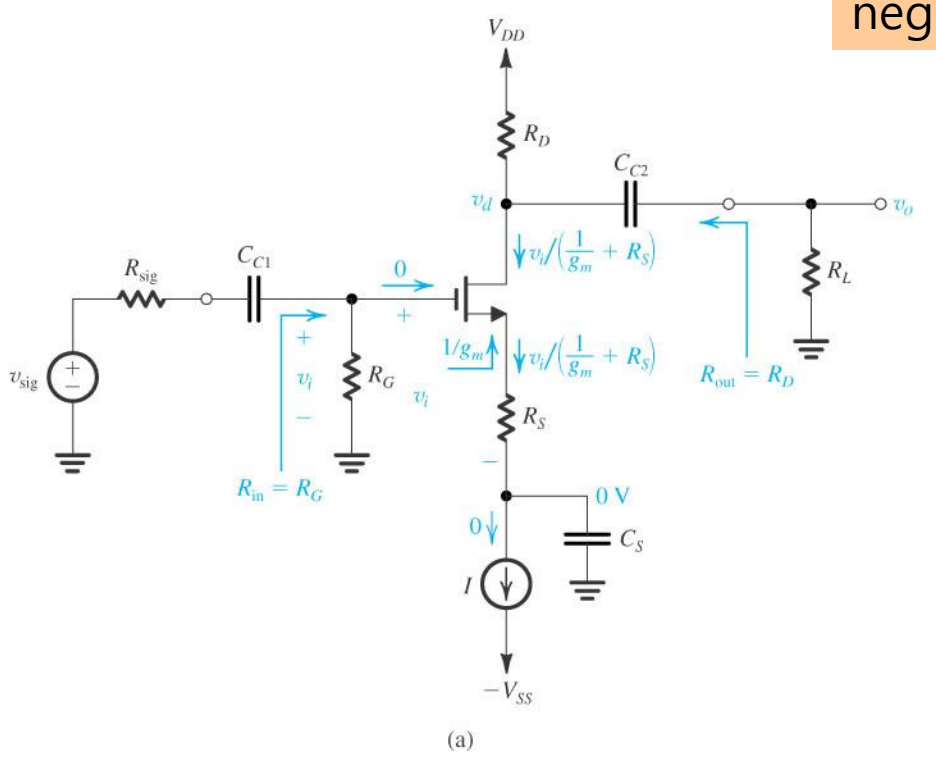
$$G_m \equiv \left.\frac{i_o}{v_i}\right|_{R_L=0} = -g_m \qquad R_{out,total} = r_o \,//\, R_D \,//\, R_L$$

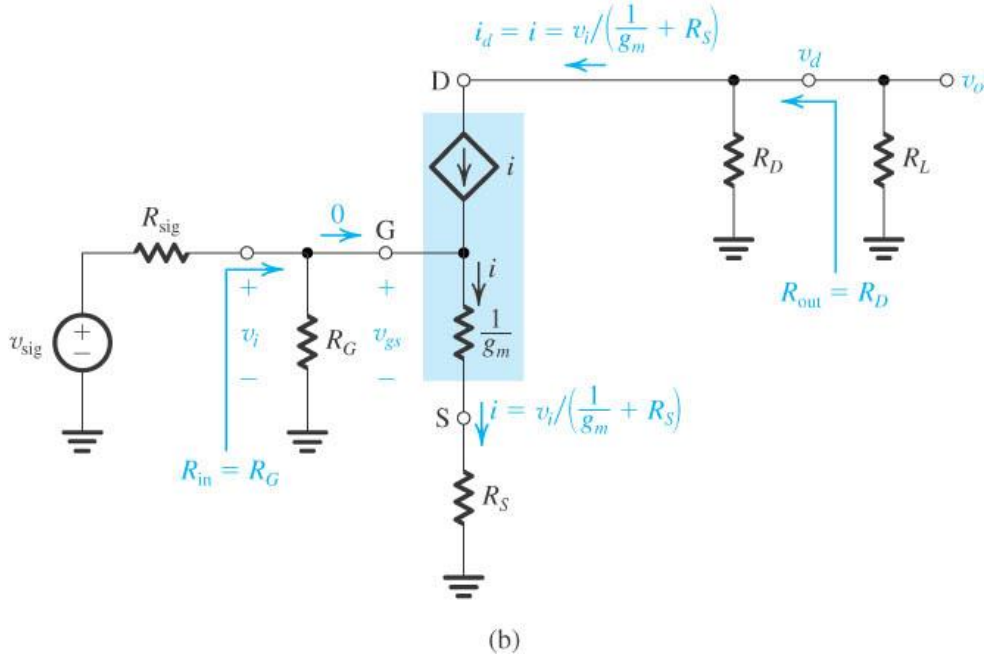
$$A_v = \frac{v_o}{v_i} = G_m R_{out,total} = -g_m (r_o \,//\, R_D \,//\, R_L)$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}} \frac{v_o}{v_i} = -\frac{R_G}{R_G + R_{sig}} g_m (r_o \,//\, R_D \,//\, R_L)$$

The Common-Source Amplifier with a Source Resistance

neglecting r_o





- input resistance : $R_{in}=R_G$
- output resistance : $R_{out}=R_D$

▶ voltage gain :

$$v_{gs} = \frac{1/g_m}{(1/g_m)+R_S} v_i = \frac{v_i}{1+g_m R_S}$$

$$i_d = i = \frac{v_i}{(1/g_m)+R_S} = \frac{g_m v_i}{1+g_m R_S}$$

$$v_o = -i_d (R_D /\!/ R_L) = -\frac{g_m (R_D /\!/ R_L)}{1+g_m R_S} v_i$$

$$A_v = -\frac{g_m (R_D /\!/ R_L)}{1+g_m R_S}$$

▶ overall voltage gain : $G_v = -\frac{R_G}{R_G + R_{sig}} \frac{g_m (R_D /\!/ R_L)}{1+g_m R_S}$

▶ source degeneration resistor R_S : reduction of the gain by $(1+g_m R_S)$

Directly on the Circuit

$$v_i = v_{gs} + R_S i_d = i_d / g_m + R_S i_d = (1/g_m + R_S) i_d$$

$$G_m \equiv \left.\frac{i_o}{v_i}\right|_{R_L=0} = -\frac{i_d}{v_i} = -\frac{1}{1/g_m + R_S}$$

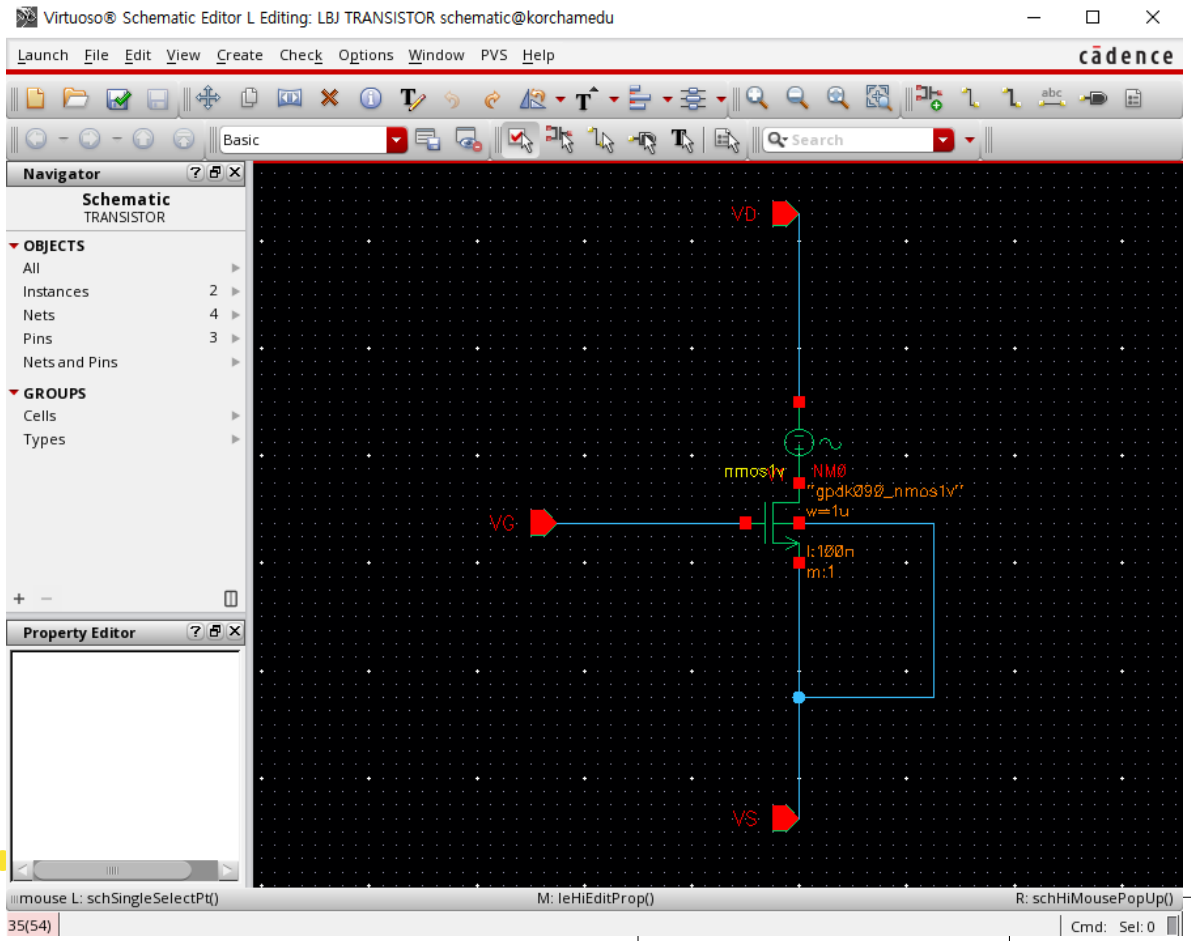
$$R_{out,total} = R_D \,//\, R_L$$

$$A_v = G_m R_{out,total} = -\frac{R_D \,//\, R_L}{1/g_m + R_S} = -\frac{g_m (R_D \,//\, R_L)}{1 + g_m R_S}$$

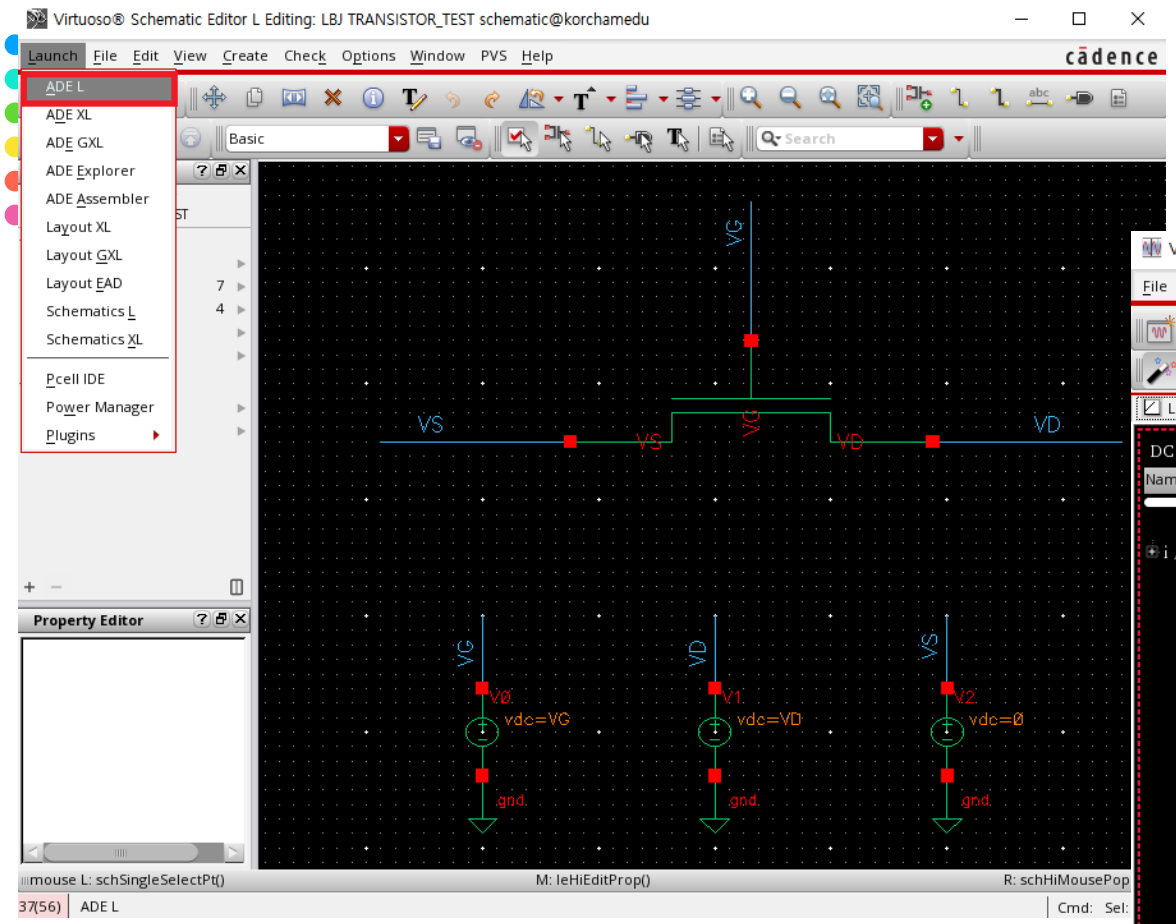
▶ useful interpretation :

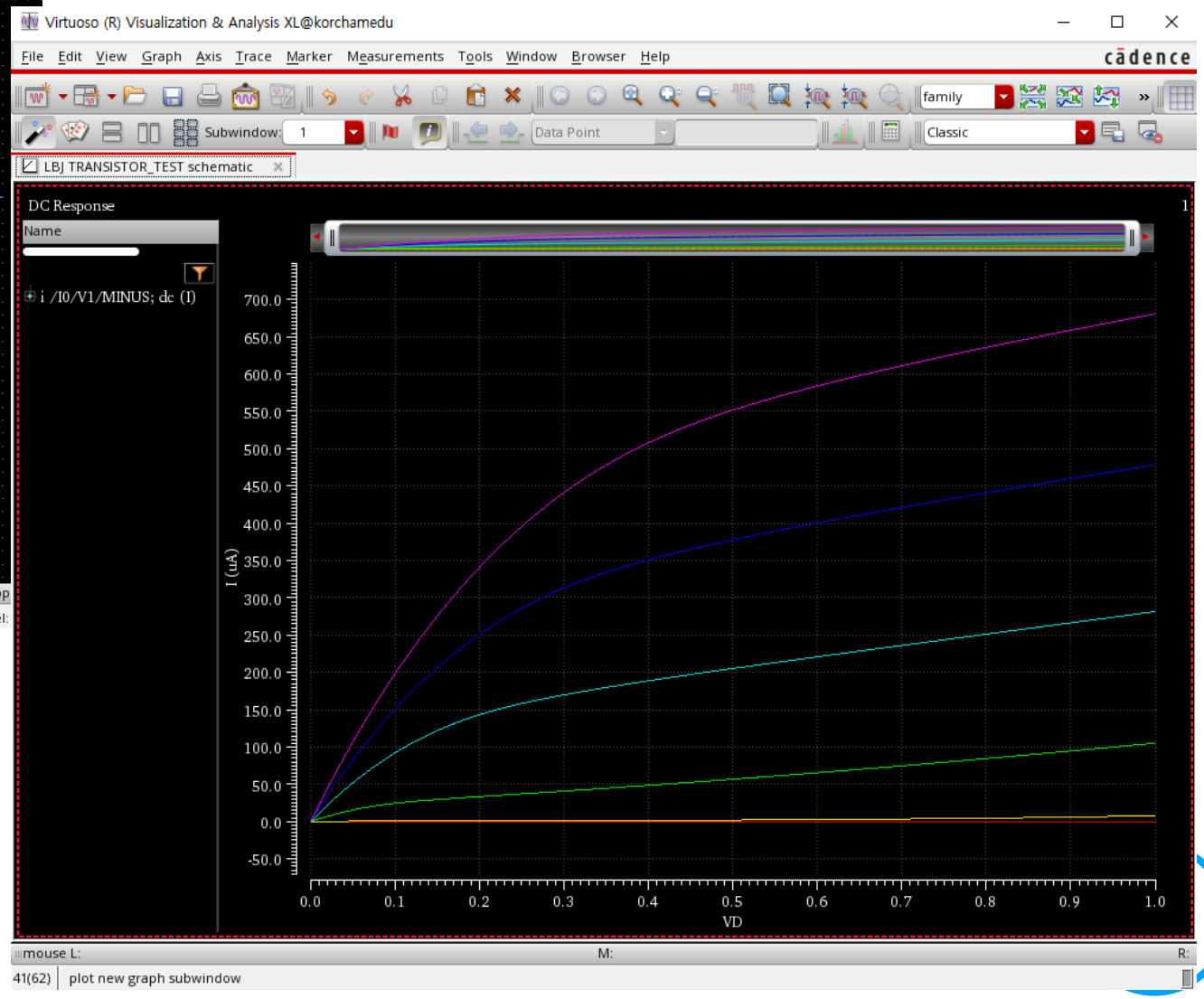
$$A_v = -\frac{\text{total resistance in the drain}}{\text{total resistance in the source}} = -\frac{R_D \,//\, R_L}{1/g_m + R_S}$$

MOSFET SIMULATION SETUP

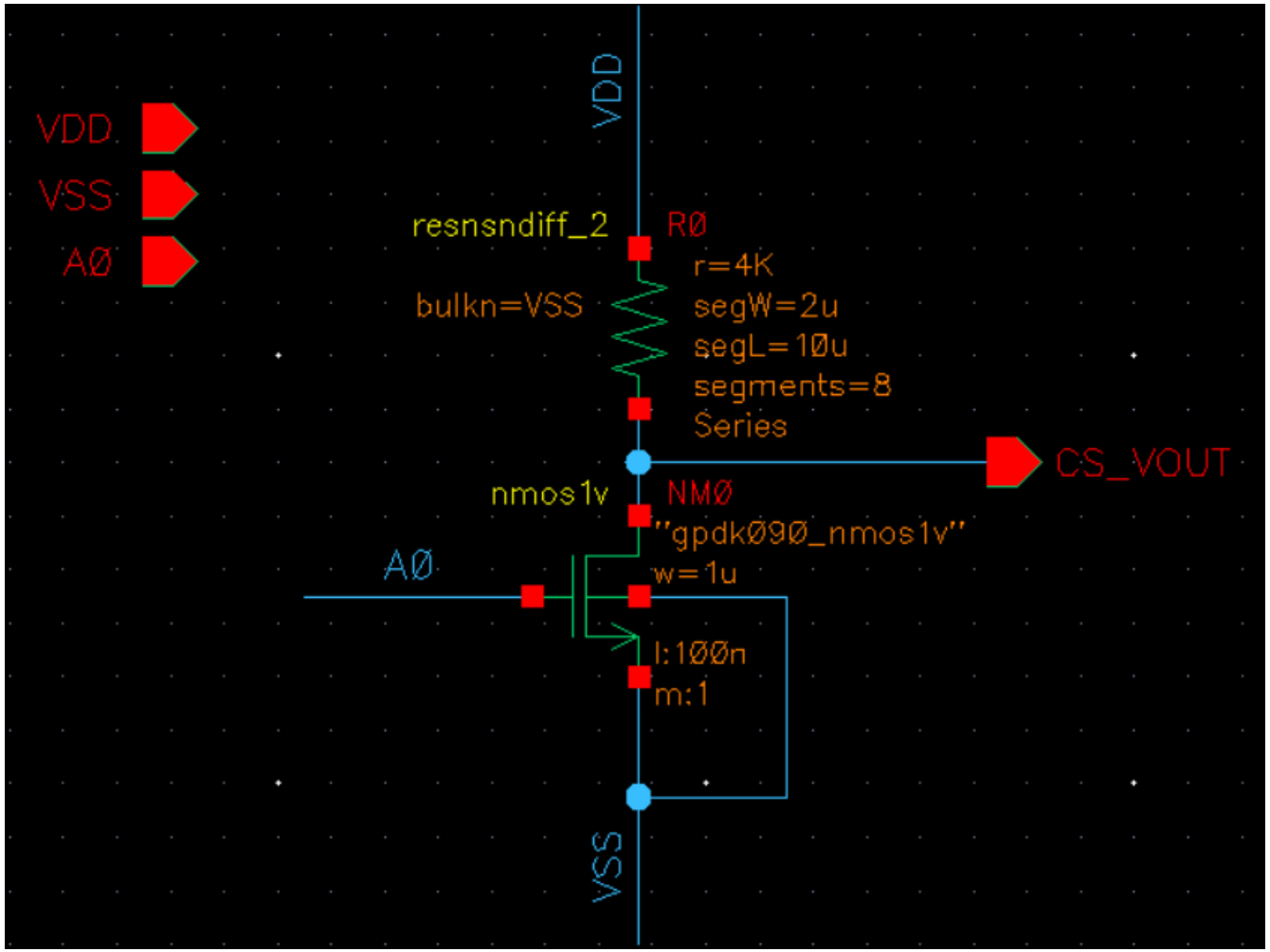


MOSFET	Length(μm)	Fingers	Finger Width(μm)	Total Width(μm)
NMOS(NM0)	0.1	1	1	1


Virtuoso® Schematic Editor L Editing: LBJ TRANSISTOR_TEST schematic@korchamedu
Launch File Edit View Create Check Options Window PVS Help
cadence
ADE L
ADE XL
ADE GXL
ADE Explorer
ADE Assembler
Layout XL
Layout GXL
Layout EAD
Schematics L
Schematics XL
Pcell IDE
Power Manager
Plugins
Basic
Search
Property Editor
VG
VS
VD
V0
V1
V2
vdc=VG
vdc=VD
vdc=0
gnd
mouse L: schSingleSelectPt()
M: leHiEditProp()
R: schHiMousePop
37(56)
ADE L
Cmd:
Sel:

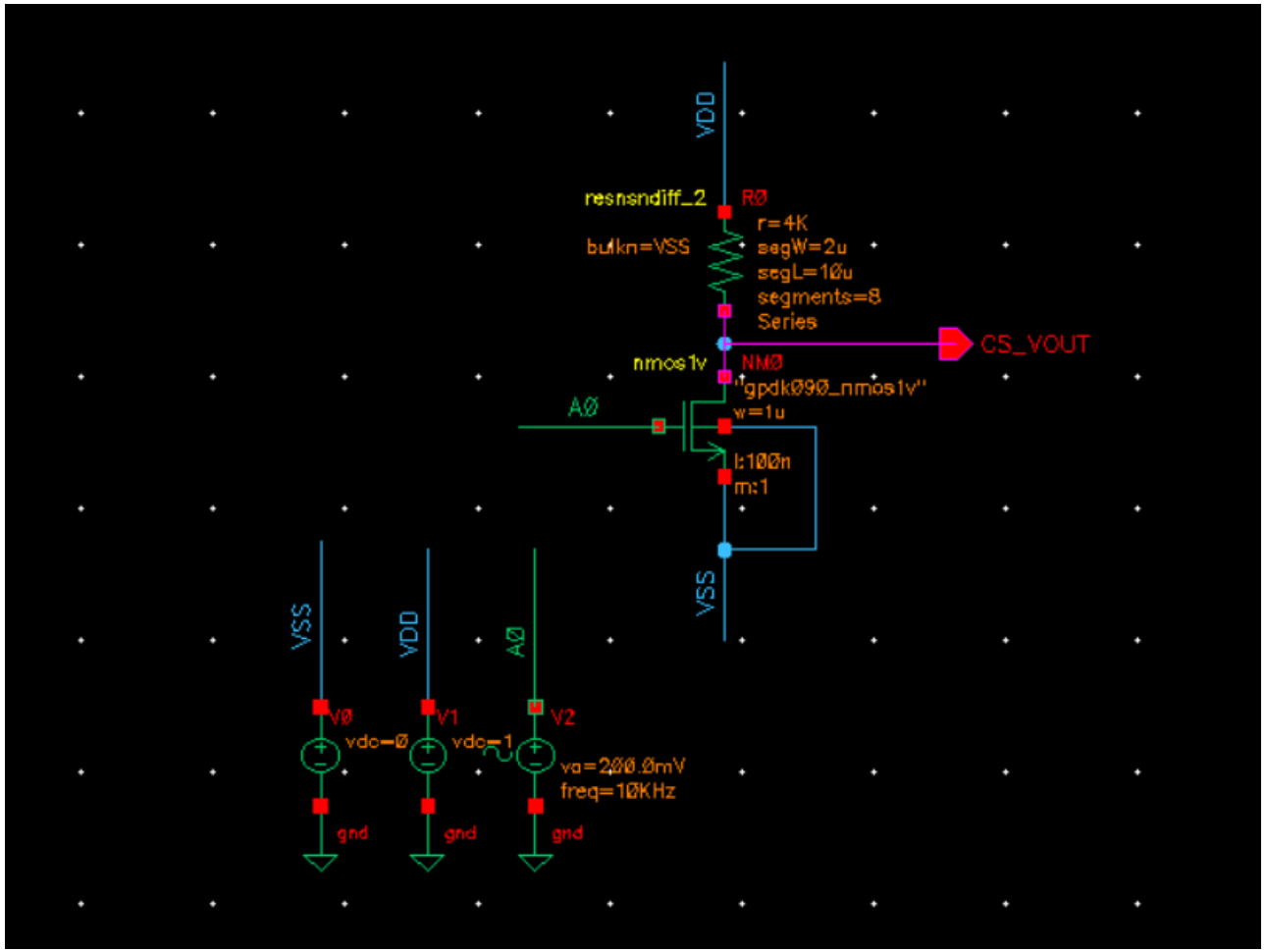

Virtuoso (R) Visualization & Analysis XL@korchamedu
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
family
Subwindow: 1
Data Point
Classic
LBJ TRANSISTOR_TEST schematic
DC Response
Name
i /I0/V1/MINUS; dc (I)
I (uA)
VD
700.0
650.0
600.0
550.0
500.0
450.0
400.0
350.0
300.0
250.0
200.0
150.0
100.0
50.0
0.0
-50.0
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
mouse L:
M:
R:
41(62)
plot new graph subwindow

CS AMP. SCHEMATIC

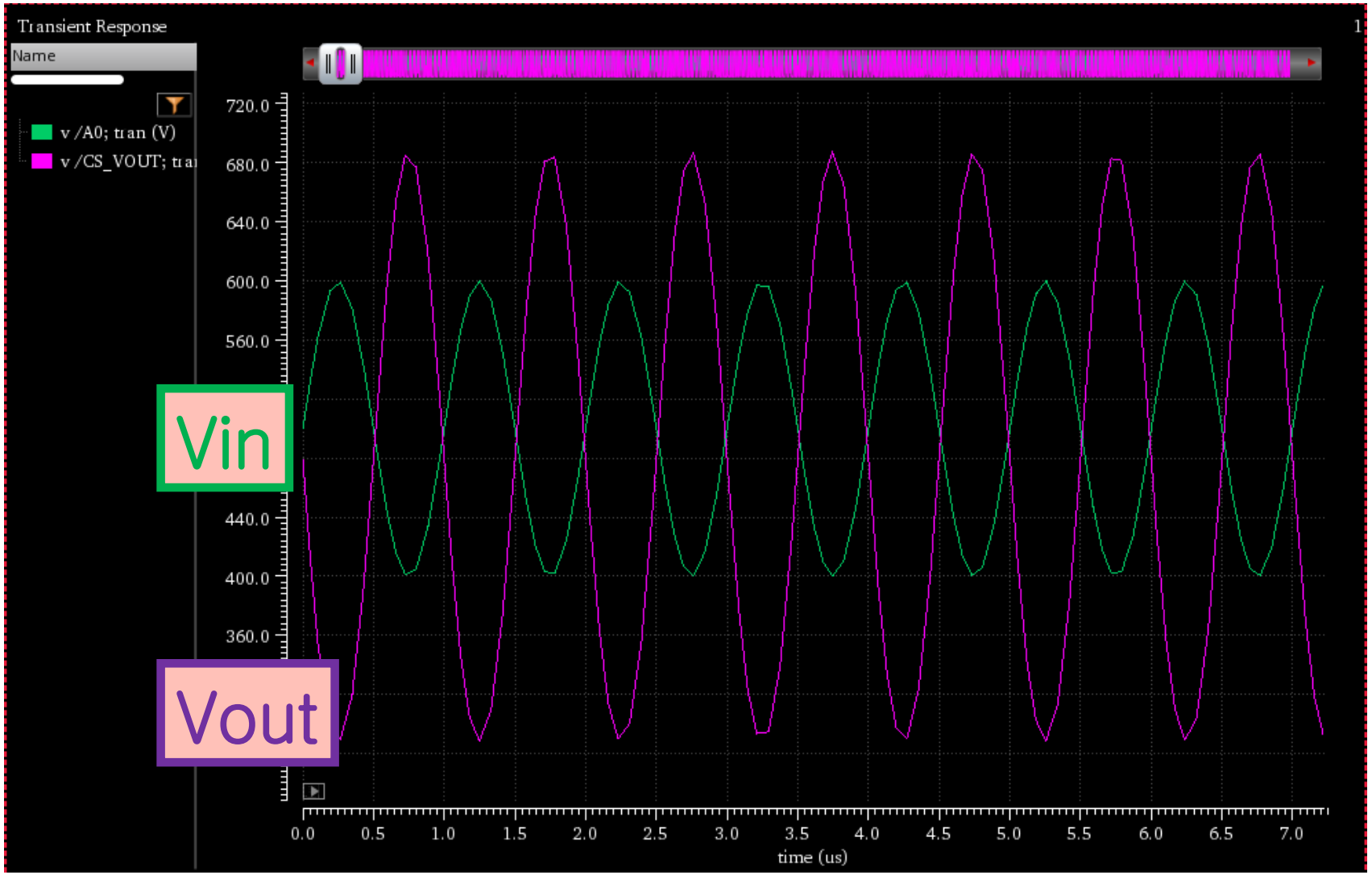


MOSFET	Length(㎛)	Fingers
NMOS(NM0)	0.1	1
Resistance	Total Resistance(ohms)	
R(R0)	4k	

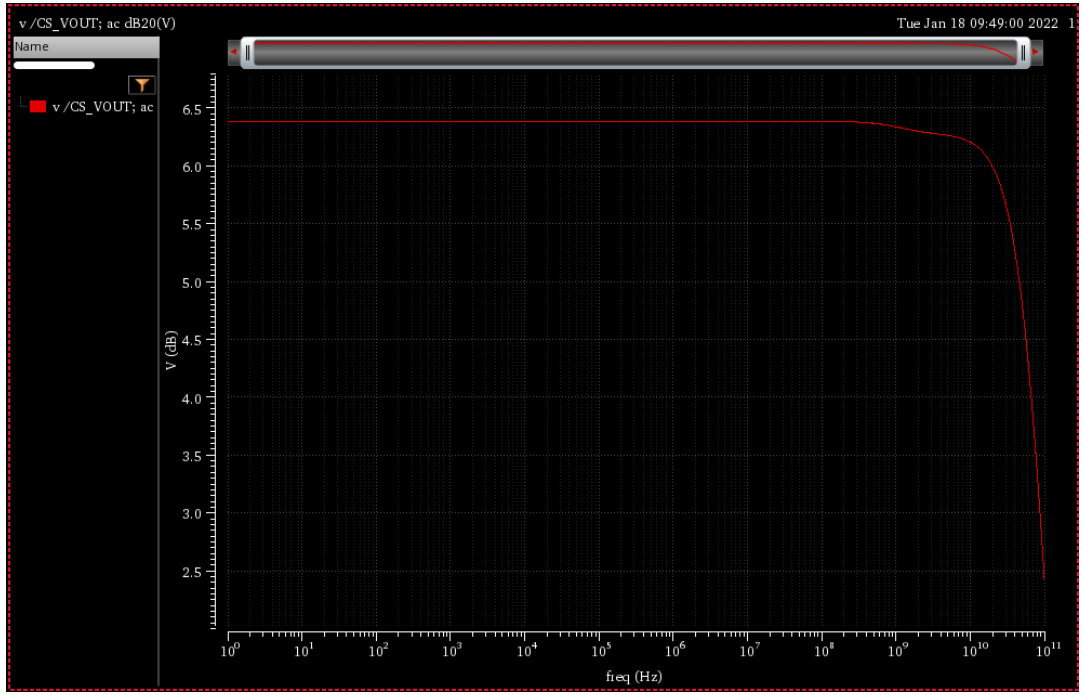
CS AMP SIMULATION SETUP

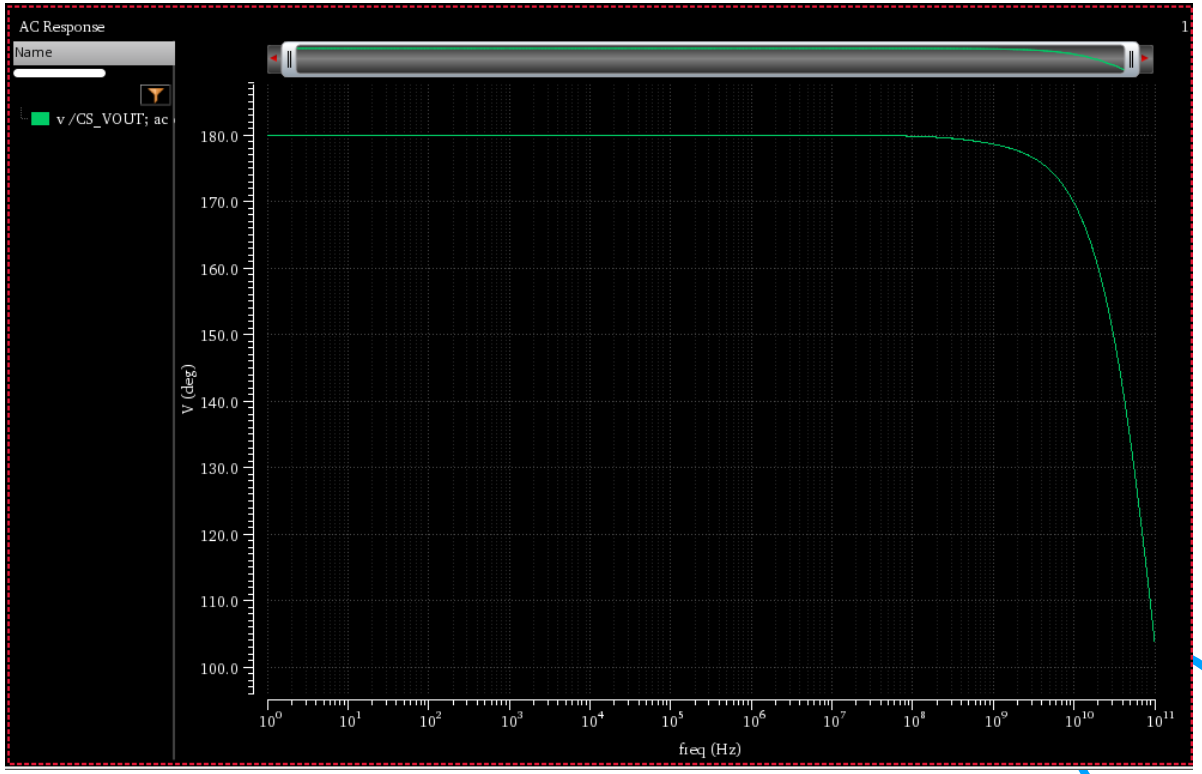


VOLTAGE GAIN

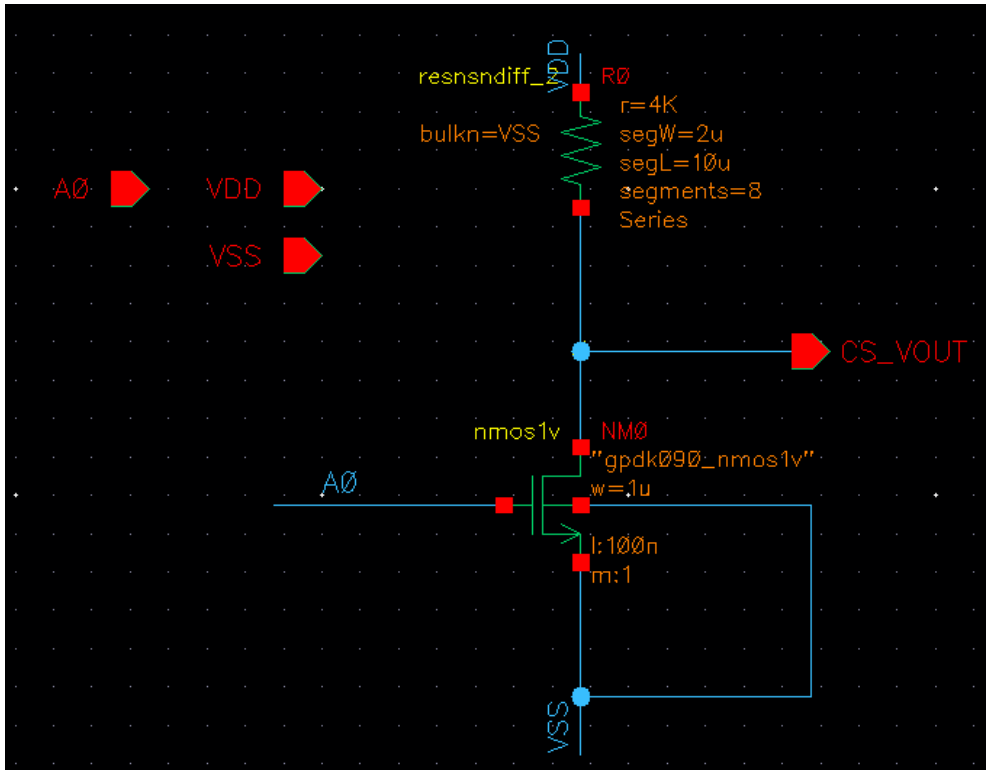


20dB & Phase


v /CS_VOUT; ac dB20(V)
Tue Jan 18 09:49:00 2022
Name
v /CS_VOUT; ac
V (dB)
freq (Hz)

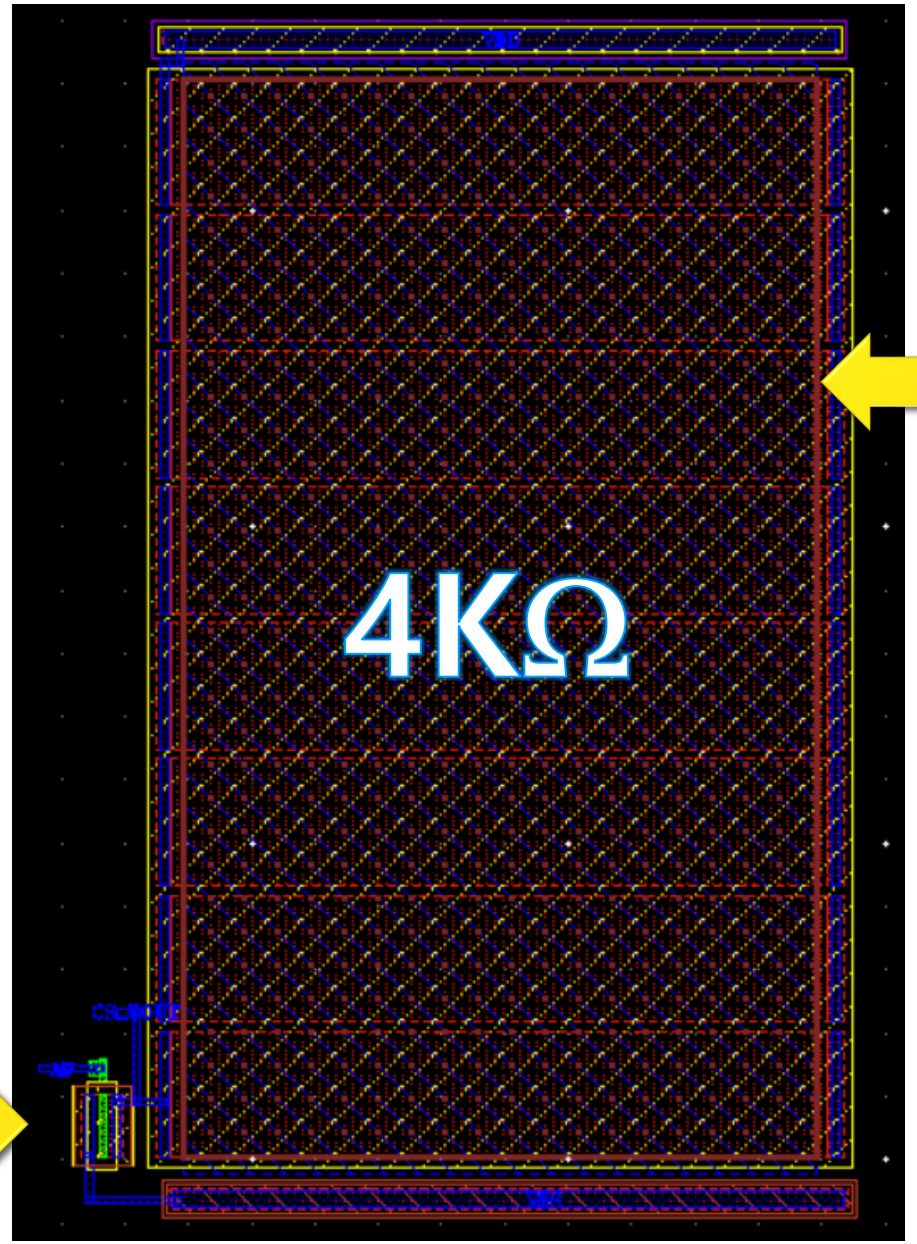

AC Response
Name
v /CS_VOUT; ac
V (deg)
freq (Hz)

CS AMP LAYOUT SETUP



Component	MOSFET	Component	Resistor
Type	nmos1v	**Type**	resnapdiff_2
Length	100nm	**Width(㎛)**	2
Finger	1	**No. of Segments**	8
Finger Width(㎛)	1	**Segment Length(㎛)**	10
Total Width(㎛)	1	**Total Length(㎛)**	80
		Total Resistance	4kΩ

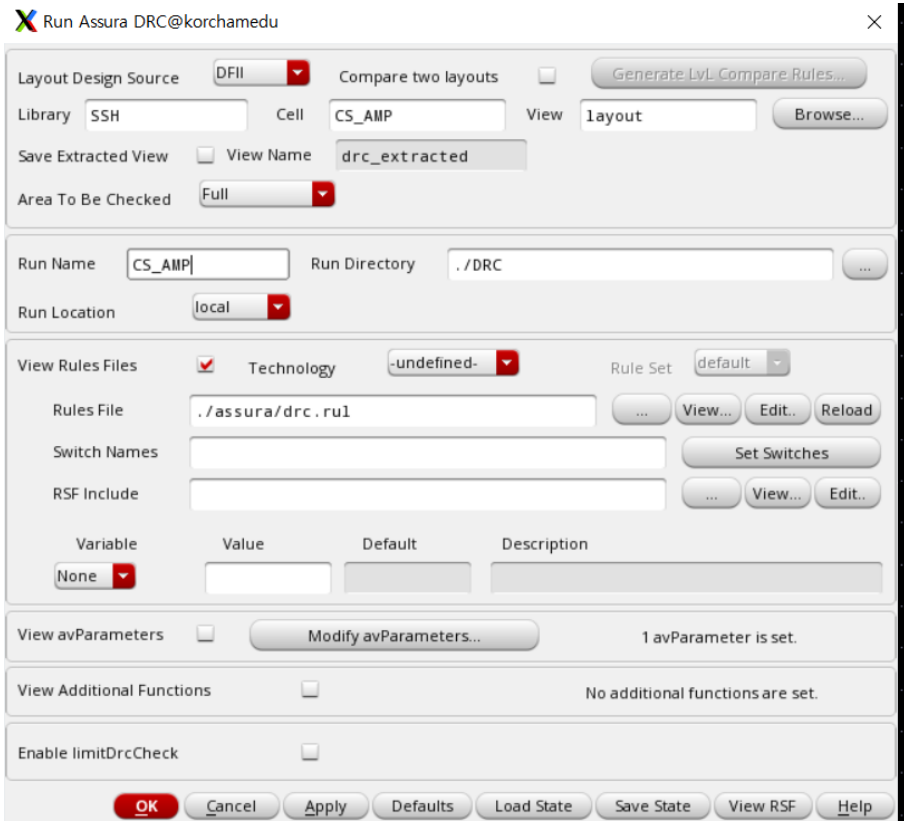
CS AMP LAYOUT

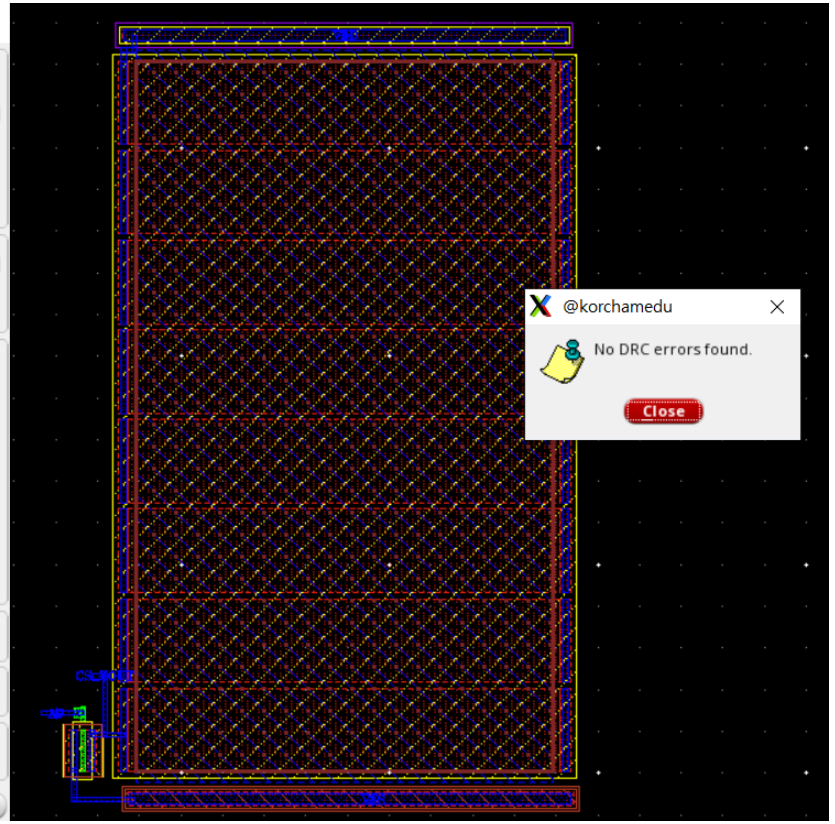


RESISTOR

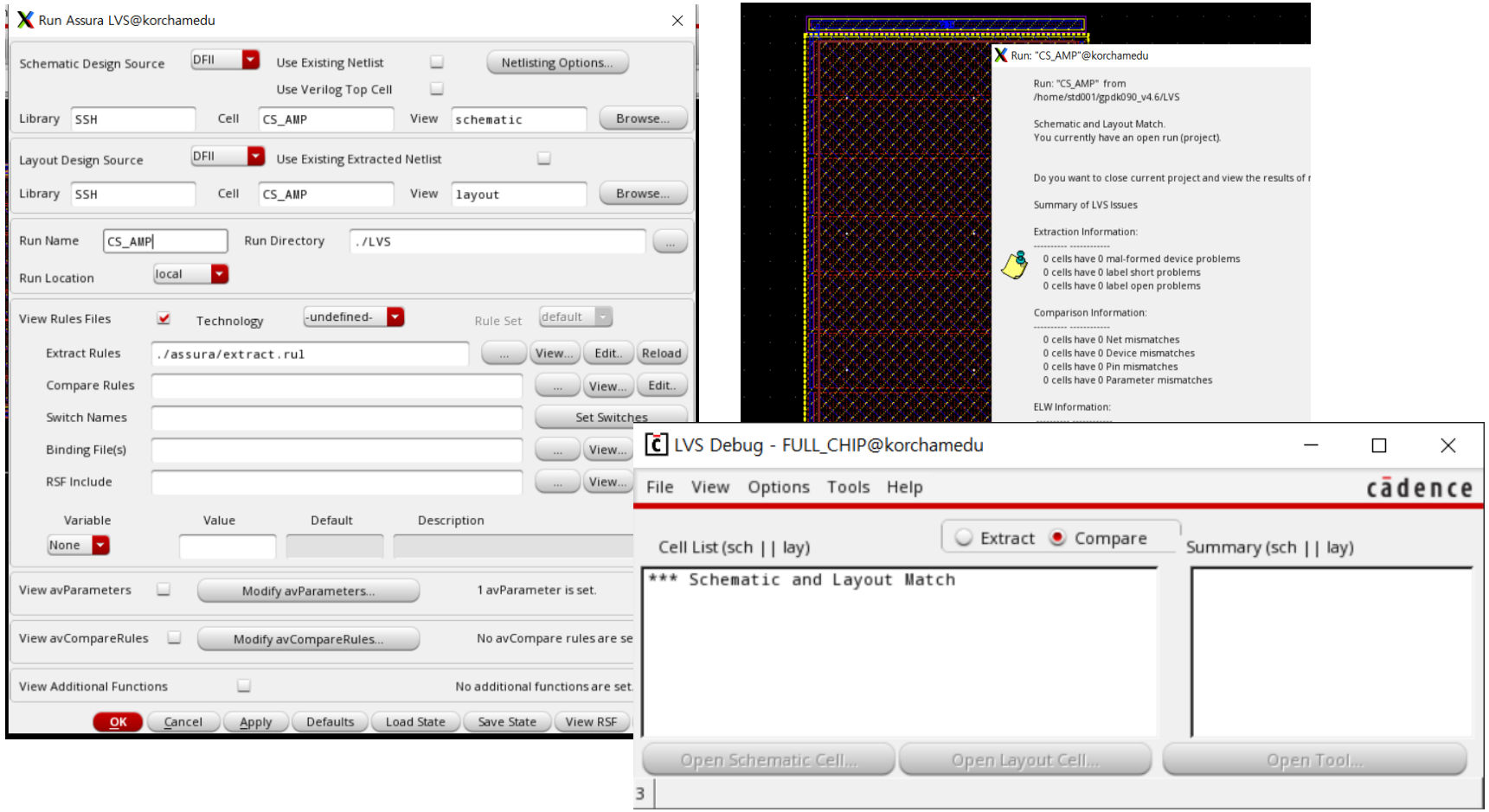
TRANSISTOR

CS AMP (DRC)


Run Assura DRC@korchamedu
Layout Design Source
DFII
Compare two layouts
Generate LvL Compare Rules...
Library
SSH
Cell
CS_AMP
View
layout
Browse...
Save Extracted View
View Name
drc_extracted
Area To Be Checked
Full
Run Name
CS_AMP
Run Directory
./DRC
Run Location
local
View Rules Files
Technology
-undefined-
Rule Set
default
Rules File
./assura/drc.rul
View...
Edit..
Reload
Switch Names
Set Switches
RSF Include
Variable
Value
Default
Description
None
View avParameters
Modify avParameters...
1 avParameter is set.
View Additional Functions
No additional functions are set.
Enable limitDrcCheck
OK
Cancel
Apply
Defaults
Load State
Save State
View RSF
Help


@korchamedu
No DRC errors found.
Close

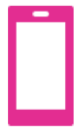
CS AMP (LVS)


Run Assura LVS@korchamedu
Schematic Design Source
DFII
Use Existing Netlist
Netlisting Options...
Use Verilog Top Cell
Library
SSH
Cell
CS_AMP
View
schematic
Browse...
Layout Design Source
DFII
Use Existing Extracted Netlist
Library
SSH
Cell
CS_AMP
View
layout
Browse...
Run Name
CS_AMP
Run Directory
./LVS
Run Location
local
View Rules Files
Technology
-undefined-
Rule Set
default
Extract Rules
./assura/extract.rul
View...
Edit..
Reload
Compare Rules
Switch Names
Set Switches
Binding File(s)
RSF Include
Variable
Value
Default
Description
None
View avParameters
Modify avParameters...
1 avParameter is set.
View avCompareRules
Modify avCompareRules...
No avCompare rules are se
View Additional Functions
No additional functions are set.
OK
Cancel
Apply
Defaults
Load State
Save State
View RSF
Run: "CS_AMP"@korchamedu
Run: "CS_AMP" from
/home/std001/gpdk090_v4.6/LVS
Schematic and Layout Match.
You currently have an open run (project).
Summary of LVS Issues
Extraction Information:
0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems
Comparison Information:
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches
ELW Information:
LVS Debug - FULL_CHIP@korchamedu
File
View
Options
Tools
Help
cadence
Extract
Compare
Cell List (sch || lay)
Summary (sch || lay)
*** Schematic and Layout Match
Open Schematic Cell...
Open Layout Cell...
Open Tool...

CONTACT

E-mail

byoungjin@hanmail.net



Phone

010 2026 3457