4BIT_ADDER

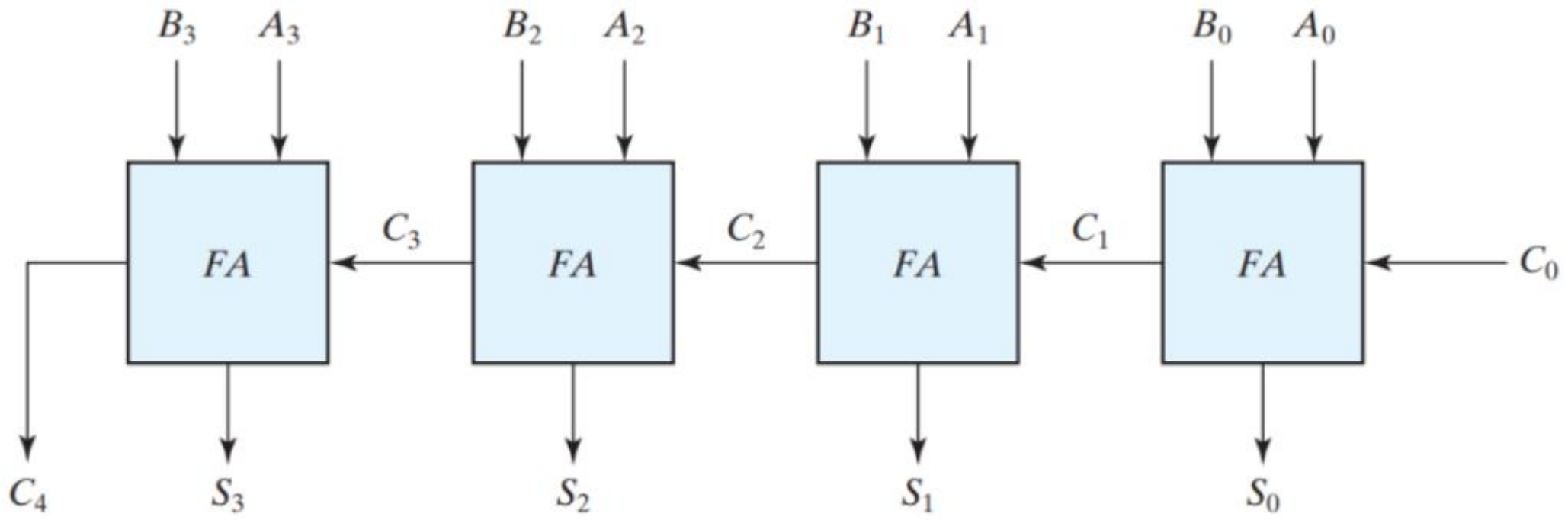
Ph. D. ByoungJin Lee

순서

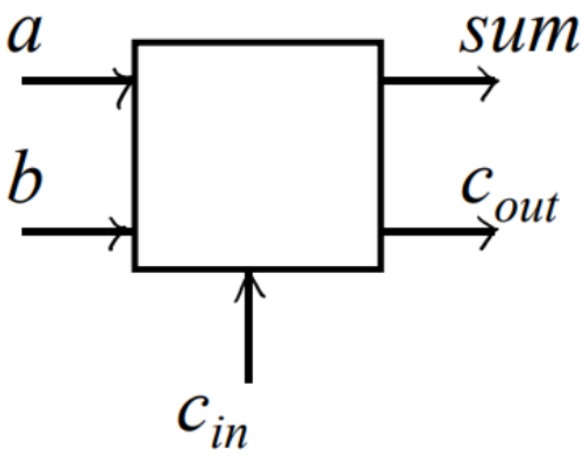
- 4Bit Adder
- Circuit design
- Schematic
- Circuit simulation
- Layout
- DRC, LVS

4Bit Adder

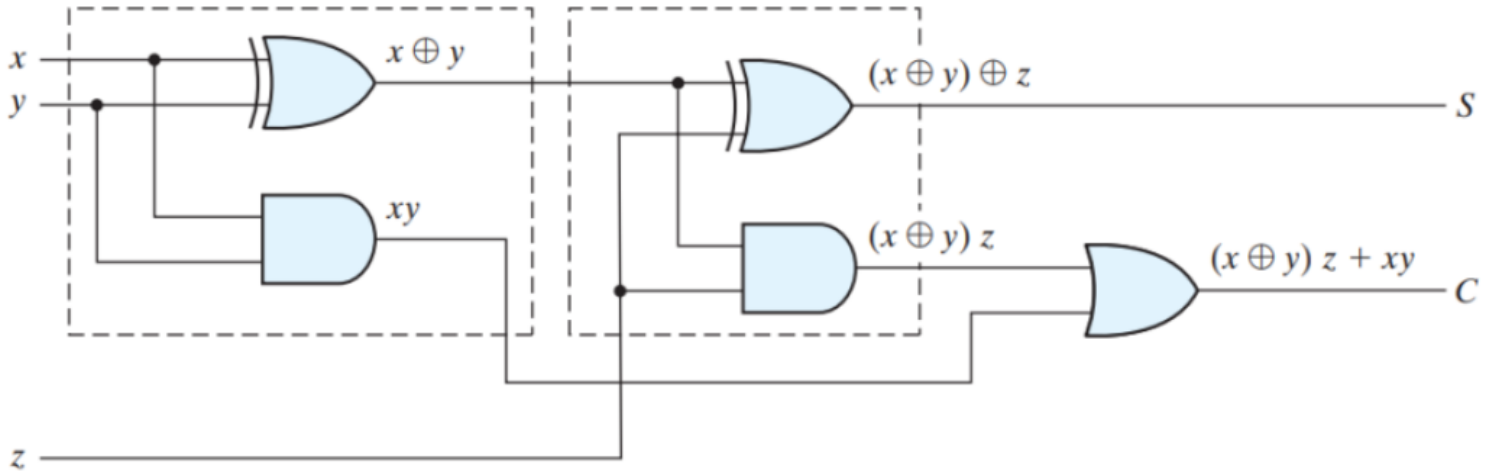
- 4비트 가산기는 4비트인 2개의 입력신호를 더하는 역할을 한다.
- 예를 들어 1011 + 1100 = 10111이다. 기본적인 4비트 병렬 가산기는 4개의 전가산기로 구성된다. 두 개의 입력 신호로 주어지며, 각 가산기의 캐리 출력은 다음 상위 가산기의 캐리 입력이 된다.



4Bit Adder



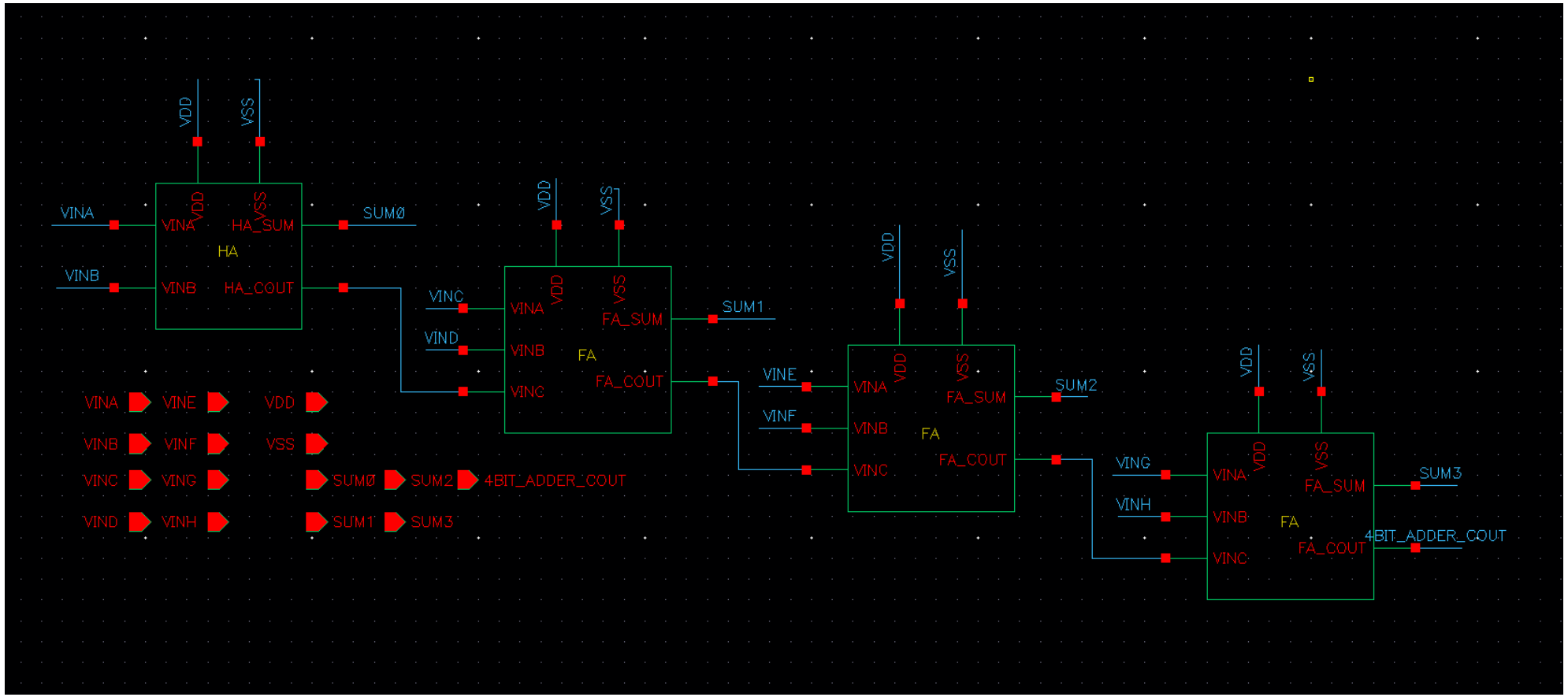
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



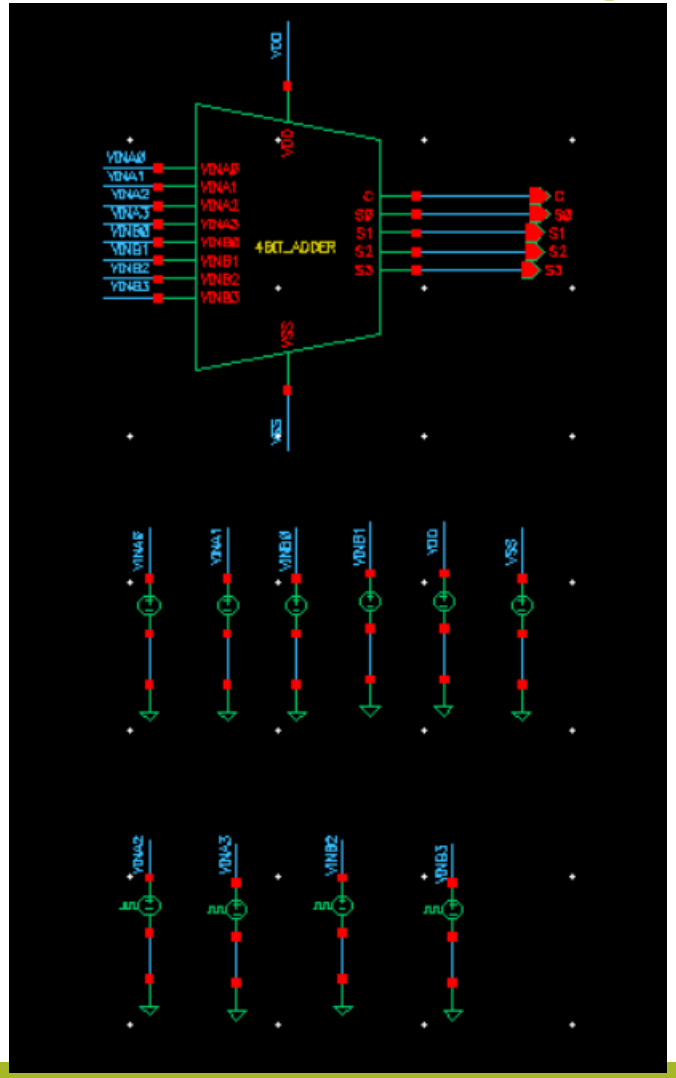
구현 방법

- Half Adder 1개와 Full Adder 3개로 4Bit Adder를 구성하였다.
- 구조가 간단하여 구현이 용이한 장점이 있다.
- Tr. 수
  - Half Adder
    - (Inverter) 3*2 + (2Nand) 4*4 = 22
  - Full Adder
    - (Inverter) 7*2 + (2Nand) 8*4 + (2Nor) 1*4 = 50

Schematic

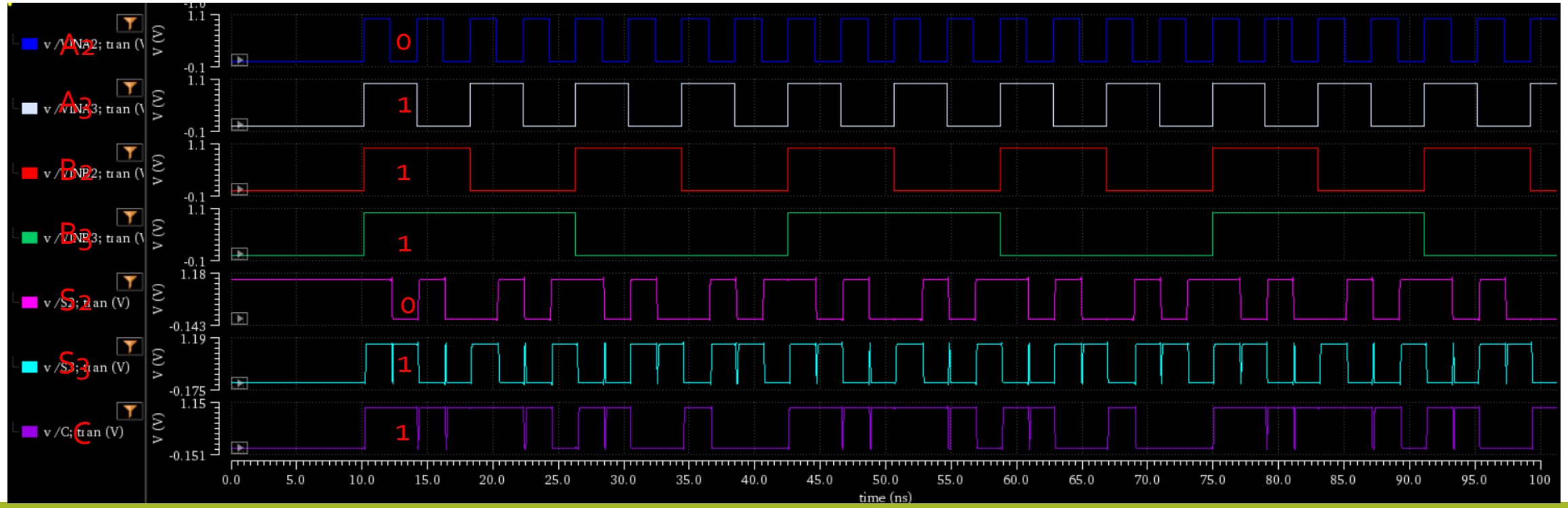

VDD
VSS
VINA
VINB
HA
HA_SUM
HA_COUT
SUMØ
VINC
VIND
FA
FA_SUM
FA_COUT
SUM1
VINE
VINF
SUM2
VING
VINH
SUM3
4BIT_ADDER_COUT

4Bit Adder simulation setup

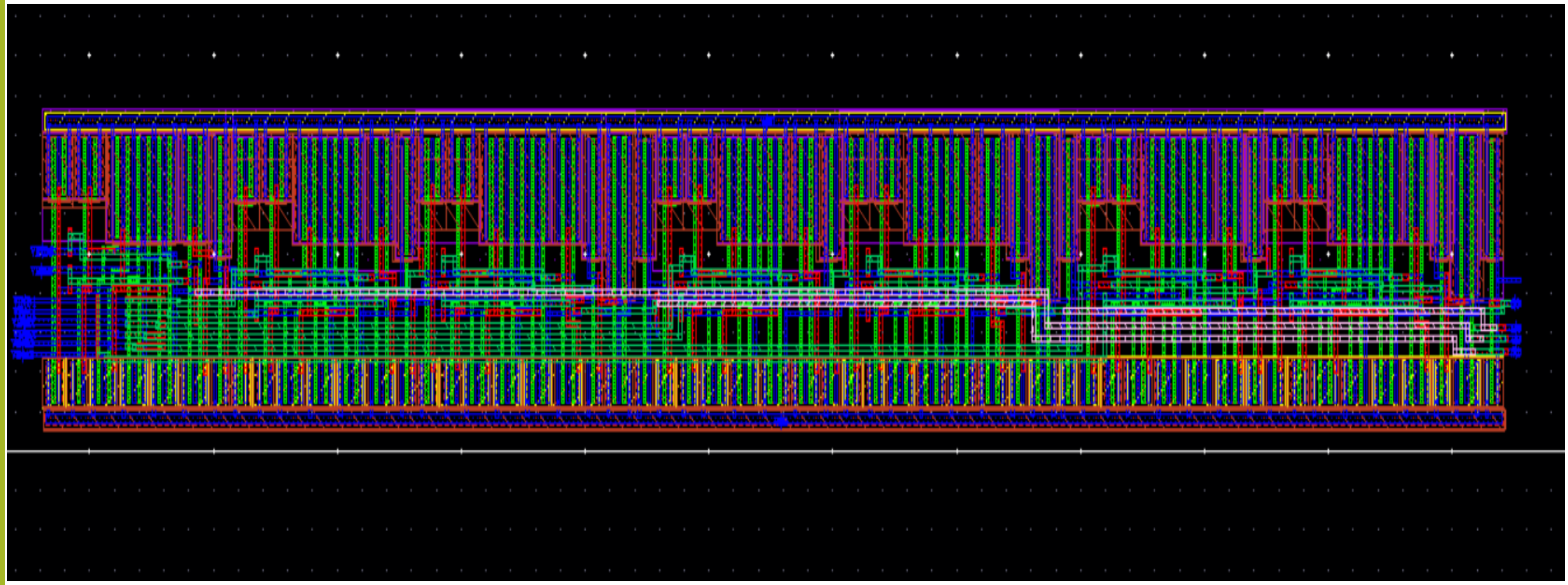


Wave Form

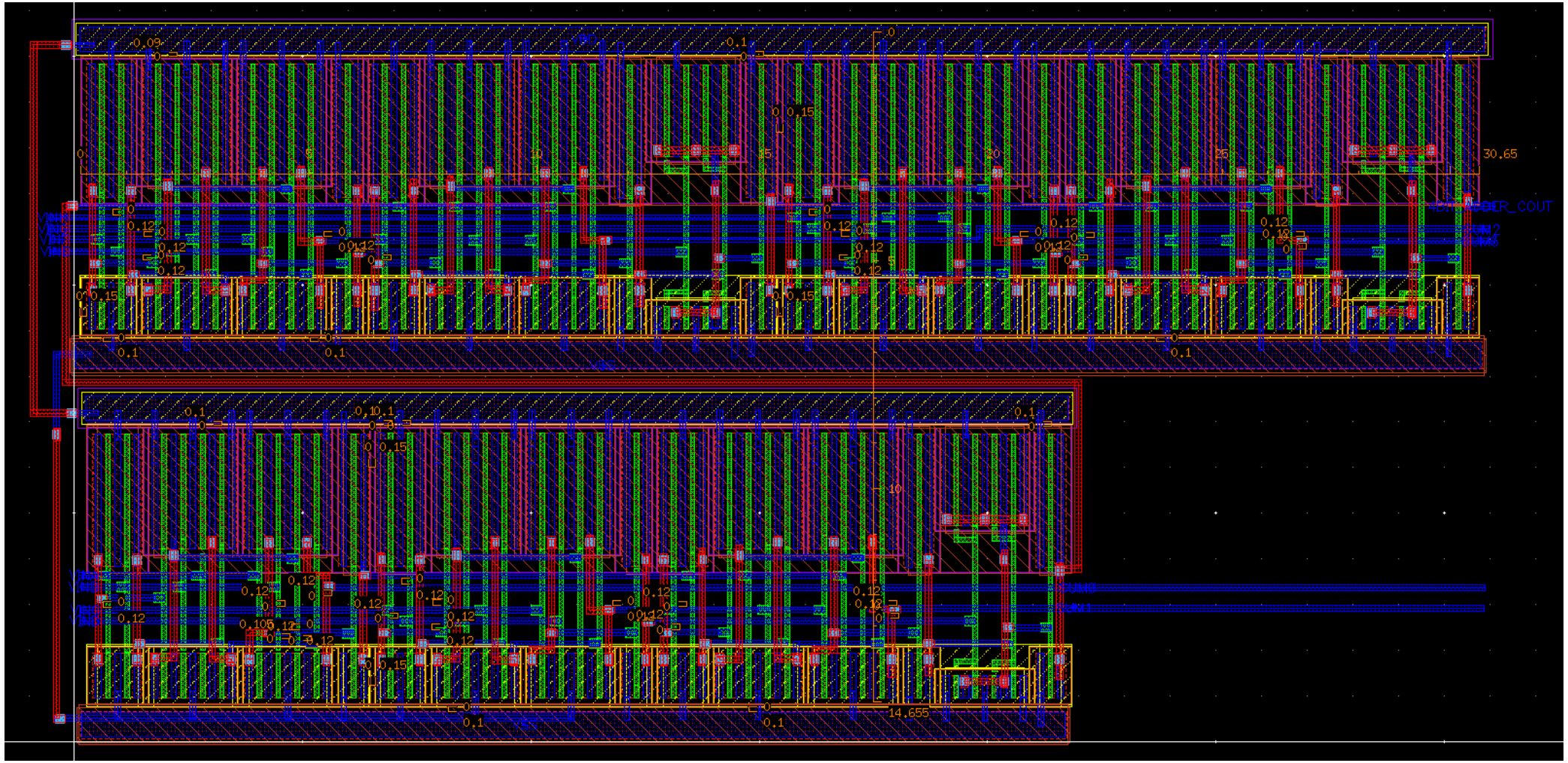
A0+B0 -> S0=1	A1+B1 -> S1 = 0 (C1=1)	A2+B2+(C1) -> S2=0 (C2=1)	A3+B3+(C2) -> S3=1 (C=1)



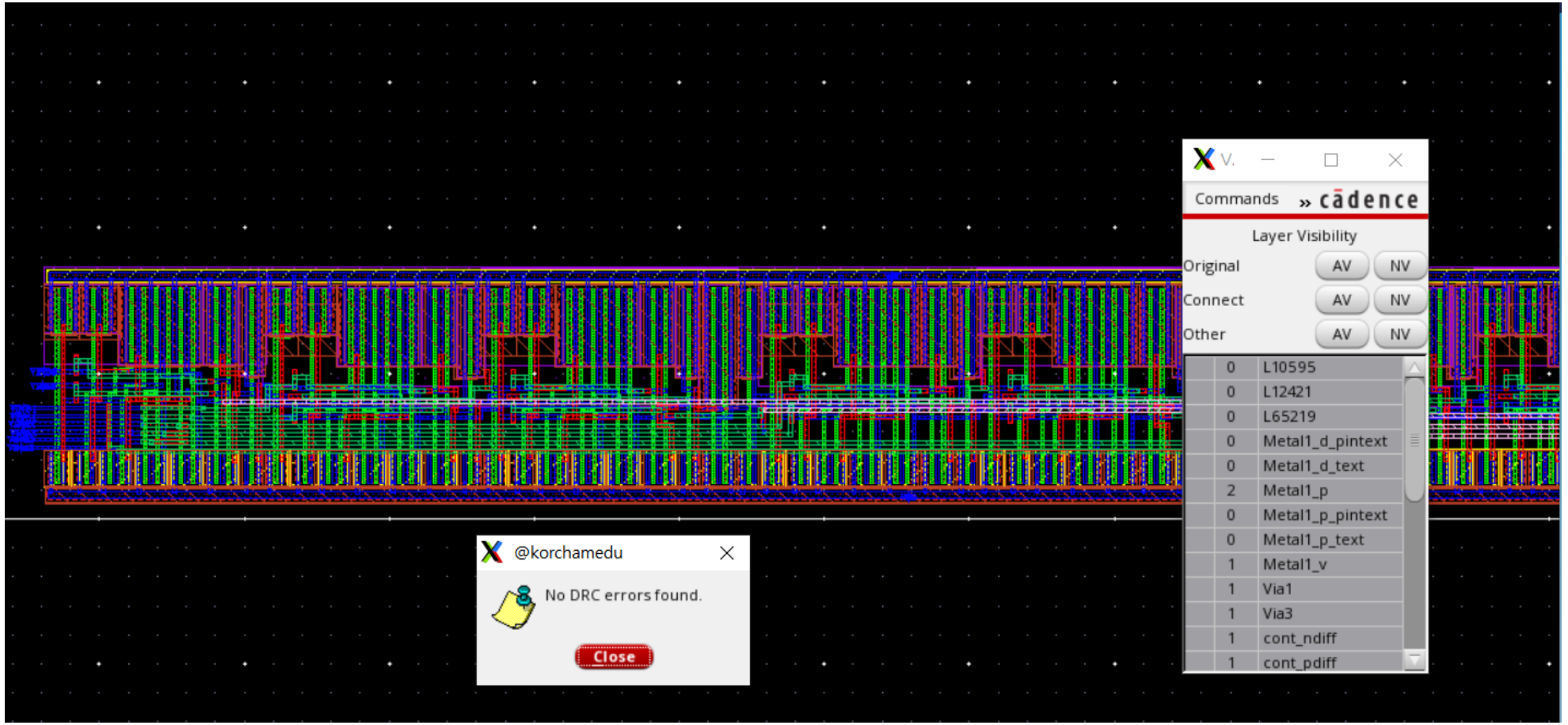
4Bit Adder (Layout)



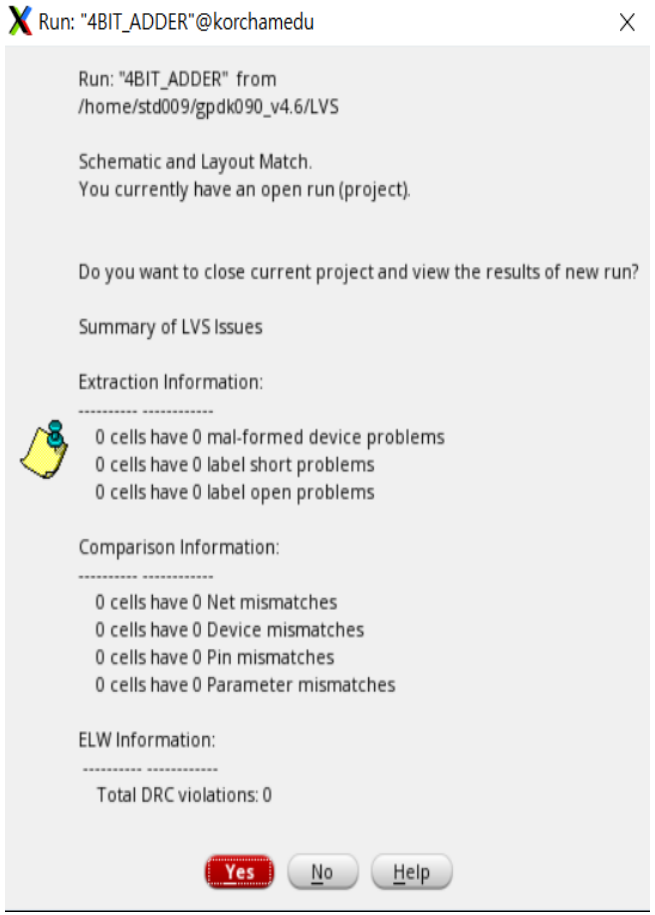
4Bit Adder (Layout)

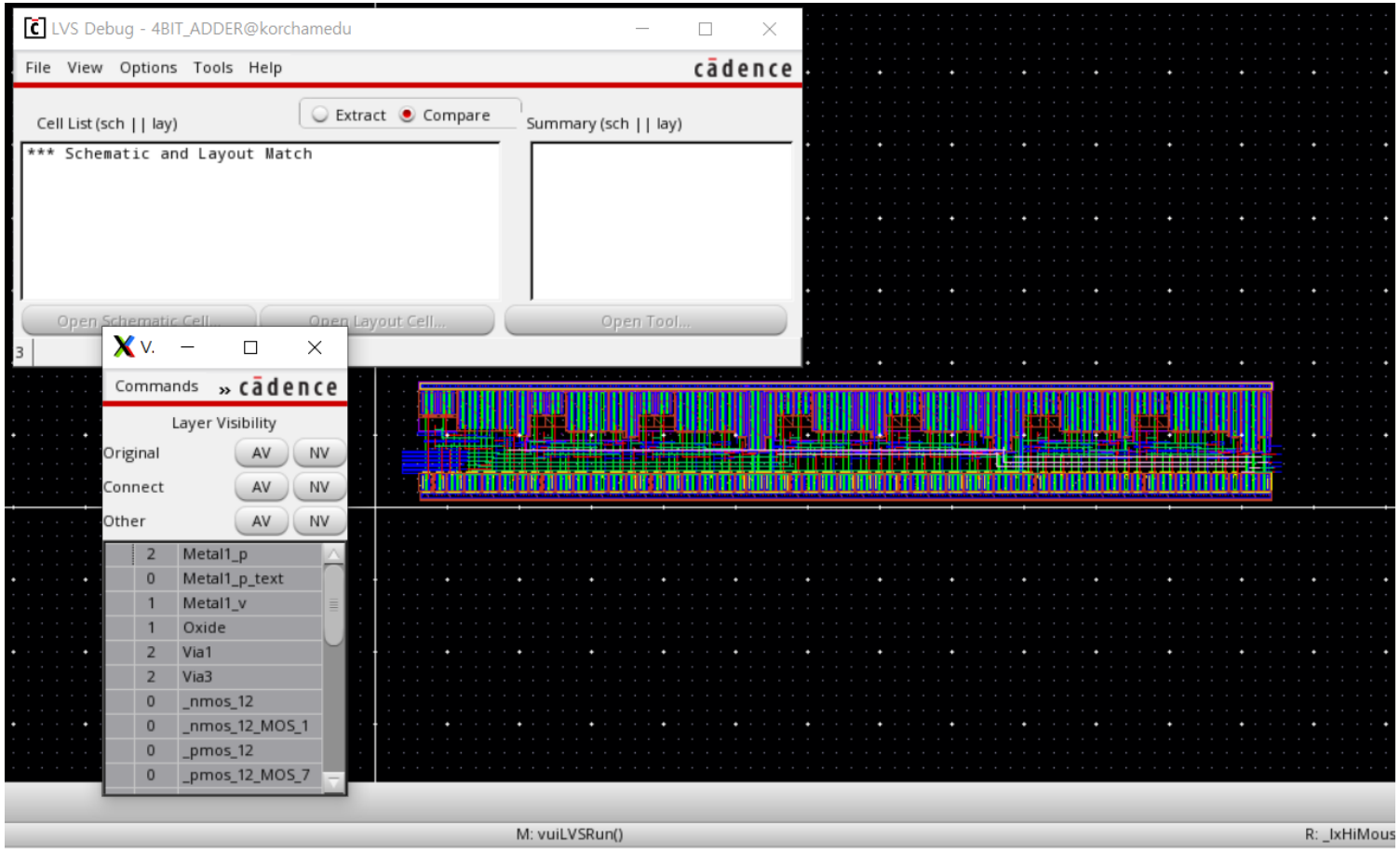


4Bit Adder (DRC)



4Bit Adder (LVS)





4Bit Adder Size

	4Bit Adder
가로	59.14
세로	8.165