Cadence
Full-Custom IC Design

Ph. D. ByoungJin Lee

CONTENTS

Step 1.

Introduction

Step 2.

Digital Circuit

(Logic Gate / MUX / Adder)

Step 3.

Analog Circuit

(CS / DIFF AMP)

Step 4.

Summary

1. INTRODUCTION

Course

Nineplus IT - Cadence® Full-Custom IC Designer

Tools

Cadence Virtuoso Schematic Editor / Layout Editor

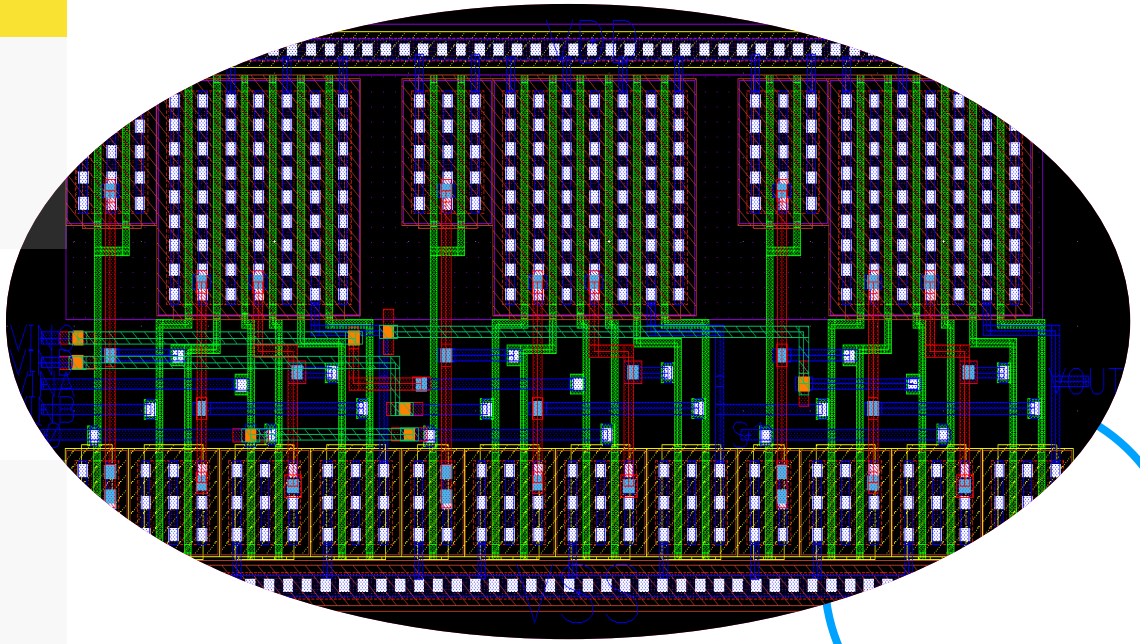
Cadence Virtuoso Spectre / ADE

Assura DRC / LVS

GPDK090

2. DIGITAL CIRCUIT

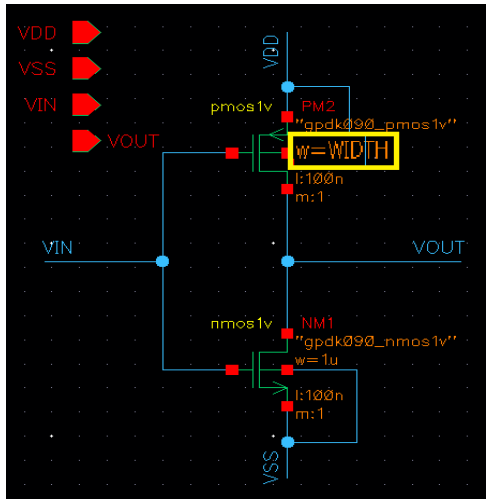
Logic Gate	Multiplexer (MUX)	Adder
NOT (Inverter)	2X1 MUX (Gate / Switch)	Half Adder
Switch (Transmission Gate)	4X1 MUX (Gate / Switch)	Full Adder
2~4 NAND / NOR	-	4-bit Adder

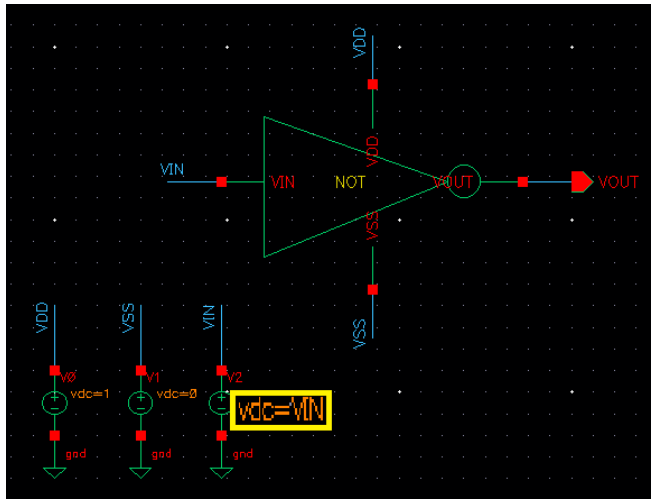


2-1. LOGIC GATE

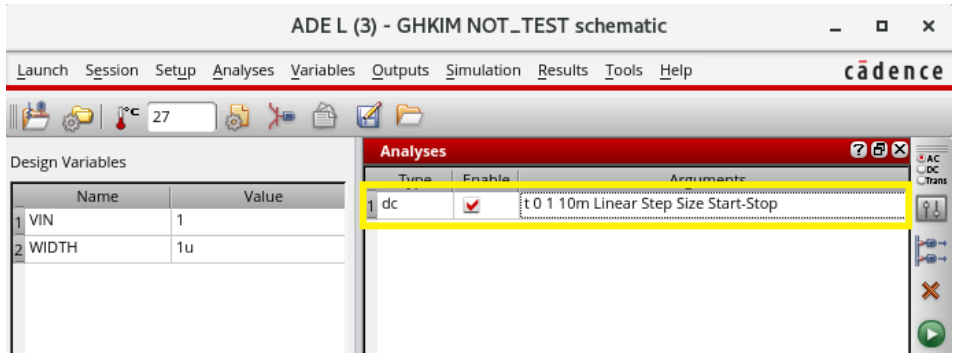
- Find the width of PMOS – NOT GATE

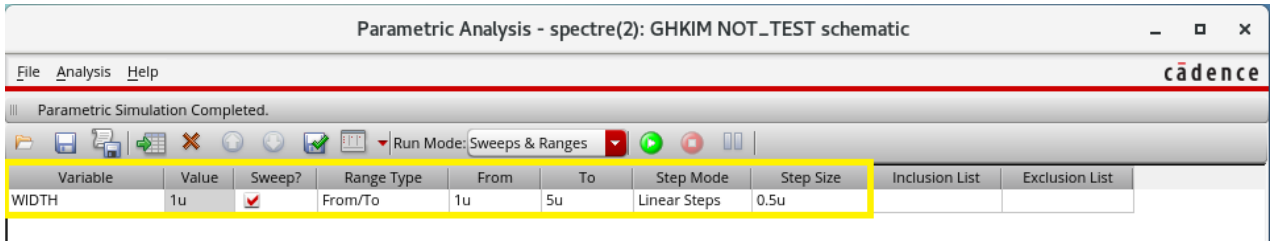
①





②

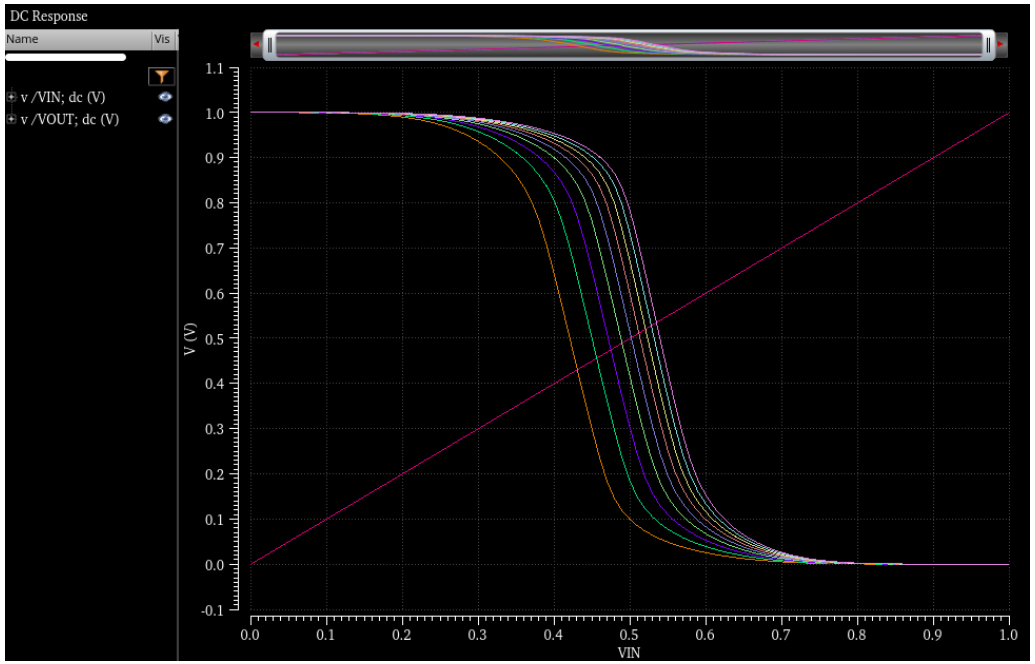


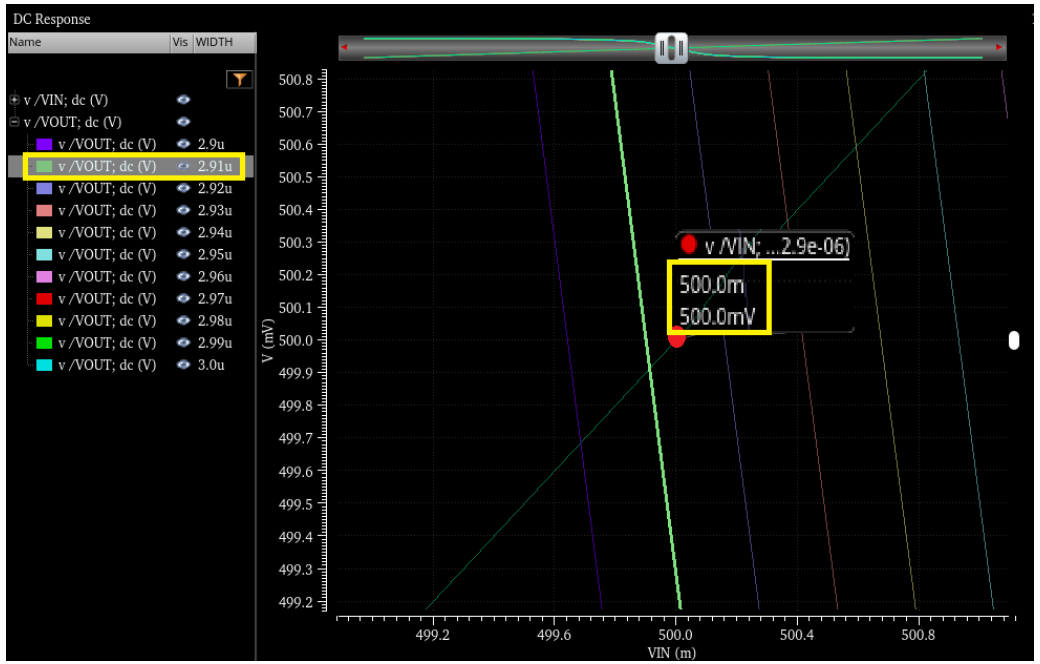


2-1. LOGIC GATE

- Find the width of PMOS – NOT GATE

③

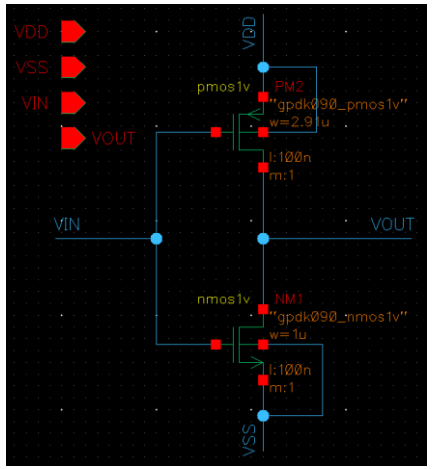


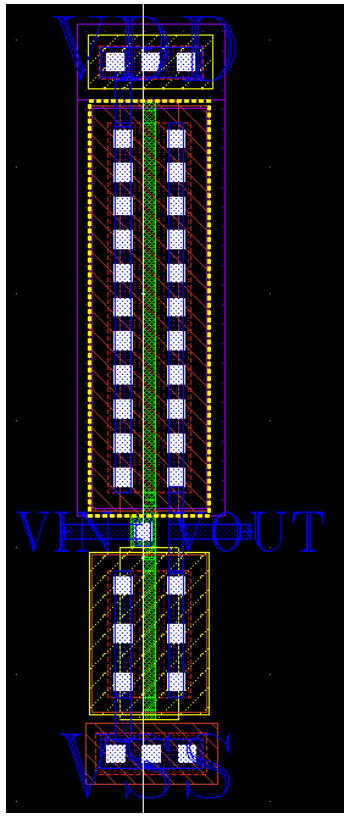


2-1. LOGIC GATE

❑ Mosfet Width (Length = 100nm)

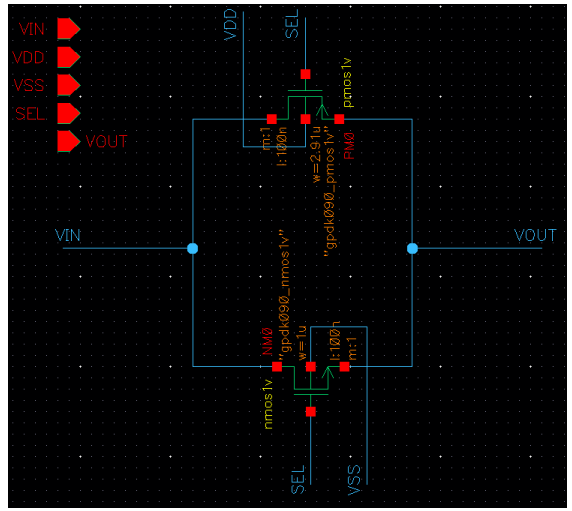
❖ NOT

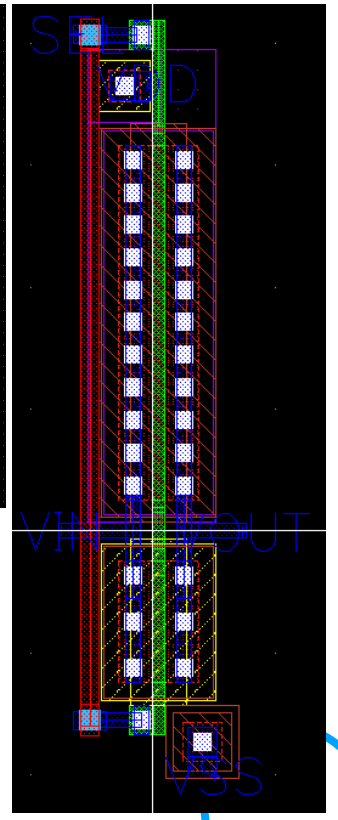




	NOT	SWITCH
NMOS	1um	1um
PMOS	2.91um	2.91um

❖ SWITCH

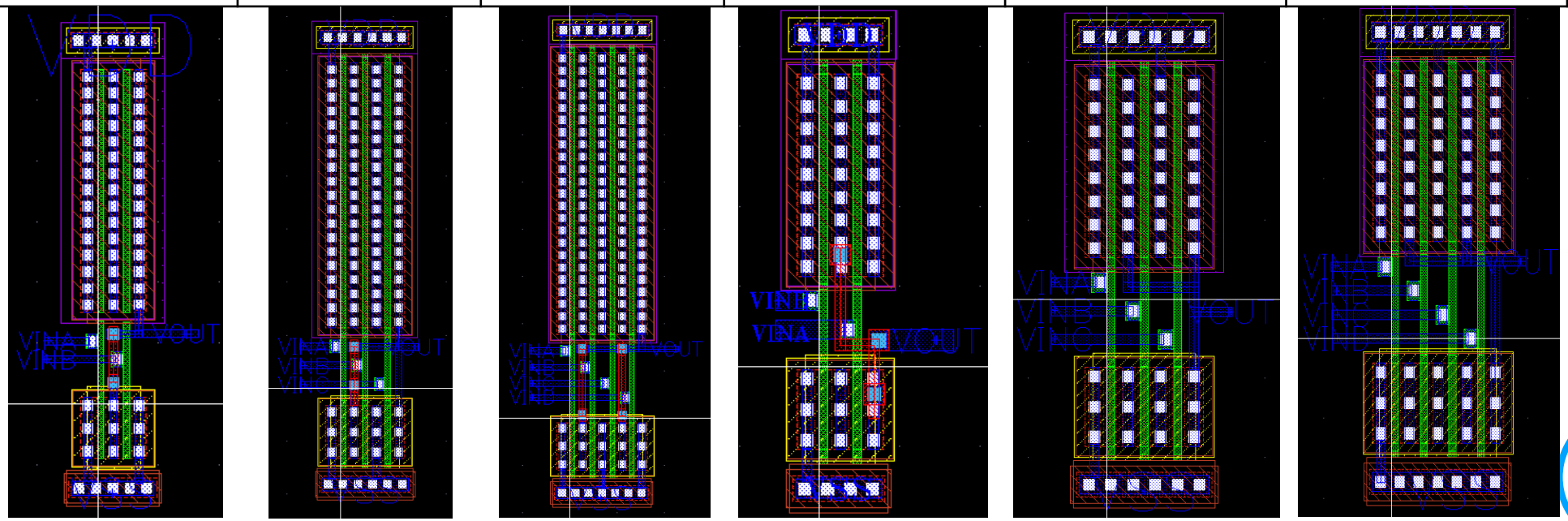




2-1. LOGIC GATE

- Mosfet Width (Length = 100nm)

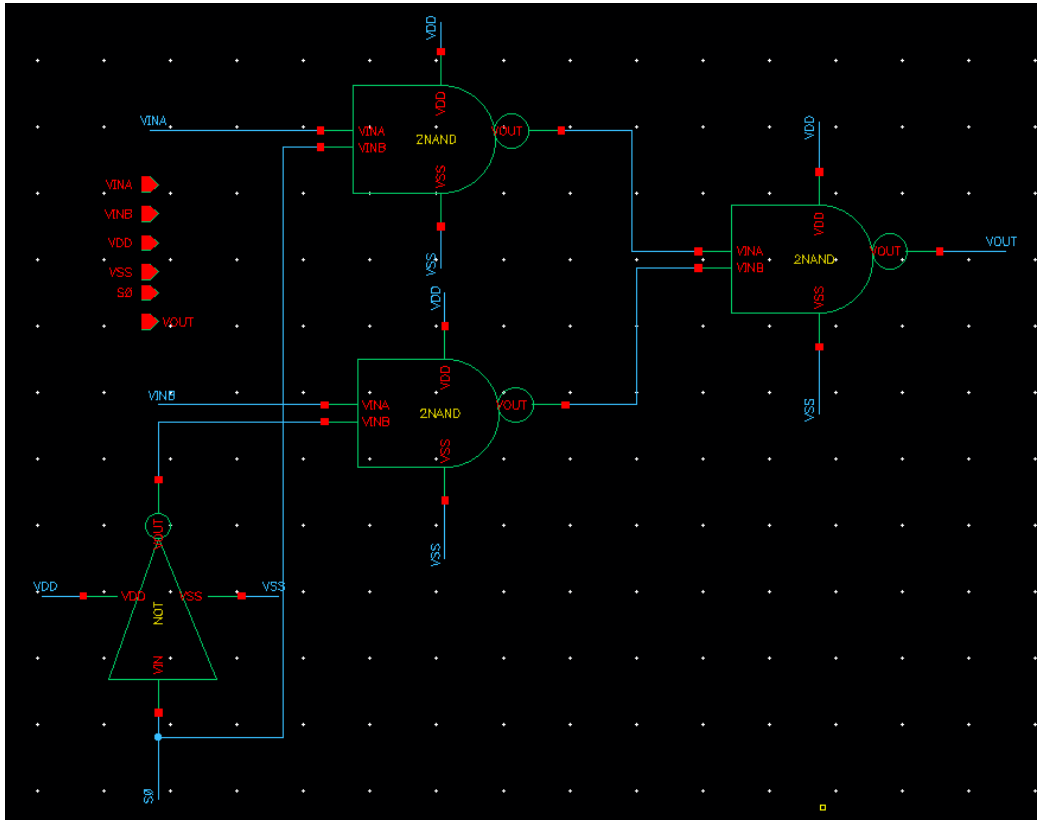
	2NOR	3NOR	4NOR	2NAND	3NAND	4NAND
NMOS	1um	1um	1um	1um	1um	1um
PMOS	3.99um	5um	5.96um	2.53um	2.31um	2.14um



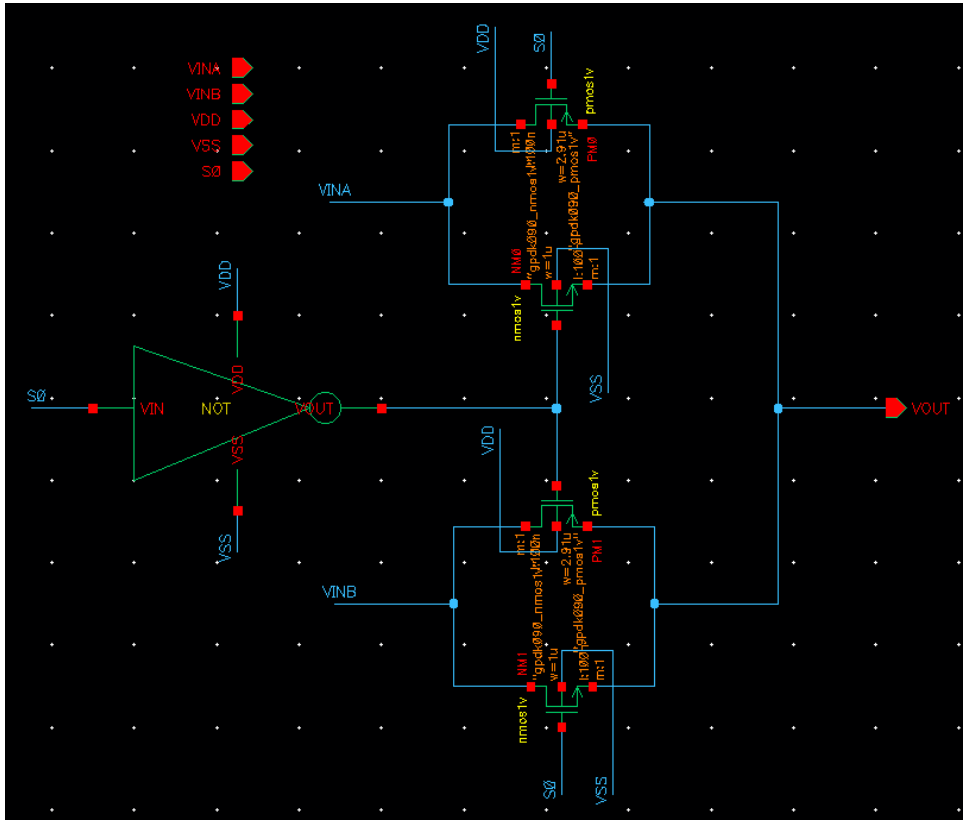
2-2. MULTIPLEXER (MUX)

2X1 MUX

2X1 MUX (Logic Gate)

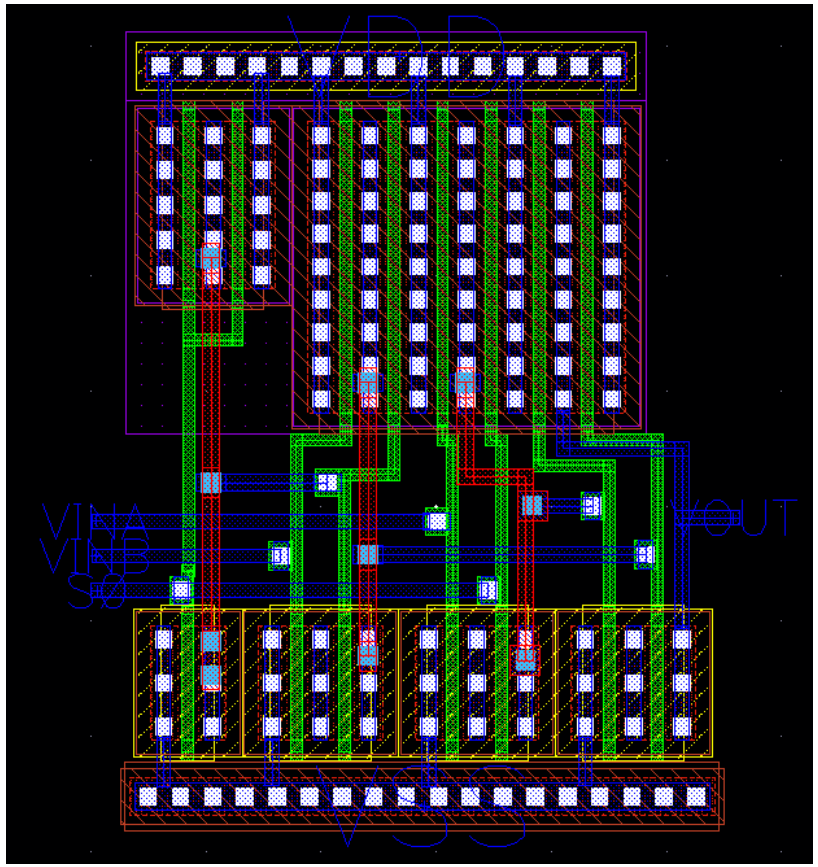


2X1 MUX (Switch)

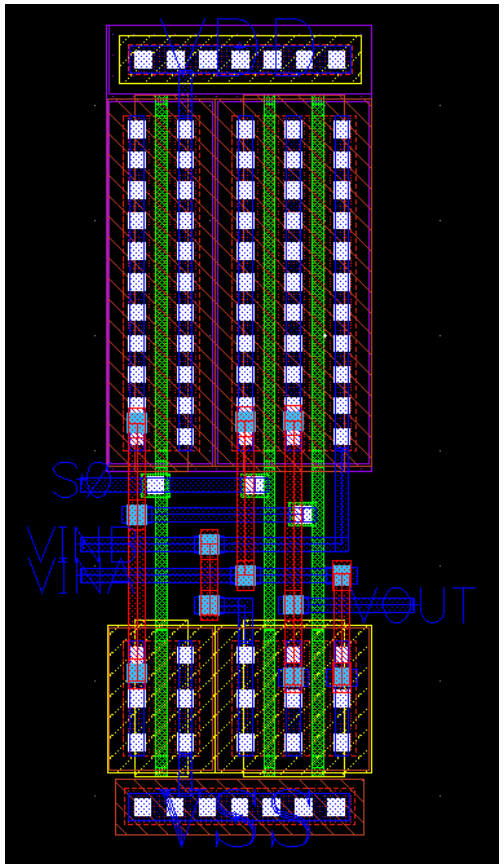


2-2. MULTIPLEXER (MUX)

❖ 2X1 MUX (Logic Gate)



❖ 2X1 MUX (Switch)

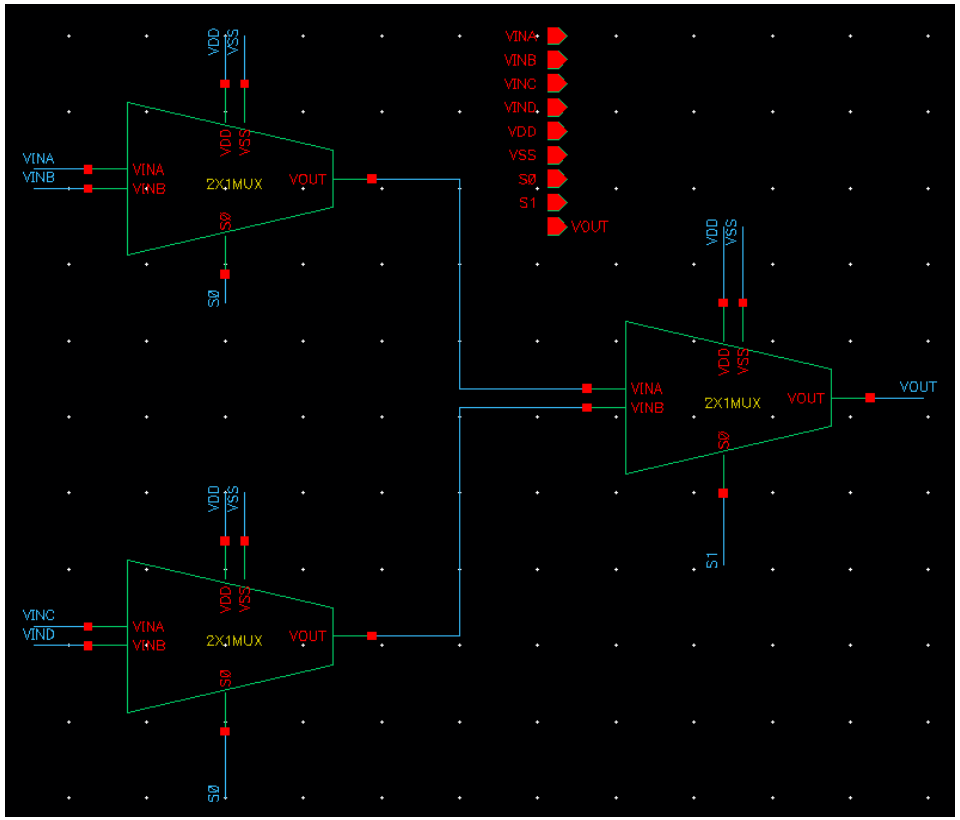


❖ 비교	2X1 MUX (LOGIC GATE)	2X1 MUX (SWITCH)
가로	5.02 nm	2.305 nm
세로	6.945 nm	7.035 nm
TR 개수	14	6

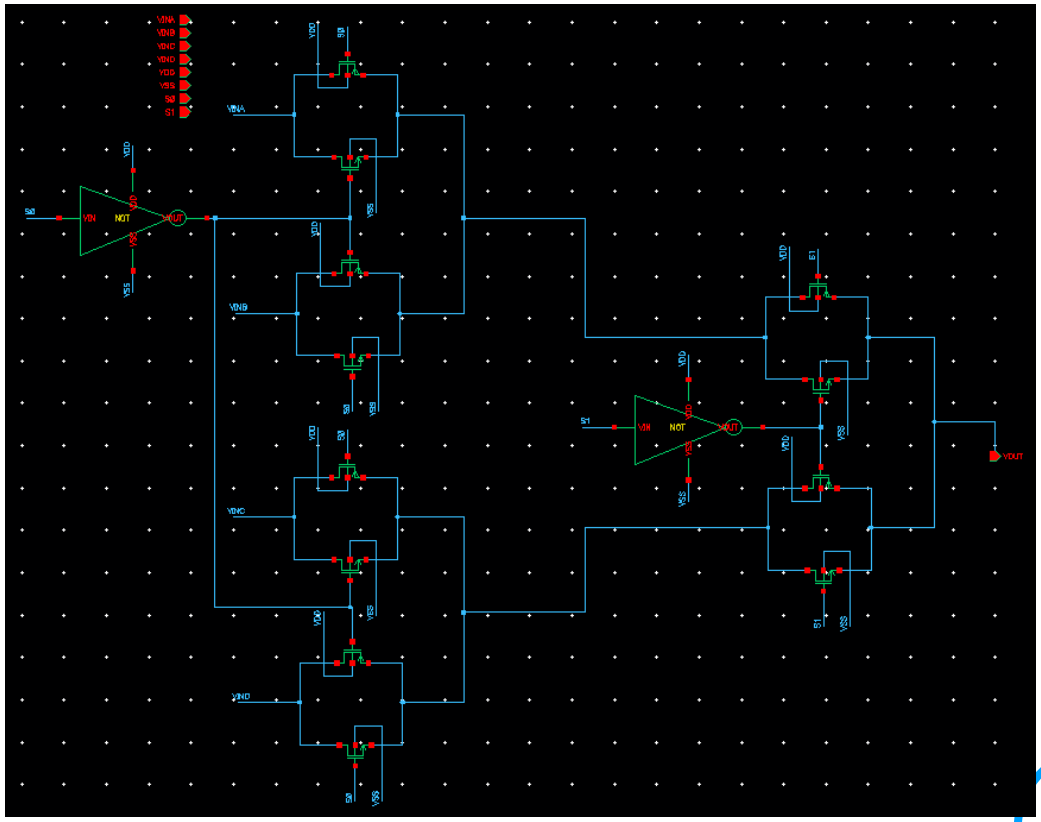
2-2. MULTIPLEXER (MUX)

4X1 MUX

4X1 MUX (Logic Gate)

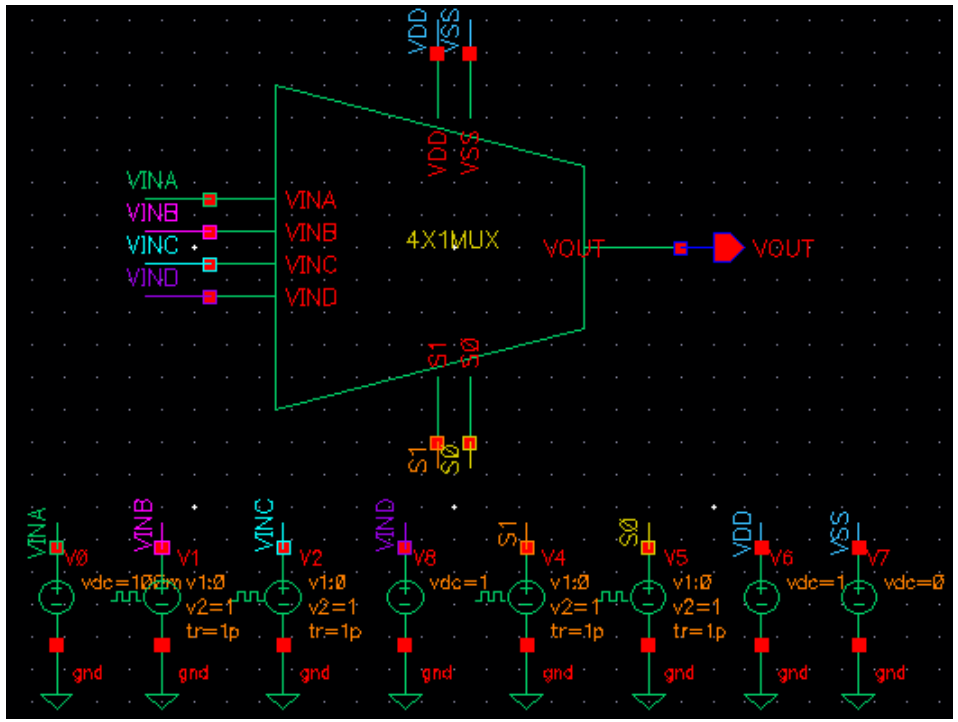


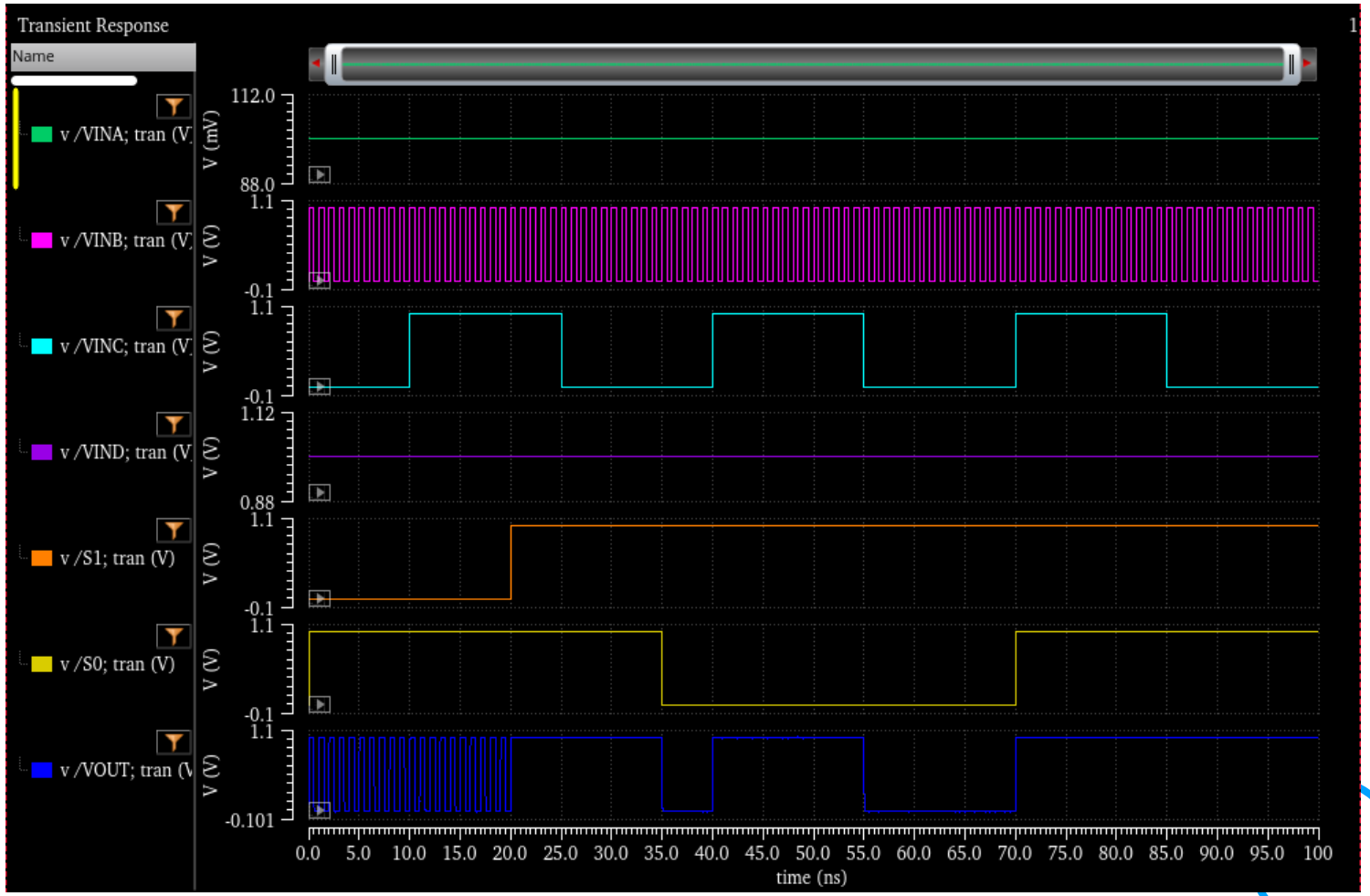
4X1 MUX (Switch)



2-2. MULTIPLEXER (MUX)

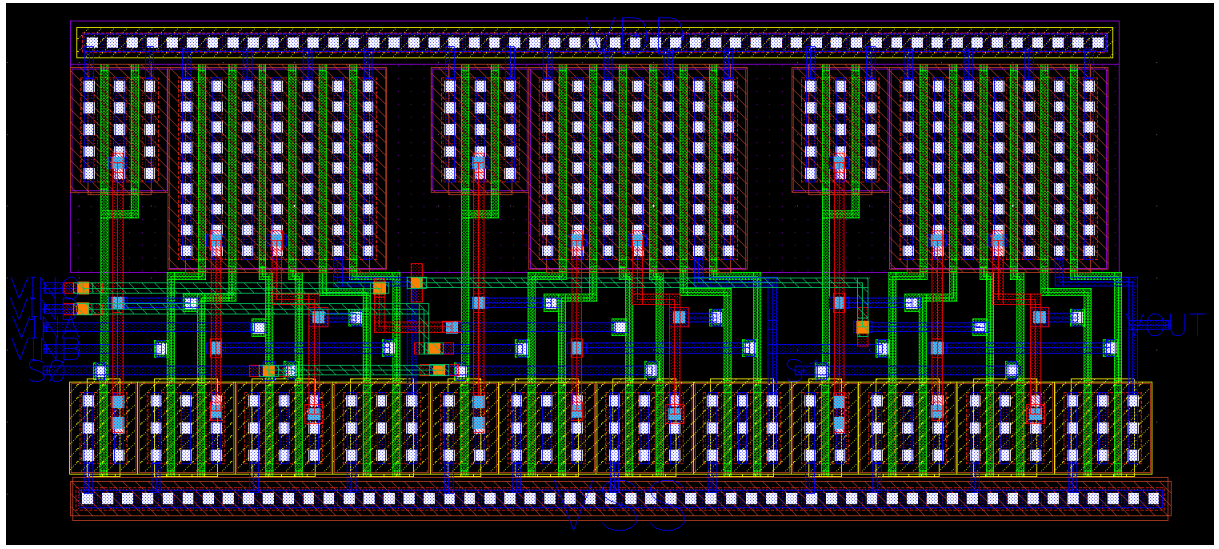
- 4X1 MUX Simulation



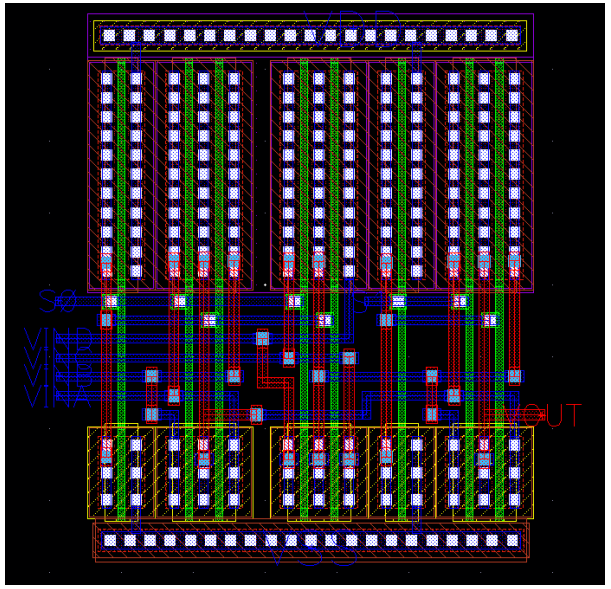


2-2. MULTIPLEXER (MUX)

❖ 4X1 MUX (Logic Gate)



❖ 4X1 MUX (Switch)



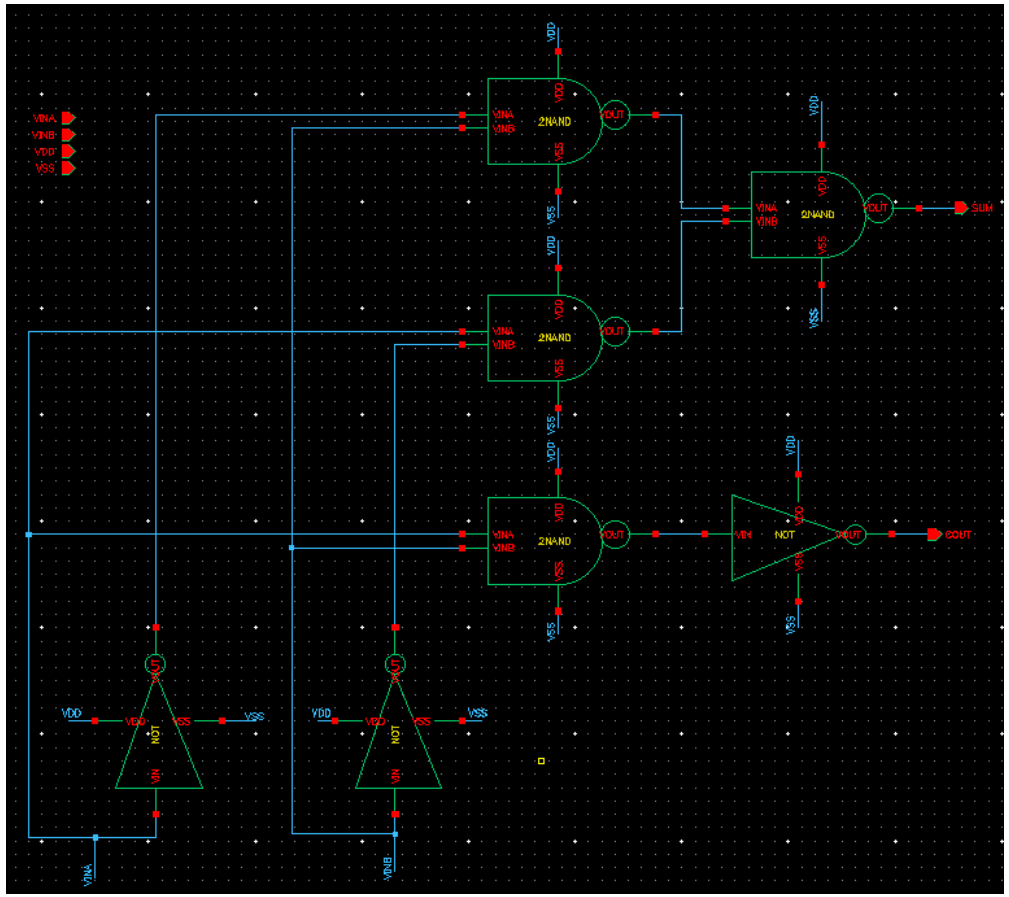
❖ 비교

	4X1 MUX (LOGIC GATE)	4X1 MUX (SWITCH)
가로	15.06 nm	6.2 nm
세로	6.945 nm	7.62 nm
TR 개수	42	16

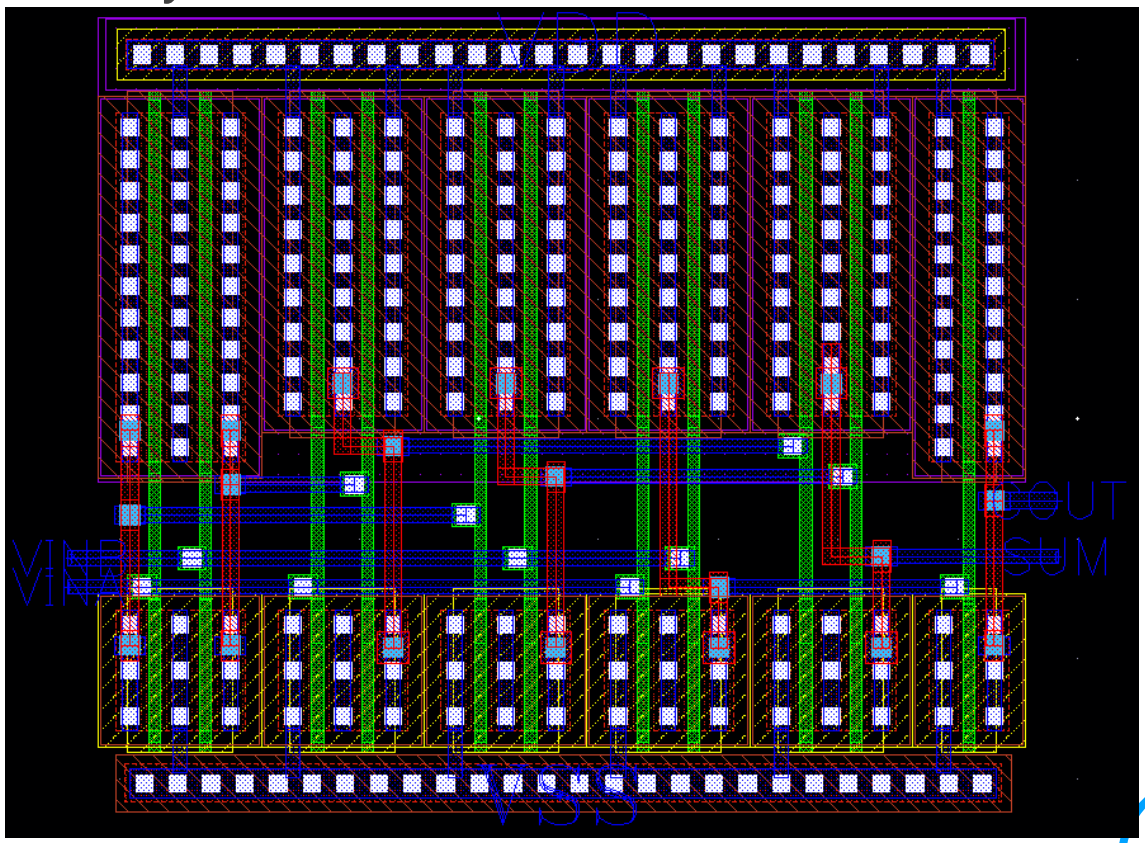
2-3. ADDER

Half Adder

Schematic



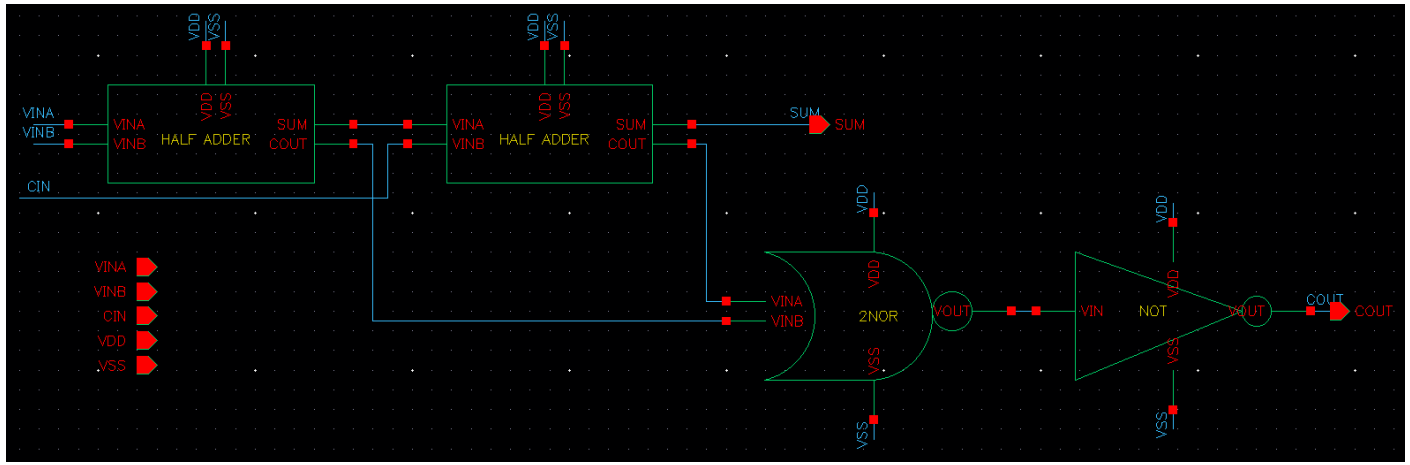
Layout



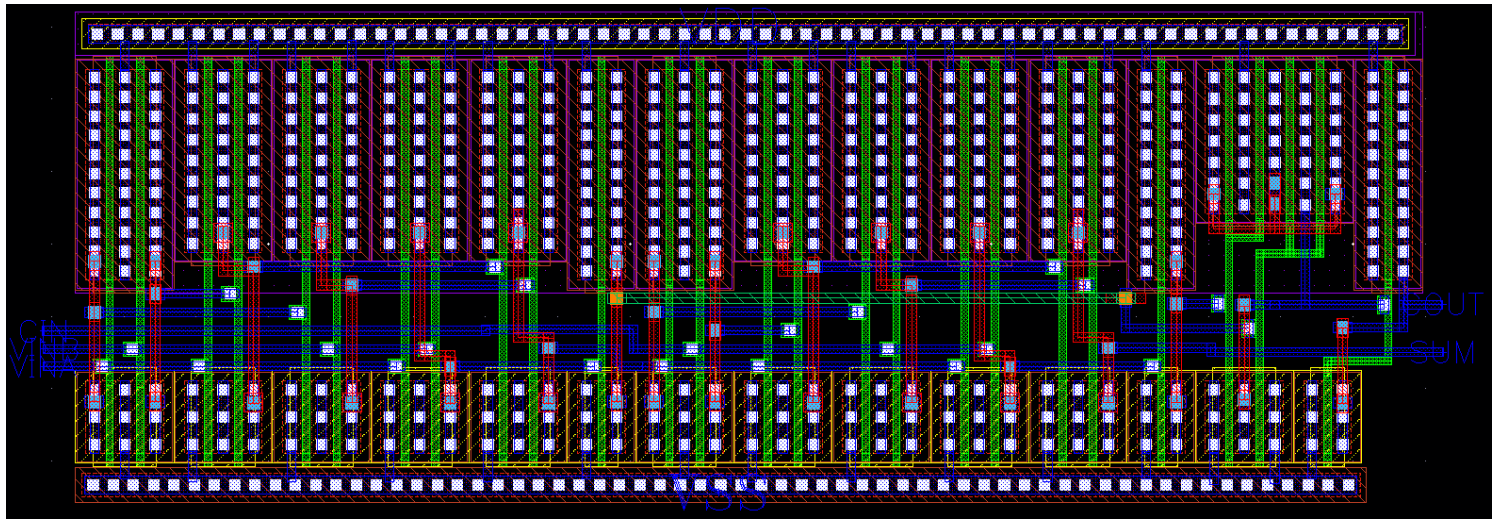
2-3. ADDER

Full Adder

Schematic



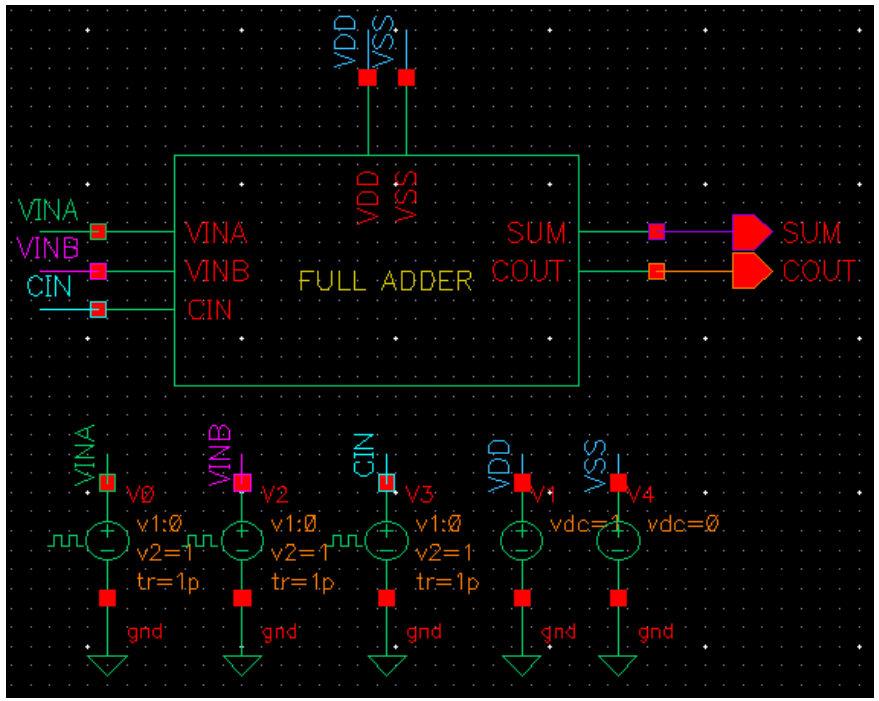
Layout

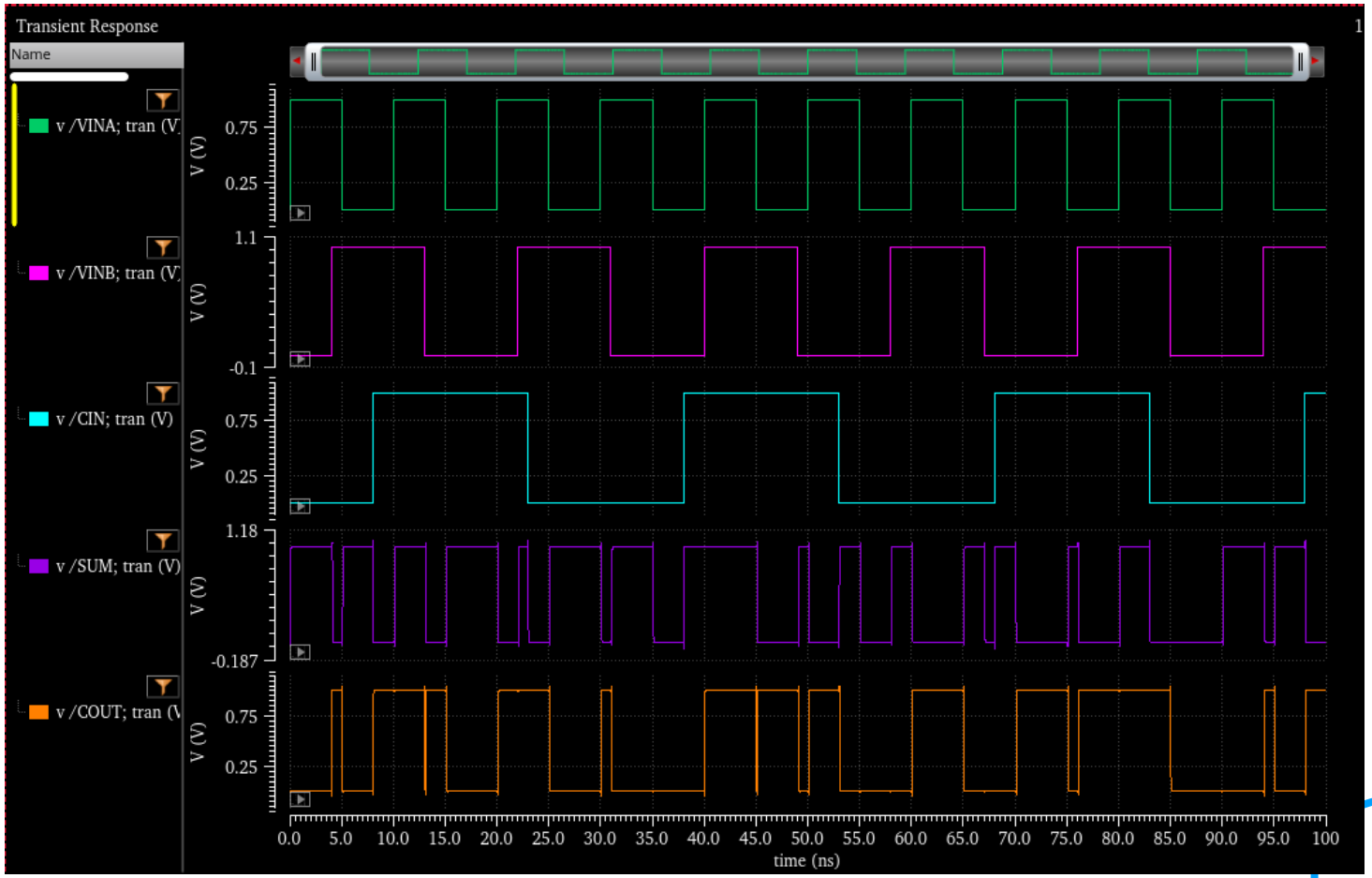


2-3. ADDER

Full Adder

Full Adder Simulation

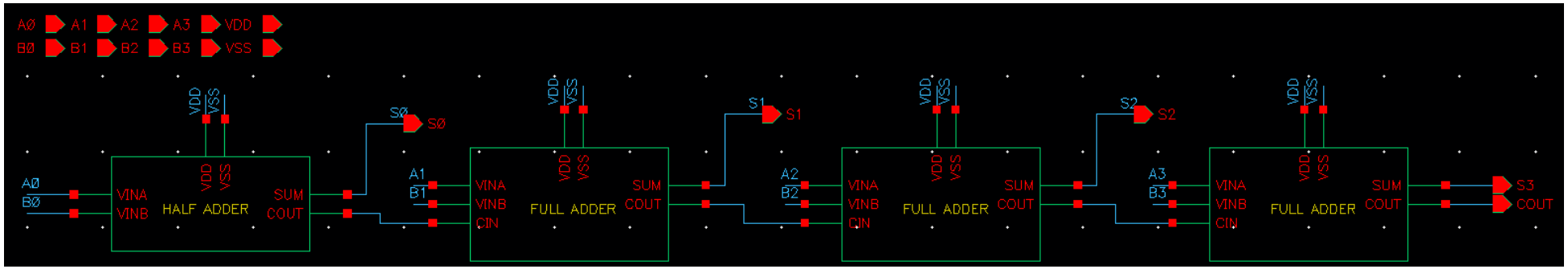




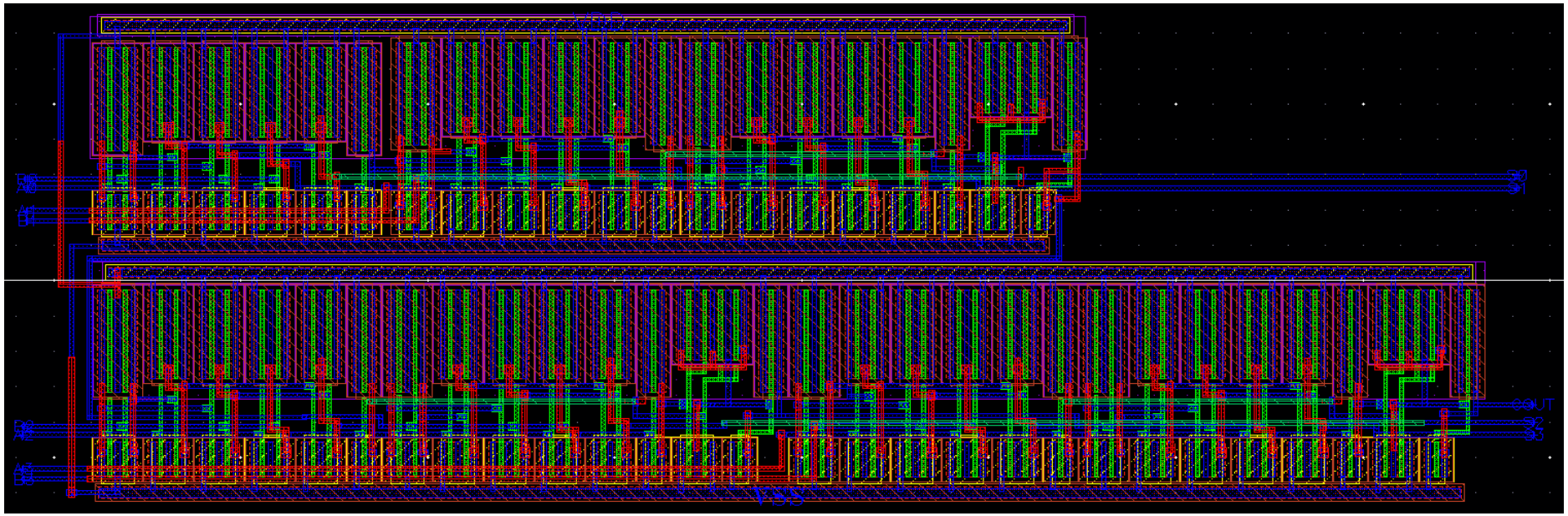
2-3. ADDER

4-Bit Adder

- Schematic



- Layout

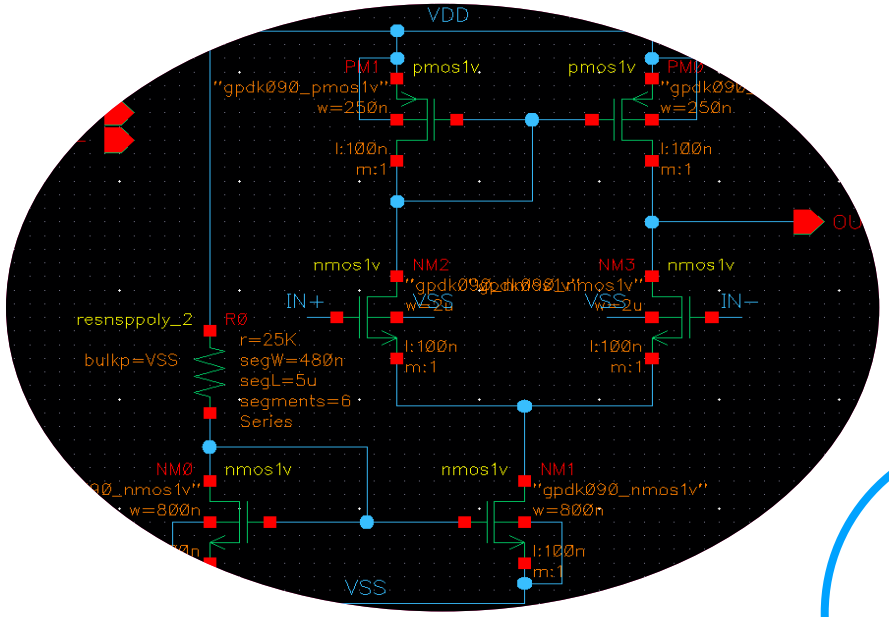


3. ANALOG CIRCUIT

Amplifier

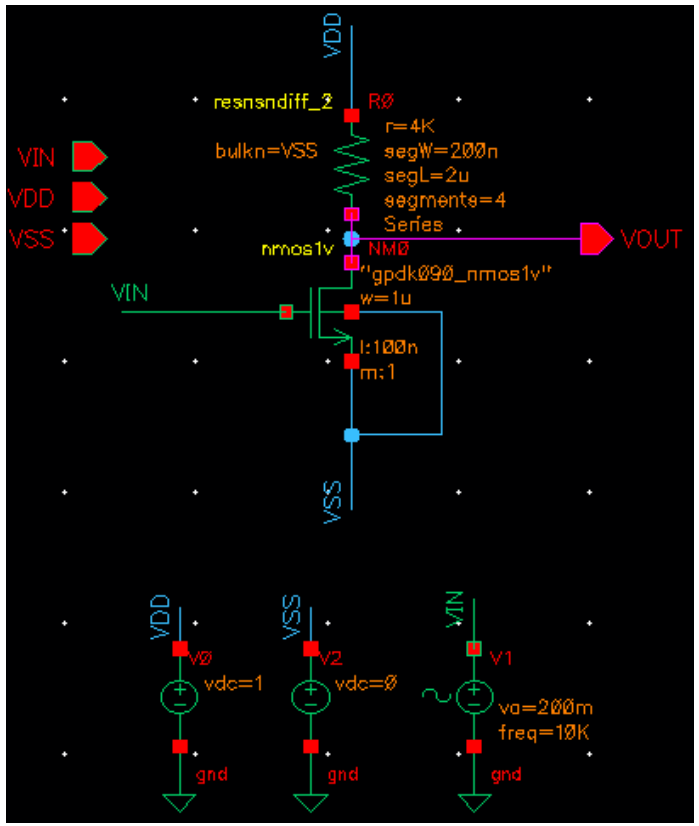
Common Source (CS) Amplifier

Differential Amplifier

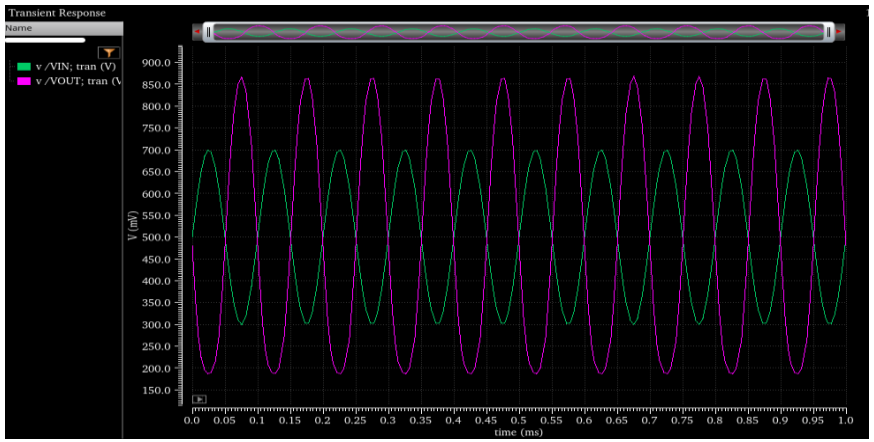


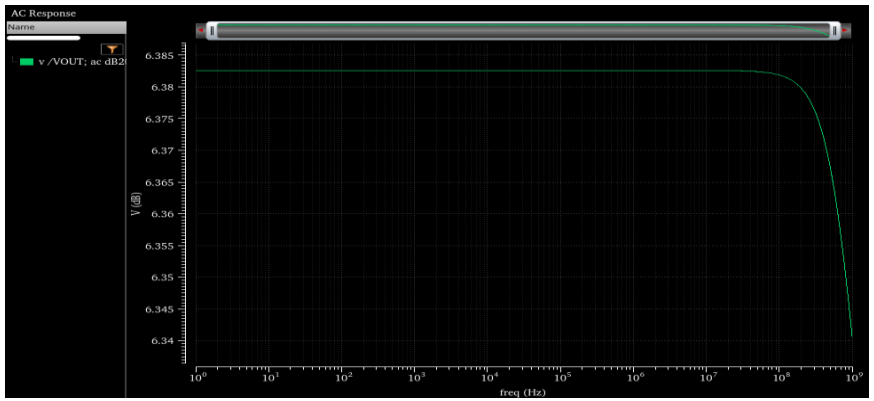
3-1. CS AMPLIFIER

Schematic

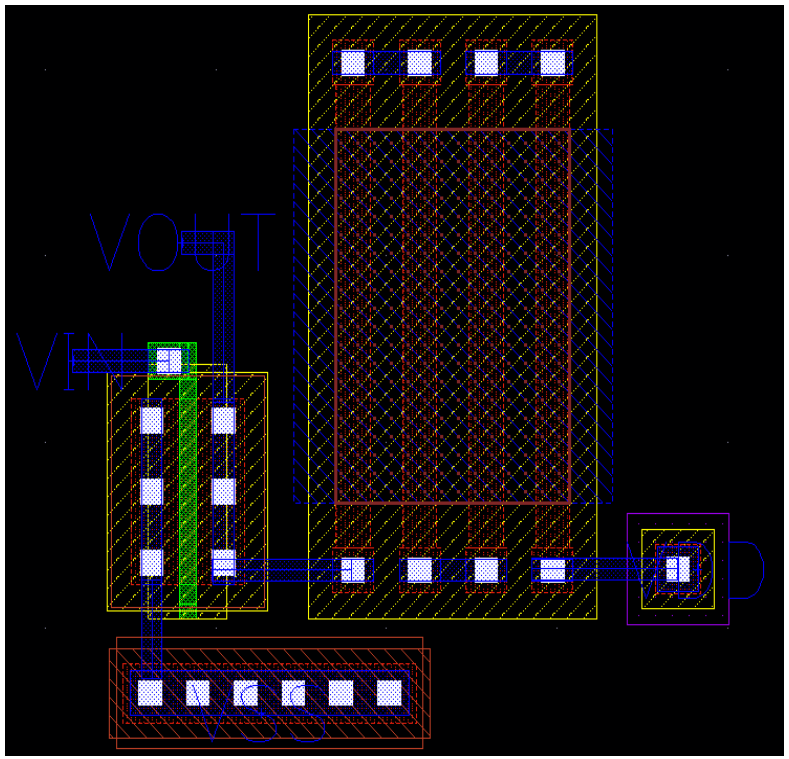


Simulation



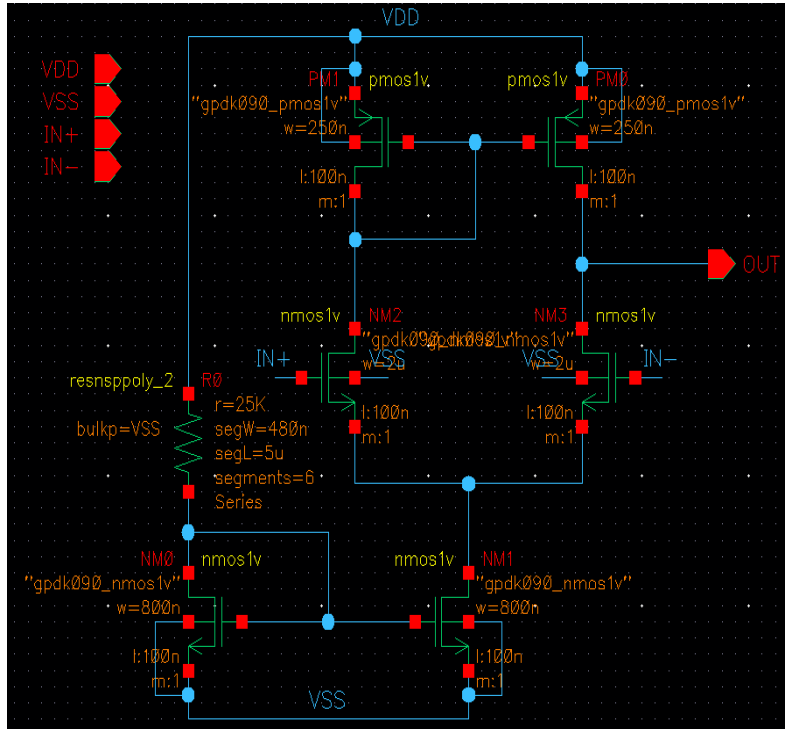


Layout

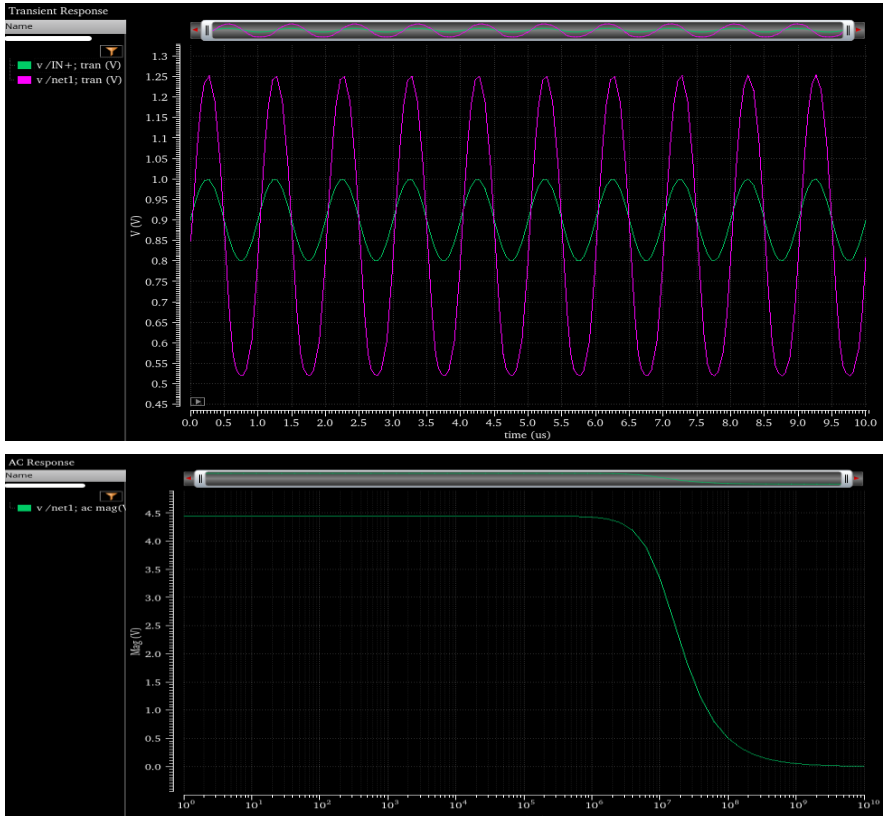


3-2. DIFFERENTIAL AMPLIFIER

Schematic



Simulation



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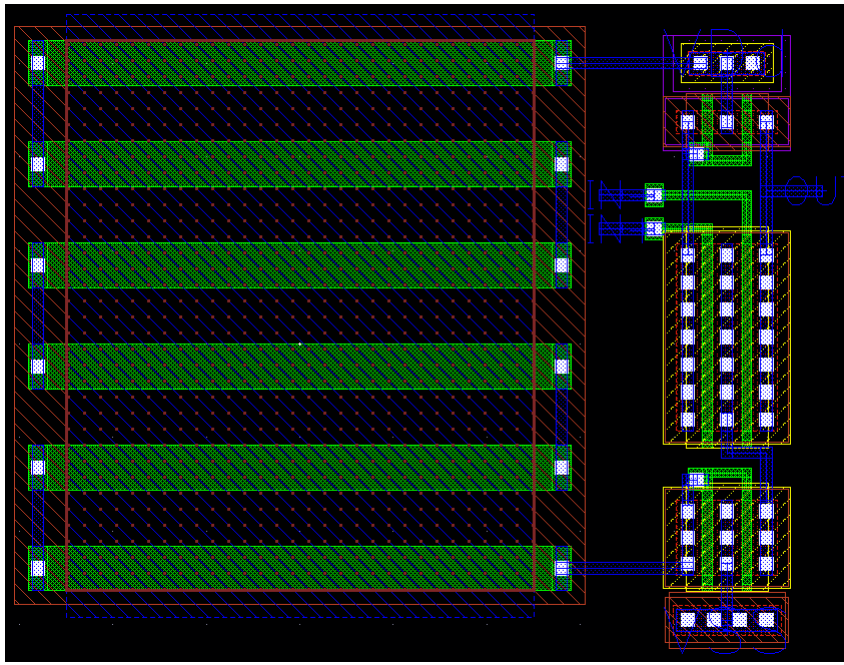

SUMMARY

- Schematic and Layout flow
- How to reduce the size of circuit
- How to reduce the number of TR

CONTACT

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