HALF_ADDER

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순서

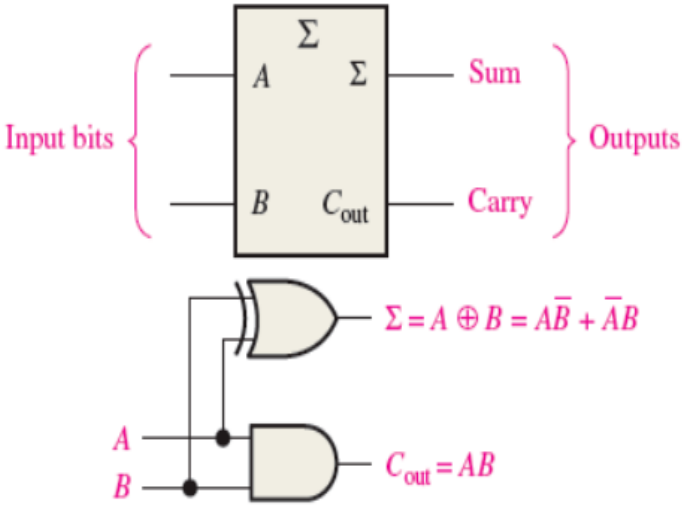
- Half_Adder
- Circuit design
- Schematic
- Circuit simulation
- Layout
- DRC, LVS

Half_Adder

Half-adder truth table.

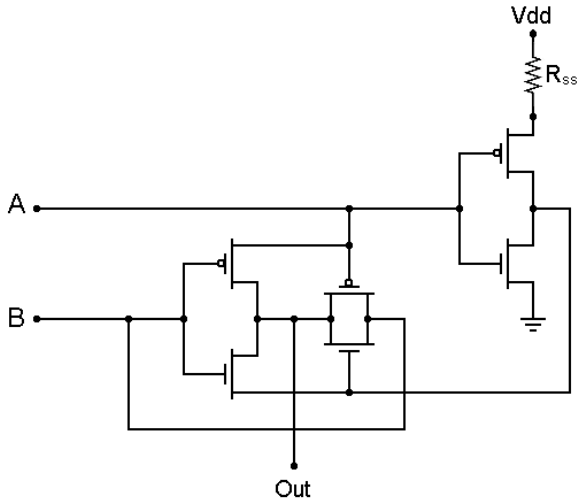
A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Σ = sum
C_{out} = output carry
A and B = input variables (operands)

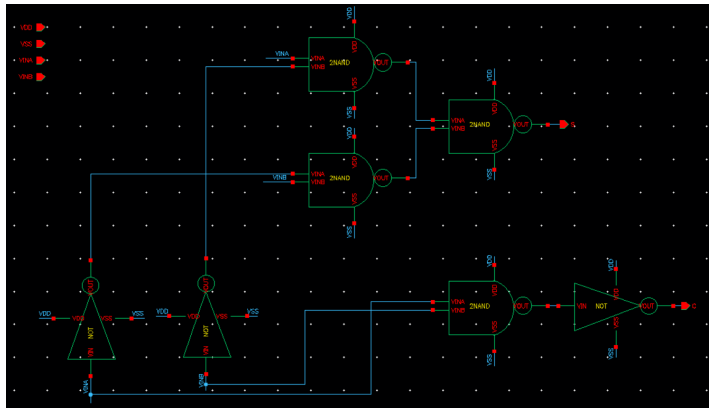


입력 A, B에 따라 Sum, Carry값이 변화하는 가산기

구현방법

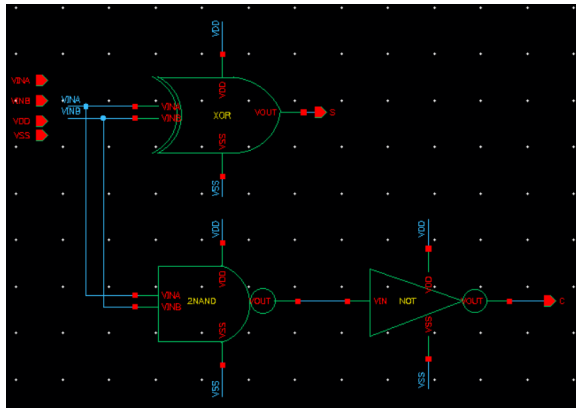


- XOR 게이트를 사용하여 크기를 줄일 수 있다.
  - XOR 사용 안했을 때



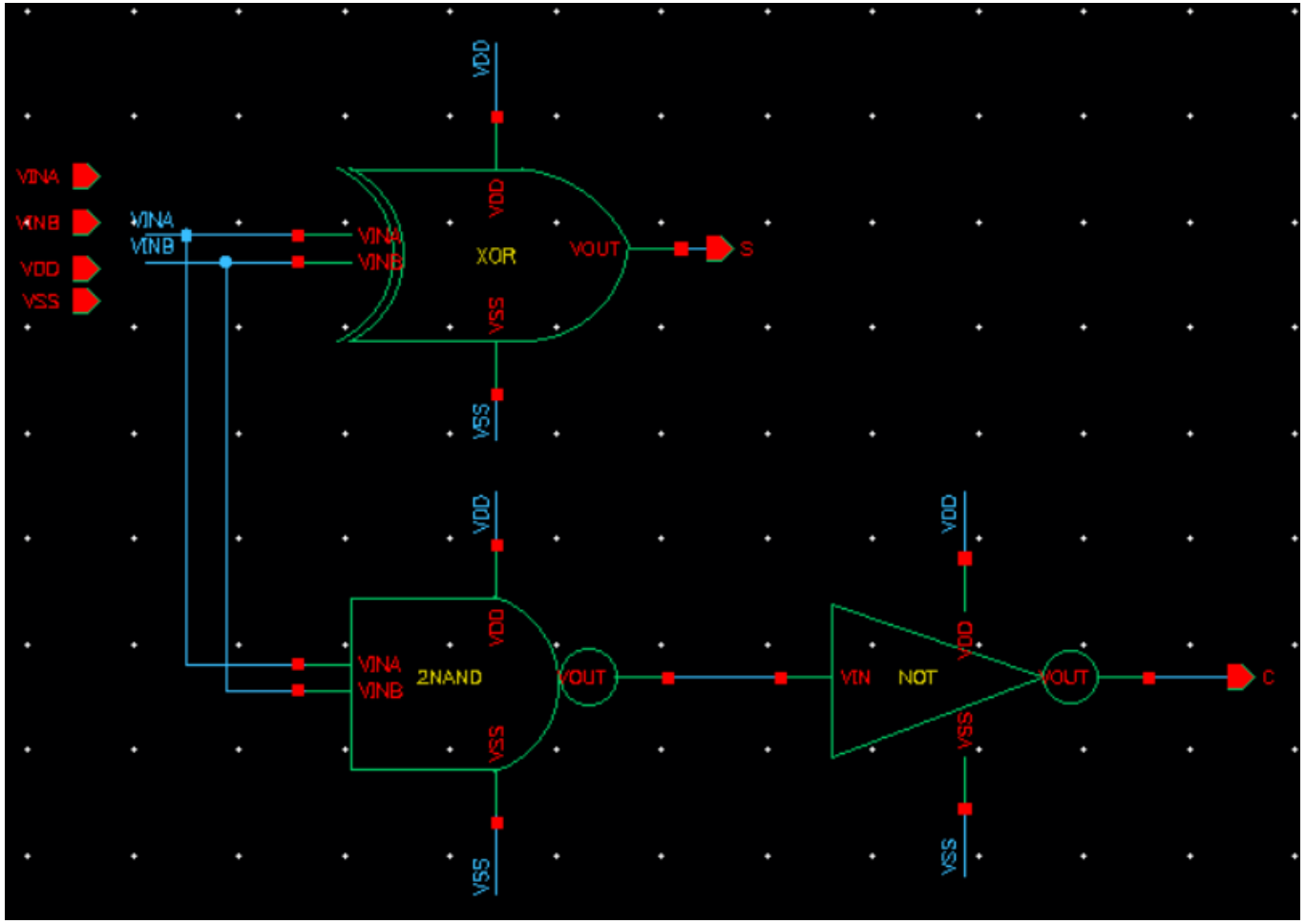
(Inverter) 2 * 3 + (2NAND) 4 * 4
= 22

  - XOR 사용 했을 때

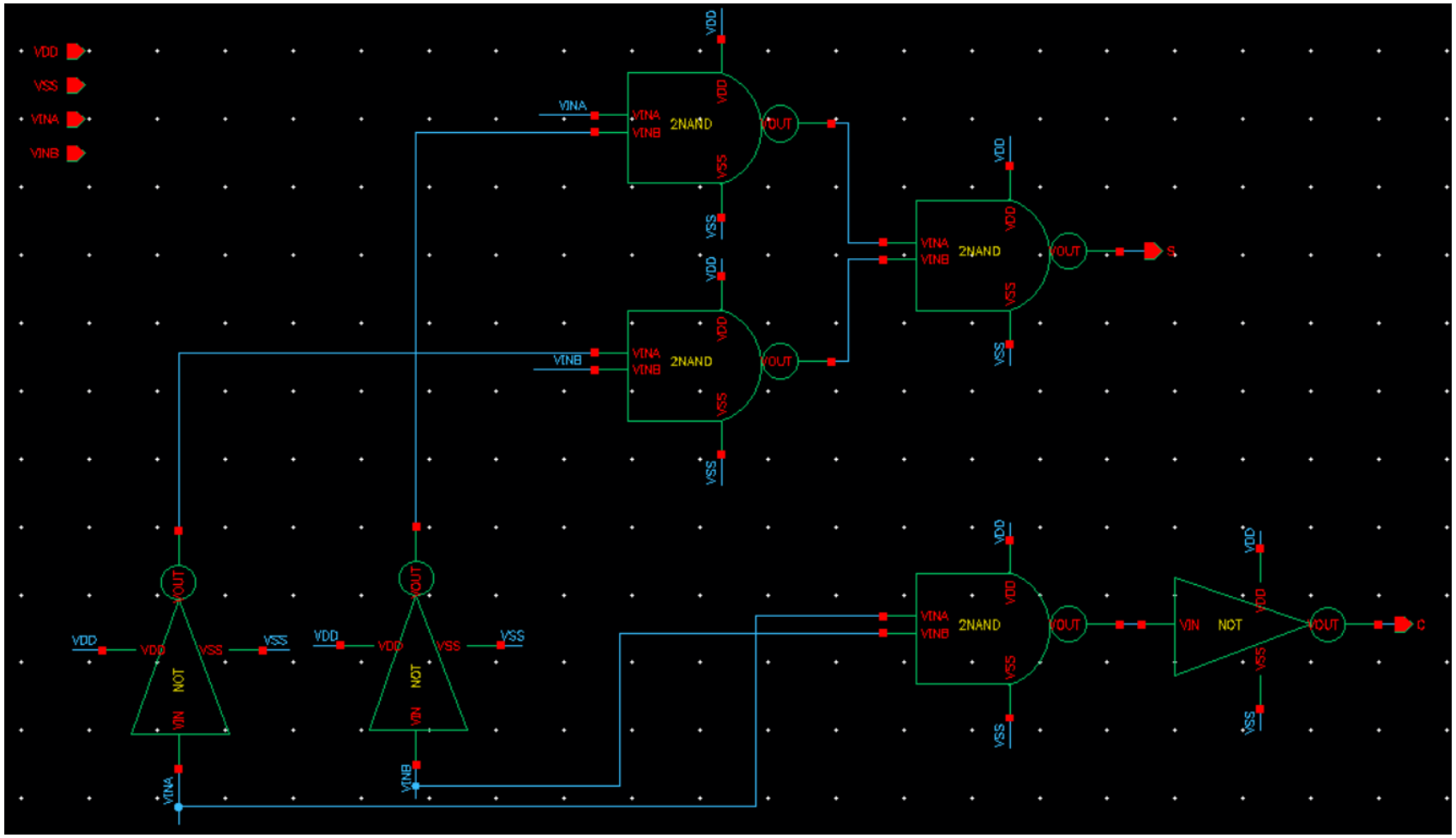


(Inverter) 2 * 1 + (2NAND) 4 * 1 + (XOR) 6 * 1
= 12

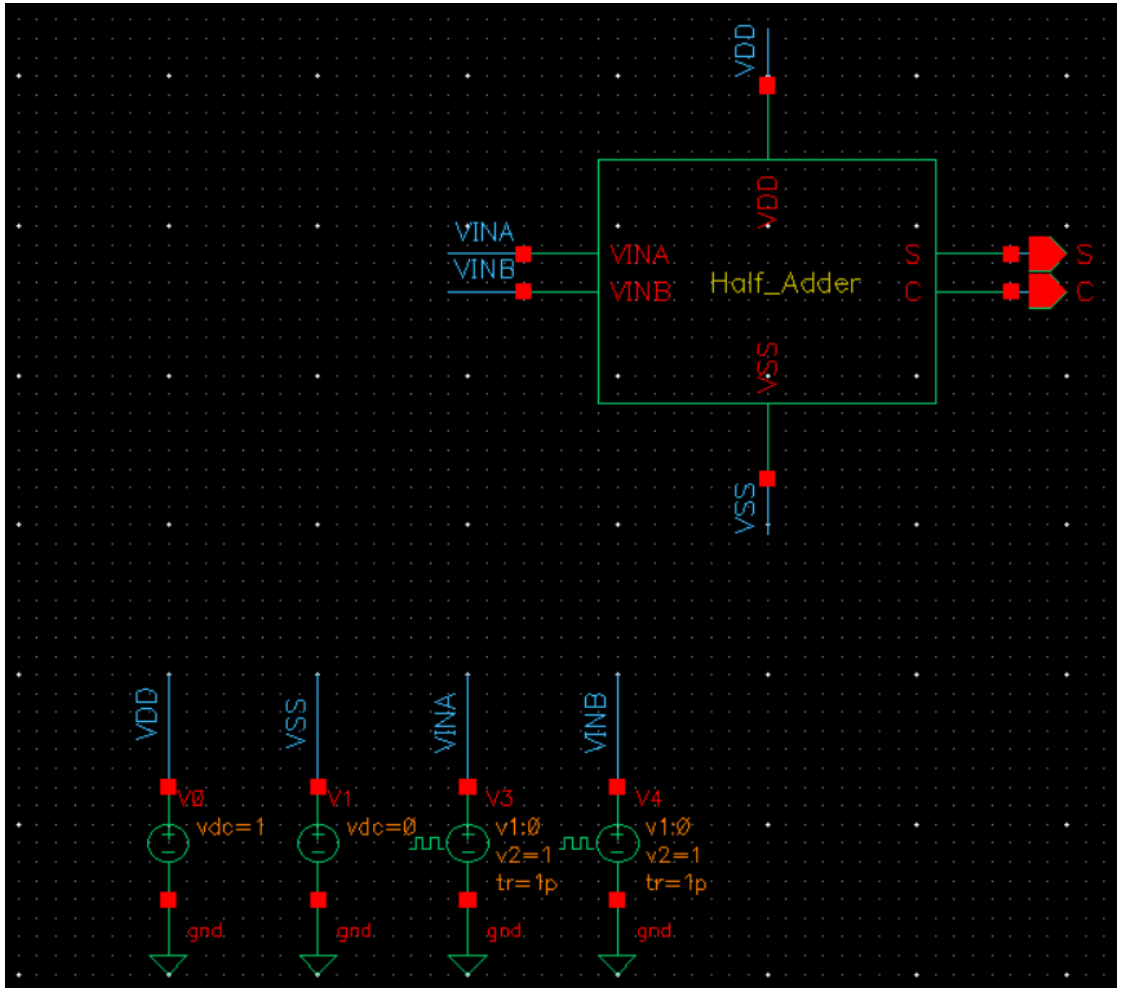
XOR O (Schematic)



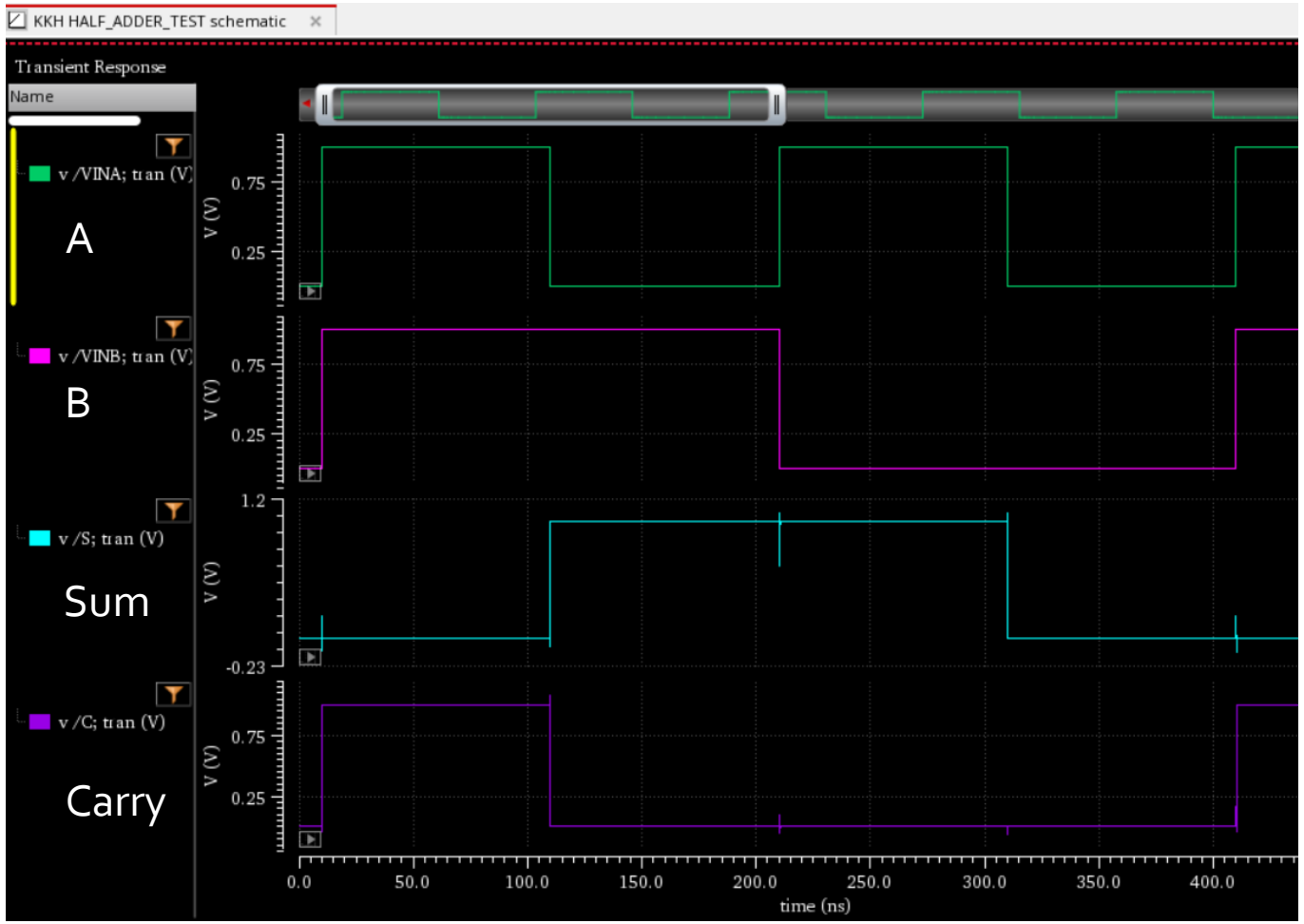
XOR X (Schematic)



XOR O (Simulation Setup)



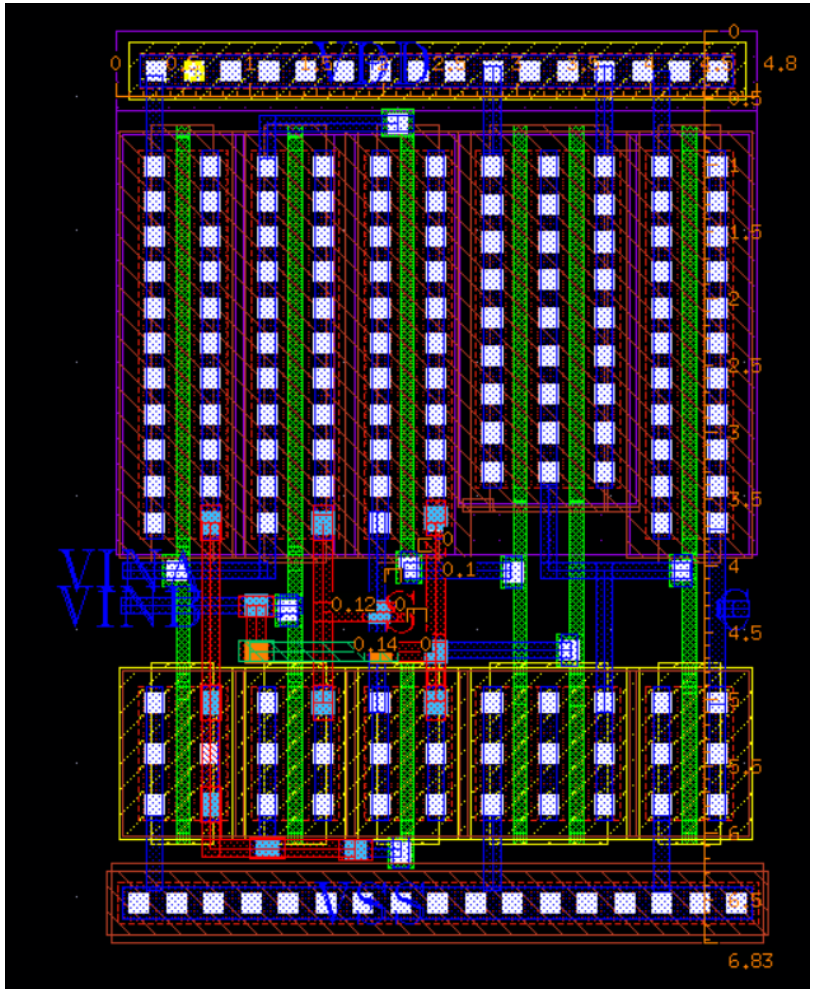
Wave Form



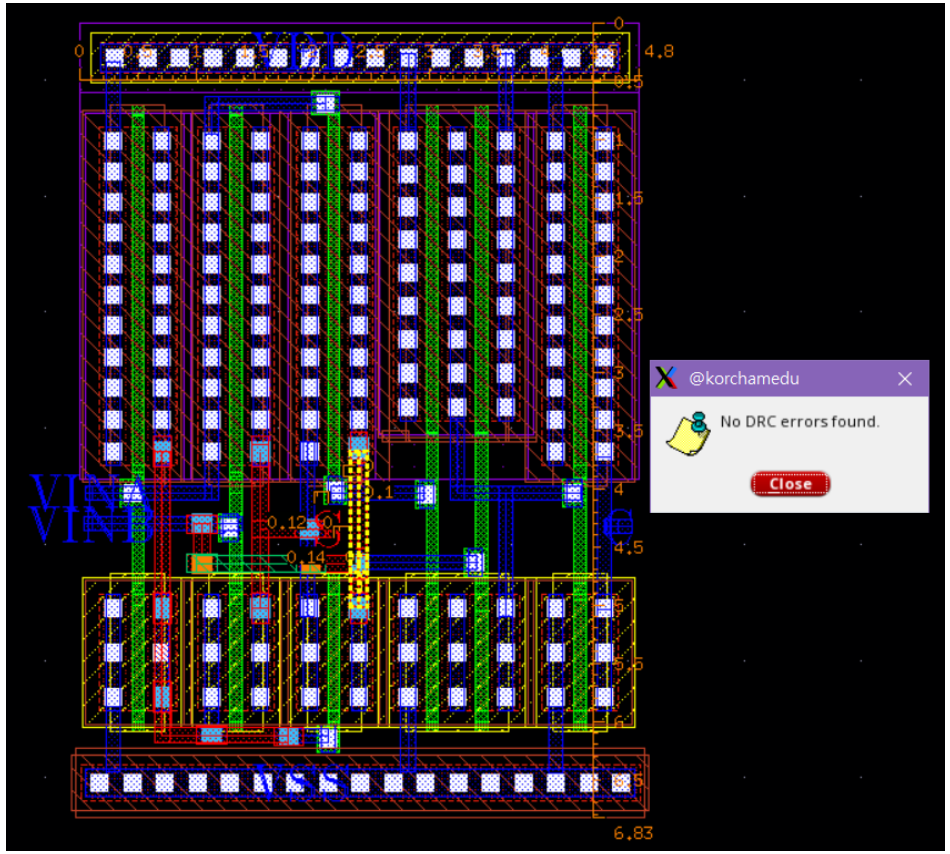
A B	S C
0 0	0 0
0 1	1 0
1 0	1 0
1 1	0 1

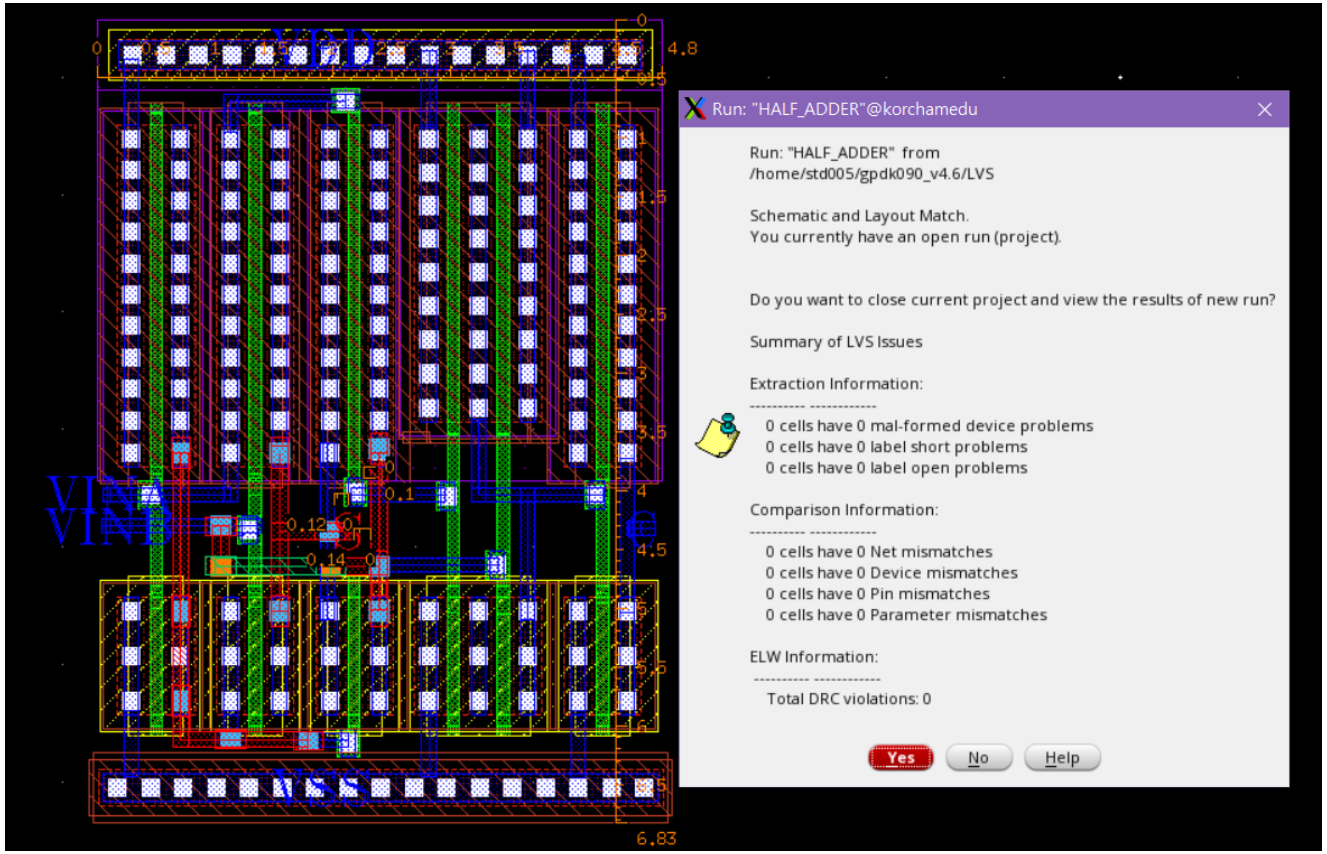
- 입력 값에 따라 출력이 변화하는걸 확인할 수 있다.

XOR O (Layout)

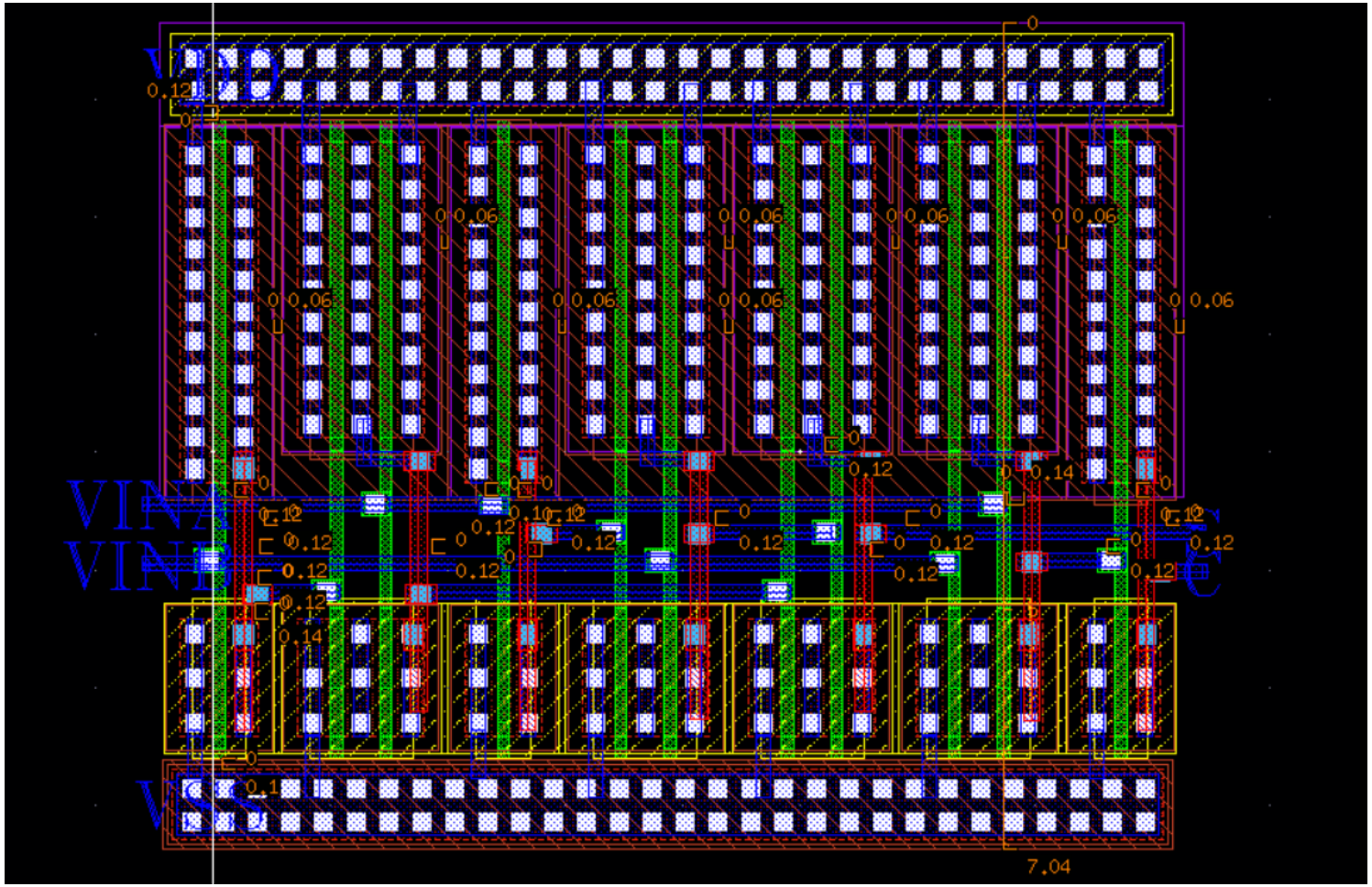


XOR O (DRC / LVS)

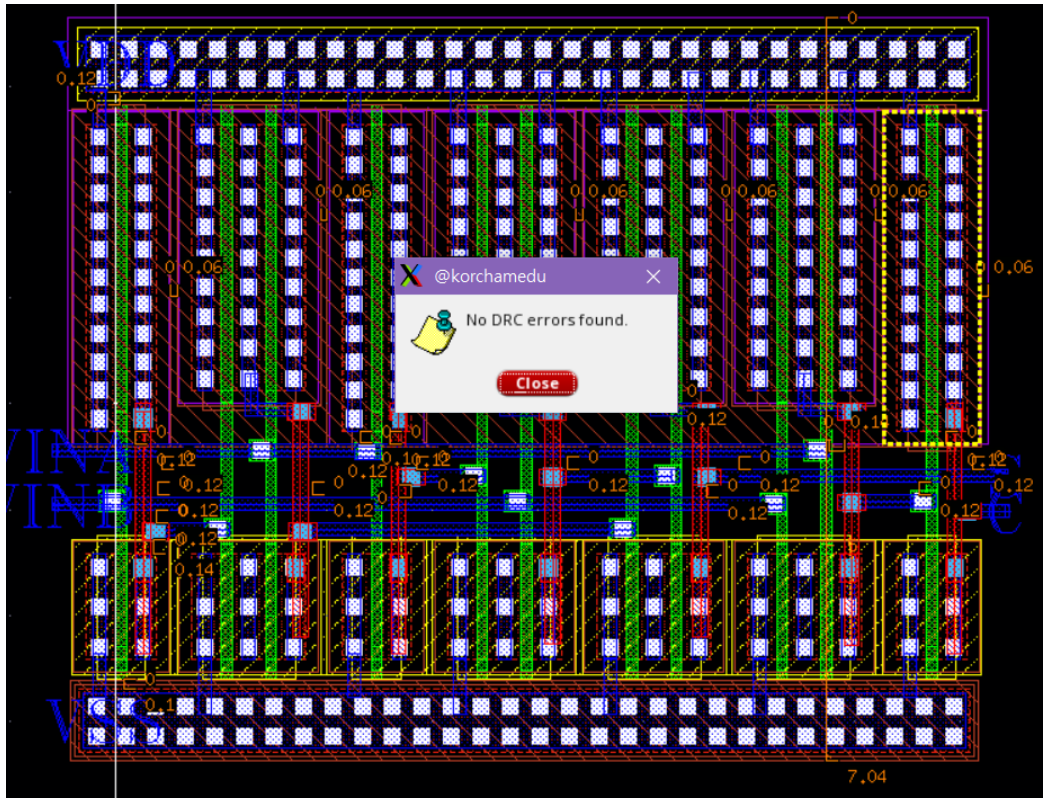

VDD
VINA
VINB
VSS
@korchamedu
No DRC errors found.
Close

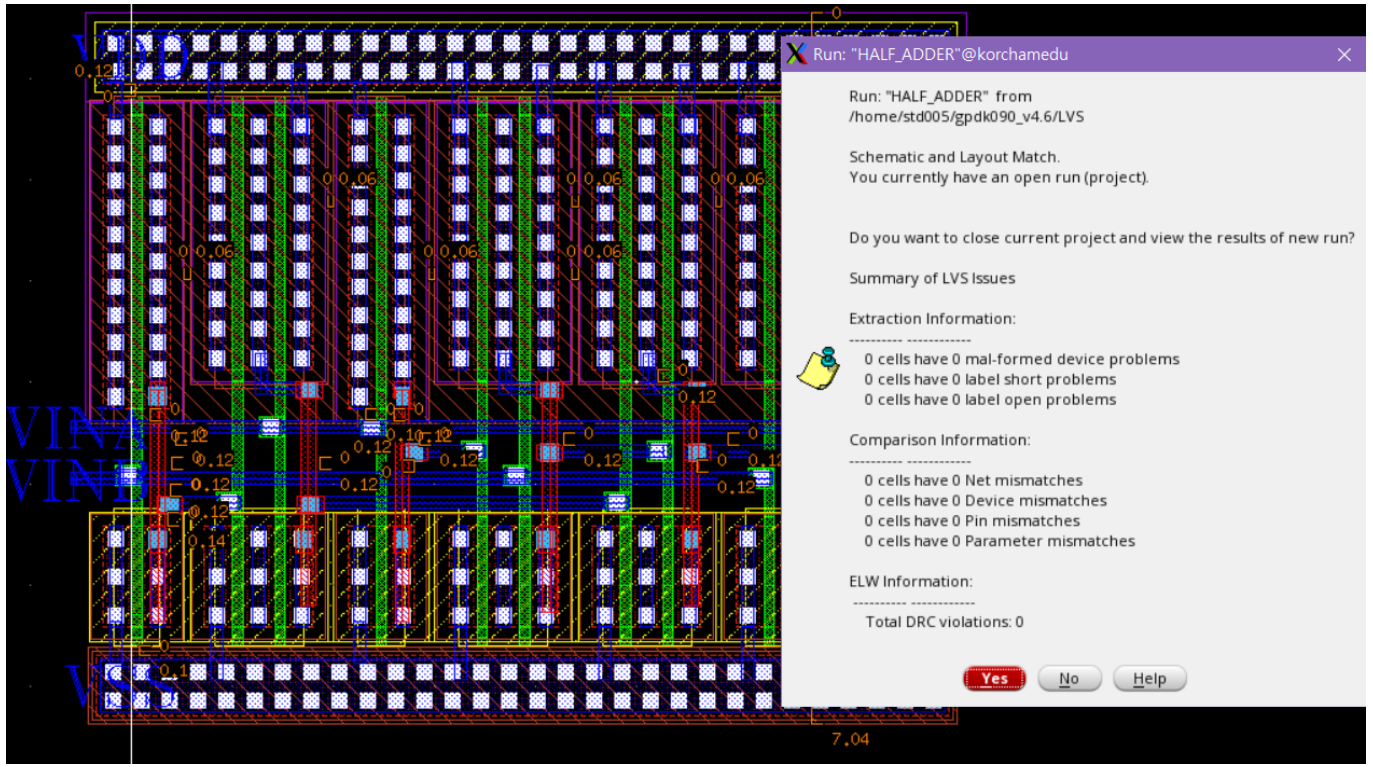

VDD
VINA
VINB
VSS
Run: "HALF_ADDER"@korchamedu
Run: "HALF_ADDER" from
/home/std005/gpdk090_v4.6/LVS
Schematic and Layout Match.
You currently have an open run (project).
Do you want to close current project and view the results of new run?
Summary of LVS Issues
Extraction Information:
0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems
Comparison Information:
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches
ELW Information:
Total DRC violations: 0
Yes
No
Help

XOR X (Layout)

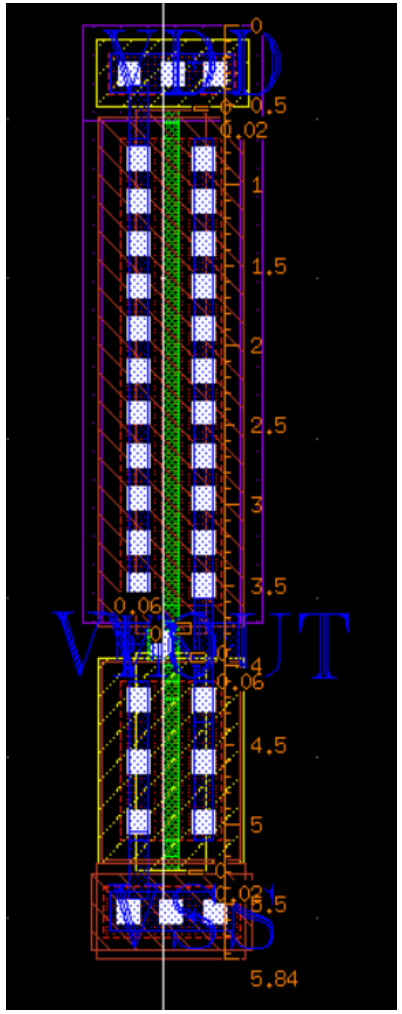


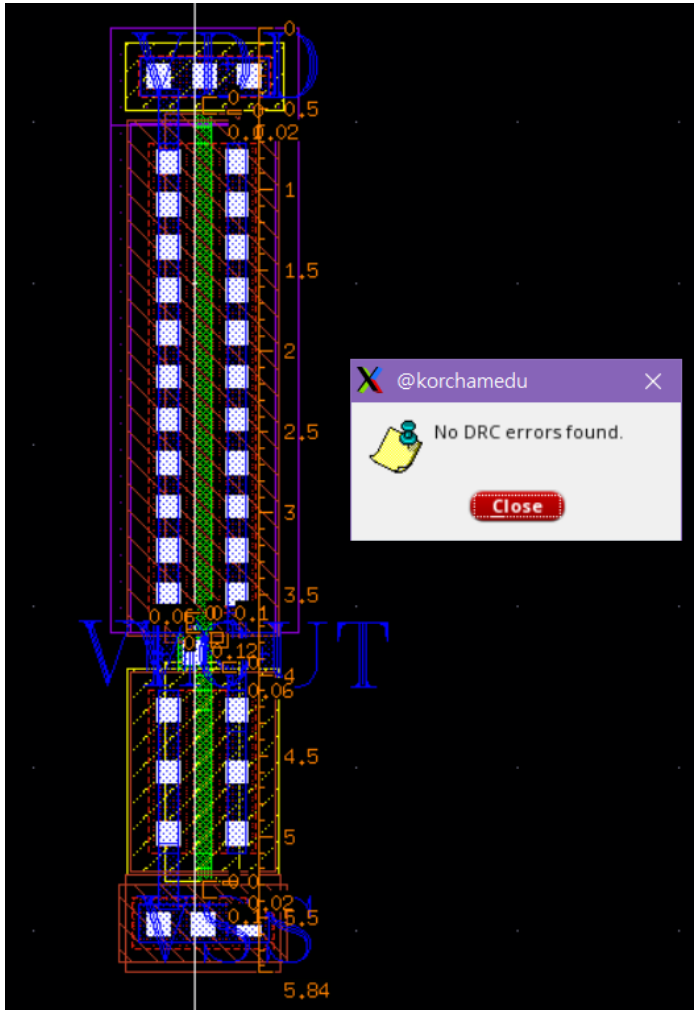
XOR X (DRC / LVS)

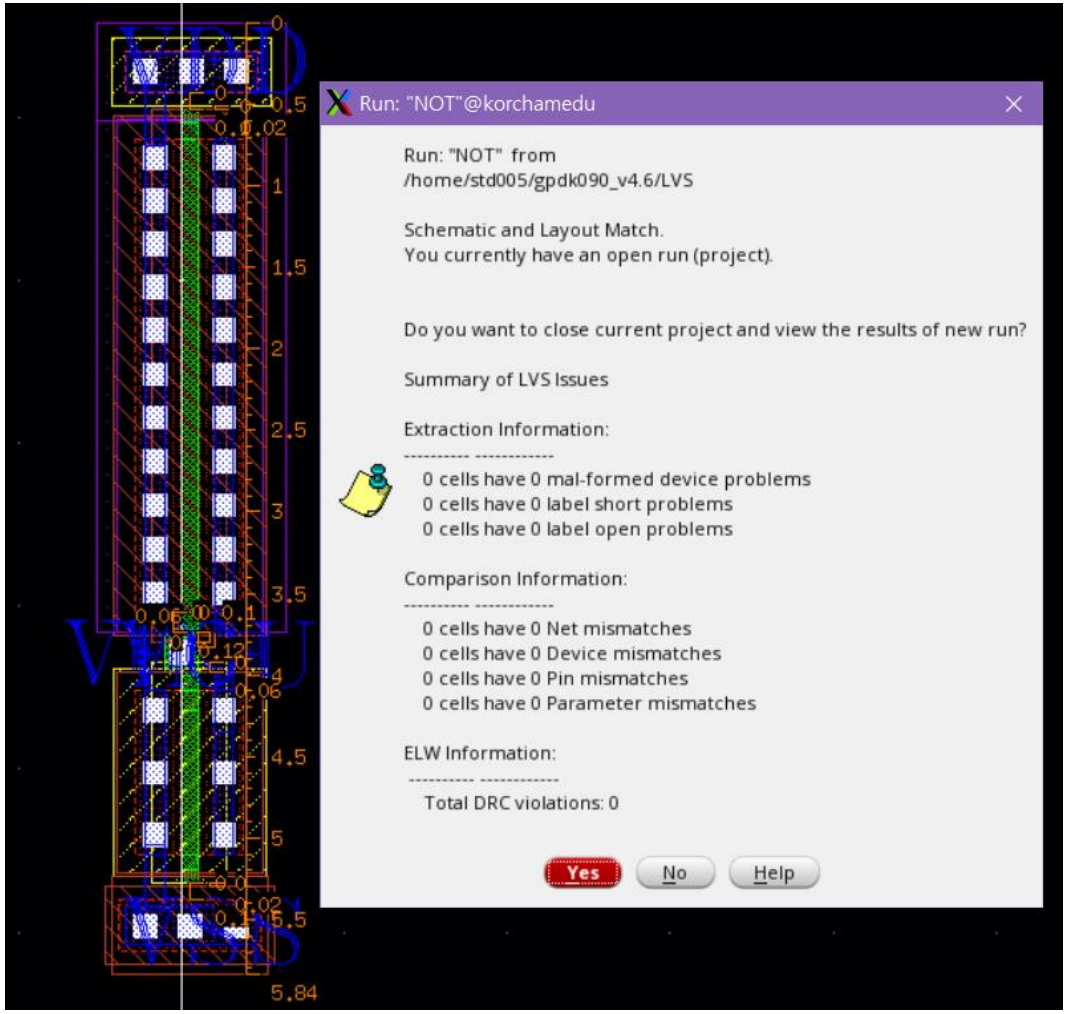

@korchamedu
No DRC errors found.
Close
VDD
VSS
7.04


Run: "HALF_ADDER"@korchamedu
Run: "HALF_ADDER" from
/home/std005/gpdk090_v4.6/LVS
Schematic and Layout Match.
You currently have an open run (project).
Do you want to close current project and view the results of new run?
Summary of LVS Issues
Extraction Information:
0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems
Comparison Information:
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches
ELW Information:
Total DRC violations: 0
Yes
No
Help
VDD
VSS
7.04

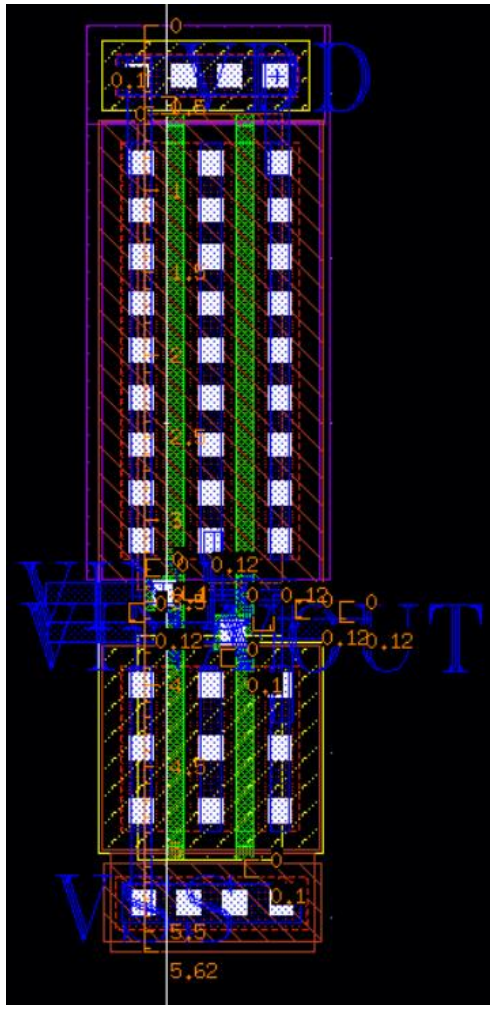
Inverter (Layout / DRC / LVS)

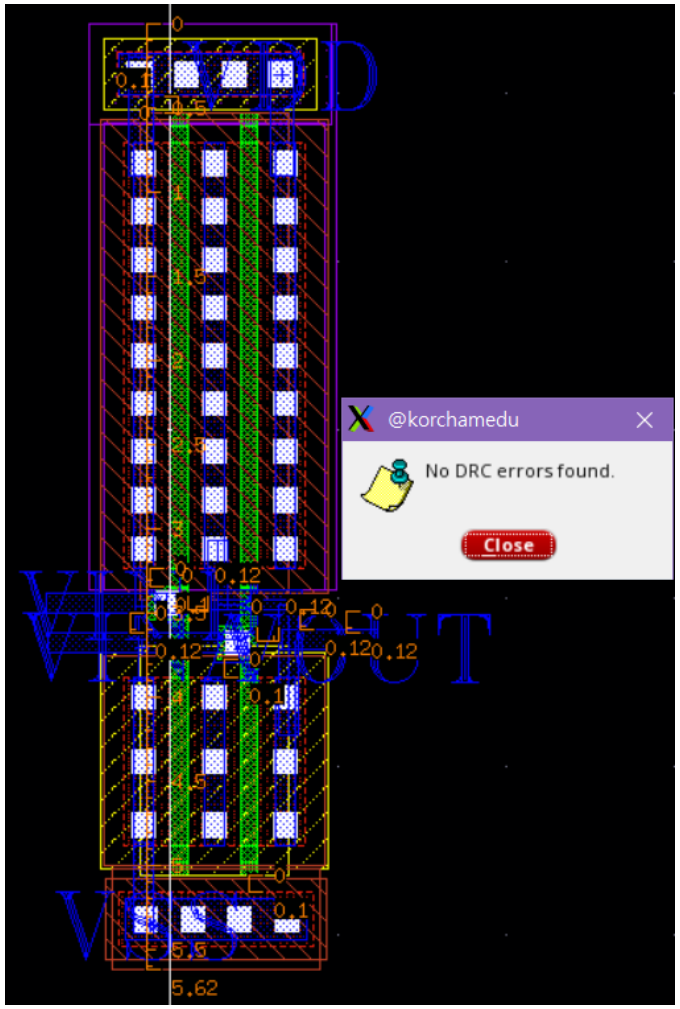


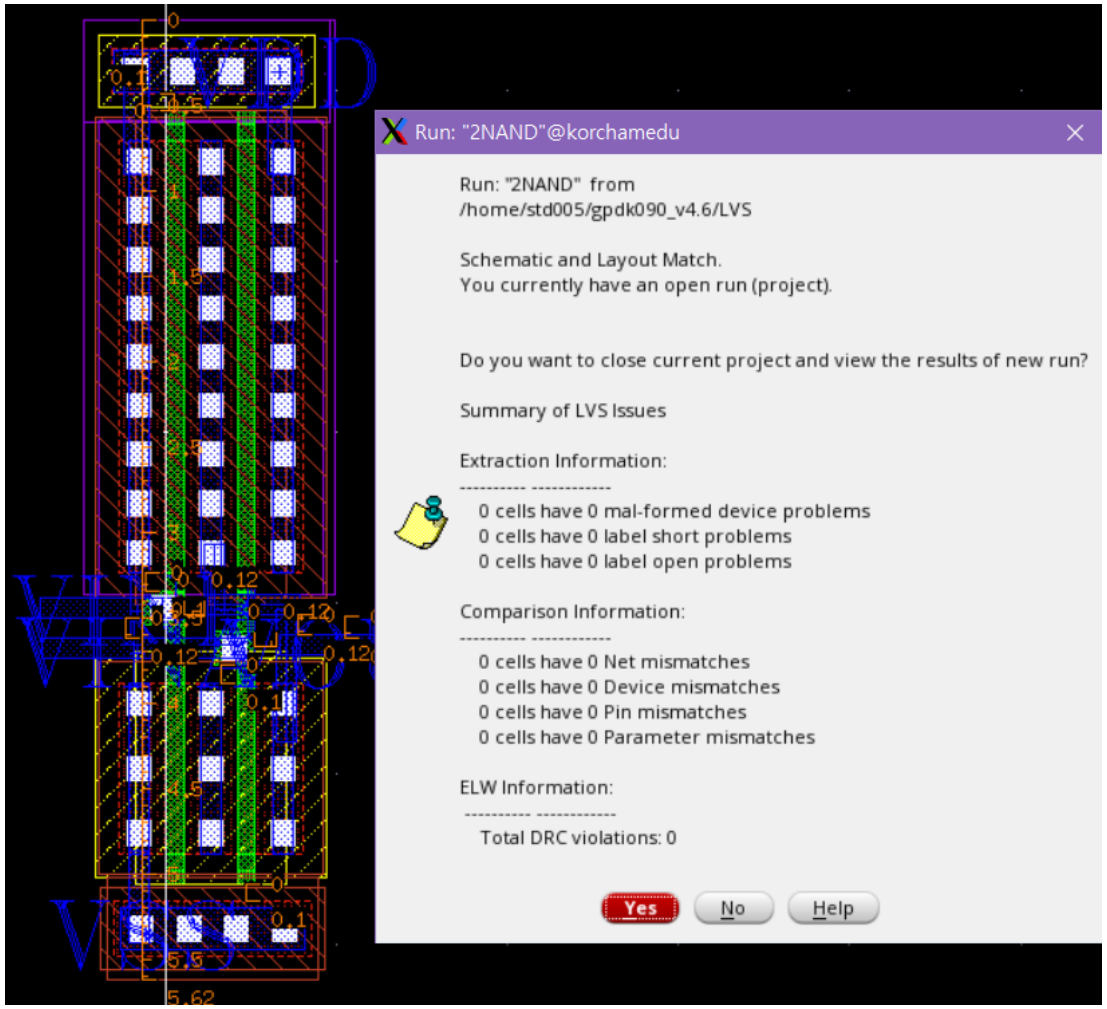




2NAND (Layout / DRC / LVS)







크기비교

	XOR O	XOR X
가로	4.8	9.36
세로	6.83	7.04