Sugandha Sharma

(226) 868 1505 . s72sharm@uwaterloo.ca
39 Shawna Road, London, ON N5X 3G9
sugandhasharma.weebly.com . ca.linkedin.com/in/sugandhasharma17/

EDUCATION

- **University of Waterloo,** Canada **Sept 2010 - April 2015**
  Bachelor of Electrical Engineering Honors with a minor in Management Engineering.
- **Relevant Courses**: Computer Architecture, Integrated Digital Electronics, Embedded Microprocessor Systems, Adaptive and Cooperative Algorithms, Neural Engineering.

SKILLS SUMMARY

- Competent at Object Oriented Programming. Languages: C, C++, Verilog, Python, Perl, Java
- Tools/Environments: WinDbg, Visual Studio, Emacs, Cadence Virtuoso, Allegro, Modelsim
- Sound understanding of modern computer architecture design and embedded systems
- Adequate knowledge of machine learning algorithms for solving complex engineering problems
- Applied knowledge of optimization and models associated with Operations Research

WORK EXPERIENCE

Software Engineer, AMD, Markham, ON **Sept - Dec 2014**

- Kernel Mode Driver development for graphics chips to work with the latest Windows OS
- Developed and tested software support for Multi GPU - Single Large Surface features in C++
- Implemented work-around for windows applications involving kernel and OS interactions
- Resolved bugs in the graphics driver by working with graphics driver architecture, OS/driver/BIOS interactions, debuggers & profilers.
- Performed software code analysis for performance optimization (optimal resource utilization)

Systems Engineer, NVIDIA, Santa Clara, CA **April - Aug 2013**

- Independently automated the efficiency measurement procedure for the graphics cards. Designed and created the tool Infrastructure using GPIB interface for communication between the electronic load machine and data acquisition system (Python).
- Automated the prediction of component values for designing compensation circuits for power converters on graphic cards. Applied concepts of control systems and stability analysis.
- Analyzed and debugged acoustic noise issues found on graphic cards and proposed fixes.

Systems Engineer, NVIDIA, Santa Clara, CA **Jan - May 2014**

- Independently developed a web UI for the company's Asset Tracker database (Perl/Html) and also hooked it efficiently to the backend server.
- Wrote QA procedures to run prior to releasing changes to the hard drive cloning system (Perl)
- Toured PCB Assembly and PCB fabrication facilities and took initiative for automating internal processes for better efficiency (VBA).
- Worked with PCB designs and updated reference schematics for the memory interface (Cadence). Learn about high speed PCB design & layout techniques and ASIC design process.

Software Engineer, BlackBerry, Waterloo, ON **Sept - Dec 2012**

- Worked as a developer for Duplicate Defect Detection (DDD) research project (Java).
- Gained extensive experience in Information retrieval techniques and search engines.
- Verified builds and virtual environments, learnt about wireless communication systems.

Software Engineer, Phoenix Interactive Design Inc., London, ON **Jan - April 2012**

- Followed a rigorous design process including software specifications, design documentation, test plans, software coding (C++) and integration.
- Successfully developed Asset Manager Applications and ATM terminal applications.
- Performed regression tests on ATM hardware, Virtual Machines & Desktop Simulators.

Eng Software Tools Administrator, Christie Digital Systems, Kitchener, ON **May - Aug 2011**

- Successfully redesigned the UI of the PLM system to provide better and quick search criteria
- Delivered Technical Presentations to train the developers in the new UI functionality

PROJECTS

Media Player System (Embedded Microprocessor Systems) - Designed and implemented a media player system in 'C', capable of playing different songs at normal, double and half speed. Used a combination of polling, synchronization, timers and interrupt handlers to interface with the devices (Push buttons, LEDs and Switches) on the Altera DE2 board. NIOS II IDE was used for development.

Machine Learning - Solved a fleet scheduling problem using meta-heuristic algorithms and the knowledge artificial intelligence. The main goal was to optimize the problem of assigning aircrafts to routes in order to meet with demands and minimize costs. Matlab was used for programming.

Interactive Programming in Python - Developed interactive applications in python. These applications involve windows whose contents are graphical and respond to buttons, the keyboard and the mouse.

5-Stage Pipelined MIPS Processor - Developed using Verilog and the Modelsim simulator. The processor executed C programs compiled using GNU GCC.

1-Bit Mirror Adder (Schematic, Layout, Extraction) - Designed and layed-out a single bit full adder. Performed analysis on the transistor sizing, critical path, power consumption and propagation delay.

High Performance D-Flip Flop - Designed a Dynamic TSPC topology flip flop. Performed analysis using metrics: Data-to-output (D-Q), Setup time, Clock-to-output (C-Q), Average Power (Pavg). Considered the process Corners, Temperatures, Power Delay Product vs. VDD, & Monte Carlo simulations for analysis.

Pipelined Sequential System - Used the DFF and the 1-bit mirror adder designed above to implement a pipelined sequential system. Determined the maximum possible clock frequency for the system.

AWARDS

- Gerry Heckman Scholarship **Winter 2015**
- Baylis Medical Capstone Design Project Award **Winter 2014**
- 3 x Deans Honours List for academic distinction, University of Waterloo **Sept 2010 - April 2013**
- Ontario Power Generation Engineering Award **Sept 2011 - 2012**
- Ontario Professional Engineers Foundation Undergraduate Scholarship **Sept 2011 - 2012**
- Awarded UW merit scholarship, University of Waterloo **September 2010**