Sugandha Sharma

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EDUCATION

- **University of Waterloo,** Canada **Sept 2010 - April 2015**
  Bachelor of Electrical Engineering Honors with a minor in Management Engineering.
  Graduated with distinction and on Dean's Honours List.

SKILLS SUMMARY

- Competent at Object Oriented Programming. Languages: C, C++, Verilog, Python, Java
- Tools/Environments: Nengo neural simulator, Visual Studio, Emacs, Cadence Virtuoso, Modelsim
- Sound understanding of modern computer architecture design and embedded systems
- Adequate knowledge of machine learning algorithms for solving complex engineering problems

WORK EXPERIENCE

Research Assistant, Center for Theoretical Neuroscience, Waterloo, ON **May 2015 – Present**

- Developing models of large scale systems to replicate behavioral performance on cognitive tasks.
- Developing software tools and reusable components for quickly constructing such models.
- Writing and Presenting research and technical findings.

Software Developer, AMD, Markham, ON **Sept - Dec 2014**

- Kernel Mode Driver development for graphics chips to work with the latest Windows OS
- Developed software support for Multi GPU - Single Large Surface features in C++.
- Implemented work-around for windows applications involving kernel and OS interactions.
- Resolved bugs in the graphics driver by working with graphics driver architecture, OS/driver/BIOS interactions, debuggers & profilers.
- Performed software code analysis for performance optimization (optimal resource utilization).

Systems Engineer, NVIDIA, Santa Clara, CA **Jan - May 2014**

- Independently automated the efficiency measurement procedure for the graphics cards. Designed and created the tool Infrastructure using GPIB interface for communication between the electronic load machine and data acquisition system (Python).
- Automated the prediction of component values for designing compensation circuits for power converters on graphic cards. Applied concepts of control systems and stability analysis.
- Analyzed and debugged acoustic noise issues found on graphic cards and proposed fixes.

Systems Engineer, NVIDIA, Santa Clara, CA **April - August 2013**

- Independently developed a web UI for the company's Asset Tracker database (Perl/Html) and also hooked it efficiently to the backend server.
- Wrote QA procedures to run prior to releasing changes to the hard drive cloning system (Perl).
- Worked with PCB designs and updated reference schematics for the memory interface (Cadence). Learn about high speed PCB design & layout techniques and ASIC design process.

Software Developer, BlackBerry, Waterloo, ON **Sept - Dec 2012**

- Worked as a developer for Duplicate Defect Detection (DDD) research project (Java).
- Gained extensive experience in Information retrieval techniques and search engines.
- Verified builds and virtual environments, learnt about wireless communication systems.

Software Engineer, Phoenix Interactive Design Inc., London, ON **Jan - April 2012**

- Followed a rigorous design process including software specifications, design documentation, test plans, software coding (C++) and integration.
- Successfully developed Asset Manager Applications and ATM terminal applications.

Eng Software Tools Administrator, Christie Digital Systems, Kitchener, ON **May - Aug 2011**

PROJECTS

Biologically Plausible Neural Model of Wason Selection Task – Built using the Neural Engineering Framework and the Nengo software package. The model is able to learn (using Hebbian learning) and performs syntactic generalization. The model also consists of a basal ganglia to perform action selection to choose between different actions (i.e., learning or answering).

Media Player System (Embedded Microprocessor Systems) - Designed and implemented a media player system in 'C', capable of playing different songs at normal, double and half speed. Used a combination of polling, synchronization, timers and interrupt handlers to interface with the Altera DE2 board.

Machine Learning - Solved a fleet scheduling problem using meta-heuristic algorithms and the knowledge artificial intelligence. The main goal was to optimize the problem of assigning aircrafts to routes in order to meet with demands and minimize costs. Matlab was used for programming.

Interactive Programming in Python - Developed interactive applications in python. These applications involve windows whose contents are graphical and respond to buttons, the keyboard and the mouse.

5-Stage Pipelined MIPS Processor - Developed using Verilog and the Modelsim simulator. The processor executed C programs compiled using GNU GCC.

1-Bit Mirror Adder (Schematic, Layout, Extraction) - Designed and layed-out a single bit full adder. Performed analysis on the transistor sizing, critical path, power consumption and propagation delay.

High Performance D-Flip Flop - Designed a Dynamic TSPC topology flip flop. Performed analysis using metrics: Data-to-output (D-Q), Setup time, Clock-to-output (C-Q), Average Power (Pavg). Considered the process corners, Temperatures, Power Delay Product vs. VDD, & Monte Carlo simulations for analysis.

Pipelined Sequential System - Used the DFF and the 1-bit mirror adder designed above to implement a pipelined sequential system. Determined the maximum possible clock frequency for the system.

AWARDS

- Undergraduate Student Research Award (NSERC) **May - August 2015**
- Undergraduate Research Assistantship, University of Waterloo **Jan - April 2015**
- Gerry Heckman Scholarship **Winter 2015**
- Baylis Medical Capstone Design Project Award **Winter 2014**
- 3 x Deans Honours List for academic distinction, University of Waterloo **Sept 2010 - April 2013**
- Ontario Power Generation Engineering Award **Sept 2011 - 2012**
- Ontario Professional Engineers Foundation Undergraduate Scholarship **Sept 2011 - 2012**
- Awarded UW merit scholarship, University of Waterloo **September 2010**