Shintaro Marzo

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Summary

Senior Verification Engineer with 7+ years of experience in ASIC and FPGA verification. Proven ability to apply full metric-driven methodologies to complex systems. Expertise in verification processes, UVM, SVA, and mixed-signal flows. Successfully verified 20+ digital and mixed-signal subsystems, with minimal to zero defects in production.

Skills

Methodologies: Universal Verification Methodology (UVM), Metric Driven Verification (MDV), Formal Verification (UNR, FPV, Connectivity), Mixed-Signal Verification, Gate-Level Simulation (GLS), Emulation
Protocols: I2C, SPI, AMBA AHB, AXI4, AXI-Stream, APB, I3C, JTAG
Verified Blocks: Fuse/OTP/NVM Controller, Design for Test (DFT), Security (PUF, Crypto), FPGA Configuration Bitstream, Analog Control Blocks
Languages: SystemVerilog (SV), Assertions (SVA), Verilog, Python, TCL, Make, C/C++, bash/csh
EDA Tools: Cadence Xcelium, vManager, SimVision, JasperGold, Verisium SimAI, Palladium
Other Tools: Git, Perforce, Jenkins, Atlassian JIRA, Confluence, VSCode, Cursor AI, DVT Eclipse
Others: Verification Planning, Feature Extraction, Architecting Testbench, Object Oriented Programming (OOP), Debugging, Regression Execution, Coverage Closure
Soft Skills: Leadership, Nimble Learner, Critical Thinking, Communicates Effectively, Mentoring and Coaching

Professional History

Senior Design Verification Engineer Feb 2024 – Present
Lattice Semiconductor (PH) Corporation

- Delivered timely verification of the security hardware, firmware, and configuration subsystem of the Lattice Avant and Nexus FPGAs
- Collaborated with DV team members to improve testbench using UVM while supporting legacy tests
- Leveraged use of emulation (Cadence Palladium) to supplement simulation and speed up verification of cryptography algorithms (RSA, ECDSA, EdDSA)
- Improved verification flow quality by setting up Cadence vManager and integrating it with the existing simulation infrastructure
- Explored and leveraged AI/ML tools (Verisium SimAI) to improve regression efficiency and maximize coverage

Senior Design Verification Engineer May 2022 – Jan 2024
Analog Devices Gen. Trias, Inc

- Led a verification team of 4 engineers in developing and executing a comprehensive UVM-based verification plan for an SoC project, enabling on-time tape-out
- Architected a reusable verification environment for a multi-project wafer consisting of 4 projects, removing redundant development cycles across each
- Automated revision control change detection for first build failure using Jenkins and Perforce, saving debug time
- Optimized simulation infrastructure using process-based save restart setup for UVM
- Mentored a senior design engineer and coached a junior DV engineer to improve their verification skills
- Active participant in verification initiatives and methodology improvements

Digital Design Verification Engineer May 2018 – May 2022
Analog Devices Gen. Trias, Inc

- Digital Verification owner for multiple projects resulting to minimal to zero defects post-silicon
- Developed and executed verification plans and strategies for complex electronic designs, ensuring timely and high-quality results
- Architect and implement testbench components using SV/UVM to expose bugs and flaws
- Setup simulation environment for both RTL and Gates verification
- Collaborate with cross-functional teams to debug and resolve design and verification issues
- Analyze coverage and plan metrics to assess the effectiveness of verification and trend towards sign off
- Contributed to team improvement initiatives, sharing knowledge and best practices to help the team achieve its goals

Engineering Student Intern Aug 2016 – Dec 2016

Analog Devices Gen. Trias, Inc

- Completed introduction to Metric Driven Verification and Assertion Based Verification trainings
- Increase verification quality by introducing JasperGold Formal Verification tools with the help of my mentor

Training Assistant Jun 2016 – Jul 2016

Philippine Institute for Integrated Circuits

- Completed fast-paced training programs that covered all aspects of IC design.
- Shared my knowledge and experience with trainees, helping them to develop a strong foundation in IC design.

Education

Batangas State University 2012 – 2017

Bachelor of Science in Electronics Engineering, Major in Microelectronics

- Developed an educational binary to decimal shooting video game using Verilog and FPGA.
- Thesis involved designing sub-blocks for an OOK RF Transceiver in 45nm CMOS process
- Ranked Top 4 in the April 2018 Professional Regulation Commission (PRC) Electronics Engineer Licensure Examination

Awards & Recognition

2025 — **Team Contributor**, Successful tapeout of an advanced Avant mid-range FPGA
2025 — **Leadership**, Led Cadence vManager working group to improve verification methodology and quality
2024 — **Individual Contributor**, Quick turn around in creating key tests to ensure the quality of the project
2023 — **Nominated**, Top Outstanding Young Professional
2022 — **Team Contributor**, Helped outside of the team that led to a successful tape out of the project
2022 — **Team Contributor**, Developed training materials used by newly hired engineers of the team
2022 — **Leadership**, Led three verification projects that taped out in a single quarter
2021 — **Individual Contributor**, Digital Verification lead of his first project after training; going beyond the scope by covering Mixed Signal verification; resulted in silicon success; gained respect and trust of his lead bringing more projects