SHINTARO MARZO

IC DESIGN VERIFICATION

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SUMMARY

Verification Engineer with 5+ years of experience in both digital and mixed-signal verification. Proven ability to apply full metric-driven methodologies to complex systems. Expertise in verification processes, UVM, and mixed-signal development flow. Successfully verified 20+ digital and mixed-signal subsystems, with minimal to zero defects in production.

PROFESSIONAL HISTORY

Analog Devices Gen. Trias, Inc.

Digital Design Verification Engineer • May 2018 - Present

- *Digital Verification lead for multiple projects resulting in timely and high-quality silicon*
- *Develop and execute verification plans and strategies for complex electronic designs*
- *Architect and implement testbench components using SV/UVM to expose bugs and flaws*
- *Setup simulation environment for both RTL and Gates verification*
- *Collaborate with cross-functional teams to debug and resolve design and verification issues*
- *Analyze code and functional coverage and plan metrics to assess the effectiveness of verification and path to sign-off*
- *Contribute to team improvement initiatives, sharing knowledge and best practices*

Engineering Student Intern • Aug 2016 - Dec 2016

- *Learned and introduced JasperGold Formal Verification tools to increase verification quality of the team*

Philippine Institute for Integrated Circuits

Training Assistant • Jun 2016 - Jul 2016

- *Completed fast-paced training programs that covered all aspects of IC design.*
- *Shared my knowledge and experience with trainees, helping them to develop a strong foundation in IC design.*

EDUCATION

B.S. in Electronics Engineering, Major in Microelectronics

Batangas State University • 2012–2017

- *Developed an educational binary to decimal shooting video game using Verilog and FPGA.*
- *Thesis involved designing sub-blocks for an OOK RF Transceiver in 45nm CMOS process*
- *Ranked Top 4 in the April 2018 Professional Regulation Commission (PRC) Electronics Engineer Licensure Examination*

SKILLS

Technical

Metric Driven Verification (MDV)	All projects used MDV to measure progress. (*Tools: Cadence Xcelium, vManager, JIRA)*
Universal Verification Methodology (UVM)	Applied UVM concepts to solve traditional testbench challenges [Badge]
Mixed-Signal Verification	Worked on a handful of mixed-signal systems
Assertion-Based Verification	Developed set of assertions that exposed bugs not found in other methodologies [Badge]
Formal Verification	Used formal to complement functional verification (*Tool: JasperGold)* [Badge]
Source Code Management (SCM)	Used various SCM tools in all projects (*Tools: Git, Perforce*)
DevOps	Automated verification processes using DevOps tools and methods (*Tool: Jenkins)*

Programming Languages

SystemVerilog (SV)	Proficient in SV and OOP concepts for verification [Badge]
Verilog	Intermediate mastery and understanding of Verilog syntax used in RTL designs
Python	Intermediate use of Python for data processing and automation scripts [Badge]
Perl/Tcl/Shell	Used for basic utility scripting tasks

Soft Skills

Nimble Learner	Takes on the challenge of unfamiliar tasks; finding new and/or better solutions
Critical Thinking	Identifies issues and comes up with different ways to resolve them
Instills Trust	Gains the confidence and trust of co-workers leading to partnerships
Communicates Effectively	Relays needed information to execute project deliverables
Mentoring and Coaching	Shares knowledge and experience to help engineers enhance their verification skills

WORK EXPERIENCE

Analog Devices Gen. Trias, Inc.

Digital Design Verification

- *Executed full MDV for the following blocks:*
  - *Various communication protocols such as I2C, SPI, AMBA APB, and others defined by ADI or customers*
  - *One Time Programmable (OTP) / Non-Volatile Memory (NVM) Controller*
  - *Design for Test/Evaluation*
  - *Analog Control Blocks*
  - *Pulse Width Modulation Control*
  - *Master-Slave modules synchronization*
  - *Physical Unclonable Function (PUF)*
- *Developed SystemVerilog Assertions (SVA) checks that can be reused in other projects*
- *Gate simulation setup, execution, and support*
- *Verification Closure Tasks*

Mixed-Signal Design Verification (MSDV)

- *Functional and connectivity verification of Mixed Signal Systems*
- *Modeled and validated basic transfer functionalities of analog blocks:*
  - *Comparators*
  - *Oscillator*
  - *Power on Reset (POR)*
  - *Bias Circuits*
  - *Low Dropout Regulators (LDO)*
  - *Level Shifters*
  - *Simple Analog/Digital Converters (ADC/DAC)*
  - *Voltage, Current, and Temperature Sensors*
  - *Custom Logic*
- *Co-simulation setup and execution at system-level*

Complementary Verification Efforts

- *Setup and execution of formal verification using JasperGold (JG)*
  - *Identify potential flaws upon detection of flops without reset before proofing*
  - *Unreachability (UNR) App to catch early design bugs related to unreachable codes*
- *Used Jenkins to automate detection if the recent change submitted to project workspace contributed to build/smoke test/regression failure*
- *Setup separate workspace for Jenkins to only pull changes from Perforce depot and reverts to the last stable version for nightly regressions*
- *Improve debug time with process-based save restart setup for UVM*
- *Metrics dashboards using vManager*
- *Configurable co-simulation and verification environment for a multi-project wafer*

WORK INITIATIVES

Analog Devices Gen. Trias, Inc.

Digital I.C. Training Committee

- *Goal: Scale the verification manpower of the team by creating training materials for new hires about digital design verification*
- *Led the creation of lecture material about SVA and improved its laboratory material such that trainees can complete it in 1-2 weeks (saved 3 weeks)*

Mixed Signal Training Committee

- *Goal: Equip experienced Digital Verification Engineers with knowledge of Mixed Signal Verification*
- *Helped develop a self-paced training program to equip trainees with mixed signal verification skills*

Design Verification (DV) Academe Linkage Committee

- *Goal: Increase awareness of DV career track among students*
- *DV Bootcamp Operations lead for the Cavite site*

More Initiatives and Support

- *Provide test engineering/evaluation support for a project that has been successfully taped-out to silicon*
- *Mentored a digital design engineer about digital verification*
- *Submitted a paper as a main author for Analog Devices Technical Symposium 2021, titled, "Change of Paradigm; A Newbie Guide from Digital to Mixed-Signal Verification"*

CITATIONS

Analog Devices Gen. Trias, Inc.

2023 **Nominated**, *Top Outstanding Young Professional*
2022 **Team Contributor**, *Helped outside of the team that led to a successful tape out of the project*
2022 **Team Contributor**, *Developed training materials used by newly hired engineers of the team*
2022 **Leadership**, *Led three verification projects that taped out in a single quarter*
2021 **Individual Contributor**, *Digital Verification lead of his first project after training; going beyond the scope by covering Mixed Signal verification; resulted in silicon success; gained respect and trust of his lead bringing more projects*