COL216

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Handling Variable Delays

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Overview

Sometimes, operations such as floating point arithmetic or memory accesses in a pipelined processor require variable delays. A floating point computation may depend on the data operands. A memory access may exhibit variable delays due to the cache hierarchy.

Goals

1. **Finding Data needed:** Used Random Number generator function rand() in C++ for calculating N=number of cycles stalled when there is a MISS for data access.
2. **Stalling the cycle in case of MISS:** Whenever we detected a MISS we stalled the pipeline for N cycles.

Specifications

1. The operation completes in one cycle with a probability x (this is considered a HIT).
2. The operation requires N cycles with a probability 1-x (this is considered a MISS).
3. Upon a memory request, at the end of one cycle, the memory indicates whether the operation was a HIT or MISS. If HIT, the operation is complete. If not, the operation completes N-1 cycles later.

Milestones

1. Generating random numbers

   Generating Random numbers for calculation of N=number of cycles by which pipeline should be stalled in case of a MISS and probability of a MISS.

2. Stalling Pipeline

   If there is a MISS, then We have stalled the pipeline for the N-1 cycles. Currently, probability for MISS is very high(0.5). So, I have done it to observe stalling. Normally it is around 0.05.