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Fabrication of vertically stacked single-crystalline Si nanowires using self-limiting oxidation

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Abstract
A simple method for fabricating vertically stacked single-crystal silicon nanowires on standard bulk silicon wafers is presented. The process uses inductively coupled plasma (ICP) etching to create silicon fins with uneven yet controllable vertical profiles. The fins are then thermally oxidized in a self-limiting process, and the narrow regions are completely consumed to create multiple nanowires vertically stacked on each other. It was found that the number of nanowires in the vertical stack depends on the number of ICP cycles. A mechanism for the formation of the nanowires is proposed and confirmed with numerical simulations.

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon nanowires (SiNWs) that are compatible with standard integrated circuits technology have shown promising potential in future-generation electronics, optoelectronics, and chemical/biological sensing applications [1–3]. However, fabricating SiNWs in a controllable manner remains very challenging. The bottom-up chemical approach utilizing metal-catalytic self-assembly can produce single-crystalline silicon wires with diameters down to 10 nm. However, a major concern of the bottom-up approach is its poor controllability over substrate and growth parameters such as growth direction and crystal orientation [4]. On the other hand, the top-down processing approach with successive stress-limited oxidation has resulted in better-controlled nanowire fabrication [5, 6]. In fact, this top-down approach was used to fabricate vertical silicon pillars down to 2 nm in diameter [5, 6].

Silicon nanowires grown by the top-down approach are extremely sensitive to the growth conditions. And from the applications perspective, vertical silicon pillars are very difficult to integrate into the traditional planar transistor technology and contacting to such pillars is very difficult. To overcome these challenges, the fabrication of horizontal silicon nanowire using self-limited oxidation was proposed. For example, in [5], an 8 nm diameter single SiNW was fabricated by combining electron-beam lithography, lift-off, silicon plasma etching and self-limited oxidation. In [6], the authors utilized self-limited oxidation of a Si fin to form a twin triangular SiNW. In these two examples cited, the location and shape of the nanowire are difficult to control. Recently, a more controllable method for fabricating stacked nanowires using a multi-material system such as Si/SiGe/Ge/SiGe stacks was reported [7], but the process was relatively complicated and requires special material handling.

2. Si nanowire fabrication

In this work, we report on a simple method for controllably forming vertically stacked multiple SiNWs by combining

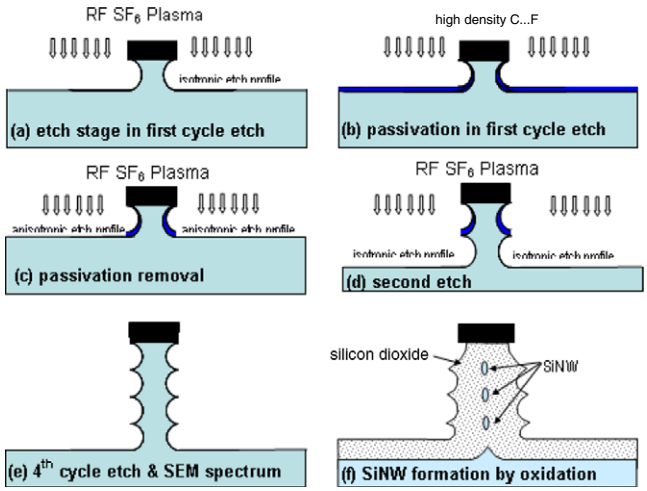

Figure 1. Schematic process flow for forming stacked silicon nanowires by plasma etching and self-limited thermal oxidation of silicon.

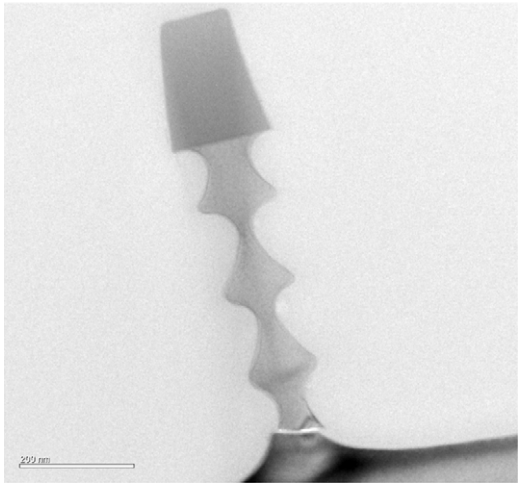

Figure 2. TEM image showing the cross-section of a silicon fin after the ICP etching.

inductively coupled plasma (ICP) etching and stress-limited oxidation of silicon. The key process flow steps for forming vertically stacked SiNWs are shown in figure 1. Starting with a ⟨100⟩ silicon wafer, first, silicon oxide is deposited and patterned by lithography. Next, oxide trimming [8] is performed to form a hard mask for various linewidths, followed by ICP etching using the oxide hard mask (figure 1(b)). Then, the patterned bulk Si is protected by a C_4F_8-based resistant polymer, and this is followed by SF_6 plasma etching of the unprotected regions, as shown in figures 1(c) and (d). The process is then repeated to form multiple fins with a non-uniform vertical profile as shown in figure 1(e).

It is known that the ICP etching process produces a scalloping structure in the sidewalls [9], so we take advantage of this property, but with a careful process optimization. After the formation of tall fins with a non-uniform vertical profile, thermal oxidation is performed to consume the narrow region of the fins. Due to the self-limiting nature of the process, a stack of multiple SiNWs is formed in the wider regions of the fin, as shown in figure 1(f).

The number of nanowires formed depends on the number of cycles of the ICP etch. Figure 2 shows the TEM (transmission electron microscopy) cross-sectional image of the silicon fins with different widths after four cycles of ICP etching. An N-cycle etching process produces $N - 1$ stacked nanowires. In order to form multiple SiNWs, the vertical profile of the silicon fin has to be carefully controlled to maintain approximately vertical sidewalls. In our process, we used 7 s etching with C_4F_8 (15 sccm), SF_6 (45 sccm), O_2 (5 sccm) at 600 W for each etching cycle. The passivation cycle is performed with C_4F_8 (75 sccm) at 200 W for 5.2 s. The sidewalls at the edge of the fins are approximately vertical in our process, although some small inclination was observed.

After the ICP etch, the oxidation step was performed at 1000 °C in an oxygen ambient. The oxidation time was varied to produce nanowires of different widths. Figure 3(a) shows the TEM cross-sectional image of stacked silicon nanowires in a fin that was formed with a 100 nm oxide hard mask after 2.5 h of oxidation. The final diameter of these nanowires is ∼10 nm.

The single-crystal property of the SiNW is maintained, as demonstrated from the atomic plane (figure 3(b)) showing the existence of the crystallographic alignment. The SiNW is too small to clearly identify in figure 3(c); however, its shadow can be observed. It is noted that crystalline Si is a better choice for the channel in transistors, as compared to polysilicon, amorphous Si or metal-induced crystallization Si. Therefore, the method described in this work shows the possibility of fabricating 3D nanoelectronic devices. The combination of nanometer dimensions and 3D stacking could dramatically shrink the electronic chip size, in the future.

3. Discussion of oxidation

In order to explore the final geometry of the SiNWs, we studied the effects of the initial geometry and processing conditions on the formation of the SiNWs. The basic process of silicon oxidation that is described by the Deal–Grove oxidation model for planar bulk silicon [10] has also been observed in our experimental results. The initial increase in oxide thickness has a linear relationship with time due to the reaction-limited oxidation. With increasing oxidation time and oxide thickness, the oxidation rate follows a logarithmic increase, the oxidation becomes more diffusion controlled and the oxidation behavior changes from a linear to a square-root variation with time. These variations are observed in figure 4 with the trend changing from linear to sub-linear when the oxidation time is longer than 90 min.

Oxidation on the nanoscale is influenced by many factors. For example, the oxidation rate of SiNWs with downscaled diameters is expected to be slower than the oxidation of a planar silicon substrate due to the accumulation of stress during the oxidation process. However, the opposite was observed as the oxidation rate of the SiNWs was higher than that of the planar silicon substrate in figure 4. It is noted that this behavior occurs when the oxidation time is less than 90 min

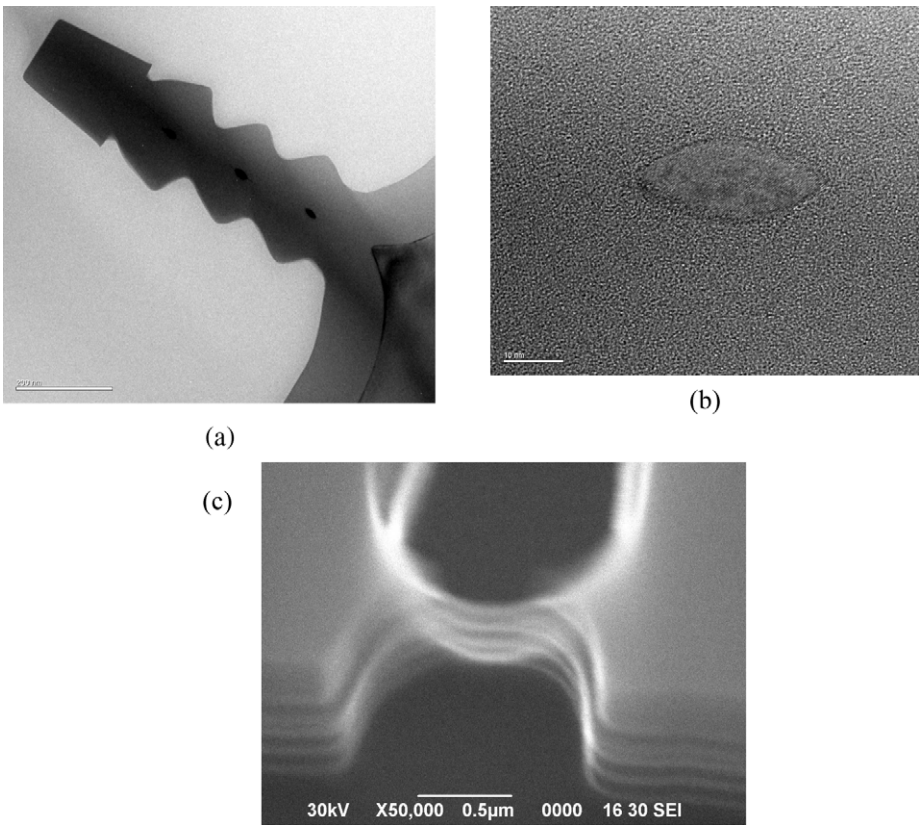

Figure 3. The TEM and SEM photos of the final Si nanowire showing (a) triple stacking, (b) the close-up atomic structure of the Si nanowire, and (c) the top-view SEM picture.

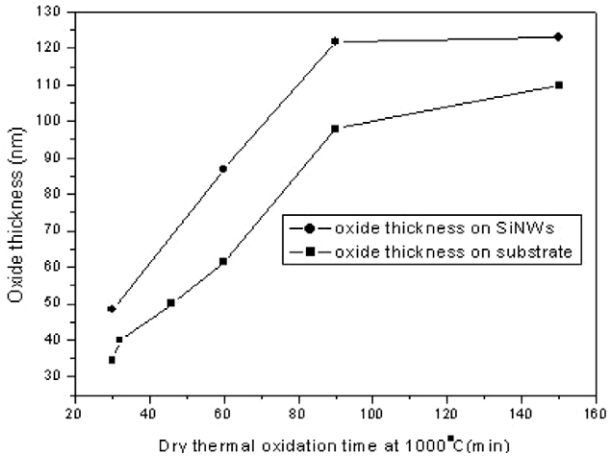

Figure 4. Oxide thickness as a function of oxidation time.

and SiNWs have not yet been fully formed. This anomalous result can be explained by two factors: (1) different crystal orientation, and (2) small geometry impacting the oxidation process. To investigate this anomalous oxidation effect further, we performed numerical simulations using the SUPREM-IV simulator.

The numerical simulation results showed that the initial geometry or the shape of the SiNW has a strong influence on the oxidation rate. The oxidation fronts with different shapes corresponding to a convex surface, a planar surface, and a concave surface are different. With other conditions kept constant, more oxygen may reach the interface in the convex configuration, leading to a faster oxidation rate. The oxide thickness on SiNWs in figure 4 is just on the convex curves of the SiNWs. This effect also leads to a slower oxidation rate in the narrow region of the silicon fin, causing an elongated shape of the SiNWs with larger diameter in the vertical direction.

As shown in figure 4, it is also observed that the oxidation rate after 90 min oxidation slows significantly to a value of 0.022 nm min^{-1} on SiNWs, which is much slower than the 0.19 nm min^{-1} oxidation rate on a planar substrate. As the unit cell volume of SiO_2 is 0.045 nm^3, which is larger than that of silicon (0.02 nm^3), the oxidation process leads to an increase in the overall thickness of the wires. The newly growing oxide at the interface must push the older oxide outwards, but the resistance that it faces results in stress at the silicon/oxide interface. It was predicted that a viscous flow may occur and the stress may be relieved in the range of 22 s for 1000 ° C for dry oxidation. However, the relaxation in SiNWs becomes more difficult, since the stress at the Si/SiO_2 surface is larger. The smaller the radius of the SiNW, the more dramatic the deformation of the oxide. In our experiments, the smallest SiNW is around 9 nm in diameter and the increased stress cannot be decreased by the viscous flow of the oxide. Therefore, the stress will then restrain further oxygen diffusion through the covered oxide layer into the reaction interface

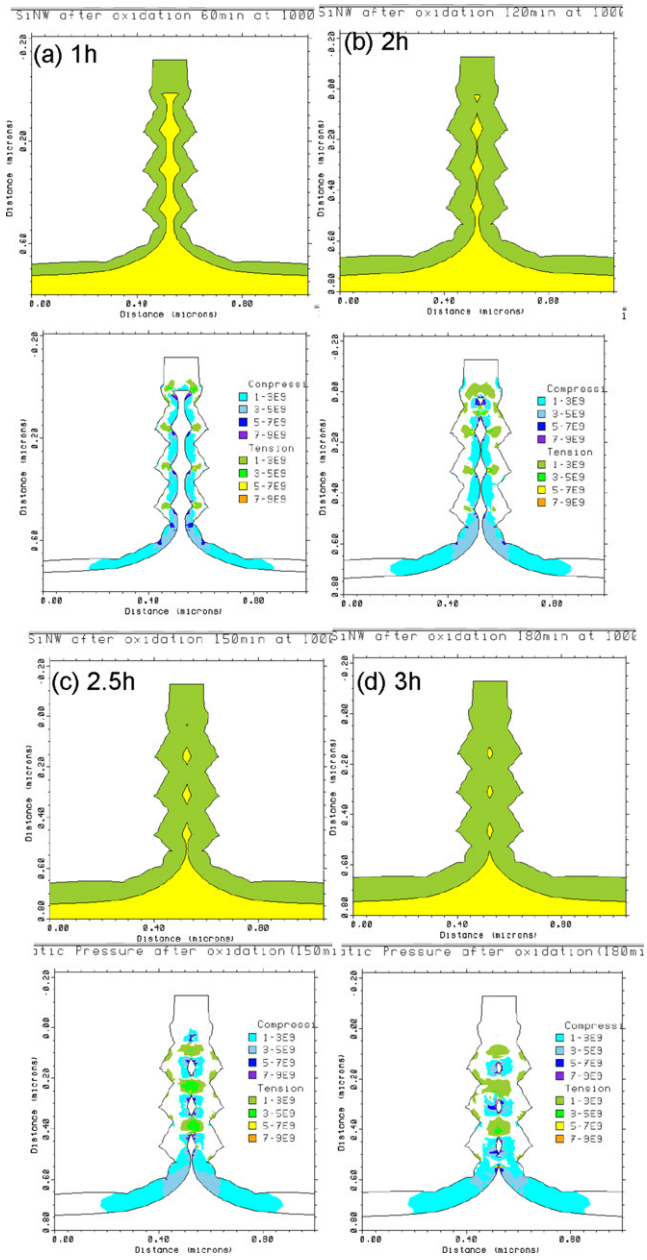

Figure 5. T-SUPREM-IV simulation result with various oxidation times and the corresponding mechanical stresses.

and the oxidation at the interface is prevented [11]. It is this increased stress that is the main mechanism responsible for slowing down the oxidation rate in the self-limiting regime. A model explaining the stress effect is provided below:

$$D = D_0 \exp(-p_{SiO_2} V_d / kT). \quad (1)$$

In equation (1), D_0 is the effective diffusion coefficient, p_{SiO_2} is the hydrostatic pressure, k is Boltzmann's constant, T is the absolute temperature and V_d is the activation energy. In the case of a SiNW, the stress is much higher than in a planar silicon surface, as the stress is compressive and 2D expansion in the volume is more difficult. This observation agrees with what was pointed out in [12] where the that slower oxidation rate becomes more prominent with longer oxidation times.

The 2D process simulation with T-SUPREM-IV results is shown in figure 5. In the initial oxidation ($t < 60$ min), the SiNWs have not formed and the stress along the sidewall is around 2×10^9 MPa. When the oxidation time is prolonged to 2 h, the SiNWs are almost formed and the stress is around 4×10^9 MPa. The further oxidation to 2.5–3 h results in a slight decrease in the size of the SiNWs. Also, simulations indicated that the stress along the Si/SiO_2 interface is around 8×10^9 MPa at almost the smallest radius, which is larger than previously reported values in [11] and [13]. This higher stress value is mainly due to higher temperature used and the thicker oxide grown in our simulations. Also, unlike most reported SiNW fabrication processes that use electron-beam lithography to form silicon lines with widths below 50 nm before reaching the self-limiting oxidation, we start with silicon fins with linewidths around 100 nm. Then, using only one single step of self-limited oxidation, we need a longer oxidation time to obtain the SiNWs with final diameters around 10 nm. From our simulation results, it is interesting to note that there is tensile stress in the neck position of the fin structure located between two vertically stacked SiNWs, when the oxidation time exceeds 2 h and SiNWs have formed.

4. Conclusion

We presented a simple top-down approach for fabricating vertically stacked multiple SiNWs using inductively coupled plasma etching of a scalloped sidewall and self-limited oxidation. By using higher temperatures to grow thicker oxides, the initial dimension can be increased, reducing the need to have precise lithography. Using thermal oxidation at 1000 °C and silicon fins of initial dimensions ~100 nm, the mechanical stress is 8×10^9 MPa and SiNWs with 10 nm diameter can be controllably formed. This proposed fabrication technique offers promise for the integration of nanoscale SiNWs into 3D structures and holds significance for future use in electronic, photonic and sensing systems [14–19].

Acknowledgments

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