ECS Journal of Solid State
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To cite this article: Vy Thi Hoang Nguyen *et al* 2020 *ECS J. Solid State Sci. Technol.* **9** 024002

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ECS Journal of Solid State Science and Technology, 2020 **9** 024002
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The CORE Sequence: A Nanoscale Fluorocarbon-Free Silicon Plasma Etch Process Based on SF_6/O_2 Cycles with Excellent 3D Profile Control at Room Temperature

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This study focuses on the development of a fluorocarbon-free directional silicon etching process, called CORE (Clear, Oxidize, Remove, and Etch) in which a switching sequence of SF_6 and O_2 is operated at room temperature. This distinguishes it from the old-fashioned room temperature and cryogenic mixed RIE processes as CORE enables a higher selectivity, creates pattern independency of etching profiles and works excellent at room temperature. The CORE process resembles the well-known SF_6-based Bosch process, but the usual C_4F_8 inhibitor is replaced by O_2 oxidation with self-limiting characteristics. Therefore the CORE result is similar to Bosch, however has the advantage of preventing the pile-up of fluorocarbon deposits at the topside of deep-etched or nano-sized features. At the same time, process drift is minimized as the reactor wall is staying perfectly clean. The CORE process has shown an excellent performance in high aspect ratio (3D) nanoscale structures with an accurate and controllable etch rate between 1 and 50 nm min^{-1} (and SiO_2-selectivity of ca. 35) using the etch-tool in the RIE-mode. By adding the ICP source (DRIE-mode), a directional etch rate up to 1 μm min^{-1} (at 50 sccm SF_6 flow) and selectivity >200 for SiO_2 is possible.
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Manuscript submitted October 24, 2019; revised manuscript received December 5, 2019. Published January 7, 2020.

Ever since the invention of the transistor in the Bell laboratories (in 1947) and the introduction of lithographic reproduction tools for integrated circuits (in 1958), the sizes of patterns have been downscaled to create more functionality or computing power on a smaller chip size. Till recently, focus has been directed to upgrade the lithographic tools to decrease the lateral resolution or improve etch tools/recipes to transfer lithographic defined patterns deeper into the bulk forming 2½D etched material (More Moore). However as this approach is predicted to reach the ultimate limit within a few years, only novel materials (Beyond Moore) and system diversity like sensor integration or truly 3D techniques (More Than Moore) can further increase chip density or functionality per cubic centimeter. To have a better understanding of current technology drivers and near future trends or needs, the reader is invited to read a few of the latest review papers on these subjects and the final International Roadmap for Semiconductors ITRS 2015 or the more recent IRDS roadmaps.[1–7]

In the early years of plasma etching, various etch gases were introduced to transfer patterns from resist-mask into silicon.[8–10] In general good directionality could be achieved, but at the expense of a poor mask selectivity. Within these years, gases like HBr and Cl_2 became the standard choice in semiconductor plasma processing and kept their position ever since. However after SF_6 was introduced and showing its high silicon etch rate potential, it became more popular in the MEMS community, especially when mixing the SF_6 with oxygen showed good directionality (less undercutting).[11] Even though the $SF_6 + O_2$ plasma mixture shows a reasonable selectivity and profile control at room temperature, it comes with a weak sidewall protection that barely can cope with the higher fluorine pressure needed for the requested high etch rates in MEMS fabrication. Furthermore, the profiles are pattern dependent (i.e. smaller trenches generally show a more positive tapered profile than the wider ones[12–14]), which is probably the most bothersome fact and partly explains why the semiconductor industry has not yet embraced this technique.

Mixed mode—Cryogenic etch.—Lowering the substrate temperature below −80 °C improves the sidewall oxygen protection as the silicon oxy-fluoride reaction products start to freeze at the surface.[15] This method enables high silicon etch rates with a good directionality and is commonly known as cryo etching (Fig. 1 top).[16–20] However, the pattern dependency cannot be removed in this way (Fig. 1 top-right) and mixed mode etch recipes are typically highly design specific and the recipes often need cumbersome optimizations. So, in general the cryogenic etch gives an acceptable performance, yet it needs proper and time-consuming fine-tuning when complex (MEMS) patterns are requested.

Switched mode—Bosch sequence.—With the introduction of the patented 2-steps Bosch process in 1994 (we call it DEM, which stands for Deposit and Etch Many times), the switched etching of complicated MEMS structures gained popularity and totally overruled the cryogenic etching within a few years.[21,22] It uses the sequential inlet of inhibitor and etch-gas. Although the cycle creates prominent scallops, it also forms nice directionality and the pattern dependency almost vanishes, which makes process optimization relatively easy (Fig. 1 bottom). Moreover, a higher selectivity than mixed mode is possible because bias is only applied during the etch step (Fig. 2 left) and not continuously.

Switched mode—DREM sequence.—The DEM sequence can be further improved by decoupling the bias from the etch step and forming the 3-steps DREM process (Deposit, Remove, and Etch Many times). Consequently, the bias time can be set just long enough to remove the bottom of the etching feature (Fig. 2 right). In this way, the mask selectivity can potentially reach infinity.[23] This DREM procedure is in fact an improved version of the 1986 patent by Okudaira, but using C_4F_8 instead of CCl_4 and a better separation between the bottom remove and etch steps.[24]

A familiar characteristic of directional plasma etching is that the etch rate decreases with the increasing etch depth and it is specifically pronounced for high aspect ratio features (holes and trenches). For the switched sequence this so-called RIE lag will result in scallops that are getting smaller and smaller for every next etch cycle further down the trench. To counteract this lag effect, the DREM sequence is able to increase the etch time of the individual cycle (called time ramping in Fig. 2 right). In this way, scallop sizes are programmed to become uniform throughout the etch process and high aspect ratio structures above AR = 50 with a minimum of profile distortion are relatively easily achieved.[23] Furthermore, 3D silicon sculpturing has become straightforward; a procedure called

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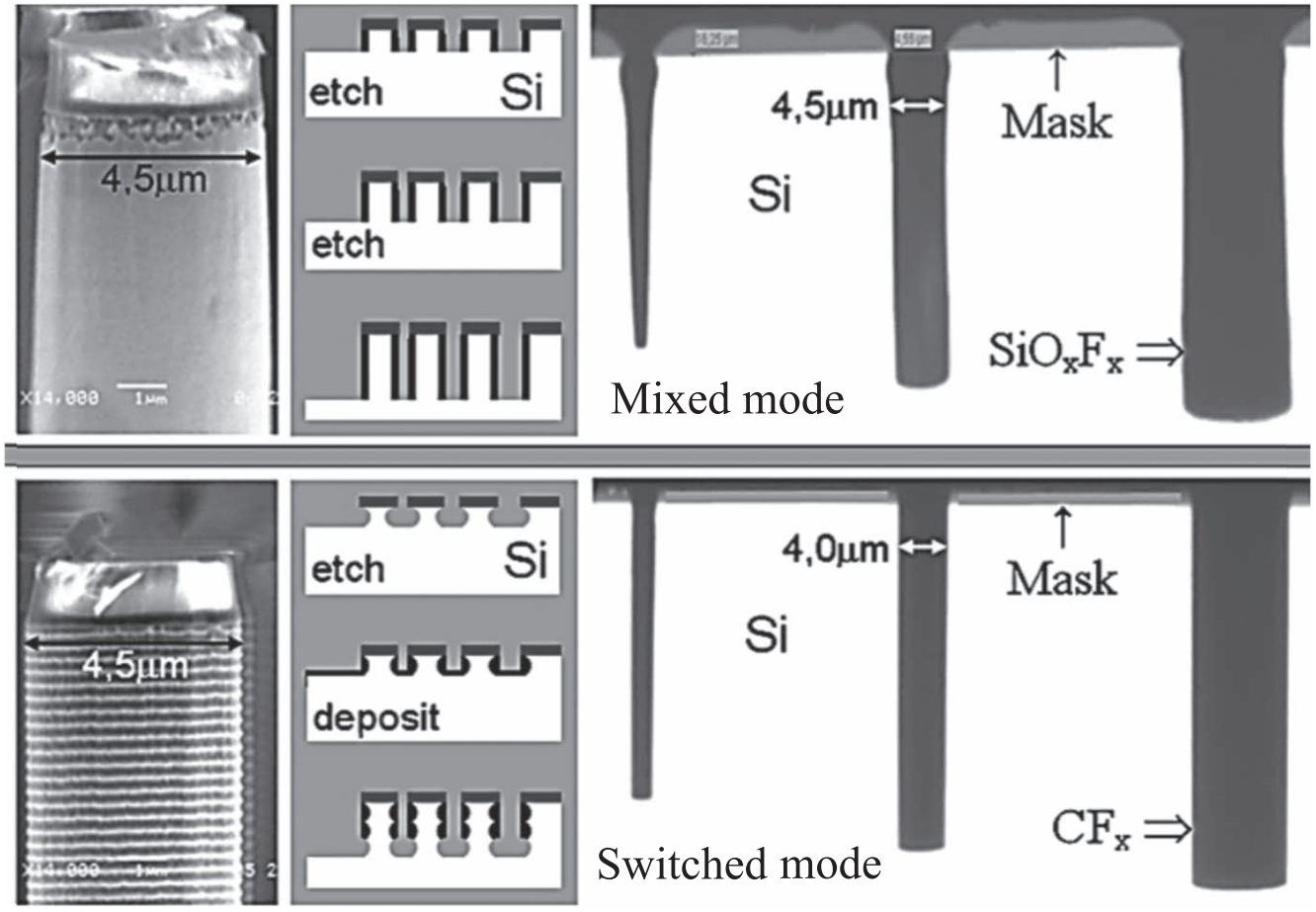


Figure 1. Cross-sectional views of trenches etched in mixed-mode versus switched-mode DRIE.[20]

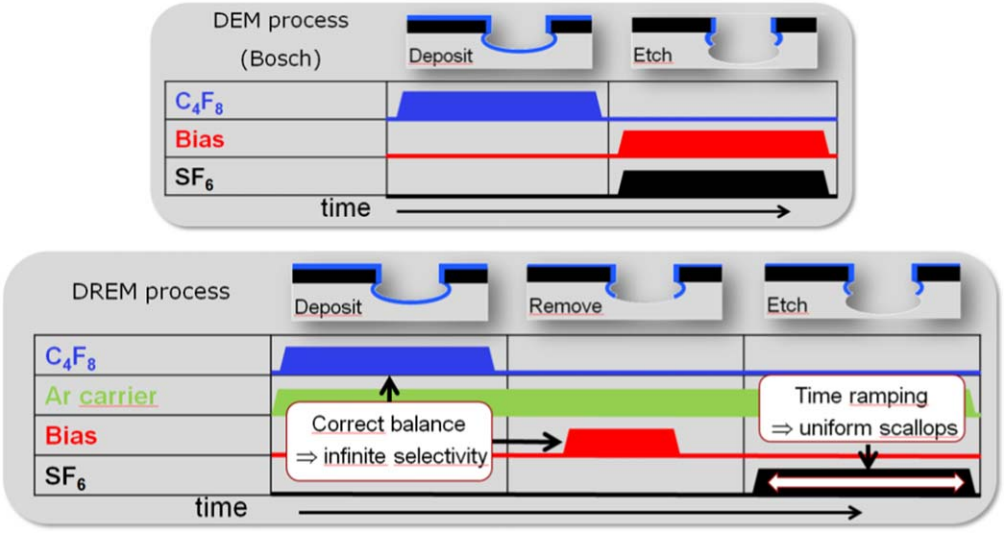


Figure 2. Process representation of the 2-steps DEM and 3-steps DREM sequences.

DREM within a DREM, because it is basically the original DREM loop chopped into a bigger DREM loop. Using this concept, silicon sausages, fences, or stacked perforated membranes are now considered to be standard manufacturing.[25–28]

Switched mode—DREAM sequence.—Like all processes derived from the 2-steps Bosch process, the 3-steps DREM process comes with a flaw: trenches tend to close at the entrance due to the pile-up of fluorocarbon (clogging) as illustrated in Fig. 3 top left, which limits the fabrication of nanoscale structures and deep trenches or holes. The consequence of a closing entrance is that the smaller dimension will be copied downwards the trench and consequently the profile becomes more positive tapered and eventually halts with proceeding etch time (Fig. 3 encircled area). This pile-up can be prevented by proper tuning, but this is time-consuming. A more appropriate approach is to introduce an

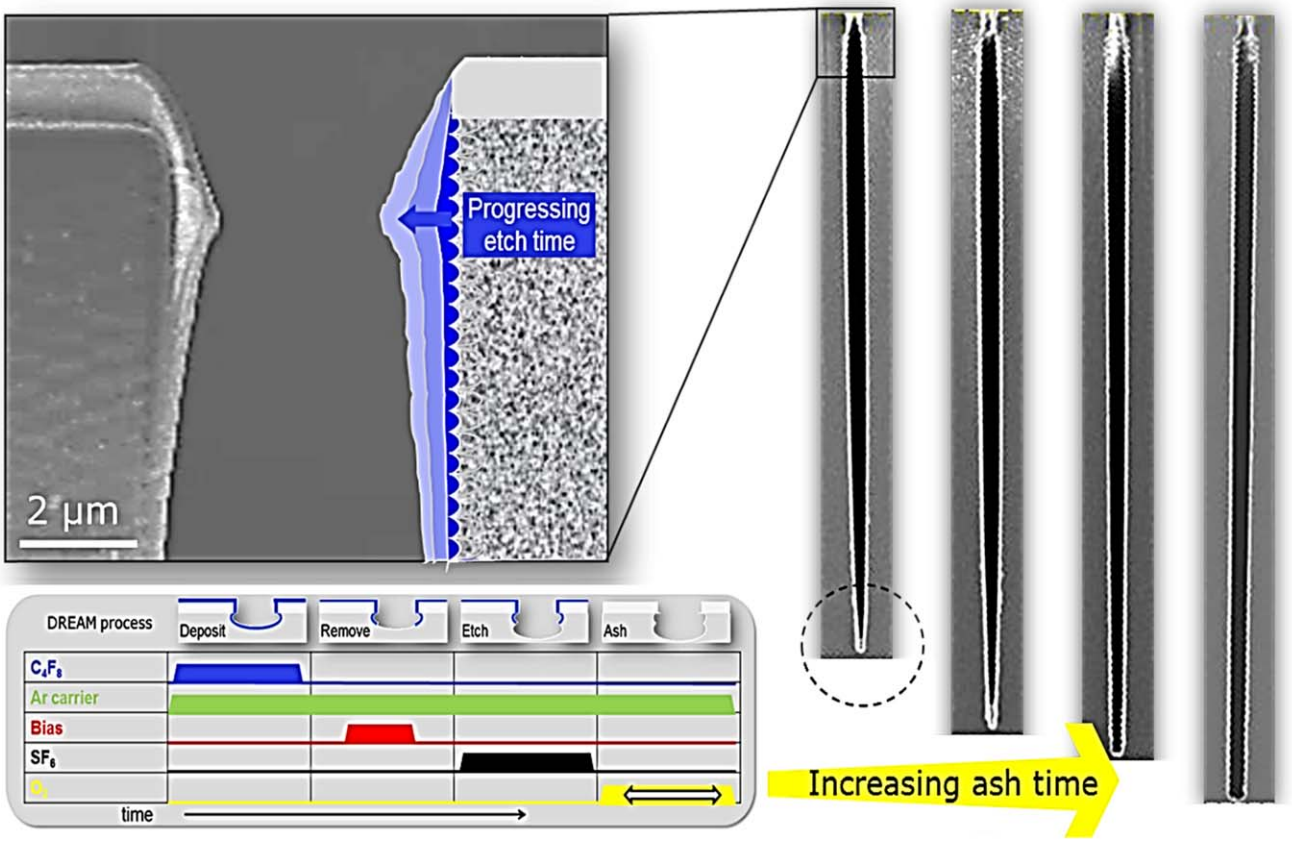


Figure 3. DREAM (Deposit, Remove, Etch, Ash Many times) sequence to prevent neck clogging (blue) and to improve directionality.

additional ash step, which takes care of the remaining fluorocarbon deposit directly after the etch step (Fig. 3 bottom left) and the 4-steps DREAM (Deposit, Remove, Etch, Ash, Many times) procedure awakes.[29] In this way the next deposition step starts with a clean sidewall and trench closing is prevented (Fig. 3 right). Again, the DREAM sequence can be part of a bigger loop to enable the manufacturing of high-quality 3D structures: the DREAM within a DREAM strategy. An additional benefit arrived from the DREAM sequence is that the tool is more protected against process drift from polymer pile-up. This is because the ashing step not only cleans the trench entrance but also the reactor walls. Of course, due to the ashing plasma we rather prefer e.g. SiO_2 than resist as the pattern transfer mask. The DREAM sequence slightly resembles the dual sidewall protection approach as proposed in 2000 by Ohara, yet following a different philosophy.[30,31]

Let us capture the previous DRIE techniques in a single picture (Fig. 4): **Mixed mode** generally shows low mask selectivity with some undercut, smooth but size dependent profiles and asks for time-consuming process development. Nevertheless—when solely using **O inhibitor**—mixed mode is clean with low process drift and is tool-friendly; the tool is easy to maintain. **FC inhibitor** causes process drift and reactor contamination, which needs frequent and time-consuming cleaning and conditioning procedures. Most FC gases are also more expensive and environment unfriendly, thus scrubbers are needed. However, the switched mode is operator/process friendly and creates design freedom (due to the pattern-independent slopes of etching features) and 3D options.

To move a step closer to an ideal process there is a need to combine the maintainability and sustainability from the mixed oxygen process with the robustness and design freedom from the switched fluorocarbon process. A proper method is found by replacing the C4F8 inhibitor gas from the DREAM sequence into O_2. This also has the advantage of addressing at least part of the quest to find environmental sustainability by exchanging the environmental non-green C4F8 for perfectly green O_2. The rest of this paper will concentrate on this novel process called CORE (Clear, Oxidize, Remove, and Etch).

Experimental

The silicon etching system used in this study is the SPTS/Pegasus DRIE, which facilitates switched mode and RIE mode. The system has been dedicated for SF_6/O_2 based plasma etching solely and has no prior fluorocarbon history. This fluorocarbon-free chamber is needed to ensure the absence of any contamination or influence on the fragile oxygen plasma oxidation that is required for the CORE sequence. The system is much like the Alcatel/Adixen AMS 100 SE DRIE system that has been described extensively in a previous review paper, but lacks the cryogenic option.[20]

Silicon ⟨100⟩ wafers (150 mm diameter, 675 μm thick, 5–10 Ωcm (i.e. 9–4½ * 10^{14} cm^{-3}), phosphorous-doped n-type) are prepared with 1.5 μm thick resist patterns (AZ MIR 701 DUV resist from MicroChemicals) and exposed using a maskless aligner (MLA150, Heidelberg) to create patterns above 400 nm. For nano-sized patterns between 30 and 100 nm, a 100 kV electron beam writing system (JEOL JBX-9500FSZ) scanning with 10 nm steps is used. Positive tone e-beam resist ZEP520A (ZEON) having a thickness of 145 nm is spin-coated for 60 s at 4000 rpm followed by a bake for 3 min at 180 °C. During the electron exposure current is set at 12 nA with 10 nm spot size and dose between 293 $\mu C\ cm^{-2}$ (30 nm lines) and 263 $\mu C\ cm^{-2}$ (100 nm lines). Exposed samples are developed for 180 s with ZED-N50 (n-amyl acetate) and rinsed with Iso-Propanol Alcohol.

The patterned wafers are cleaved into 1 cm × 1 cm chips and individually mounted on a silicon carrier wafer using Galden® PFPE fluid (Solvay Solexis SpA) for sufficient thermal contact or only to

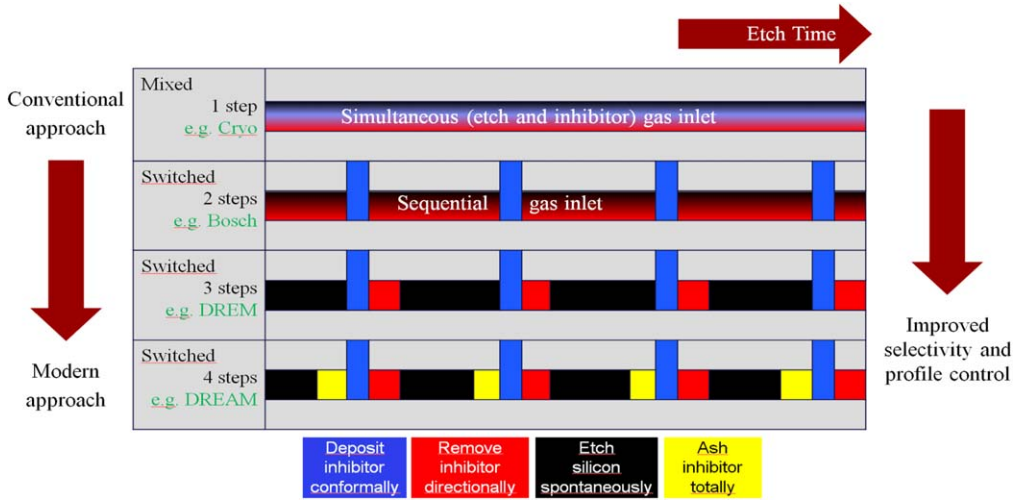


Figure 4. Resume of all the established (D)RIE modes.

fix it.[32] As the current study is aiming at nanoscale accuracy useful for the semiconductor industry, the etch tool is put in the RIE-mode and set for low etch rate (between 1 and 50 nm per minute for sufficiently tight dimensional control). This is done by adjusting the SF_6 flow (ca. 15 sccm) and the platen power (ca. 10 W) accordingly. The oxidation step is set for 50 sccm O_2 flow. The SF_6 MFC has a maximum of 50 sccm and, thus, providing an accuracy of better than 1 sccm. After the etching, the Galden heat transfer fluid is wiped gently from the backside of the sample with alcohol sprayed on a tissue and the sample is cleaved manually using a diamond pen for SEM analysis.

To determine the optical thickness of growing films less than 5 nm, the film is scanned by 690 wavelengths between 210 nm and 1690 nm to get the corresponding Psi-Delta values (Variable Angle Spectroscopic Ellipsometer M2000XI-210, J.A. Woollam Co.) at standard cleanroom conditions (22.5 °C and 45% humidity). 5 different impinging incident angles (59, 60, 61, 62, 63 degrees) and 5 s acquisition time are used to improve accuracy further. This data is analyzed and fitted with inbuilt models as provided by Woollam. The most convenient model to fit the growing oxide films in this study has been found to be an interfacial layer resembling silicon monoxide film (Intr_JAW) on top of silicon (Si_JAW). So we assumed the film to be having a known refractive index spectrum and only fitting the optical film thickness for the best root mean square error (RMSE) value. Even though this SiO-equivalent might present faulty values as the growing film most likely changes its composition in the initial stages resulting in a graded index.[33–35] And it will for sure incorporate a water layer, it has the advantage of making the analysis far simpler while still keeping good statistical parameters (high confidence level of the presented variance and low RMSE). So, the ellipsometric measurement is accurate, but the interpretation (or analysis) can be very wrong. Nevertheless, independent of the model used, the observed trends are correctly presented and can be trusted.

The CORE recipe always starts with a non-selective 60 s so-called "DeDamage" etch in front (15 sccm SF_6 at 100% Throttle → 0.5 mT and 10 W Platen) to remove any wafer process history (e.g. resist scum and native or subsurface plasma oxide) without etching the silicon or harming its subsurface too much. The CORE sequence is specifically aiming at the nanoscale and operates without coil power (i.e. ICP source) or plasma focusing funnel and outer electromagnet at 10 A. For higher etch rates and improved selectivity, the ICP source can be added (DRIE-mode), but care should be taken to prevent reactor wall sputtering (e.g. by using a Faraday cage). That is, the normally strong Al_2O_3 ceramic of the reactor wall can be transformed into the much weaker AlF_3 that subsequently sputters onto the wafer causing roughening (e.g. for 100 sccm and 2 mT Ar and 2 kW we observed 0.3 nm min^{-1} sputter-deposition). The silicon carrier is electrostatically clamped with 10 Torr Helium backside pressure at 20 °C with platen down even though the nanoscale CORE performs excellent without backside cooling or clamping as well. The main reason is that the oxidation step improves with increasing temperature and therefore thermal runaway is prevented when the wafer-temperature rises. This is another disadvantage of the Bosch and cryogenic techniques where a slight increase in temperature will slightly reduce the passivation that will slightly increase the etch rate and increasing the temperature even further, i.e. thermal runaway.

Finally, to stress the issue, it is advised not to use any fluorocarbon-based chemistries in the etch tool (and limit the excessive use of Galden oil). These processes have shown to affect adversely the CORE etch performance. Fluorocarbon residues are very persistent and tough to remove even after prolonged cleaning plasma (O_2 or NF_3) and might cause process drift. For example, trying to perform the CORE sequence on an identical DRIE tool—but mainly used for Bosch processing—gave unsatisfactory results (lot of sidewall erosion) even after several hours of O_2 plasma cleaning.

Results

Even though switched etch processing that uses oxygen for the sidewall passivation is already known for a decade, these existing techniques rely on cryogenic temperatures in order to freeze the silicon etch products (SiO_xF_y) and to enable sufficient profile control.[36,37] The current innovation discusses the use of O_2 pulses to oxidize surfaces (or rather terminates the silicon surface atoms with atomic oxygen) conveniently at room temperature in a fluorine-based chemistry to create high-raised silicon structures. The proposed room temperature oxidation technique has its roots in the early years of continuous (or mixed) mode plasma etching.[11]

The procedure to find the correct profile is following the Black Silicon Method as described extensively in literature before, and basically boils down to 3 steps[12,20]: **1**) determine the spontaneous silicon etch rate for the whole SF_6 plasma spectrum (e.g. gas flow, pressure, plasma power) and select an appropriate etch rate (e.g. for nanoscale etching around 20 nm min^{-1}), **2**) switch on the oxygen inhibitor to suppress the etch to almost zero, and **3**) add or adjust the bias to increase the ion bombardment and create the requested directionality. For **1**, a convenient continuous etch rate of 15 nm min^{-1} is found for 15 sccm SF_6 flow at 2% throttle position (resulting in 50 mTorr process pressure) and 10 W platen power. For **2** we used 50 sccm O_2 flow, also at 50 mTorr and 10 W platen power, to block the silicon etching. And for **3** we used 5 sccm SF_6

with APC throttle valve fully opened (giving a pressure below 0.2 mT) to clear the bottom.

The initial test was simply transforming the DREAM sequence into CORE (Fig. 5 left) and coarse-tuning the observed profile for directionality and to form big scallops that are easily detectable by SEM. Fig. 5 right shows the result after performing a sequence of 5 cycles. The 5 scallops of around 60 nm in size are correctly shaped and without severe erosion such as etch pits. The following sections will investigate the impact of the individual steps of the CORE sequence on the final etch result.

Clear step.—The Clear step might be the surprising step in the CORE cycle, but it is found to be crucial to include this reactor clearance step in order to get a reliable etched result. Basically, the step is performed with an oxygen sweeping flow (to prepare the mass flow controller for the upcoming Oxidation step), but without plasma. The turbo throttle valve is fully opened to ensure the fastest removal rate of silicon etch gas residue left inside the reactor. The step prevents the SF_6 plasma that has created SiF_x products during the previous Etch step to come into contact with the O_2 plasma of the next Oxidize step. This contact would annihilate part of the incoming oxygen radicals by the leaving fluorine radicals and, therefore, the passivation would be compromised. A second possibility of arriving oxygen radicals that briefly meet the departing silicon fluoride is that they may combine into silicon-oxide species. The latter are nonvolatile and will contaminate the etching, for instance causing surface roughness; the well-known black silicon.[37]

Samples with a 1 micron diameter pillar array were etched and observed using SEM with a fixed setting (e.g. 3 kV high voltage and 400 KX magnification). As observed in Fig. 6, when the C-time is zero seconds, which means that there is no Clear step at all, the profile is strongly undercut as oxygen radicals are lost. Only after at least 4 s C-time, both plasmas (SF_6 and O_2) is separated correctly and the SEM images look alike.

Oxidize step.—Obviously, the plasma oxidation is essential to enable a directional switching plasma sequence. It is assumed that the silicon surface is highly fluorinated after the Etch-step and the fluorine-terminated silicon will be preserved during the Clear step even while sweeping oxygen molecules are already present. It is only after the plasma is started that (atomic) oxygen radicals are formed. They will start to replace fluorine radicals and create an oxygen-terminated silicon surface.

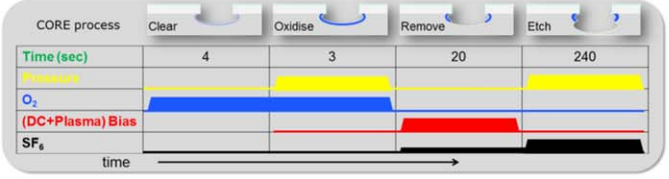
Figure 7 shows the effect of additional oxidation (O-time = 3, 4, 5, and 6 s) on the profile at a fixed E-time of 8 min It is observed that the scallops only become smooth and correct when at least 5 s O-time is taken. Further experiments (not included) showed correct scallops for the combination O-time versus E-time: 2 s → 2 min, 3 s → 4 min, 4 s → 6 min, 5 s → 8 min, 6 s → 10 min, 7 s → 12 min, and 8 s → 14 min. ***This gives us the first CORE design rule: every extra second O-time will enable 2 min extra E-time.*** However, above 8 s O-time, this linear rule doesn't apply anymore. For instance, to enable 20 min E-time it is found that instead of 11 s, at least 25 s O-time is needed. More about this abnormality, which is basically caused by the self-terminating feature of the oxidation process, will be presented in the Discussions section.

Remove step.—The removal at the bottom of etching features is the most crucial step for creating the requested directionality. The question is how we can raise the bias and ion energy only during this step and with only a single power source (remembering that the ICP source is not used to increase accuracy and to prevent wall sputtering). The answer lies in the effect of the reactor pressure on the plasma potential. As can be found in many in-depth textbooks, the plasma potential is a function of the pressure; the lower the pressure, the higher the potential.[38] With this in mind, we can manipulate the plasma potential simply by adjusting the reactor pressure. This is accomplished by opening the throttle valve completely in this step. An additional benefit of this approach to get adaptable ion energy is that at the same time the ion angular distribution function becomes much sharper as ion collisions in the dark space vanish and accurate process synchronization is guaranteed.[23] On top of this plasma potential, the usual mentioned DC self-bias is still present and the total kinetic energy gained by the ions accelerated in the dark space facing the wafer will be the summation of both potentials: V_p+V_{DC}. (Note: all the other surfaces —grounded and floating—will have to deal with V_p only. Basically, this means that V_p can still cause reactor wall sputtering).

While performing the Remove step, it makes sense to assume that the removal rate of the passivation layer will increase linearly with the removal time and that this step can be halted when all the passivation has gone. Figure 8 shows the result of increasing R-time at a fixed CORE setting (C-time = 4 s, O-time = 8 s, and E-time = 8 min). The result for 5 s R-time is still rather rough (i.e. black silicon or micro grass appears) at the features bottom because not all the passivation has been removed, but after 25 s R-time it is correct as expected. Indeed, checking also other O-time settings, we found a correct smooth bottom when the R-time was set to roughly 3 times the O-time for 8 min E-time. ***This provides us the second CORE design rule: every second of O-time needs 3 s R-time.*** Beyond 25 s R-time, the bottom becomes a bit rougher again. The latter is probably because the additional R-time starts to damage the silicon below the passivation.

Etch step.—Till now we have focused on the normal etch rate and assumed that the lateral etch will follow in the same way as many papers claim: pure SF_6 plasma etches isotropically. However, only in a perfect diffusion-controlled (viscous) isotropic etch (e.g.

CORE	Time	Pressure	SF_6	O_2	Power
Step	s	mTorr	sccm	sccm	W
C	0-10	~0	0	50	0
O	3-6	50	0	50	10
R	5-30	0.2	5	0	10
E	120-480	50	15	0	10



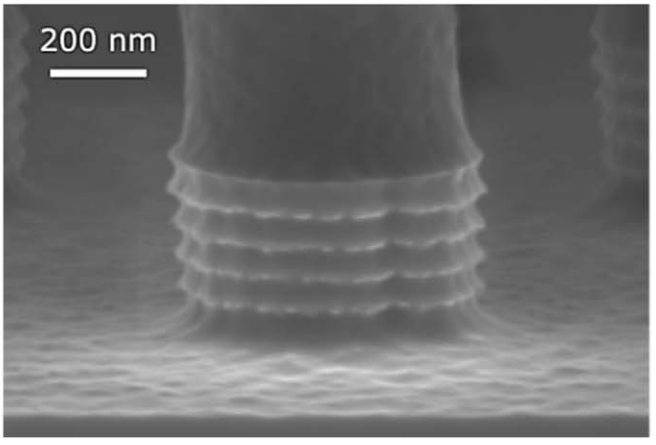


Figure 5. (Left) Coarse-tuned CORE cycle used as the center point run in the designed experiments.(Right) 5 well-controlled regular 60 nm scallops along silicon pillars with resist still on top.

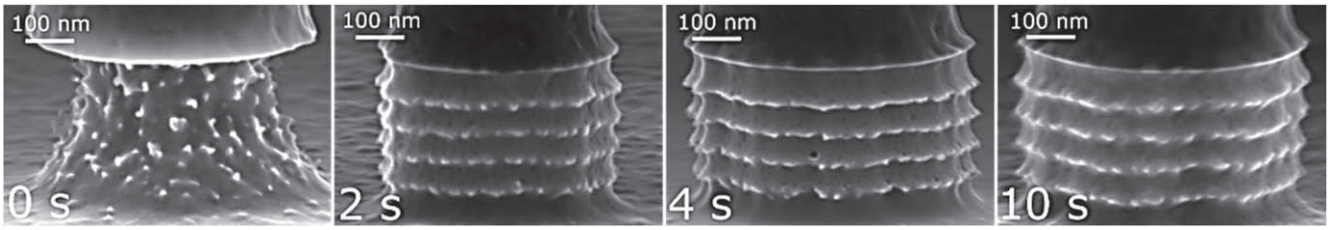


Figure 6. Effect of varying the C-time. From left to right: C-time = 0, 2, 4, and 10 s with O-time = 3 s, R-time = 20 s, and E-time = 4 min always.

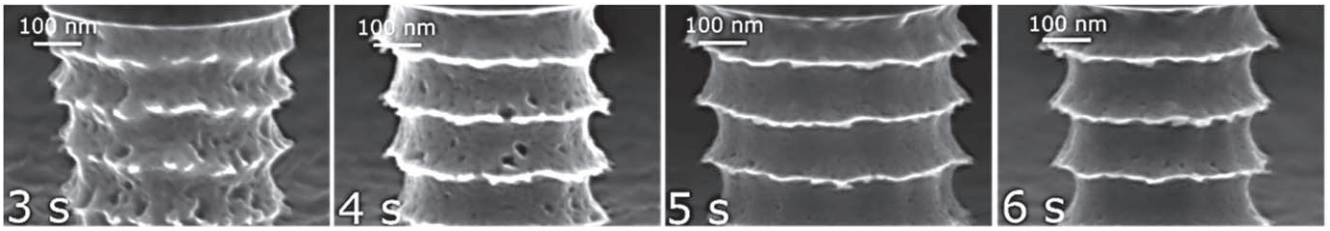


Figure 7. Prolonged O_2 oxidation time saturates the sidewall protection. From left to right: O-time = 3, 4, 5, and 6 s with C-time = 4 s, R-time = 20 s and E-time = 8 min always.

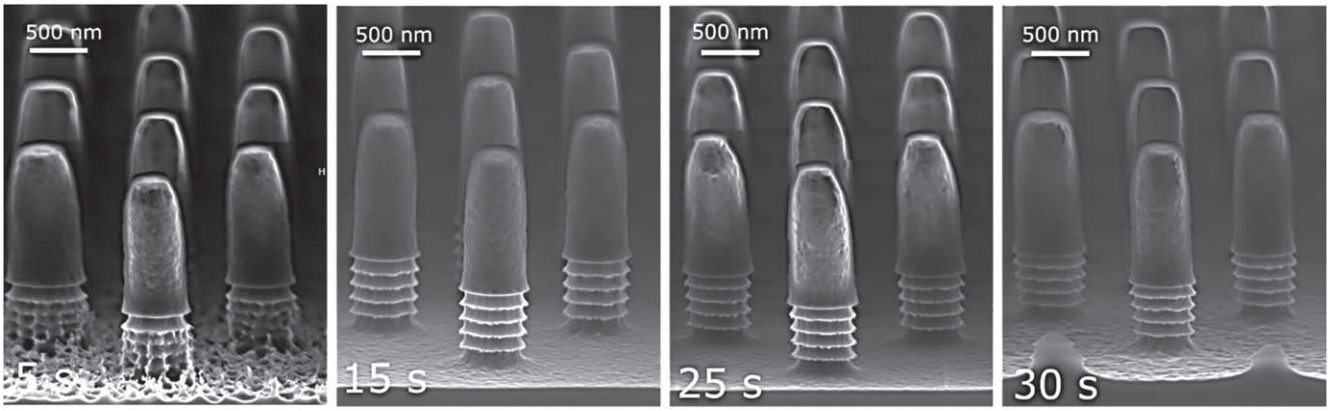


Figure 8. Prolonged R-time clears the bottom protection. From left to right: R-time = 5, 15, 25, and 30 s with C-time = 4 s, O-time = 8 s, and E-time = 8 min always.

liquids), the horizontal etch (undercut) will match the vertical etch (etch depth) as depicted in Fig. 9 left. In case of free molecular transport, which is close to expectation in DRIE, there cannot be etching directly underneath the mask and ideally a semicircle will form (Fig. 9 right). In reality the result is bit of both: the lateral etch is between 2 and 3 times slower than the normal etch (Fig. 9 mid). Surface transport might be responsible for the result. For the plasma setting used in the current CORE sequence, we found that the undercut is around 5 nm when the etch depth gain per cycle is 10 nm. ***This brings us to the third CORE design rule: the undercut is the normal etch per cycle divided by 2.***

As already stated in the first CORE design rule, the maximum allowed E-time is fixed by the O-time. But we did not yet show implicitly what happens if the E-time exceeds its optimum value. Figure 10 shows the result of the CORE sequence for increasing SF_6 etching time at 3 s O-time. Here, we highlight the moment where the fluorine pressure starts to degrade the scallop's oxide protection and causing so-called sidewall pitting. Only by keeping the etch time at or below 4 min, the scallops are showing up virtually without pitting. Furthermore, it is observed that open field structures (the pillars in Fig. 10 top) suffer much more from sidewall erosion than enclosed structures (the trenches in Fig. 10 bottom). This is probably related

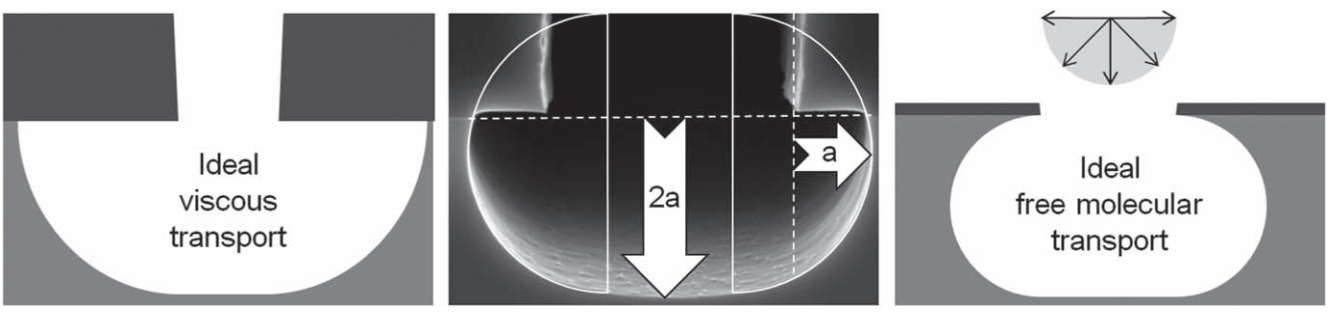


Figure 9. "Isotropic behavior" in SF_6 plasma etching of silicon. The normal etch rate is typically twice the lateral etch rate (undercut).

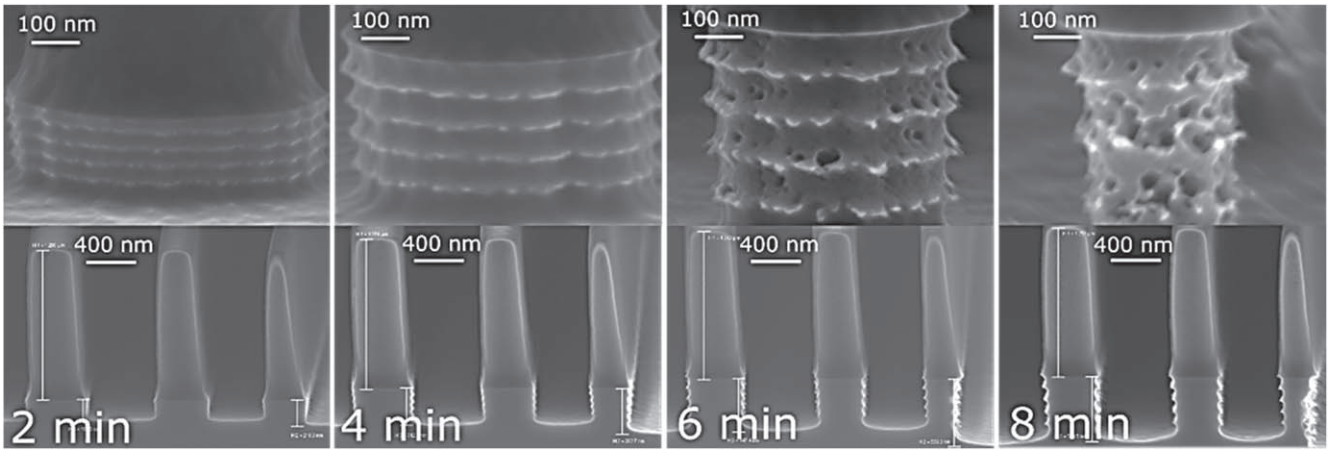


Figure 10. Prolonged SF_6 E-time degrades the sidewall protection. From left to right: E-time = 2, 4, 6, and 8 min with C-time = 4 s, O-time = 3 s and R-time = 20 s always.

to the difference in fluorine supply, e.g. due to Knudsen restriction in high aspect ratio features.[17]

The CORE cycle design rules and optimized recipe.—We are now ready to put together the design rules that control the CORE sequence for the etch rate per cycle fixed at 15 nm per minute E-time:

Rule 1: 2 min E-time needs 2 s O-time. Every 2 min extra E-time will need 1 s extra O-time until a maximum of 14 min E-time.

Rule 2: Every second of O-time needs at least 3 s R-time (for 8 min E-time).

Rule 3: The undercut is roughly half of the gained etch depth per CORE cycle.

It is noticed that when the CORE sequence is performed at an elongated E-time (>2 min), surface particles below a certain threshold of lateral size (<30 nm) will be undercut totally rendering the surface relatively smooth. The shorter the E-time, the smaller this threshold will be and this results in an increased number of particles that are able to survive the lateral undercutting. Consequently, surface roughening becomes more pronounced so that a longer R-time is required to prevent it. For E-time shorter than 1 min, we found that the bottom surface is smooth and clean only after at least 20 s O-time as presented in Fig 11. Using this fine-tuned CORE cycle, the scallop-size reduces and proper profiles emerge with smooth, straight sidewalls and minimum undercutting of resist mask (Figs. 12a–12c). This virtual scallop-free ability is very attractive for applications where surface roughness compromises the application (e.g. for imprinting or high-density trench capacitors). Furthermore, the lack of inhibitor deposits makes the CORE procedure outstanding with respect to Bosch and related techniques. CORE also outperforms the cryogenic etching, because complicated cryogenic chucks are unnecessary (Infrastructure adaptations to support the supply of liquid nitrogen can be a major roadblock for many small laboratories). Furthermore, the same recipes that perform well for microstructures are now also showing excellent performance for nanostructures down to 30 nm resolution (Fig. 12d). Note that unlike all the other samples of this study, the 1 cm × 1 cm sample with the nanostructures is taken from a silicon-on-insulator (SOI) wafer. It is also shown in the same image, due to the extreme mild plasma condition in which the etching is performed, plasma-induced silicon (sub-) surface damage is low and notching is virtually non-existing.[39,40] Consequently, over-etching—to take care of the notorious RIE lag—is not at all degrading the etched features.

CORE and profile tuning.—Even though a perfectly straight profile is probably the most requested demand in directional etching, sloped profiles are sometimes beneficial for specific applications. For example, in nanoimprint lithography, a slightly scallop-free and positive taper of the (silicon) mold will ease demolding.[41–44] The CORE sequence is able to support this request by ramping the E-time while etching proceeds. As established in the previous sections, the amount of undercutting is directly related to E-time and therefore it controls the profile. Figure 13 demonstrates the difference between a fixed E-time (left and middle) and ramping E-time (right). It is observed that the CORE sequence for a fixed E-time delivers a slightly positive taper whereas the ramping E-time is slightly negative.

CORE and mask selectivity.—Till here, only photoresist is used as a mask to create the silicon structures. Of course, resist is etched by the plasma as well and having a selectivity of ca. 10. Moreover, the use of oxygen to passivate the silicon sidewalls will inevitable

CORE	Time	Pressure	SF_6	O_2	Power
Step	s	mTorr	sccm	sccm	W
C	4	~0	0	50	0
O	3	50	0	50	10
R	20	0.2	5	0	10
E	73	50	15	0	10

Figure 11. Typical fine-tuned CORE cycle.

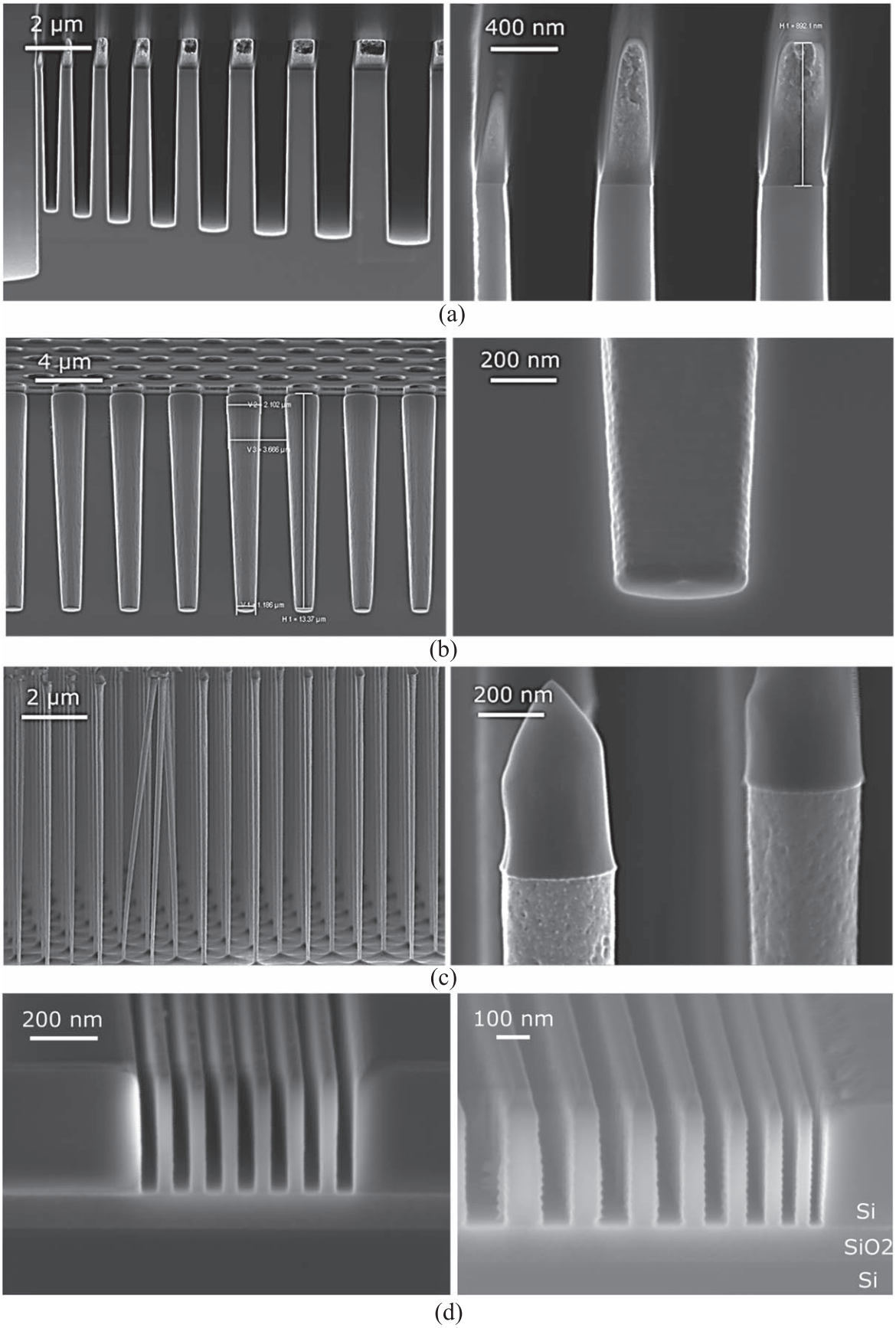


Figure 12. (a) Submicron silicon trenches and lines derived from the fine-tuned CORE sequence. (b) Submicron silicon holes derived from the fine-tuned CORE sequence. The side wall angle is ca. 2°. (c) Submicron silicon pillars derived from the fine-tuned CORE sequence. (d) Notch-free nanostructures in SOI material derived from the fine-tuned CORE sequence Left) Grating with 80 nm periodicity. Right) RIE lag test structure between 30 and 100 nm.

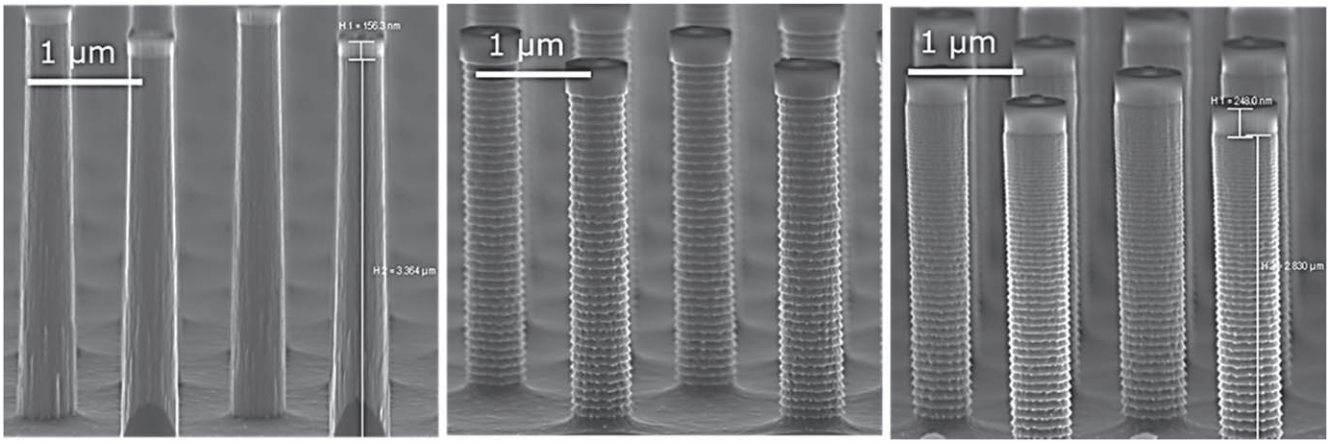


Figure 13. Profile tuning by fixing or ramping the E-time in the CORE sequence from Fig 11. Left) A fixed E-time of 73 s results in a positive taper, Center) a fixed E-time of 300 s shows a straight profile, and Right) E-time that is ramped from 70 s to 330 s with steps of 5 s during the sequence will provide a negative taper.

consume hydrocarbons and therefore the resist will slowly retract (i.e. not only at its top surface but also from aside).[45] To show this effect, in Fig. 14 a dot pattern is CORE etched using solely photoresist (left) and SiO_2 with resist still on top (right). Evidently, the pillars having only resist as mask are heavily eroded at their top while the SiO_2 pattern is nicely preserved even though the resist on top of it has clearly retracted. The reason for this behavior is the lateral etch of the resist pattern in time. While etching proceeds, the diameter of the resist dots will slowly decrease and therefore leaving the top part of the silicon pillars exposed. Consequently, the incoming ions in the final stages of the CORE etch will also attack the unprotected top part of the pillars and degrade the sidewall. A hard mask like SiO_2 is not suffering from this mask retraction effect and therefore will enable better control and shows an improved selectivity of ca. 35. Al_2O_3 is even better with selectivity around 700.

3D CORE.—Just like the DREAM sequence, CORE can handle 3D features too.[46–50] In Fig. 15 top, a total of 100 cycles of the "standard fine-tuned" CORE sequence of Fig. 11 is alternated every 10 cycles by much longer isotropic etches or undercuts (10 min at 15 sccm SF_6 and 10 W platen power). This creates a vertically modulated etch profile having a 400 nm periodicity and that consists of 10 straight cylinders separated by 9 bottlenecks. It is noticed that there is still sufficient oxide mask left. This allows for even higher aspect ratio structures. Furthermore, the number of cycles of the standard CORE sequence and the etching time of isotropic etch can be varied at will in different ways to create various 3D patterns. Fig. 15 bottom is an example of such a modified structure having shorter and longer cylinders separated by different size of bottlenecks. This demonstrates the ability of CORE process to fabricate various 3D structures, thus enable novel functionalities and better device performance in many fields.

MICRO CORE.—Besides the CORE sequence aiming at the nanoscale, it is obvious to find out how far we can push the limit to higher etch rates that are favorable in MEMS technology. Surely, the self-limitation is now a true burden as this will limit the amount of allowed etching during the E-step. To speed up the process, the ICP source is used to promote stronger oxidation, which allows a higher fluorine pressure during the E-step (Fig. 16). When the ICP source is used, the platen source can be discarded, thus removing the DC bias which improves selectivity. Figure 17 shows silicon pillars etched with the micro CORE sequence at the etch rate of 330 nm min^{-1} resulting in 113 μm depth and a selectivity of 200 towards SiO_2. Of course the higher etch rate will sacrifice the nanoscale accuracy due to the larger undercut and higher fluorine pressure at the sidewalls. Another disadvantage might be the increasing risk of reactor wall sputtering that will contaminate the etching process. A Faraday cage, with the ability of blocking the electric fields produced by the ICP source, could be used to avoid this reactor wall erosion.

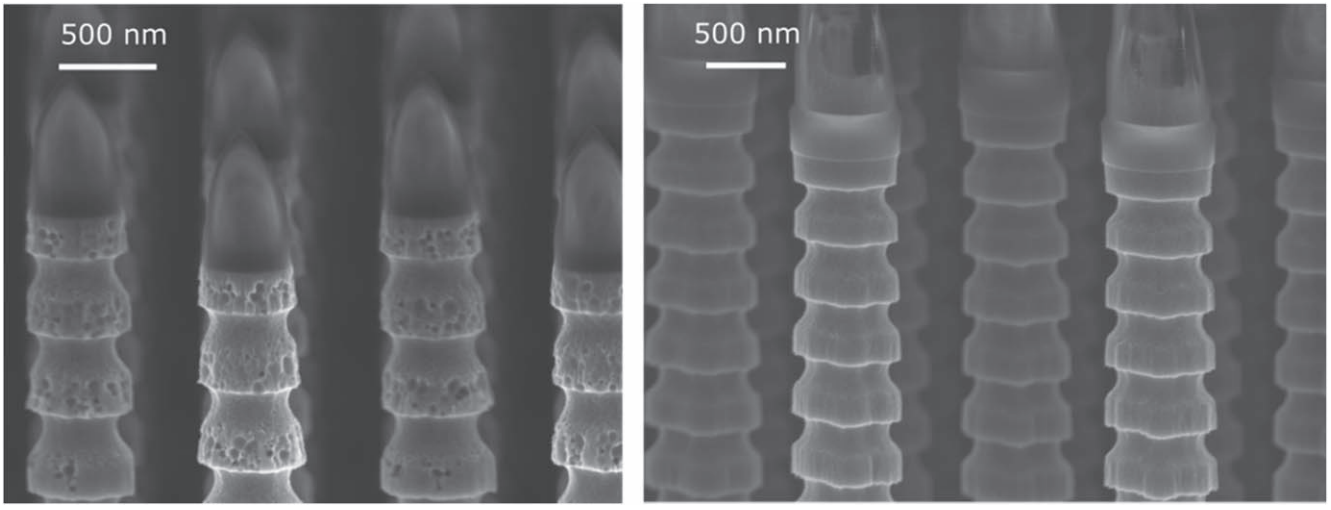


Figure 14. Submicron silicon pillars derived from resist dots only (left) and SiO_2 with resist on top (right)

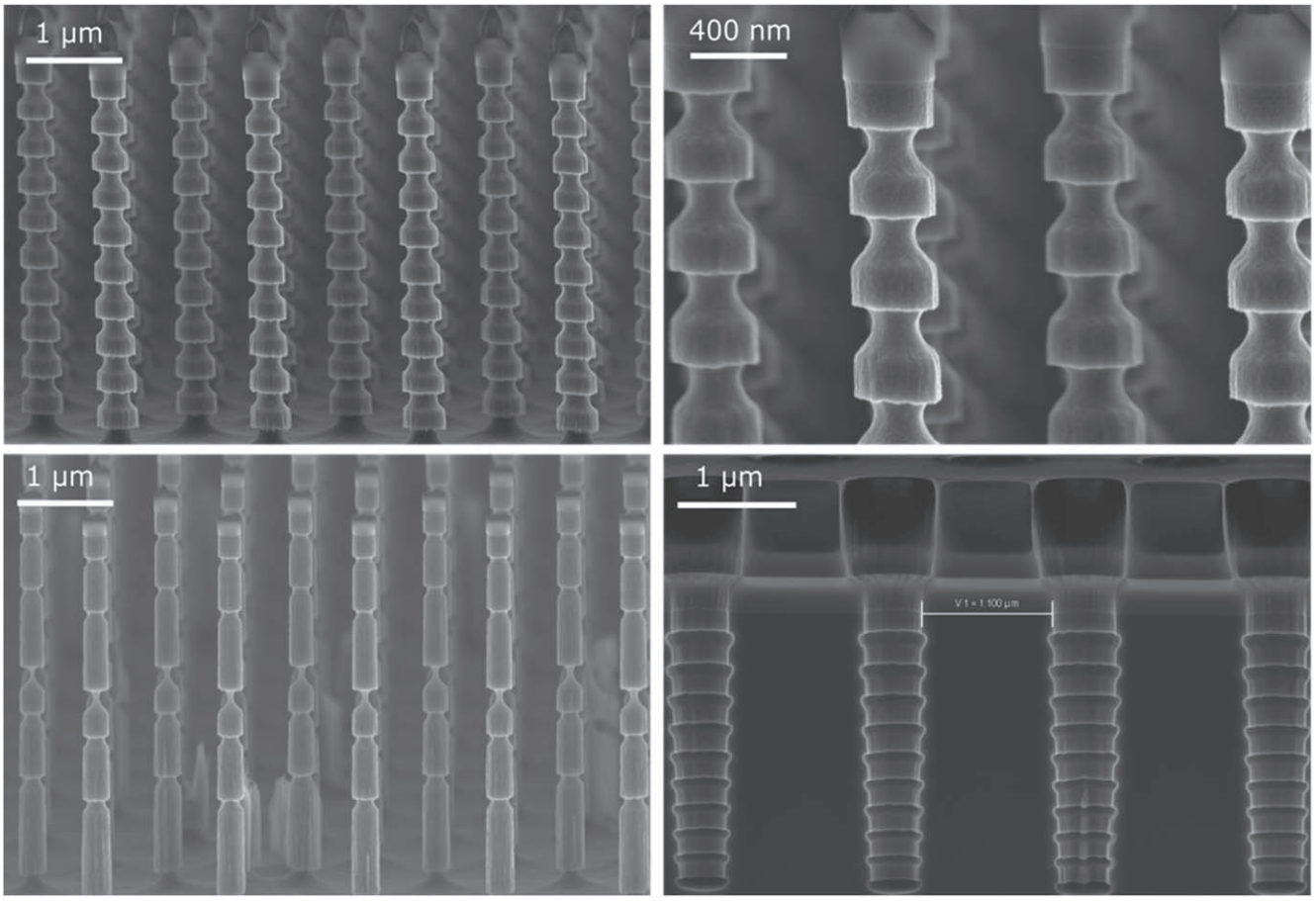


Figure 15. 3D CORE: Various 3D structures shaped by interrupting a train of e.g. 10 normal CORE cycles by a single much bigger "isotropic" undercut.

Discussions

In the previous section we found that the plasma oxidation process of a freshly created F-terminated silicon surface initially seems to depend linearly on the oxidation time and—for 50 sccm O_2 at 50 mTorr and 10 Watt—is finished after ca. 8 s. Why is that?

CORE and self-termination.—It is well known that a cleaved silicon surface will immediately start to oxidize when exposed to open air. It will then slow down quickly and virtually halt within a few weeks after only a few nanometers. This is the so-called native oxide growth. It is scientifically accepted that this retardation happens because the growing oxide layer acts as effective barrier and delays oxygen reaching the Si-SiO_x interface.[51–64] We assume that the plasma oxidation is much like native oxidation, if only proceeding much faster because radicals and negative O-atoms are plenty available. We further assume that, in the initial plasma oxidation process directly following an etch step, the whole silicon surface is transformed from fully F-terminated into fully O-terminated. After this rather fast surface exchange reaction, the usual plasma oxidation growth process of the subsurface starts, but at a much slower rate and finally virtually stops as oxygen cannot penetrate the dense oxide. To test this hypothesis, unprocessed full wafers are loaded in the reactor and a 60 s "DeDam-step" (15 sccm SF_6 at 0.5 mTorr and 10 Watt platen) is performed that removes the native oxide and leaves the silicon surface F-terminated. Subsequently, the wafer is in-situ oxidized using the O-step parameters from Fig. 5 (i.e. 50 sccm O_2 at 50 mTorr and 10 W) for a selected amount of time *t*, unloaded and analyzed using ellipsometry. To minimize the influence of a varying cleanroom condition within the experimental time frame, the measurements were taken always within the first minute after releasing the wafer from the reactor loadlock.[65–67] The initial growth rate under standard cleanroom condition was confirmed to be sufficiently low to guarantee the correctness of this experimental procedure.

CORE	Time	Pressure	SF_6	O_2	Platen	ICP
Step	s	mTorr	sccm	sccm	W	W
C	4	~0	0	50	0	0
O	3	50	0	50	0	2000
R	20	0.2	5	0	20	0
E	33	50	15	0	0	2000

Figure 16. Micro CORE cycle etching using the ICP source.

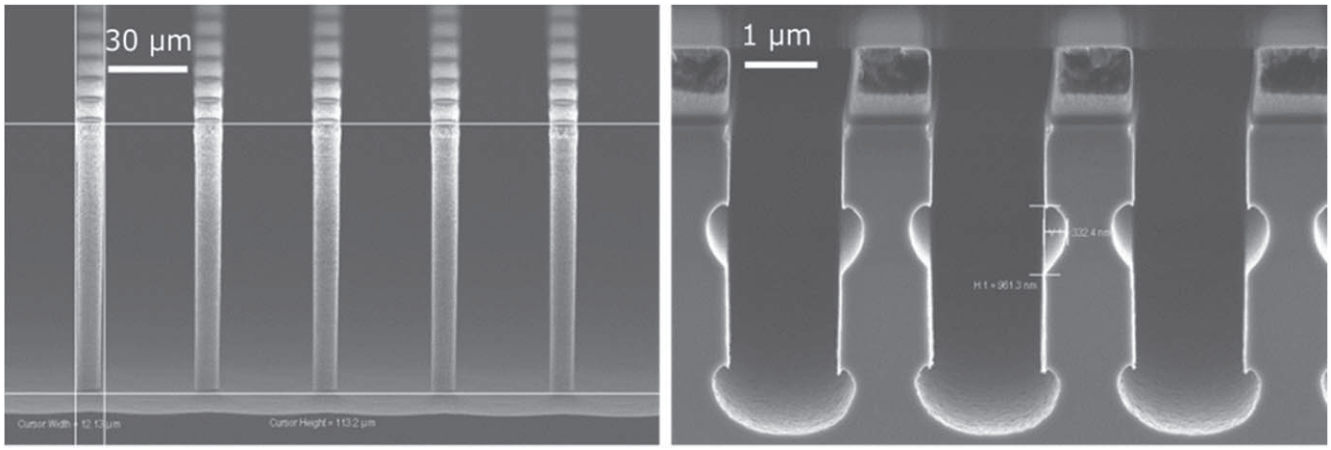


Figure 17. Left) 113 μm high silicon features arrived from the micro CORE sequence and etching at 330 nm min^{-1}. Right) 3D micro CORE.

Figure 18 left presents the linear plot of the plasma oxidation step time t versus observed layer thickness d. The blue "×" crosses are ellipsometric points (typically with a 0.03 nm variance at 90% confidence interval + 0.02 nm error due to temperature and humidity fluctuations of the cleanroom air) and the green line represents a logarithmic model fit as proposed by Fehlner and Mott as a follow up for the famous Cabrera-Mott model to explain anodic oxidation[68,69]:

$$d(t) = d_0 + d_0' \cdot \tau \cdot \ln\left(1 + \frac{t}{\tau}\right) \quad [1]$$

The model has three parameters to be fitted with the ellipsometric data: d_0, d_0', and τ. $d_0 = 1.1$ nm denotes the initial thickness modeled at $t = 0$ s, $d_0' = 0.03$ nm s^{-1} stands for the initial growth rate at $t = 0$, and $\tau = 10$ s is a time constant. The experimental curve starts with a $\Delta = 0.84$ nm offset and shows a rapid increase of surface oxide within the first minutes, but then continues to slow down until after ca. 1 h the growth is virtually halted. So, the model predicts the plasma oxidation correctly except for the first second. The growth rate within the first second is extremely fast—possibly 1 nm s^{-1} or more—but could not be determined accurately. This initiation period is thought to be caused by the rapid replacement of the fluorine termination of the silicon surface by oxygen (≡Si-F → ≡Si-O). The slope between 1 and 5 s is more or less linear ($d_o' \sim 0.03$ nm s^{-1}) and represents the beginning of the usual oxidation process which follows a purely logarithmic law. After ca. 1 h the layer has grown to a few nm and due to diffusion limitations this barrier will effectively compromise further growth, i.e., the growth proceeds at a rate of 0.65 nm/decade ($=d_o' \cdot \tau \cdot \ln 10$) for $t \gg \tau$. So, no indication is found that supports the Deal-Grove model.[51] (in which the growth should have been following a linear-parabolic law) as made clearer with the help of the plot in Fig. 18 right, which confirms the perfect logarithmic growth behavior in plasma oxidation. Neither we observed any sign of layer-by-layer growth as observed by Taft and confirmed by many others.[54–59] A reasonable explanation why some researchers find time-logarithmic law and others layer-by-layer growth is studied by Cerofolini.[70] He provides evidence that the difference is likely to be caused by difference in the initial surface roughness: only atomically smooth wafers will cause layer-by-layer growth.

However why does the film directly after a DeDam etch start off with $\Delta = 0.84$ nm? This peculiar offset is repeatedly found in literature and never explained satisfactory.[52,54,71,72] We believe the following could happen: in case of the plasma oxidized surfaces presented in Fig. 18. These surfaces are highly hydrophilic and consequently between 3 and 4 monolayers of water ought to be present (at 22.5 °C and 45%RH), corresponding to roughly 1 nm of (ice-like) water having a refractive index of 1.31.[73–76] In the model we assumed a growing silicon monoxide (SiO, n = 2.0) to be present, so we should have found a Δ-value of 0.54 nm.[77] This is still not the 0.84 nm offset we found, therefore we further propose the presence of an additional Si-OH interfacial layer bridging the Si-O and adsorbed water. So, when we measure plasma oxidation, we measure as well a layer of Si-OH with a few monolayers of water. This is believed to be the initial Δ-value measured by ellipsometry immediately (within a minute) after the plasma oxidation.

Besides the previous abnormalities, the observed behavior most certainly corresponds with the CORE behavior found before in the O-step section. In the first 8 s the passivation improves fast, almost linearly with performed plasma oxidation time due to the rapid replacement of Si-F by Si-O. For O-time longer than 8 s, the

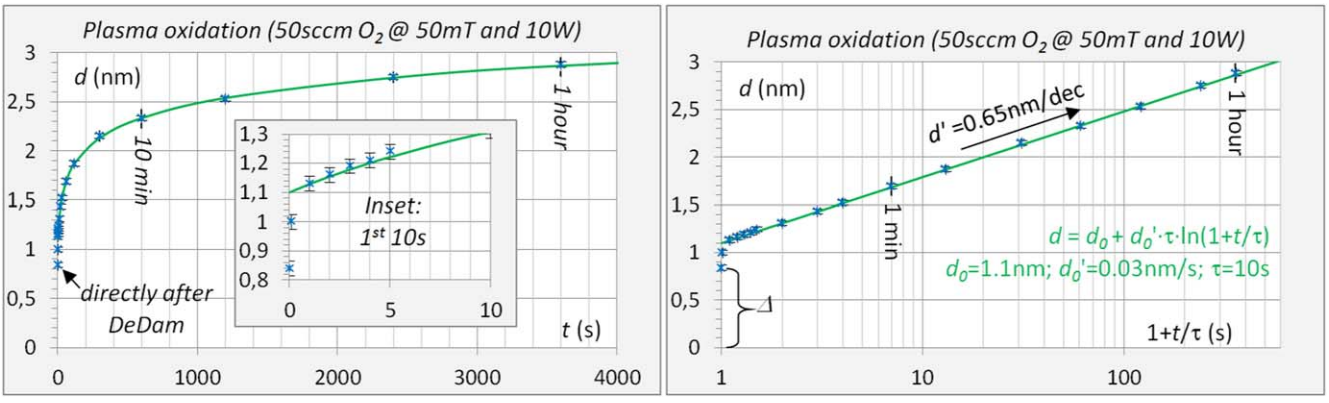


Figure 18. Prolonged plasma oxidation time after a 60 s mild SF_6 pre-etch ("DeDam"). Left) linear scale. Right) logarithmic scale.Inset for the magnified view of the first 10 s. Immediately after the DeDam $\Delta = 0{,}84$ nm. Long term growth $d' = 0.65$ nm/decade.

passivation does not improve as quickly as before and practically halts at a few nm, because the slow bulk oxidation regime is entered. Then, when the E-time becomes very large the profile degradation cannot be fixed at all by extra O-time anymore because of this inherent self-limiting feature. Nevertheless, even though the plasma oxidation is self-limiting, in some cases increasing the O-time will be beneficial to give high aspect ratio trenches and holes sufficient time to reinforce their sidewall to counteract transport limitations (Knudsen diffusion) of the oxygen species. A final note to make here is that the ellipsometric experiments can only partly represent the real O-step behavior of the CORE sequence. For example, very recently Takahashi showed aspect ratio dependency of silicon trench oxidation using oxygen plasma.[78]

Conclusions

A fluorocarbon-free directional silicon etch procedure using a conventional RIE procedure at room temperature is demonstrated. It is based on a sequence of SF_6 and O_2 plasma cycles called CORE—meaning Clear, Oxidize, Remove, and Etch. It performs excellent in traditional high aspect ratio processing (2½D) of nanoscale structures and is particularly specialized in 3D shaping and nanoscale accuracy (i.e. ultralow etch rates). The latter is required for the More than Moore heterogeneous integration architectures for which the CORE sequence allows convenient programming and parameter ramping of the individual cycle steps in a single plasma run. Besides shaping at the nanoscale, by switching on the ICP source the technique also performs for microstructures without the need for further process optimization in between. Therefore, the procedure creates a lot of design freedom and is operator and tool friendly. A typical silicon etch rate of a fine-tuned CORE sequence is 15 nm min^{-1} with a selectivity of ca. 10 towards resist (both DUV and e-beam), ca. 35 for HSQ and SiO_2, and ca. 700 for ALD Al_2O_3. When the ICP source is used and the platen source is discarded to remove the DC bias, the etch rate can be above 1 μm min^{-1} and the selectivity can be as high as 200 for SiO_2 masking and low silicon loading.

The silicon oxidation from the CORE sequence works excellent at room temperature. This means that the more troublesome cryogenic alternative—that freezes the reaction products to protect the silicon sidewalls while etching—is not needed. In addition, the use of oxygen as the inhibitor has the advantage of being self-terminating: the plasma oxidation effectively halts after around 2 nm of growth irrespective of the feature's dimension. This is because the silicon-oxide acts as a diffusion barrier just like in thermal oxidation. Consequently, additional oxidation time to ensure sufficient sidewall passivation of high aspect ratio trenches or holes will not negatively affect the low aspect ratio open field structures (as is the case for e.g. C_4F_8, Cl_2, or HBr based plasma chemistries due to passivation buildup resulting in clogging). After the silicon surface has become fully O-terminated, the plasma oxidation of the bulk silicon will continue but at the hampered speed due to the growing silicon oxide barrier. The oxidation will eventually come to a halt when reaching 2 nm or so. Important to remember here is that the first monolayers form quickly and these layers that are used in the CORE sequence as it provides sufficient passivation during the E-time.

The result of the CORE sequence is similar to the conventional Bosch process, but has the advantage of not struggling for the pile-up of fluorocarbon deposits at the topside of the deep-etched or nano-sized features. At the same time, process drift is prevented as the reactor walls are staying perfectly clean. There is no need for excessive reactor cleaning or process conditioning procedures that generally kill the overall throughput and reproducibility. Therefore, the replacement of C_4F_8 by O_2 has at least removed part of the sustainability problem coming with the Bosch related techniques.

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