ELSEVIER

Directed self-assembly of block copolymers for next generation nanolithography

Seong-Jun Jeong[1,*], Ju Young Kim[2], Bong Hoon Kim[3], Hyoung-Seok Moon[2] and Sang Ouk Kim[2,*]

[1] Devices R&D Center, SAIT, Samsung Electronics, Yongin 446-712, Republic of Korea
[2] Center for Nanomaterials and Chemical Reactions, Institute for Basic Science (IBS), Department of Materials Science and Engineering, KAIST, Daejeon 305-701, Republic of Korea
[3] Department of Materials Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA

Directed self-assembly of block copolymers has received a great deal of research attention as a promising nanolithography to complement the intrinsic limitations of conventional photolithography. In this review, we highlight the recent progress in the development of the directed self-assembly process for practical utilization in semiconductor applications. Various advanced directed self-assembly approaches are examined, in which block copolymer self-assembly is synergistically integrated with conventional photolithography, such as ArF lithography or I-line lithography, via either epitaxial self-assembly or the graphoepitaxy principle. We focus on the practical advantages anticipated from directed self-assembly integration, such as pattern density multiplication, feature size uniformity improvement, line edge roughness reduction, as well as cost reduction. Additionally, a direction for future research on directed self-assembly is suggested with diverse potential applications.

Introduction

Nanolithography is a fundamental technological requirement for semiconductor device fabrication [1]. However, no viable technology for sub-14 nm scale patterning has yet been established. Directed self-assembly (DSA) of block copolymers (BCPs) generates laterally ordered, periodic arrays of self-assembled spheres, cylinders, or lamellae with a typical feature size in the 3–50 nm region [2–6]. The highly ordered self-assembled nanopatterns can be exploited for lithographic masks for parallel line arrays or hexagonal/square dot arrays [6–13]. As a result of prolonged research effort over the last two decades, DSA is attracting tremendous attention as a complementary technology for conventional photolithography with a variety of potential benefits, such as molecular scale pattern precision, ultrafine line edge roughness (LER), and low-cost processing [14–29].

Recently, several DSA consortiums were organized worldwide, including both industry and academia, as summarized in Table 1 [31–33]. Those consortiums have systematically investigated the basic requirements for the effective integration of DSA into commercial semiconductor processes in terms of materials, equipment, and process flows. In addition, considerable research effort has been devoted to the optimization of the DSA process, relevant material development, defect analysis/reduction, etch stack integration, and so on. Such collaborative efforts came to bear a fab-compatible DSA process line for 300 mm wafers. This rapid advent of a practical DSA process is largely down to the inherent compatibility of DSA with a conventional wafer track process [31–35].

DSA integrates bottom-up self-assembly with top-down conventional lithography [8,16,20]. Surface patterns generated by conventional photolithography, such as E-beam lithography, ArF lithography, and I-line lithography, direct the orientation and positional ordering of BCP self-assembled nanodomains for laterally ordered periodic nanopatterns [14–29]. The DSA principle is generally classified into 'epitaxial self-assembly' and 'graphoepitaxy' according to the nature of the structure-directing surface pattern. 'Epitaxial self-assembly' employs dense chemical patterns

*Corresponding authors:. Jeong, S.-J. (noah.jeong@samsung.com), Kim, S.O. (sangouk.kim@kaist.ac.kr)

 1369-7021/06/$ - see front matter http://dx.doi.org/10.1016/j.mattod.2013.11.002

TABLE 1

DSA consortiums for 300 mm-wafer scale fab-compatible DSA line

Process	Equipment	Materials	Year of consortium	Ref
CEA-Leti	Tokyo Electron Ltd., SOKUDO	ARKEMA, Laboratory of Microelectronics Technologies (LTM), Laboratoire de Chimie des Polymères Organiques (LCPO)	2009	[31]
IBM	Applied Materials	JSR Micro. Inc., AZ Electronic materials	2010	[32]
IMEC	Tokyo Electron Ltd.	AZ Electronic materials, University of Wisconsin-Madison	2012	[33]

to direct BCP self-assembly, as illustrated in Fig. 1a. Highly ordered nanopatterns are anticipated if the surface chemical pattern period is commensurate with the equilibrium period of the BCP self-assembled nanostructure. The orientation control of BCP nanodomains with nanoscale chemical patterns was introduced by Russell et al. in 1997 [30]. However, the first defect-free DSA nanopatterning integrated with top-down lithography was demonstrated by Kim et al. in 2003 [16]. 'Graphoepitaxy' utilizes the topographical features of lithographically pre-patterned substrates for DSA (Fig. 1c), as first introduced by Kramer et al. in 2001 [20]. The selective wetting of a particular BCP component at the trench side walls enforces the lateral ordering of the self-assembled BCP nanodomains along the trenches and thereby enhances the pattern density by subdividing the topographical pre-pattern. Figure 1b,d presents SEM images of directed assembled lamellae morphologies in poly(styrene-*block*-methyl methacrylate) (PS-*b*-PMMA) thin film attained by epitaxial self-assembly and graphoepitaxy, respectively [18,36].

To date, the two aforementioned DSA principles have successfully progressed for practical device-oriented processes. The main focus of this article is to review the current status of advanced DSA technology for practical semiconductor device fabrication processes. It is noteworthy that many well-prepared review articles for BCP based nanopatterning are already available [5,6,8,13,37–52]. While those previous articles have focused on scientific achievements, this article principally summarizes recent technological progress for the practical device fabrication process accomplished from both academia and industry.

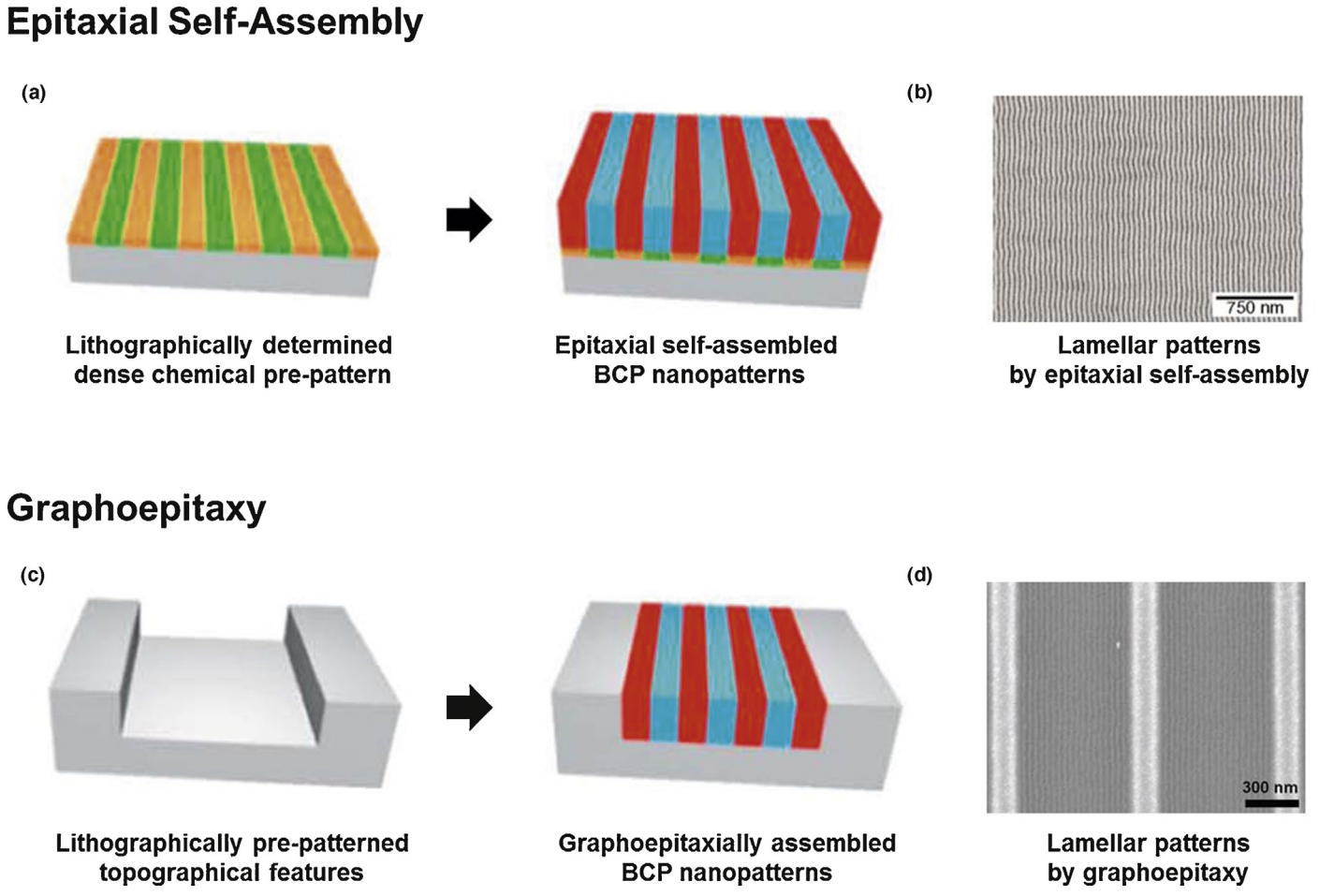

FIGURE 1

(a) Schematic illustration of epitaxial self-assembly exploiting nanoscopic chemical patterns to direct BCP self-assembly [16]. (b) SEM image showing defect-free lamellar patterns attained by epitaxial self-assembly [16]. (c) Schematic illustration of graphoepitaxy utilizing topographic pattern to direct BCP assembly [20]. (d) SEM image showing highly aligned lamellar patterns prepared by graphoepitaxy [35].

TABLE 2

Advanced DSA processes of 'epitaxial self-assembly' and 'graphoepitaxy'

DSA process	Pre-pattern type/ materials	Photolithography type	Published maximum pattern density multiplication	Organization
Epitaxial self-assembly	Thermal flow Lift off Pattern trimming	ArF ArF immersion ArF immersion	A factor of three A factor of four A factor of four	KAIST (2009′) IBM (2010′) IMEC U of Wisconsin-Madison (2010′) IMEC
Graphoepitaxy	Negative tone photoresist NTD photoresist	I-line ArF immersion KrF		KAIST (2009′) IBM (2010′) IMEC CEA-Leti

Epitaxial self-assembly integrated with conventional photolithography

In the early days of the research, epitaxial self-assembly approaches were based on a 1:1 pattern period commensuration between an equilibrium BCP self-assembled pattern and a structure-directing surface chemical pattern [12]. By contrast, current advanced DSA approaches aiming at practical device processing commonly exploit the pattern density multiplication of conventional photolithography by self-assembly principles. Effective pattern density multiplication integrated with conventional photolithography is highly desired, particularly due to the unexpected delay of the development of next-generation extreme ultraviolet (EUV) lithography. The pattern density enhancement strategies can be summarized by the following three approaches; 'thermal flow process', 'lift-off process,' and 'pattern trimming process', as summarized in Table 2 [53–61].

Thermal flow process

The first successful integration of the epitaxial self-assembly principle with conventional ArF lithography was based on a 'thermal flow process', which was achieved by our research group in collaboration with Samsung Electronics in 2009 [53]. In this work, 193 nm ArF lithography was used to generate chemical patterns upon a neutrally modified substrate surface, as illustrated in Fig. 2a. Highly asymmetric photoresist patterns with pattern periods much larger than BCP pattern periods are prepared via the thermal flow process following ArF photolithography. An oxygen reactive ion etching (RIE) process is utilized to selectively oxidize the neutral layer exposed in the narrow space region of the photoresist pattern. Asymmetric surface chemical patterns consisting of an alternating wide neutral stripe and a narrow oxidized polar stripe are prepared on the substrate surface after solvent washing of the photoresist. The pattern density of the chemical

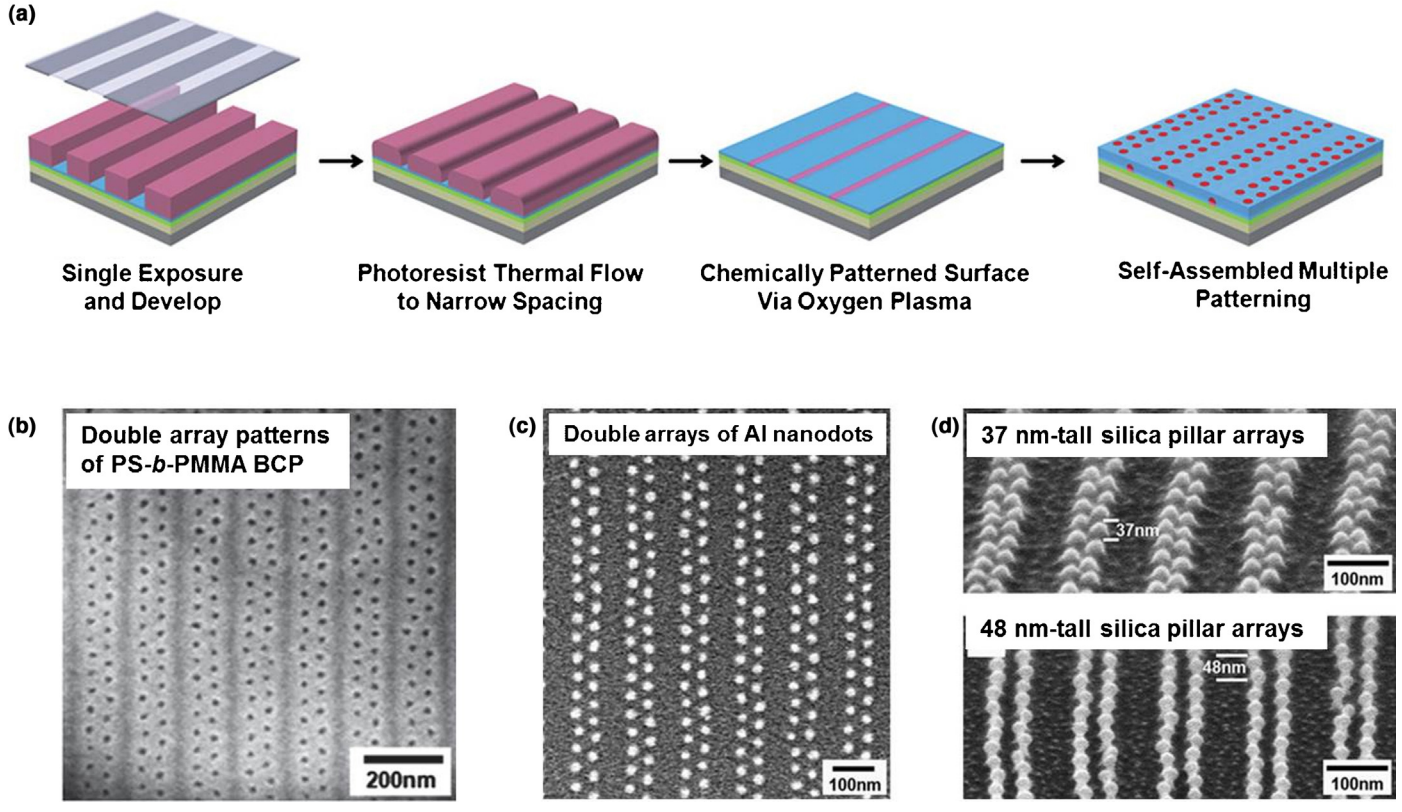

FIGURE 2

(a) Schematic illustration of epitaxial self-assembly procedure based on a 'thermal flow process' [53]. SEM images of (b) vertical nanocylinder double arrays in BCP films, (c) Al nanodot double arrays, and (d) silica pillar arrays prepared by pattern transfer.

pattern defined by conventional lithography is successfully enhanced by a factor of two or three with BCP self-assembly. Figure 2b,c shows SEM images of a vertical nanocylinder double array in BCP patterns and 20 nm scale Al and silica nanodot double arrays prepared by subsequent pattern transfer. This work firstly demonstrates that epitaxial self-assembly can be synergistically integrated with conventional photolithography for a significant advantage in pattern density multiplication.

Lift-off process

Pattern density multiplication based on a 'lift-off process' was reported by IBM at 2010 [54]. In this method, ArF immersion lithography was used to create a chemical pattern on an anti-reflective coating (ARC) surface. The overall process is briefly described in Fig. 3a. Positive-tone photoresist patterns are prepared by ArF immersion lithography on a spin-coated silicon ARC. To improve the solubility in a developer, the polarity of the remaining photoresist pattern is switched by using UV exposure and a baking step. A neutral layer is spin-coated on the photoresist pattern with switched polarity. The photoresist pattern is lifted-off by the developer diffused through the neutral layer. This generates asymmetric chemical patterns containing narrow silicon ARC strips interlaced with wide neutral layer stripes. Finally, BCP thin films are spin-casted and thermally annealed to generate high density BCP line patterns. Figure 3b,c presents SEM images of a chemical pattern (35 nm lines/112 nm pitch) prepared by ArF immersion lithography and 14 nm line/space lamellar PS-*b*-PMMA patterns, respectively. It is noteworthy that this work was carried out in the 300 mm-fab process line of IMEC [33]. Several process variables for success on 300 mm-wafers may be summarized as follows: (i) the photoresist layer thickness should be below 60 nm to minimize line edge/width roughness of the photoresist pattern, (ii) BCP film thickness should be optimized for defect-free pattern formation, and (iii) non-uniform neutral layer formation near the side walls of the photoresist pattern should be minimized for process tolerance [33].

Pattern trimming process

The 'pattern trimming process' was first developed by the Nealey group in 2010 [55]. In this process, ArF immersion lithography was used to prepare chemical patterns (Fig. 4a). In the first step, a crosslinked polystyrene (PS) layer was prepared on an inorganic ARC layer (silicon nitride thin film in this work). After, positive-tone photoresist patterns are generated on the crosslinked PS substrate by ArF immersion lithography. The resultant photoresist line patterns are trim-etched and transferred into the underlying PS layer. A neutral layer is spin-coated over the entire surface and thermally annealed to selectively graft at the silicon nitride substrate. The subsequent solvent rinsing removes un-grafted brush molecules. In this way, planar asymmetric chemical patterns with narrow PS stripes and wide neutral brush stripes can be created. Finally, while BCP thin films are spin-coated upon the asymmetric chemical pre-pattern and thermally annealed, multiple line patterns are spontaneously assembled with improved pattern densities. Figure 4b–d shows SEM images of a photoresist pattern (35 nm lines/100 nm pitch) and trim etched guide patterns of 15 and 12.5 nm-line/space self-assembled lamellar patterns generated by 4× multiplication performed at the IMEC fab 300 mm wafer process line, respectively [56]. Owing to the generation of a planar asymmetric chemical pre-pattern, this approach may offer a stable DSA process integrated with conventional lithography. IMEC and TEL note that this approach provides a large process window for process latitude and defectivity [31,56].

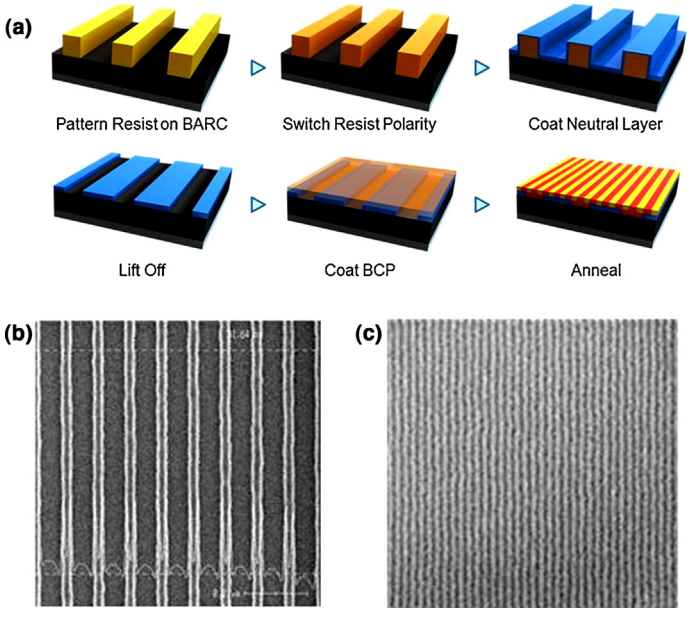

FIGURE 3

(a) Schematic illustration of epitaxial self-assembly based on a 'lift-off process' [54]. SEM images of (b) a photoresist pattern prepared by immersion ArF lithography (35 nm lines/112 nm pitch) and (c) 14 nm-line/space BCP lamellar patterns prepared by epitaxial self-assembly [33].

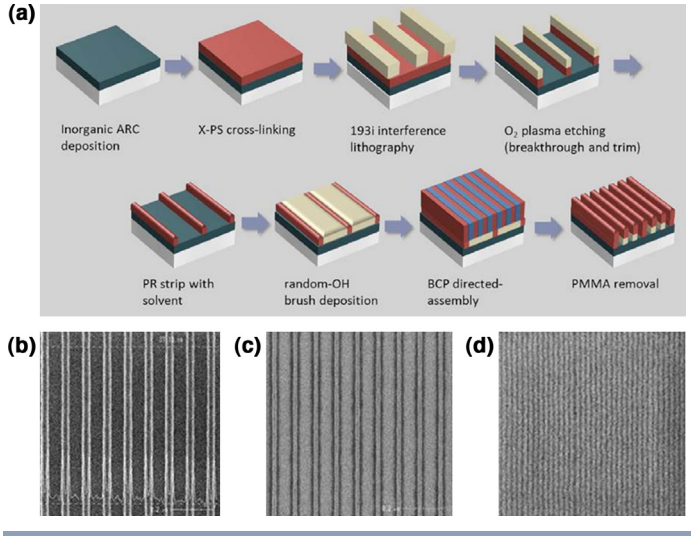

FIGURE 4

(a) Schematic illustration of epitaxial self-assembly based on a 'pattern trimming process' [55]. SEM images of (b) photoresist patterns having 35 nm lines and 100 nm pitch generated by ArF lithography, (c) trim etched guide pattern having 15 nm lines, and (d) defect-free 12.5 nm-line/space BCP lamellar patterns generated by 4× multiplication of epitaxial self-assembly with a 'pattern trimming process' on a 300 mm wafer, respectively [55].

Advanced graphoepitaxy with disposable topographic pre-patterns

Unlike original graphoepitaxy approaches usually based on etched hard substrate patterns, which remain after pattern transfer, advanced graphoepitaxy approaches employ organic photoresist patterns as disposable topographic pre-patterns to integrate BCP self-assembly with conventional photolithography [54–61]. This simple idea leads to a nanofabrication process with no trace of the structure-directing topographic pre-pattern after pattern transfer, which is highly desired for the practical device fabrication requiring multilayer architectures. The relevant approaches are summarized in Table 2.

Process based on negative tone photoresist

Graphoepitaxy with a disposable topographic pre-pattern was firstly introduced by our research group in 2009 [57]. This approach utilizes an 'organic negative-tone photoresist pattern' prepared by I-line lithography as disposable topographic pre-patterns for graphoepitaxial BCP assembly. Consequently, any trace of the topographic pattern is completely removable by a mild cleaning process after pattern transfer. Figure 5a schematically illustrates the overall procedure. The negative tone photoresist pattern is prepared by I-line lithography. BCP thin films are spin-coated over the photoresist trenches and are thermally annealed to induce a highly ordered morphology. In this approach, a rational choice of organic negative tone photoresist is crucial for successful DSA. In this regard, we emphasize several requirements: (i) a disposable photoresist pattern must maintain its structural integrity during the thermal/solvent annealing step for BCP self-assembly [57,61] and (ii) the trench region of the photoresist pattern must be protected from high-energy radiation to prevent radiation damage of the neutral organic layer. Figure 5b presents an SEM image of PS-*b*-PMMA lamellar morphology laterally ordered along the photoresist pattern prepared by I-line photolithography. This work also demonstrates that metal or semiconductor nanowire arrays (20 nm-Al NWs) can be produced by a lift-off process with no trace of the structure-directing topographic pattern (Fig. 5c).

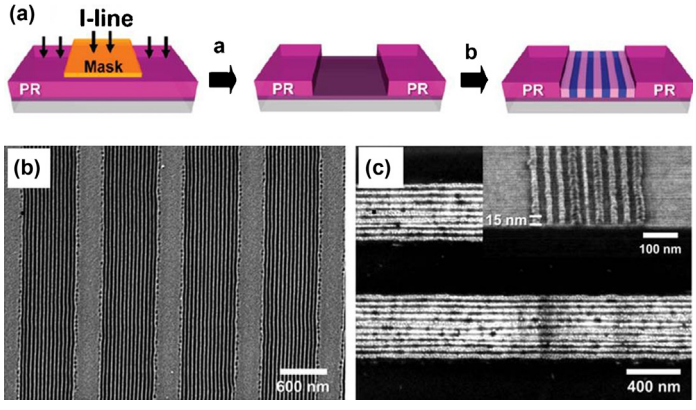

FIGURE 5

(a) Schematic illustration of graphoepitaxy utilizing a negative tone photoresist pre-pattern prepared by conventional lithography [57]. SEM images of (b) highly ordered BCP lamellar patterns along the photoresist topographic patterns and (c) pattern-transferred Al nanowire arrays with no trace of the structure-directing topographic pre-pattern.

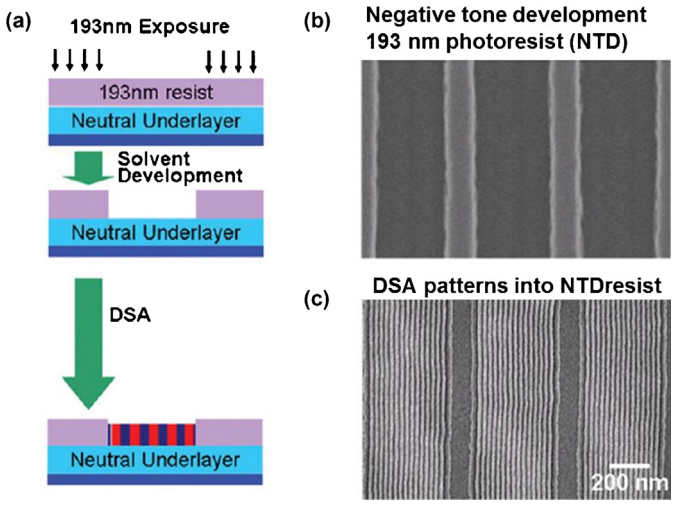

FIGURE 6

(a) Schematic illustration of graphoepitaxy employing a negative tone development (NTD) resist pre-pattern prepared by ArF lithography [54]. SEM images of (b) the hardened NTD photoresist structure and (c) highly aligned 14 nm-line/space BCP lamellar patterns within NTD photoresist topographic patterns [54].

Process based on negative tone development

An article entitled 'NTD photoresist based topographic pre-pattern' was published by IBM in 2010 [54]. In this approach, a negative tone development (NTD) photoresist was selected as a novel topographic material for the effective integration of BCP self-assembly with KrF [62]/ArF [63,64] lithography. In an NTD step, a non-exposed region of a positive tone photoresist is removed during development instead of removing an exposed

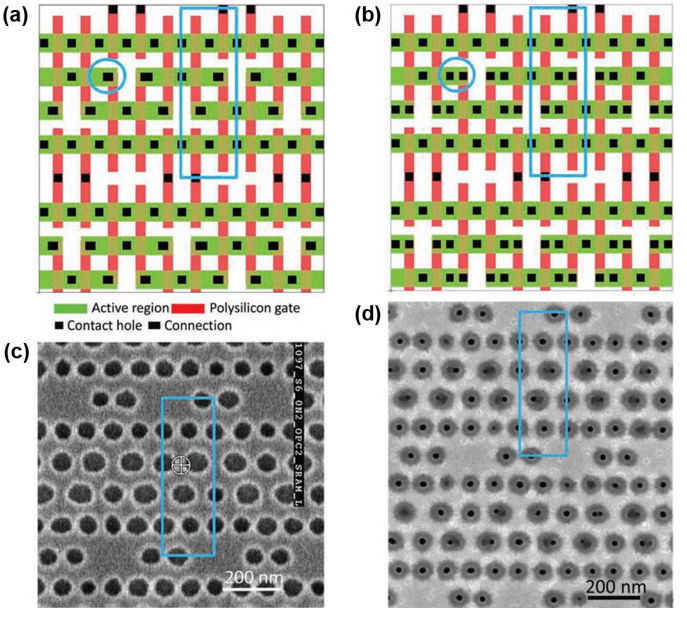

FIGURE 7

(a) Contact hole layout of the IBM 22 nm 6T-SRAM circuit. (b) Modified layout by replacing the rectangular connections with square holes and one of the modification (highlighted by blue circles) [66]. SEM images of (c) Si contact holes fabricated with ArF immersion photolithography and (d) corresponding contact hole shrinkage result for IBM 22 nm 6T-SRAM circuit layout [66].

region. An NTD photoresist includes a crosslinking agent to harden the photoresist with thermal baking after the NTD step [65]. Consequently, the NTD photoresist pattern has a superior thermal stability while it can be readily removed by mild solvent washing. Figure 6a shows the schematic illustration of a graphoepitaxy employing an NTD photoresist [54]. Owing to the high thermal/chemical stability of the hardened NTD photoresist, there is no deterioration of the photoresist pattern during the spin casting of BCP films and thermal annealing at 200°C (Fig. 6b). Figure 6c presents an SEM image of high quality 12.4 nm-line/space PS-*b*-PMMA patterns generated utilizing NDT-based topographic pattern process [55]. Recently, IMEC also carried out this approach to test the process feasibility in a 300 mm-fab line. It was reported that (i) the LER of BCP pattern improves compared to NTD pre-pattern and (ii) a defect-free DSA pattern is attained while the NTD process window is under ±3% exposure latitude [33].

Contact hole shrinkage

Owing to the relative technological simplicity, pattern size shrinkage with a DSA process is a close target in the semiconductor process [31–34,54,66]. In particular, graphoepitaxy with an NTD-based topographic pattern has been extensively investigated to reduce the critical dimension (CD) and contact edge roughness (CER) of the contact hole since the IBM report in 2010 [54]. Recently, a CEA-Leti 300 mm DSA pilot line was used to demonstrate that a 100 nm contact hole size can be effectively reduced down to 15 nm by this approach [31]. In addition, Tokyo Electron Ltd. (TEL), the world's largest wafer track supplier, demonstrated that (i) the wet development process provides the best possible condition to remove the PMMA core in the shrunken hole and (ii) CD healing is observed in the improvement of critical dimension uniformity (CDU; from 1.8 nm to 0.9 nm) and contact edge roughness (CER; from 3.7 nm to 0.8 nm) from

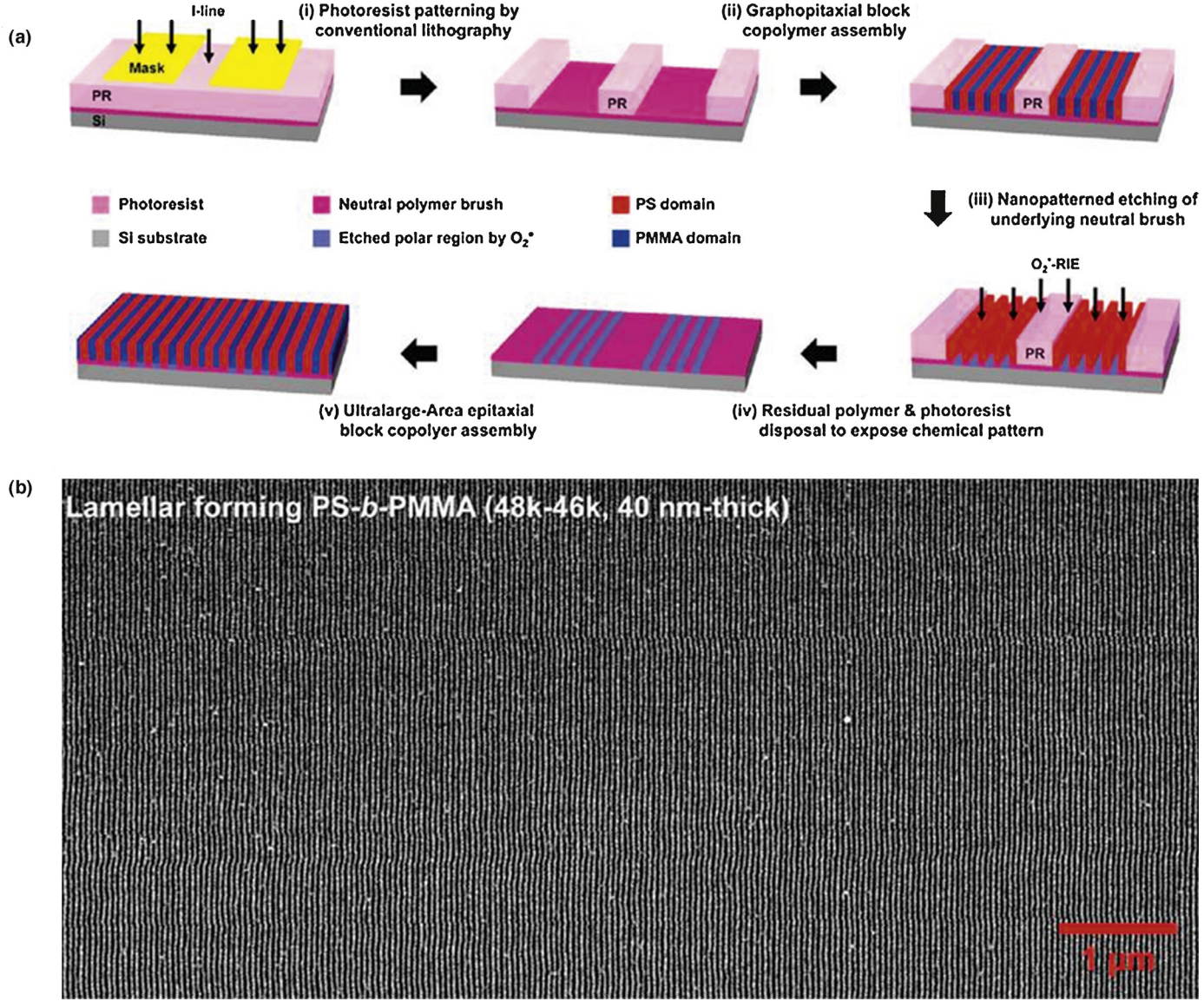

FIGURE 8

(a) Schematic illustration of synergetic integration of epitaxial self-assembly and graphoepitaxy [60]. (b) SEM image of large-area highly ordered BCP lamellar nanopatterns created by the synergetic integration of epitaxial self-assembly and graphoepitaxy.

the hole guide pattern [33]. Recently, the Wong research group presented the potential of a DSA process for practical integrated circuit contact hole patterning [66]. Figure 7a,b shows a contact hole layout of an IBM 22 nm 6T-SRAM circuit and a modified layout by replacing the rectangular connections with square holes, respectively. Figure 7c,d presents the SEM images of the silicon contact holes of the modified layout fabricated with 193 nm ArF immersion photolithography and the corresponding contact hole shrinkage result, respectively. While this work employed Si guide patterns, it demonstrates that the hole shrinkage with DSA can attain a minimum critical dimension of 15 nm and over-lay accuracy of 1 nm in a practical contact hole layout [66].

Synergistic integration of epitaxial self-assembly and graphoepitaxy

The synergistic integration of the two principles of 'epitaxial self-assembly' and 'graphoepitaxy' was demonstrated by our research group in 2010 [60]. This approach was originally developed to address the intrinsic limitation of the maximum patternable area by the graphoepitaxy principle. In this approach, as schematically illustrated in Fig. 8a, hierarchical graphoepitaxial morphology composed of the disposable photoresist pattern and BCP lamellar arrays is utilized as a chemical patterning mask for the chemical patterning of the underlying substrate. After the BCP film and disposable photoresist pre-pattern are removed by solvent washing, the same BCP film is epitaxially assembled on the remaining chemically patterned substrate. A highly oriented lamellar morphology is created with no trace of structure directing the photoresist pre-pattern over an arbitrarily large area. We note that the substrate areas previously protected by the photoresist layer are not chemically patterned. Nonetheless, the lamellar arrays registered on the neighboring chemically patterned regions enforce the lateral ordering of lamellar nanodomains in the non-patterned regions. Figure 8b shows the SEM image of the resultant large-area self-assembled lamellar nanopattern.

Emerging direction and applications of the DSA process

DSA process for sub 10 nm scale nanolithography

DSA is considered a potential lithographic solution that can be integrated with ArF immersion photolithography for 16 nm-line/space DRAM process scheduled in 2018 [1]. In this target, widely used PS-*b*-PMMA BCP with a minimum lamellar period of ~12 nm can be employed. By contrast, there are challenges for 11 nm-line/space lithography process of NAND Flash production targeted at 2019, as summarized in Table 3 [1]. Among them, the most significant issue is the minimum feature size, which is inherently determined by the Flory–Huggins interaction parameter (χ) of BCPs. χ is a parameter associated with the enthalpy of mixing for chemically different BCP blocks [2]. Widely used PS-*b*-PMMA has a low value of $\chi = 0.05$ [68], which leads to the minimum pattern period of ~12.5 nm line/space. For smaller feature sizes, diverse high χ BCPs, such as polystyrene-*block*-polyethylene oxide (PS-b-PEO; $\chi = 0.17$) [69], polystyrene-*block*-poly(dimethylsiloxane) (PS-*b*-PDMS; $\chi = 0.26$) [67], and poly(2-vinylpyridine)-*block*-poly(dimethylsiloxane) (P2VP-*b*-PDMS; $\chi = 1.07$), have been exploited for sub-11 nm line/space patterns. In addition, since the interfacial width between the chemically different nanodomains of a BCP pattern is proportional to $\chi^{-1/2}$, a high χ may lead to a low LER of the self-assembled pattern [8]. Various DSA processes employing high χ BCP materials have been introduced by the Ross research group and others [25,26,70–77]. Figure 9a,b shows SEM images of highly ordered 8 nm BCP pattern and 9 nm NW arrays prepared using PS-*b*-PDMS, respectively [73]. Recently, Jung and Ross also introduced another high χ BCP, P2VP-*b*-PDMS that can generate 6 nm-scale-line/space patterns (Fig. 9c,d) [75].

Flexible/transferable DSA with graphene

Recently, several application fields for DSA other than semiconductor device process have emerged. Among them, our research group recently demonstrated flexible/transferable DSA technology

TABLE 3

Photoresist requirements and DSA challenges for potential lithographic solution

Year of production	2013	2016	2018	2019	2020
DRAM ½ pitch (nm)	28	20	16	14	13
MPS/ASIC Metal ½ pitch (nm)	27	19	15	13	12
Flash ½ pitch (nm)	18	14	12	11	10
Resist thick. (nm, single layer)	35–65	25–50	20–45	20–40	20–40
Low frequency LWR (nm, 3 sigma)	2.2	1.5	1.3	1.1	1.0
Defects (#/cm^2)	0.02	0.01	0.01	0.01	0.01

DSA potential lithography solution year

DSA challenges	Emerging direction
Higher density patterns (than conventional lithography)	Up to 2× pattern multiplication process development
Smaller critical dimension (than conventional lithography)	• ~12 nm line/space: PS-*b*-PMMA • Sub-11 nm line/space: high χ BCP
Reduced line edge roughness (LER) Defect density	• DSA pre-pattern design issue
Annealing times	• Annealing process design based on kinetics/thermodynamics
Etch selectivity	• Vertical BCP morphology • Inorganic–organic hybrid BCP design

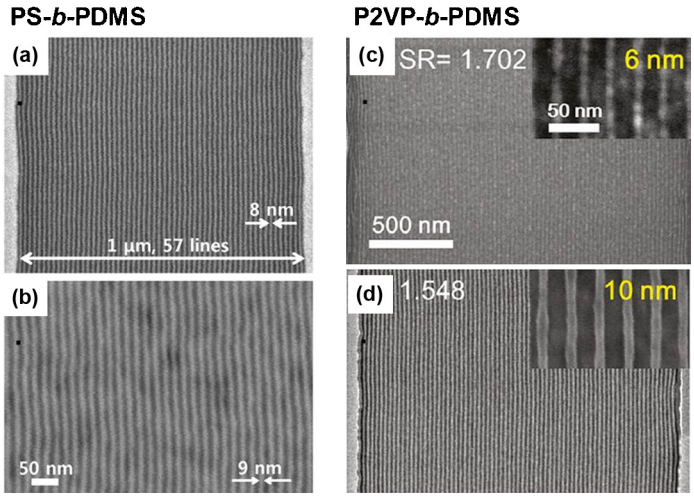

FIGURE 9

SEM images of (a) high χ PS-*b*-PDMS parallel cylinder patterns for sub-10 nm DSA process and (b) 9 nm width NWs [73]. SEM images of (c and d) P2VP-*b*-PDMS patterns of 6 nm and 10 nm line/space, respectively [75].

utilizing chemically modified graphene (CMG) [78,79]. Along with the rapid advance of flexible and 3D devices, lithography technology for nonplanar/flexible geometry is becoming crucial. Nonetheless, nanolithography technologies, including DSA, generally require spin-casting of a uniform thick organic layer, photolithographic radiation exposure, and a thermal/chemical annealing process step, which are inherently incompatible with a flexible and nonplanar geometry. In this work, CMG can serve as a disposable flexible substrate to transfer DSA structure onto nonplanar and flexible geometries (Fig. 10). After all processing steps for DSA are completed on CMG films in flat geometry, the entire patterned structures are isolated from the flat geometry and transferred to any nonplanar/flexible geometry with the support of robust and flexible CMG. This approach also enables the multiple repeatability of the DSA process at the same location, which can be exploited for the creation of complex multilayer structures, such as crossbar nanowire arrays or rectangular nanopost arrays. Figure 10a schematically illustrates the multilayer DSA process. Firstly, CMG films are prepared on a Si substrate by spin-casting and thermal/chemical reduction. A photoresist pre-pattern is formed on the CMG by conventional I-line lithography. Graphoepitaxy of BCP films and subsequent pattern transfer produce parallel metal NW arrays. After this first cycle, CMG film is spin-casted over the fabricated NW arrays. The second photoresist patterning was performed on the CMG film with the orientation of trenches orthogonal to those of the bottom NWs. The following DSA and pattern transfer complete the metal NW crossbar arrays. In this work, CMG has the following advantages as a flexible and transferable substrate: (i) an atomically flat CMG surface, enabling uniform BCP thin films formation and robust self-assembly and (ii) thermally/chemically stable CMG that endures harsh chemical treatment and high temperature annealing required for BCP self-assembly, and (iii) mechanically robust but flexible CMG that is easily transferable to desired flexible and non-planar substrates. Further development of flexible/transferable DSA will offer novel applications of DSA for various flexible electronics/optoelectronics and 3D device architectures.

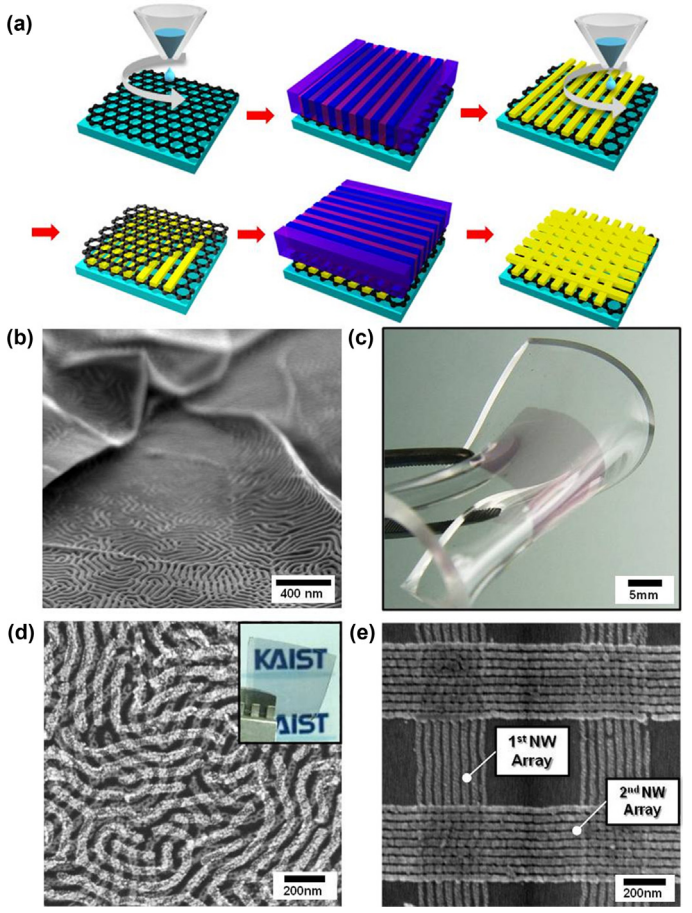

FIGURE 10

(a) Schematic illustration of a flexible/transferable DSA process utilizing chemically modified graphene (CMG) [78,79]. (b) SEM image of vertical PS-*b*-PMMA lamellar structure self-assembled on CMG [78]. (c) Photograph of Au nanodot array formed on a flexible PDMS substrate [79]. SEM images of (d) a double layered Au nanowire random network and (e) an Al NW crossbar array by double layer repeated orthogonal DSA [79].

Conclusion and outlook

We have reviewed the current progress of advanced DSA technology for practical device fabrication processes. Two successful DSA principles of 'epitaxial self-assembly' and 'graphoepitaxy' have been synergistically integrated with conventional photolithography via collaborative efforts among industry and academia. The intrinsic advantages of BCP self-assembly, including low-cost spontaneous pattern generation, molecular scale pattern precision, dense areal packing of nanodomains, and smooth/narrow interfacial width, offer cost-effective large-area scalable nanopatterning for device-oriented ultrafine nanopatterns. Notably, advanced DSA process already realizes the fab-compatible process line for 300 mm size wafers. Further research effort for high χ BCPs materials, perfect defect control, effective pattern transfer and nonplanar/flexible nanopatterning will be critical for the ultimate application of DSA to various commercial device manufacturing situations as a next-generation lithography solution.

Acknowledgement

This work was supported by Institute for Basic Science (IBS) [CA1301-02].

References

[1] International Technology Roadmap for Semiconductors (ITRS) 2012 Edition, Semiconductor Industry Association, San Jose, CA, 2012.
[2] F.S. Bates, G.H. Fredrickson, Annu. Rev. Phys. Chem. 41 (1990) 525.
[3] G.H. Fredrickson, F.S. Bates, Annu. Rev. Phys. Chem. 26 (1996) 501.
[4] F.S. Bates, G.H. Fredrickson, Phys. Today 52 (1999) 32.
[5] C.J. Hawker, T.P. Russell, MRS Bull. 4 (2005) 19.
[6] J.K. Kim, et al. Prog. Polym. Sci. 35 (2010) 1325.
[7] M. Park, et al. Science 276 (1997) 1401.
[8] C. Black, et al. IBM J. Res. Dev. 51 (2007) 605.
[9] S.-J. Jeong, et al. Adv. Mater. 20 (2008) 1898.
[10] G. Xia, et al. Nanotechnology 20 (2009) 225.
[11] D.H. Lee, et al. Adv. Mater. 20 (2008) 2480.
[12] B.H. Kim, et al. Adv. Mater. 23 (2011) 5618.
[13] B.H. Kim, et al. Soft Matter 9 (2013) 2780.
[14] C. Tang, et al. Science 322 (2008) 429.
[15] T. Thurn-Albrecht, et al. Science 290 (2000) 2126.
[16] S.O. Kim, et al. Nature 424 (2003) 411.
[17] M.P. Stoykovich, Science 308 (2005) 1442.
[18] S.O. Kim, et al. Adv. Mater. 19 (2007) 3271.
[19] R. Ruiz, et al. Science 321 (2008) 936.
[20] R.A. Segalman, et al. Adv. Mater. 13 (2001) 1152.
[21] D. Sundrani, et al. Nano Lett. 4 (2004) 273.
[22] J.Y. Cheng, et al. Nat. Mater. 3 (2004) 823.
[23] S.-M. Park, et al. Adv. Mater. 19 (2007) 607.
[24] R. Ruiz, et al. Adv. Mater. 19 (2007) 2157.
[25] I. Bita, et al. Science 321 (2008) 939.
[26] J.K.W. Yang, Nat. Nanotechnol. 5 (2010) 256.
[27] B.H. Kim, et al. Adv. Mater. 20 (2008) 2303.
[28] B.H. Kim, et al. Adv. Funct. Mater. 19 (2009) 2584.
[29] D.O. Shin, et al. Macromolecules 42 (2009) 1189.
[30] L. Rockford, et al. Phys. Rev. Lett. 82 (1999) 2602.
[31] S. Tedesco, et al., IDeAL Program: DSA Activity at LETI. SOKUDO Lithography Breakfast (11 July 2012).
[32] Y. Hishiro, et al., Applications of DSA for Lithography. SOKUDO Lithography Breakfast (11 July 2012).
[33] B. Rathsack, et al. Proc. SPIE 8323 (2012) 83230B-1.
[34] C. Bencher, et al. Proc. SPIE 7970 (2011) 79700F.
[35] SOKUDO DUO, "Defect Free" DSA Patterning Spin-on Coat & Anneal Track, SOKUDO Lithography Breakfast (11 July 2012).
[36] S. Kim, et al. Small 8 (2012) 1563.
[37] M. Lazzari, et al. Adv. Mater. 15 (2003) 1583.
[38] C. Park, et al. Polymer 44 (2003) 6725.
[39] R. Segalman, et al. Mater. Sci. Eng. R 48 (2005) 191.
[40] M. Stoykovich, P. Nealey, Mater. Today 9 (2006) 20.
[41] J. Cheng, et al. Adv. Mater. 18 (2006) 2505.
[42] S.B. Darling, Prog. Polym. Sci. 32 (2007) 1152.
[43] C.T. Black, et al. ACS Nano 1 (2007) 147.
[44] N. Zhihong, K. Eugenia, Nat. Mater. 7 (2008) 277.
[45] H. Kim, W.D. Hinsberg, J. Vac. Sci. Technol. 26 (2008) 1369.
[46] J. Bang, et al. Adv. Mater. 21 (2009) 1.
[47] I.W. Hamley, Prog. Polym. Sci. 34 (2009) 1161.
[48] W. van Zoelen, G. ten Brinke, Soft Matter 5 (2009) 1568.
[49] H. Yu, et al. Adv. Mater. 23 (2011) 3337.
[50] F.H. Schacher, et al. Angew. Chem. Int. Ed. 51 (2012) 7898.
[51] C.G. Hardy, C. Tang, J. Polym. Sci. B: Polym. Phys. 51 (2013) 2.
[52] M. Ramanathan, et al. J. Mater. Chem. C 1 (2013) 2080.
[53] S.H. Park, et al. Soft Matter 6 (2010) 120.
[54] J. Cheng, et al. ACS Nano 4 (2010) 4815.
[55] C.C. Liu, et al. J. Vac. Sci. Technol. B (2010) 28.
[56] M. Somervell, et al. SPIE Proc. 8325 (2012) 83251G-1.
[57] S.-J. Jeong, et al. Nano Lett. 9 (2009) 2300.
[58] S.-J. Jeong, et al. Nano Lett. 10 (2010) 3500.
[59] H.S. Moon, et al. J. Mater. Chem. 22 (2012) 6307.
[60] S.-J. Jeong, et al. ACS Nano 4 (2010) 5181.
[61] S.-J. Jeong, S.O. Kim, J. Mater. Chem. 21 (2011) 5856.
[62] J.G. Maltabes, et al. Proc. SPIE 1262 (1990) 2.
[63] S. Tarutani, et al. Proc. SPIE 6923 (2008) 69230F-1-8.
[64] S. Tarutani, et al. J. Photopolym. Sci. Technol. 21 (2008) 685.
[65] H. Ito, Adv. Polym. Sci. 172 (2005) 37.
[66] H. Yi, et al. Adv. Mater. 24 (2012) 3107.
[67] T. Nose, Polymer 36 (1995) 2243.
[68] T.P. Russell, Macromolecules 23 (1990) 890.
[69] S. Park, et al. Science 323 (2009) 1030.
[70] Y.S. Jung, et al. Nano Lett. 7 (2007) 2046.
[71] Y.S. Jung, et al. Nano Lett. 8 (2008) 2975.
[72] Y.S. Jung, et al. Adv. Mater. 21 (2009) 2540.
[73] Y.S. Jung, et al. Nano Lett. 10 (2010) 1000.
[74] V.P. Chuang, et al. ACS Nano 22007 (2008) 2014.
[75] J.W. Jeong, et al. Nano Lett. 11 (2011) 4095.
[76] A.S. Zalusky, et al. J. Am. Chem. Soc. 124 (2002) 12761.
[77] T. Hirai, et al. Macromolecules 42 (2009) 8835.
[78] B.H. Kim, et al. ACS Nano 4 (2010) 5464.
[79] J.Y. Kim, et al. Adv. Mater. 25 (2013) 1331.