PVD-Treated ALD TaN for Cu Interconnect Extension to 5nm Node and Beyond

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***Abstract*—We report a novel approach to enable thin (≤15Å) ALD-based TaN barriers. The use of a post-ALD treatment in a PVD chamber resulted in ALD films with resistivity, density and Ta/N ratio similar to industry-standard PVD TaN. This approach enables conformal Cu barrier without reliability degradation compared to PVD TaN. This new approach overcomes the shadowing effect of the traditional PVD approach, improves the metal-fill process window, and promotes lower via resistance through barrier thickness reduction, proving it to be a viable Cu-barrier candidate for 5nm node and beyond.**

Keywords—TaN; barrier; copper interconnect; reliability; resistance; back end of line (BEOL)

I. INTRODUCTION

Resistance and reliability are the most critical problems for Copper (Cu) interconnect extension to 5nm technology node and beyond. State-of-the-art Cu metallization primarily uses Physical Vapor Deposition (PVD) of Tantalum Nitride (TaN) as metal barrier together with PVD Ta or Chemical Vapor Deposition (CVD) Cobalt (Co) or Ruthenium (Ru) liners. Barrier and liner are crucial to maintain gap-fill and reliability but occupy conductor volume. In addition, non-conformal PVD step coverage leads to gap-fill challenges with overhang and high via resistance with thicker barrier at via bottom.

To address the above issues, conformal thin barrier is preferred to maximize gap-fill window and minimize via resistance. However, conformal barrier, such as ALD or CVD TaN, could not meet the PVD TaN performance because of low density and high resistivity. As such, a transitional approach of ALD TaN + PVD TaN bilayer barrier was proposed to reduce the PVD TaN overhang. Thus, a lower via resistance and a wider gap-fill window can be achieved. By maintaining the PVD TaN and liner interface, there is no reliability penalty when compared to an all PVD TaN approach.

As critical dimension continues to shrink to 5nm node and beyond, the bilayer approach faces scaling challenges such as thickness control and PVD TaN over-hang. To overcome such challenges, an approach of treating ALD TaN in a PVD chamber was proposed and validated.

II. CONCEPT OF TAN BARRIER TREATMENT

Thermally deposited ALD TaN is a nitrogen rich film with low density and high resistivity [1]. Therefore, ALD TaN leads to poor Cu diffusion barrier property and high via resistance.

To make ALD TaN a suitable Cu diffusion barrier, it is necessary to reduce N as well as other impurities, such as C and O, and increase Ta concentration in the film. For such purpose, a novel process in a PVD chamber is introduced to treat ALD TaN. The proposed treatment is performed on an ALD TaN surface instead of directly on a porous Ultra Low-k (ULk) dielectric surface, thus there is less dielectric damage concern. PVD treatment turns ALD TaN from a low density, high resistivity film into a PVD-TaN-like film with optimized density and resistivity. In addition, TaN thickness is minimized to achieve low via resistance.

III. RESULTS AND DISCUSSION

A. Blanket film characterization

As a first step for TaN based Cu barrier selection, we identified film density and resistivity as key performance indicators for TaN process development. These are based on blanket films characterizations.

TaN density was calculated from X-Ray-Reflectivity (XRR) curve fitting of 100Å TaN on a SiO_2 substrate. Fig.1(a) shows the density ratio of ALD TaN based films to PVD TaN. As-deposited thermal ALD TaN has ~30% lower density than PVD TaN, which is a proven barrier. With a treatment in a PVD chamber, ALD TaN reaches an equivalent density as PVD TaN.

Fig. 1(b) compares blanket TaN film resistivity from 4-point probe measurements. PVD treatment is able to reduce ALD TaN film resistivity by more than 100 times, reaching the same resistivity as PVD TaN.

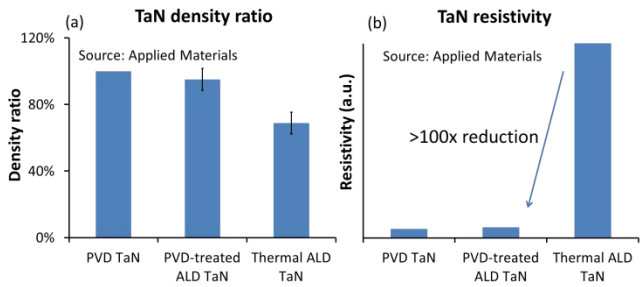

Fig. 1. TaN based films density(a) and resistivity(b) comparison.

B. Cu diffusion barrier

To evaluate a TaN film's capability of preventing Cu diffusion, a single-damascene metal-oxide-semiconductor

capacitor (MOSCAP) test vehicle was developed. The MOSCAP structure consists of Cu/TaN/40nm SiO_2/P-type Si as shown in Fig. 2. The structure is fabricated through a single-damascene metallization process, which include Cu barrier seed deposition, Cu electroplating fill, chemical-mechanical-planarization (CMP), passivation, etc. The process flow simulates the back-end-of-line (BEOL) Cu interconnect process.

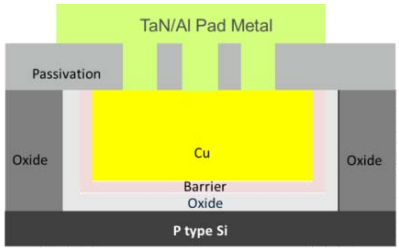

Fig. 2. A single-damascene MOSCAP structure (not to scale) for a Cu barrier evaluation.

During a MOSCAP structure electrical test, a capacitance-voltage (CV) sweep curve is recorded with an AC voltage (1MHz) and a DC voltage that is swept from 5v to -15v. Then the structure goes through a bias thermal stress (BTS). Electric field is set at 2.5MV/cm. Electrical stress time is set for 1 hour. Stress temperature is set at 180°C. After BTS, CV is measured again. Barrier failure is reviewed by comparison of pre and post BTS CV curves. A negative flat band voltage (Vfb) shift indicates Cu ion diffusion or barrier break down [2].

Fig.3 compares pre and post CV curves of thermal ALD TaN and PVD-treated ALD TaN at the same thickness. There is ~10V Vfb shift for thermal ALD TaN after BTS. It is believed that barrier failure leads to Cu ion diffusion, thus Vfb shifts in this case. For PVD-treated ALD TaN, the pre and post BTS CV curves overlap, indicating that the barrier remains intact after BTS. PVD TaN control film shows the same results (CV curves are not shown) as PVD-treated ALD TaN of the same thickness. Therefore, a treatment in PVD chamber can turn ALD TaN from an inadequate Cu diffusion barrier to an effective Cu diffusion barrier.

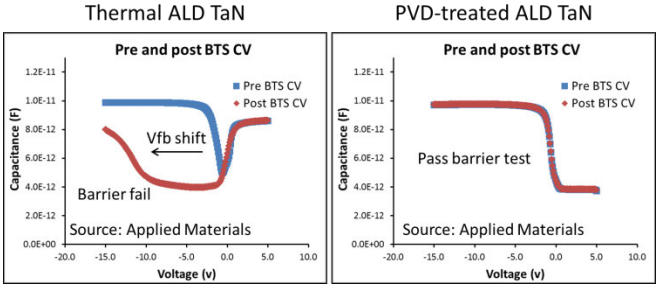

Fig. 3. CV-BTS comparison of thermal ALD TaN and PVD-treated ALD TaN.

The PVD-treated ALD film was then integrated in a 44nm-pitch Copper-ULK(k~2.6) test vehicle to characterize Cu fill, time-dependent dielectric breakdown (TDDB), electromigration (EM) and via resistance. Fig.4 shows a cross-sectional transmission electron microscopy (TEM) image of the test vehicle.

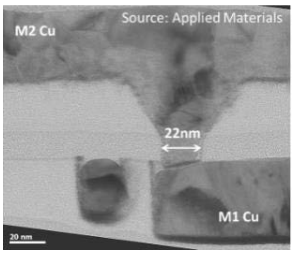

Fig. 4. Cross-sectional TEM of 44nm-pitch Copper-ULK(k~2.6) test vehicle.

C. *Cu gap-fill*

One of the key differentiations of PVD-treated ALD TaN is overhang reduction when compared to PVD TaN. This leads to a wider Cu gap-fill window for small features.

Fig. 5 shows scanning electron microscope (SEM) images of 15nm-CD dual-damascene (DD) structures after ion milling. Structures at different locations were ion milled to different depths. For example, the left part of the SEM image represents the lower part of DD structures; the right part represents the middle or upper part of DD structures. Accordingly, gap-fill can be assessed with statistics. It is confirmed in Fig. 5 that PVD-treated ALD TaN provides wider gap-fill window than PVD TaN. In this study, Co liner is used with both barriers, and fill is by electroplating.

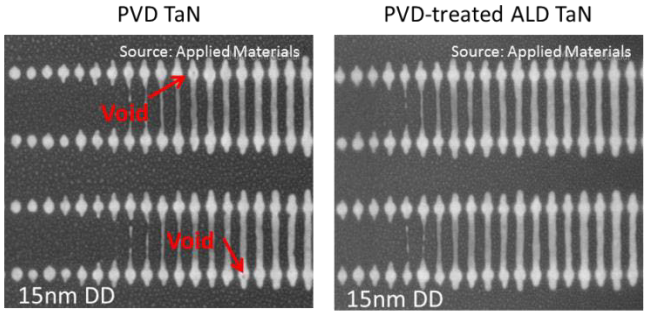

Fig. 5. Post ion milling SEM images to assess Cu gap-fill performance.

D. *Time-dependent dielectric breakdown (TDDB)*

TDDB is another approach to check the Cu diffusion barrier performance. A weak barrier will lead to Cu diffusion into the dielectric, causing leakage and dielectric breakdown. TDDB testing was performed on a structure with 22nm half-pitch comb capacitors in porous ULk (dielectric constant ~2.6). The dielectric space is 20nm. Test temperature was set at 105°C and electrical field was selected based on breakdown voltages. When the leakage current exceeds the threshold current of 0.1mA, the structure is considered "broken down". TDDB lifetime is then predicted based on exponential model, which is a conservative lifetime prediction model [3].

Fig.6 shows a TDDB comparison of TaN based barriers, both with Co liner and Cu electroplating fill. It was found that ALD TaN alone couldn't pass TDDB 10-year lifetime criterion, indicating barrier failure. With the same barrier thickness as ALD TaN, PVD-treated ALD TaN increases TDDB lifetime to be equivalent to the PVD-TaN-based control, which requires a thick film deposition to maintain

sidewall coverage. Therefore, PVD-treated ALD TaN is a good barrier from TDDB perspective.

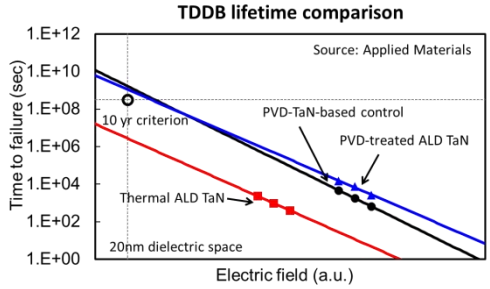

Fig. 6. TDDB comparison of TaN based barriers deposited with different approaches.

E. Electromigration (EM)

Cu EM can be affected by multiple interfaces [4], such as Cu-dielectric barrier, porous ULK dielectric-barrier, barrier-liner, and liner-Cu interfaces. An ideal barrier should provide good adhesion between porous ULK and liner. In addition, the barrier should also provide a good nucleation surface for subsequent liner deposition, which is critical for Cu gap-fill and EM.

In this study, EM stress was performed on a 2-level metal structure after passivation on packaged dies. An upstream EM structure with 22nm via and trench was stressed with a current density of 1.5 MA/cm^2 at 325°C. EM line resistance was monitored during the stress. 10% resistance increase indicates EM failure.

Fig.7 shows EM lifetime comparison of PVD-treated ALD TaN and PVD-TaN-based control. Except for the barrier difference, both conditions are using the same process flow with Co liner, Cu fill and Co cap. It is shown that PVD-treated ALD TaN is able to achieve equivalent EM lifetime as the PVD-TaN-based control condition.

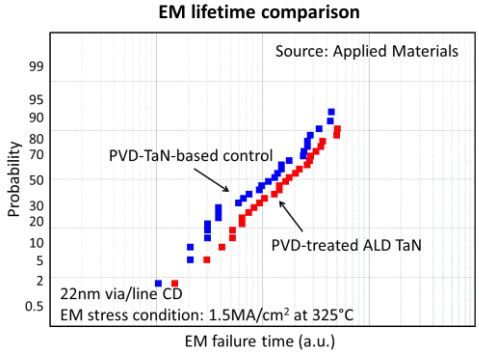

Fig. 7. EM lifetime comparison of PVD-TaN-based control and PVD-treated ALD TaN.

F. Via resistance

The barrier plays a key role in RC scaling [5]. In a line structure, barrier thickness reduction enables more Cu conductor volume, thus lower interconnect resistance. Via resistance consists of barrier, liner, and Cu resistors in a series, so each film resistance contributes to the total via resistance. In addition, TaN barrier resistivity is more than 10 times higher than Cu and liner, such as Co or Ru, thus the barrier plays the dominant role in controlling via resistance. Barrier thickness and resistivity reduction are the most effective ways to reduce via resistance.

Fig.8 compares Kelvin via resistance of PVD-TaN-based control and PVD-treated ALD TaN collected from the 44nm-pitch test vehicle. PVD-treated ALD TaN shows 20% lower via resistance than the PVD-TaN-based control. Both films show the same resistivity based on blanket wafer characterization as shown in Fig. 1(b). Thus, a via resistance benefit comes from the barrier thickness reduction offered by PVD-treated ALD TaN when compared with PVD-TaN-based control. In order to achieve a minimum barrier thickness on the sidewall, a PVD TaN deposition must be thick at via bottom due to step-coverage effect, thus higher via resistance.

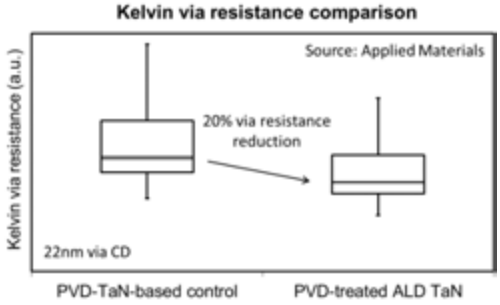

Fig. 8. Via resistance comparison of PVD-TaN-based control and PVD-treated ALD TaN.

IV. CONCLUSIONS

In summary, we have evaluated a novel approach to improve ALD TaN as a Cu diffusion barrier by treating the film in a PVD chamber. Our blanket wafer characterization shows that PVD-treated ALD TaN is able to reach equivalent density and resistivity as PVD TaN. Electrical performance, measured by CV-BTS and TDDB, shows PVD-treated ALD TaN is an effective Cu barrier. EM of PVD-treated ALD TaN is also equivalent to control condition indicating good ULK dielectric-barrier and barrier-liner interfaces. Thus, PVD-treated ALD TaN is a viable barrier candidate for Cu interconnect extension to 5nm technology node and beyond.

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