Advanced Logic Synthesis HW3 Report

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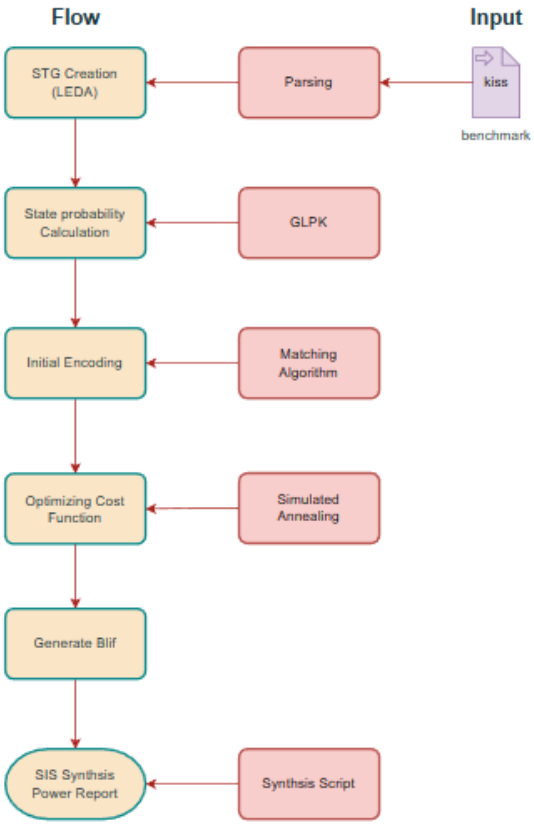
Design Flow :

下圖是我的 design flow :



1. input 一個 benchmark 的 kiss 檔，透過 LEDA 將 Finite State Machine 的 State Transition Graph 建立出來，建出來的 Graph 是一個 Direct Weight Graph，將每條 Edge 的 Weight 做 Normalization 得出 Transition Probability 。
2. 計算 State 的 Stable Probability，用前面的 Transition Probability 建立 Markov Matric，把它 Formula 成 Linear Programming 的問題，交給 GLPK 解出 Stable Probability 。有了 Transition Probability 和 Stable Probability 就能算出 Total Transition Probability。
3. 產生 Initial 的 Encode，需要建立一個 Undirect Weight Graph 來運行 Maximum Matching 。Graph Edge 的 Weight 為 Total Transition Probability，將會影響 Power 的 Total Transition

Probability 作為 Cost，接著運行 Matching 將高的 Cost 的 Edge 存起來，幫它們編上僅一個 bit 不同的編碼，至於沒被選上的 Edge 就照順序 Sequence 的編碼，這樣 Initial 的編碼就完成了。

$$cost = \sum_{allpairs(s,t)} w(s,t) * hanminDist(enc(s)\ ,\ enc(t))$$

4. 接著透過 Simulated Annealing 來優化 Encode 的結果，並將結果存成 Blif 檔再透過 SIS 來分析結果，而 SA 用的 cost 則是直接以 SIS 的 Power 結果來取值

Experiment Result :

seting : 20 MHz clock , VDD = 5v (using Zero delay model)

Initial Encode 的 Power 結果 :

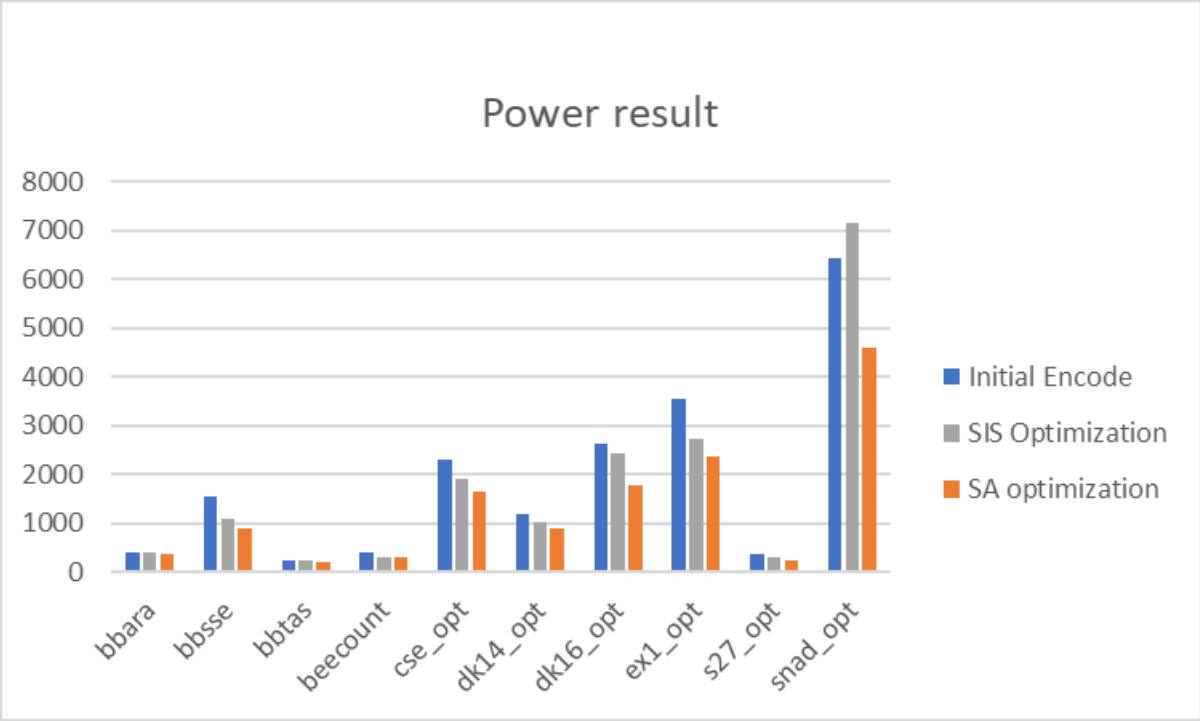
```
Network: bbara_opt.blif, Power = 401.3 uW assuming 20 MHz clock and Vdd = 5V
Network: bbsse_opt.blif, Power = 1551.4 uW assuming 20 MHz clock and Vdd = 5V
Network: bbtas_opt.blif, Power = 241.2 uW assuming 20 MHz clock and Vdd = 5V
Network: beecount_opt.blif, Power = 406.6 uW assuming 20 MHz clock and Vdd = 5V
Network: cse_opt.blif, Power = 2298.1 uW assuming 20 MHz clock and Vdd = 5V
Network: dk14_opt.blif, Power = 1178.2 uW assuming 20 MHz clock and Vdd = 5V
Network: dk16_opt.blif, Power = 2620.2 uW assuming 20 MHz clock and Vdd = 5V
Network: ex1_opt.blif, Power = 3555.5 uW assuming 20 MHz clock and Vdd = 5V
Network: s27_opt.blif, Power = 373.4 uW assuming 20 MHz clock and Vdd = 5V
Network: snad_opt.blif, Power = 6420.8 uW assuming 20 MHz clock and Vdd = 5V
```

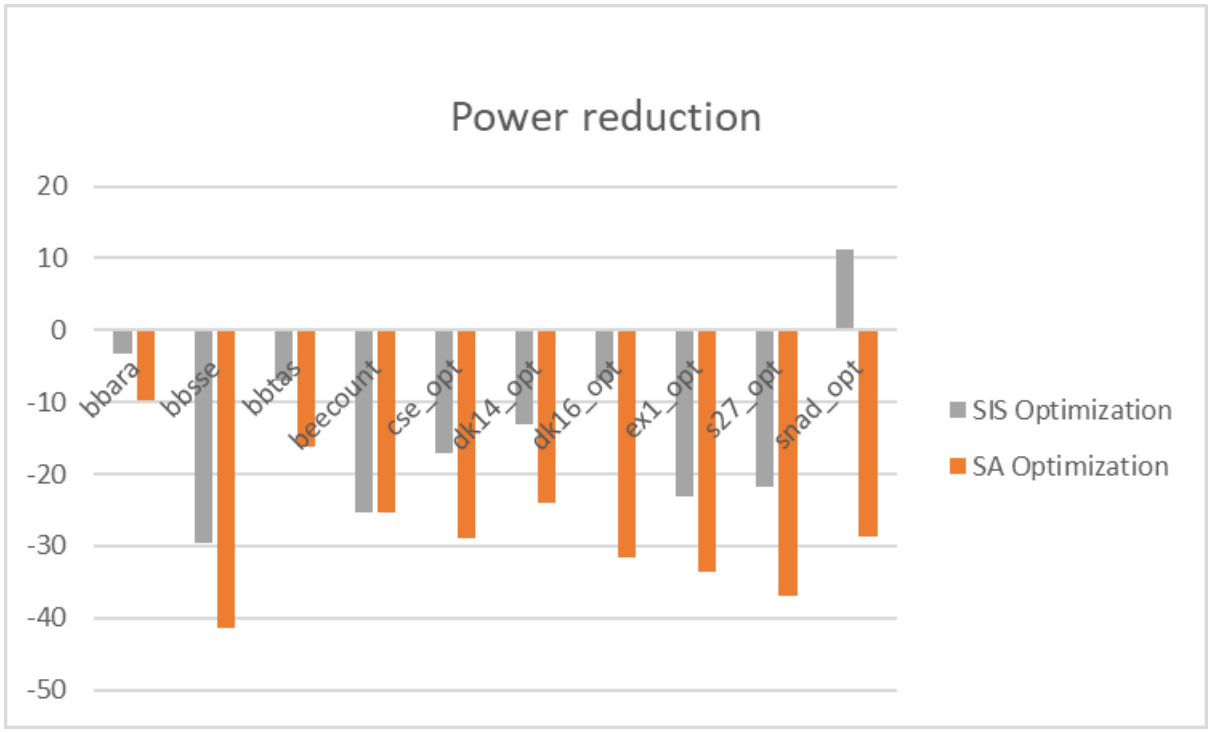
SA 優化後的 Power 結果 :

```
Network: bbara_opt.blif, Power = 362.2 uW assuming 20 MHz clock and Vdd = 5V
Network: bbsse_opt.blif, Power = 909.5 uW assuming 20 MHz clock and Vdd = 5V
Network: bbtas_opt.blif, Power = 202.2 uW assuming 20 MHz clock and Vdd = 5V
Network: beecount_opt.blif, Power = 303.5 uW assuming 20 MHz clock and Vdd = 5V
Network: dk14_opt.blif, Power = 895.7 uW assuming 20 MHz clock and Vdd = 5V
Network: cse_opt.blif, Power = 1605.8 uW assuming 20 MHz clock and Vdd = 5V
Network: dk16_opt.blif, Power = 1792.8 uW assuming 20 MHz clock and Vdd = 5V
Network: ex1_opt.blif, Power = 2363.0 uW assuming 20 MHz clock and Vdd = 5V
Network: s27_opt.blif, Power = 235.6 uW assuming 20 MHz clock and Vdd = 5V
Network: snad_opt.blif, Power = 4584.1 uW assuming 20 MHz clock and Vdd = 5V
```

以我 Initial 的 encode 當 Baseline 跟 SIS 的 state assign 還有我的 SA 結果進行比較 :

	Initial Encode	SIS optimization	Result	SA Optimization	Result
<testcase>.kiss	Power(uW)	Power(uW)	Reduction(%)	Power(uW)	Reduction(%)
bbara	401.3	388.2	- 3.2	362.2	- 9.7%
bbsse	1551.4	1092.9	- 29.5	909.5	- 41.3%
bbtas	241.2	224.0	- 7.1	202.2	- 16.1
beecount	406.6	303.5	- 25.3	303.5	- 25.3
cse_opt	2298.1	1906.2	- 17	1605.8	- 30.1
dk14_opt	1178.2	1023.2	- 13.1	895.7	- 23.9
dk16_opt	2620.2	2433.0	- 7.1	1792.8	- 31.5
ex1_opt	3555.5	2727.9	- 23.2	2363.0	- 33.5
s27_opt	373.4	292.1	- 21.7	235.6	- 36.9
snad_opt	6420.8	7142.8	11.2	4584.1	- 28.6




Power reduction
20
10
0
-10
-20
-30
-40
-50
bbara
bbsse
bbtas
beecount
cse_opt
dk14_opt
dk16_opt
ex1_opt
s27_opt
snad_opt
SIS Optimization
SA Optimization