

## CS 516000 FPGA Architecture & CAD Final Project

1. 獨力完成 111062697 吳律穎

2.

How to compile :

In 111062697\_final\_project/ directory, enter the following command:

\$ make

It will generate the executable file "topart" in "

If you want to remove it, please enter the following command:

\$ make clean

How to execute :

In 111062697\_final\_project/ directory, enter the following command:

Usage: ./[exe] ./input/[input.txt] ./output/[output.txt]

e.g.

./topart ./input/B1.txt ./output/output1.txt

3. 執行結果: Fixed 和 Partition size 都有 pass, 且執行時間並未超過 10min

```
fpga-111062697@MakLab:~/final/111062697_final_project$ ./verify ./input/B1.txt ./output/output
1.txt
===== Evaluator =====
Check Fixed node constraint pass.
Check Partition size constraints violation pass.
The total topology constraints violations is 0
The sum of external degree is 45
=====
fpga-111062697@MakLab:~/final/111062697_final_project$ ./verify ./input/B2.txt ./output/output
2.txt
===== Evaluator =====
Check Fixed node constraint pass.
Check Partition size constraints violation pass.
The total topology constraints violations is 32
The sum of external degree is 258
=====
fpga-111062697@MakLab:~/final/111062697_final_project$ ./verify ./input/B3.txt ./output/output
3.txt
===== Evaluator =====
Check Fixed node constraint pass.
Check Partition size constraints violation pass.
The total topology constraints violations is 10
The sum of external degree is 648
=====
fpga-111062697@MakLab:~/final/111062697_final_project$ ./verify ./input/B4.txt ./output/output
4.txt
===== Evaluator =====
Check Fixed node constraint pass.
Check Partition size constraints violation pass.
The total topology constraints violations is 3
The sum of external degree is 1444
=====
fpga-111062697@MakLab:~/final/111062697_final_project$ ./verify ./input/B5.txt ./output/output
5.txt
===== Evaluator =====
Check Fixed node constraint pass.
Check Partition size constraints violation pass.
The total topology constraints violations is 197
The sum of external degree is 13549
=====
fpga-111062697@MakLab:~/final/111062697_final_project$ ./verify ./input/B6.txt ./output/output
6.txt
===== Evaluator =====
Check Fixed node constraint pass.
Check Partition size constraints violation pass.
The total topology constraints violations is 1872
The sum of external degree is 73090
=====
fpga-111062697@MakLab:~/final/111062697_final_project$ ./verify ./input/B7.txt ./output/output
7.txt
===== Evaluator =====
Check Fixed node constraint pass.
Check Partition size constraints violation pass.
The total topology constraints violations is 3471
The sum of external degree is 145254
=====
fpga-111062697@MakLab:~/final/111062697_final_project$ ./verify ./input/B8.txt ./output/output
8.txt
===== Evaluator =====
Check Fixed node constraint pass.
Check Partition size constraints violation pass.
The total topology constraints violations is 8645
The sum of external degree is 295646
```

```

fpga-111062697@MakLab:~/final/111062697_final_project$ time ./topart ./input/B1.txt ./output/output1.txt
real    0m0.003s
user    0m0.002s
sys     0m0.001s
fpga-111062697@MakLab:~/final/111062697_final_project$ time ./topart ./input/B2.txt ./output/output2.txt
real    0m0.004s
user    0m0.004s
sys     0m0.000s
fpga-111062697@MakLab:~/final/111062697_final_project$ time ./topart ./input/B3.txt ./output/output3.txt
real    0m0.025s
user    0m0.025s
sys     0m0.000s
fpga-111062697@MakLab:~/final/111062697_final_project$ time ./topart ./input/B4.txt ./output/output4.txt
real    0m0.066s
user    0m0.059s
sys     0m0.008s
fpga-111062697@MakLab:~/final/111062697_final_project$ time ./topart ./input/B5.txt ./output/output5.txt
real    0m0.805s
user    0m0.768s
sys     0m0.036s
fpga-111062697@MakLab:~/final/111062697_final_project$ time ./topart ./input/B6.txt ./output/output6.txt
real    0m20.834s
user    0m20.769s
sys     0m0.064s
fpga-111062697@MakLab:~/final/111062697_final_project$ time ./topart ./input/B7.txt ./output/output7.txt
real    1m19.652s
user    1m19.509s
sys     0m0.140s
fpga-111062697@MakLab:~/final/111062697_final_project$ time ./topart ./input/B8.txt ./output/output8.txt
real    4m52.708s
user    4m52.431s
sys     0m0.272s

```

#### 4. Describing the details

演算法的部分依照 Reference paper 來實作，可是沒有實現 B 部分的 Candidate FPGA-driven Coarsening，其餘部分都有做出來