

VLSI HW1

(1) 111062697 吳律穎

(2)比較表格

設 period : 20, waveform : 10 , core utilization : 0.7

	(congestion-driven, timing-driven)					
	(L, off)	(L, on)	(M, off)	(M, on)	(H, off)	(H, on)
Slack(ns)	16.379	16.511	16.346	16.496	16.346	16.496
total wirelength(um)	311835.948	309829.965	312612.562	310789.010	312612.562	310789.010

設 period : 3.5 , waveform : 1.0 , core utilization : 0.96

	(congestion-driven, timing-driven)					
	(L, off)	(L, on)	(M, off)	(M, on)	(H, off)	(H, on)
Slack(ns)	0.111	0.097	0.138	0.154	0.138	0.154
total wirelength(um)	271019.872	273476.395	271526.590	271747.555	271526.590	271747.555

(3)於我的實驗中，

- congestion-driven 調高強度時傾向多拉 wire 來解決 congestion
- timing-driven 則是透過減少 wire 長度使 arrive time 提早

但在我的 best result 的設置下，情況如第二個表格，(L,on)的情況下反而出現加長了長度而且 slack 還變小，根據其 timing report 中在同一條 path 上在前面幾個 Instance 時 arrive time 會比較快，但在最後卻變慢了，應該是有一些 greedy 的方法在裡面所導致

(4) 為了填充 cell 中間的空隙，把擴散層連接起來，以滿足 DRC 規則和設計需求。

(5) My best result

Clock period : 3.5 1.0

```
create_clock [get_ports {clk}] -name VCLK -period 3.5 -waveform {0.0 1.0}
```

Core Utilization : 0.96

```
floorPlan -coreMarginsBy die -site FreePDK45_38x28_10R_NP_162NW_340 -r 1.0 0.96 4.0 4.0 4.0 4.0
```

Congestion Effort : low , Run Timing Driven Placement : off

```
setPlaceMode -congEffort low -timingDriven 0 -clkGateAware 1 -powerDriven 0 -ignoreScan 1 -reorderScan 1 -ignoreSpare 0
```

Total area of chip : 40377.842 um²

Total area of Standard cells: 37134.398 um²
Total area of Standard cells(Subtracting Physical Cells): 34631.072 um²
Total area of Macros: 0.000 um²
Total area of Blockages: 0.000 um²
Total area of Pad cells: 0.000 um²
Total area of Core: 37134.398 um²
Total area of Chip: 40377.842 um²

Total wire length : 271019.8725um

Total metal1 wire length: 2013.6650 um
Total metal2 wire length: 70258.2250 um
Total metal3 wire length: 95926.7175 um
Total metal4 wire length: 50455.3000 um
Total metal5 wire length: 31951.1050 um
Total metal6 wire length: 14081.0600 um
Total metal7 wire length: 1481.2000 um
Total metal8 wire length: 3386.9200 um
Total metal9 wire length: 812.1600 um
Total metal10 wire length: 653.5200 um
Total wire length: 271019.8725 um
Average wire length/net: 14.3739 um

Slack Time : 0.111ns

Other End Arrival Time	0.000
- Setup	0.044
+ Phase Shift	3.500
= Required Time	3.456
- Arrival Time	3.345
= Slack Time	0.111

DRC : 0 Viols

```
VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {136.080 133.920 201.970 199.920} 9 of 9 Thread : 7
VERIFY DRC ..... Sub-Area: {136.080 0.000 201.970 66.960} 3 of 9 Thread : 0
VERIFY DRC ..... Sub-Area: {0.000 0.000 68.040 66.960} 1 of 9 Thread : 3
VERIFY DRC ..... Sub-Area: {0.000 133.920 68.040 199.920} 7 of 9 Thread : 4
VERIFY DRC ..... Sub-Area: {136.080 66.960 201.970 133.920} 6 of 9 Thread : 0
VERIFY DRC ..... Sub-Area: {0.000 66.960 68.040 133.920} 4 of 9 Thread : 4
VERIFY DRC ..... Sub-Area: {68.040 0.000 136.080 66.960} 2 of 9 Thread : 4
VERIFY DRC ..... Sub-Area: {68.040 133.920 136.080 199.920} 8 of 9 Thread : 0
VERIFY DRC ..... Thread : 4 finished.
VERIFY DRC ..... Sub-Area: {68.040 66.960 136.080 133.920} 5 of 9 Thread : 0
VERIFY DRC ..... Thread : 0 finished.

Verification Complete : 0 Viols.
```

