HF Controls

HFC-6000 Control System

HFC-FPC08
C-Link/FCL Link Gateway
(PAS Version)

Software Requirement Specification

RS901-002-24 Rev E

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Revision History

Date	Revision	Author	Changes
01/20/2020	A	Samuel Wang	Initial Revision.
04/28/2021	B	D. Pantalion	Add FPGA PN and OV/UV Checking
06/28/2023	C	N. Shrestha	Add master side validation for slave firmware Add application files validation
01/15/2024	D	N.Shrestha	Added Redundancy requirements (CR2023-0175)
04/25/2024	E	N.Shrestha	Added requirements for controller diagnostics, C-link ethernet status, packet data format

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1. Introduction

1.1 Purpose of the Document

The purpose of this document is to identify all software requirements for the HFC-FPC08 controller board implementation of C-Link to FCL link and FCL link to C-Link gateway. The gateway for PAS should provide FCL link connectivity.

1.2 Scope of the Software

The scope of this document is to specify the software requirements for the HFC-FPC08 C-Link/FCL link Gateway card for PAS project.

The gateway software mainly contains two categories of functionality. One is C-Link module, and another is FCL link module. C-Link module includes C-Link protocol submodule, incoming remote DDB data monitoring/processing/recording, and outgoing DDB data broadcasting. FCL link module includes FCL link messages broadcast to FPCIOs from incoming remote DDB data and FCL link messages response/processing.

1.3 Scope of the Hardware

The HFC-FPC08 assembly is a single-board computer that provides the capability for 4 Ethernet CAT5 connections and FCL link connectivity through FPGA.

1.4 Definitions, Acronyms, and Abbreviations

CPU	Central Processing Unit
CPC	Communication Protocol Controller
CRC	Cyclic Redundancy Check
DDB	Dynamic Data Base
DPM	Dual Ported Memory
EWS	Engineering Work Station
FCL	FPCIO Communication Link
FPGA	Field Programmable Gate Array
F-Link	FPGA communication link that uses the token-passing protocol developed for the C-Link and backplane hardware traces developed for the ICL.
G-Link	Gateway communication link that uses the token-passing protocol developed for the C-Link and backplane hardware traces developed for the ICL.
HFC	HF Controls
I/O	Input/Output
KHNP	Korean Hydro Nuclear Power
LED	Light Emitting Diode
OIS	Operator Information Station
PAS	Plant Annunciator System
PCS	Plant Control System
RX	Receive
TCP/IP	Transmission Control Protocol/Internet Protocol
TX	Transmit
UCP	Universal Communication Protocol
V&V	Verification and Validation

LPC	Low Pin Count (connection interface between redundant FPC08s)

1.5 References & Standard Compliance

40103881	HFC-FPC08 PCB Assembly
WI-ENG-202	Development of Software/Firmware Requirements Specification, Rev. F
RS901-000-85	HFC-FPC08 Requirement Specification, Rev B
DS002-000-01	C-Link Protocol Design Spec, Rev D
DS901-001-99	HFC-FPC08 G-Link Gateway Software Design Spec., Rev. A
WI-VV-001	Software Verification and Validation Procedures

2. Overall Description

2.1 System Perspective

The gateway is typically used as a bridge between a C-Link and a FCL link. One example of its implementation is SOE Input controller system on the C-Link side, and 6 FPCIOs cards on the FCL link side.

2.2 System Functions

The FPC08 collects all incoming remote DDB data from the C-Link and formats the FCL link data for broadcasting to the FCL links. It also can provide a FCL interface implementation for use by the FPCIO side to broadcast response data to the EWS on the C-Link.

2.3 HFC-FPC08 Gateway Cards

A 14-slot HFC-6000 rack is used to install redundant HFC-FPC08 gateway controllers. The HFC-FPC08 has 2 Ethernet ports to be used for C-Link networks and FCL link for 6 paired FPCIO cards.

2.4 User Characteristics

The user can configure the incoming remote DDB FILTER of the gateway.

2.5 Constraints

RS901-002-24-2-5

The FPC08 operating system shall be QNX 6.3.2.

2.6 Assumptions and Dependencies

We assume that the FCL link network connection from the FPC08 controllers to the C-Link network and the C-Link network from the FPC08 controllers to FCL link network connection will have enough bandwidth to support the performance requirements of the system.

3. Specific Requirements

3.1 HFC-FPC08 C-Link Gateway module

3.1.1 Operating Modes

RS901-002-24-311-1

1. The master shall validate the slave firmware. If validation fails, the system should log the error, and fail the board.

RS901-002-24-311-2

2. Application files for RQ Table and Rem Config shall be validated. If validation fails, the system should log the error, and fail the board.

3. During initialization, the module shall perform memory tests, initialize variables, and create memory regions as needed. If successful, the firmware shall enter normal mode.
4. In normal mode, the module shall perform its function as described in the functional requirements.

3.1.2 External interface requirements

1. The module uses two Ethernet interfaces on the FPC08 to connect to the C-Link (redundant).
2. The C-Link remote number is read from the front panel rotary switches. The C-Link sequence number is identical to the remote number.

3.1.3 User Interface requirements

There is no user interface for this module. There are no user interface requirements.

3.1.4 Software Interface requirements

There is a shared memory segment that the module uses to store all C-Link data.

3.1.5 Internal Interface requirements

There are no internal interface requirements.

3.1.6 Function Requirements

RS901-002-24-316-1

1. The C-Link monitoring protocol submodule shall do token passing on the C-Link.

RS901-002-24-316-2

2. The C-link monitoring submodule shall collect all incoming remote DDB data and UCP data from the C-Link and store it in shared memory for use by the FCL link module.

RS901-002-24-316-3

3. The FPC08 shall configure internal data based on the C-Link traffic that it receives through mapping table. The mapping table is a text file with the name rqDat63.sxx The format for filtering DDB data in rqDat63.sxx is as follows:

   FILTER(DDB,`startPt`,`numPts`,`srcRem`,`srcPtType`,`srcPtNum`,`defQW`, `defAct`)

```
UCHAR8    desPtType;     /* destination point type */
UWORD32   startPt;       /*  starting point # */
UWORD32   numPts;        /*  #of points for this transfer*/
UWORD32   srcRem;        /*  source remote # */
UWORD32   srcPtType;     /*  source point type */
UWORD32   srcPtNum;      /*  source point # */
UWORD32   defQW;         /*  default quality word */
UWORD32   defAct;        /*  default action */
```

   For Example: FILTER(DDB,2497,528,1,FL,2497,0,0)

RS901-002-24-316-4

4. The broadcast submodule shall broadcast the DDB data from FCL link response messages using C-Link packets.
   The format for broadcasting DDB data is defined in rqDat63.sxx as follows:
   DDB(point type, starting number, number of points)

```
UCHAR8    ptType;        /* point type */
UWORD32   startPt;       /* starting point # */
UWORD32   numPts;        /* # of points */
```

   For example: DDB(CO,1,1000)

RS901-002-24-316-5

5. The packets shall conform to the data format as specified below while also supporting ddb combo mode.

   The data structure for C-link packet is defined as follows:

```
typedef struct _CPCMAC_BLOCK {
        BYTE  destAddr[6];
        unsigned char  srcAddr[6];
        WORD  length;
        unsigned char  destID;
        unsigned char  srcID;
        WORD  sendSeqNo;
        BYTE  packetNo;
        BYTE  controlByte;
        WORD  msgNo;
        WORD  pduSize;
        BYTE  controlIntf;
        BYTE  headerType;
        WORD  messageSize;
        BYTE  tag[2];
```

```
        BYTE  commArrayNo;
        BYTE  destIntCmd;
        BYTE  securityCD;
        BYTE  destBufPtr[3];
        BYTE  iopbPtr[4];
        BYTE  rtnBuf[3];
        BYTE  rtnDesInt;
        BYTE  rtnNoting;

        WORD  rtnByteCount;
        BYTE  soeTimer[7];
        BYTE  rsFlag;
        WORD  rsCatgry;
        BYTE  rsPrists;
        BYTE  rsStatus;
        BYTE  rsRcount;
        BYTE  rsNumEnt;
        unsigned char  rsRemNo;
        WORD  rsCatgry1;
        BYTE  rsPrists1;
        BYTE  rsStatus1;
        BYTE  rsRcount1;
        BYTE  ddbSpr;
        BYTE  ddbFlag;
        BYTE  ddbType;
        WORD  ddbNo;
        WORD  ddbStartNo;
        WORD  ddbCurrentStartNo;
        WORD  ddbCurrentNo;
        BYTE  ddbdata[1500];
    } CPCMAC_BLOCK, *PCPCMAC_BLOCK;
```

RS901-002-24-316-6

6. The data broadcast rate shall be at the same rate as the source data is received by the C-Link monitoring submodule.

RS901-002-24-316-7

7. The software shall monitor the link status of the C-Link Ethernet Ports. The link status shall be available in system flag (FL) points.

3.2 HFC-FPC08 FCL link module

3.2.1 Operating Modes

RS901-002-24-321-1

1. Application file for 'IO table' shall be validated. If validation fails, the system should log the error, and fail the board.

2. In normal mode, the module shall perform its function as described in the functional requirements.

3.2.2 External interface requirements

The module uses DPM memory interface of FPGA (FCL link implementation) to communicate with 6 pair FPCIO cards.

3.2.3 User Interface requirements

There is no user interface for this module. There are no user interface requirements.

3.2.4 Software Interface requirements

The FCL link module is compatible with FCL link protocol standards.

3.2.5 Internal Interface requirements

There are no internal interface requirements.

3.2.6 Function Requirements

RS901-002-24-326-1

1. The incoming remote DDB data available to broadcast to FPCIO cards shall be executed by FCL link Transfer submodule.

RS901-002-24-326-2

2. The FCL link response messages available to convert to system DDB (broadcast to C-Link) shall be executed by FCL link Response submodule.

RS901-002-24-326-3

3. The FPGA overvoltage and undervoltage GPIO signals shall be checked to ensure reliable operation of FPGA hardware. If FPGA overvoltage/undervoltage signal is detected, an error message shall be logged before shutting down the FCL link module.

3.3 Redundancy

RS901-002-24-33-1

1. The redundant FPC08 processors shall both operate in parallel with I/O images being updated as primary controllers. The primary controller's FPGA and C-link module shall handle both transmitting and receiving FCL and C-Link communications correspondingly. Conversely, the secondary controller's FPGA

and C-Link module shall only receive FCL and C-Link communications correspondingly.

RS901-002-24-33-2

2. Redundant controllers shall transition from primary to secondary without bumping ("bumpless") the control process.

RS901-002-24-33-3

3. The FPC08 controllers are hot-swappable. The controllers shall be maintainable, permitting removal and replacement of a controller with equalization of the new controller to full synchronized status.

RS901-002-24-33-4

4. The controllers shall include equalization functions to insure internally calculated statuses, values, and time related conditions match in both controllers.

RS901-002-24-33-5

5. The equalization functions shall only occur if the application files in both primary and secondary controllers are identical.

RS901-002-24-33-6

6. The redundant controllers shall maintain one controller as "primary" and the other as "secondary". For cold start conditions, both controllers shall initialize (including diagnostic checks) as secondary and the first controller to complete initialization shall take primary responsibility.

RS901-002-24-33-7

7. The redundant controllers shall use software mailboxes to monitor controller statuses in support of the controller's "sane" status and "primary/secondary" state. The LPC bus shall be the communication link for this process.

3.4 Controller Diagnostics

RS901-002-24-34-1

1. The software shall monitor the other redundant controller's operational state. "Other controller mailbox" failure will occur if the other controller does not strobe within a certain amount of time (while still meeting the failover time requirement). "Other controller mailbox" failure shall cause the software to treat the other controller as offline on LPC and to become primary (if not already primary) if the other board is also detected offline on C-link.

RS901-002-24-34-2

2. The software shall include diagnostics, including CRC checking of firmware and application. In the event of a CRC failure, indicating corruption of firmware or application files, the software shall exit all tasks to preserve the integrity and stability of the board, preventing potential issues that may arise from the use of corrupt firmware or applications.

RS901-002-24-34-3

3. Any failure of a "task mailbox" shall cause the controller to fail and, if the failed controller was primary, cause the secondary controller to become primary. After a controller failure, the controller shall require a power reset to restart its software.

RS901-002-24-34-4

4. If remote numbers between LPC redundant controllers mismatch, the secondary FPC08's software shall fail itself by exiting all tasks to prevent incorrect application execution in case of primary failure.

4. Performance Requirements

There are no specific performance requirements for the modules at this time. The modules should process the packets from the C-Link interface without disturbing C-Link communication.