Bit Synchronization on Controller Area Network (CAN) Bus

Introduction

The Controller Area Network (CAN) bus is a serial asynchronous bus used in instrumentation applications for industries such as automobiles. The digital messages known as CAN frames are broadcast by the nodes on this shared bus through electronic transceivers. The most popular version of the CAN bus has three wires, one ground wire, and two differential CAN signals. The nodes on the bus broadcast the CAN frame when the bus is idle. The receiving nodes acknowledge the receipt of the correct frame by inserting the dominant bit at the acknowledgement bit position. It is possible for two nodes to start transmitting the CAN frame at the same time. The node with lower precedence CAN frame will withdraw in case of a bus contention.

Baud Rate

The CAN specification does not restrict the baud rate to any specific value. There are many popular baud rates. However, all nodes on the bus must operate at the same predetermined fixed baud rate. The maximum allowed baud rate on a CAN bus is 1 Mbps.

Bit Synchronization

There is no separate clock signal on the CAN bus to synchronize the node the CAN frame itself is used for synchronization of the clocks on all the nodes. To a effectively achieve this CAN frames have NRZ-5 coding. If there are five bits at the same level in the CAN frame a sixth bit of the opposite level is stuffed by the transmitter. This extra stuffed bit is removed by the receiver node before processing the CAN frame.

There is hard synchronization and soft synchronization of node clocks using the CAN frame while all nodes have clocks running at the same baud rate. When the transmitting node sends a CAN frame all the clocks of the receiving nodes are synchronized to the transmitter clock at the falling edge of the "Start of Frame" (SOF) bit. This is the hard synchronization of the clocks. Subsequent falling edges of the CAN frame are used for soft synchronization of the nodes. The difference between the hard synchronization and soft synchronization is that the sampling clock cannot shift by more than a specific amount indicated within the CAN specification.

CAN Clock

The CAN clock used to sample bit value of the CAN frame is derived from a clock running at a much higher frequency. The time period of this clock is known as "one time quanta" and is denoted by Tq. One bit time of the CAN clock is comprised of many time quanta (Tq). The total CAN clock duration is a sum of Synchronization segment (1 Tq), Propagation segment (1-8 Tq), Phase segment 1 (1-8) and Phase segment 2. For ESG CAN IP the Phase segment 2 has the same value as Phase segment 1. The synchronization segment of 1 Tq in the clock period is because of synchronization delay that can occur because the synchronization segment can occur any time within the 1 Tq period. The propagation segment represents the propagation delay that occurs in the transceiver and the cable. The phase segment 1 and phase segment 2 are used to take care of phase errors.

Bit Sampling and Soft Synchronization

The CAN frame is sampled by the receiving node at the middle of phase segment 1 and phase segment 2. The CAN clock can vary between 8 to 25 time quanta (Tq) depending upon the basic clock, baud rate and other factors like phase delay, cable length and the number of nodes. There are many causes of timing errors which lead to the incorrect sampling of data. The most important is the error in the main clock from which the CAN clock is derived and delays in the cable. The CAN frame can be as long as 149 bits. To sample such a long frame correctly the restrictions on clock error and cable length are not practical to achieve.

CAN specifications allow solving this problem by the use of soft synchronization of the CAN clock. The receiving nodes synchronize the CAN clock at all recessive to dominant edges of the CAN frames. Soft synchronization takes care of both positive and negative phase errors in the received CAN frame. A phase error is positive, if the arriving edge is delayed from the expected time; and negative, if it is ahead of the expected time. If there is a positive phase error then the sampling point is delayed by increasing the phase segment 1 delay by positive phase error but not more than the maximum synchronization jump width. Similarly, if there is a negative phase error the sampling point is moved ahead by the amount of the phase error by decreasing the phase error by 2, again limited by the maximum synchronization jump width.

Simulation Results

Following figures show the results for both positive and negative phase errors in the CAN frame corrected by the soft synchronization. The main clock is 50 MHz in each of the waveforms shown below. A 10 MHz clock is derived from it by a divide-by-five counter. The baud rate here is 1 Mbps. To achieve this baud rate the registers are programmed with the following values, propagation segment = 1, phase segment 1 = 4, phase segment 2 = 4 and maximum synchronization jump width = 4. The synchronization segment always equals 1. The sum of all the segments is 10 and provides a CAN clock equal to 10 time quanta (Tq), in this case 1 micro second, time quanta being 100 nano seconds.

No Phase Error

Figures 1 and 2 show the CAN frame (CAN_BUS_SIGNAL), CAN clock (CAN_CLOCK) synchronized to the received CAN frame, the derived sampling clock (RX_CLOCK) and sampled bits (RX_BIT) for the case of no phase error. The baud rate is 1 Mbps, the grid in Figure 1 is 1 micro second and in Figure 2 it is 100 nano seconds. When there is no phase error the CAN signal is sampled 600 nano seconds after the CAN clock.
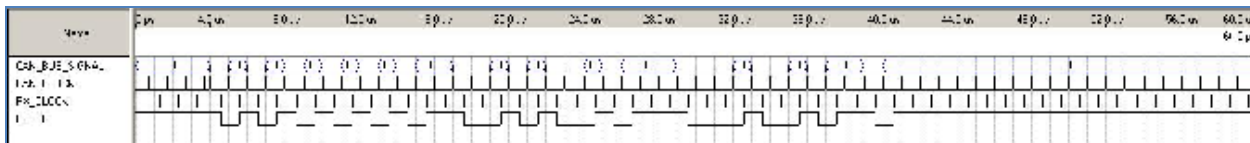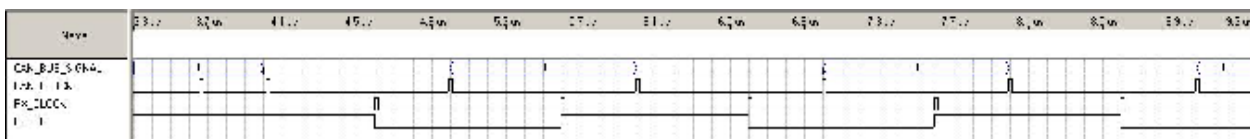

Figure 1 - CAN Frame with No Phase Error

Figure 2 - CAN Frame with No Phase Error (Zoomed View)

Positive Phase Error – 200 nano seconds

Figures 3 and 4 show the CAN frame when the bit following the Start Of Frame SOF bit is delayed by 200 nano seconds. This causes the next falling edge to arrive 200 nano seconds after CAN clock. The sampling clock is delayed by 200 nano seconds by stretching the phase segment 1 by 200 nano seconds.
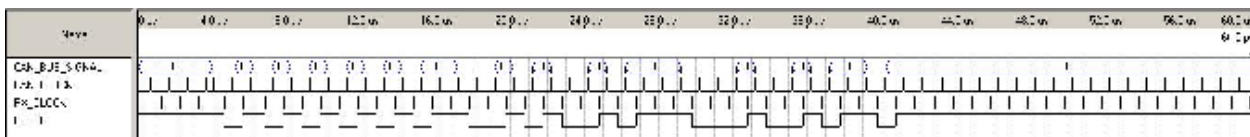

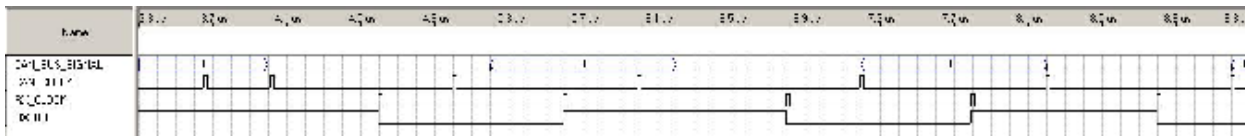**Figure 3 - CAN Frame with 200 nano second Positive Phase Error**

Figure 4 - CAN Frame with 200 nano second Positive Phase Error (Zoomed View)

Negative Phase Error – 200 nano seconds

Figures 5 and 6 show the CAN frame when the bit following the SOF bit is early by 200 nano seconds. It causes the next falling edge to arrive 200 nano seconds early. The sampling clock comes 600 nano seconds after the CAN clock. However, the next CAN clock comes 200 nano seconds early because the Phase segment 2 is shortene by 200 nano seconds.
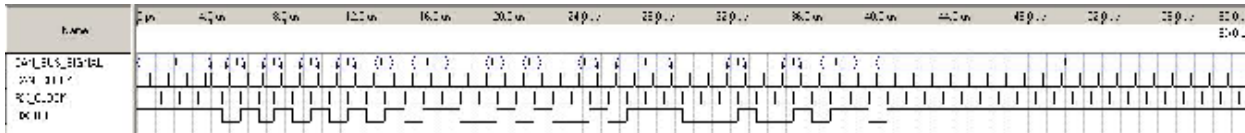
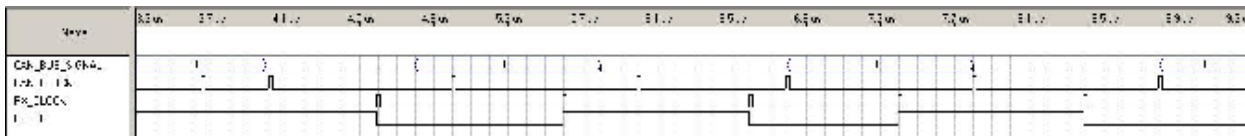**Figure 5 - CAN Frame with 200 nano seconds Negative Phase Error**

Figure 6 - CAN Frame with 200 nano seconds Negative Phase Error (Zoomed View)