UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Fall 1394
Computer Assignment 2
Gates to Expressions in Verilog
Week 5-7

Name:
Date:

1. Write AO (w=a.b+c) description using Verilog gate primitives (and, or, not, nand, etc). Use approximate delay values based on #(3, 4, 5) delay for the NMOS transistors and #(5, 6, 7) for the PMOS transistors back-annotated into structure of AO.
2. Using AO gates of Part 1 to develop the following Boolean expressions. These expressions have four data inputs (A, B, C, and D), four select inputs (i, j, k, and l), and four data outputs (W, X, Y, Z). Assume that at any one time, only one of i, j, k, or l is 1, and the rest are 0.

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W = A . i  +  B . j  +  C . k  +  D . l
X = B . i  +  C . j  +  D . k
Y = C . i  +  D . j
Z = D . i
```

3. Using **assign** statements, develop a Verilog module to perform expressions of Part 2. Assuming AO gates of Part 1 are used, come up with two delay values #(To1, To0) for each of these expressions.
4. The above expressions describe a 4-bit Barrel Shifter. The output becomes the input shifted *n* places if the n^{th} input is 1; only one input can be 1 at the same time (this is a one-hot arrangement). The inputs (i.e., i, j, k, and l) are numbered 0, 1, 2 and 3, respectively. Write the description of the 4-bit Barrel Shifter of Part 2 in Vector form, i.e., use D[3:0] for the data inputs, N[3:0] for shift counts inputs, and W[3:0] for the outputs.
5. Show an iterative network implementing a 16-bit Barrel Shifter. Show Verilog description of this iterative network using AO gates of Part 1. Use Verilog **generate** statement. Simulate and find the worst-case delay of this circuit.
6. Use the worst-case delay obtained from Part 5 in a vector-base description that uses **assign** statements, concatenation operations, and conditional statements. Annotate this description from delays obtained in Part 5.
7. In a simulation testbench, instantiate the 16-bit Barrel Shifter of Part 5 and that of Part 6. Compare results, and record and explain discrepancies.

8. (Optional) Show Verilog description an 8-bit Barrel Shifter using only nMOS transistors only. You will get bonus points depending on how well and how deep you get into completing this part.