# UNIVERSITY OF TEHRAN
## Electrical and Computer Engineering Department
## Digital Logic Design, ECE 367, Fall 1394
## Computer Assignment 4
## Latches and flip-flops
## Week 12

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| **Name:** |
| **Date:** |

1. Generate a clocked SR-latch with active low S, R, and Clock inputs. Show this circuit in terms of an all-NAND circuit. Describe this circuit in Verilog using NAND primitives.
2. Annotate the circuit of Part 1 with gate delays that are based on switch level delays of 4 NS for the NMOS and 6 NS for the PMOS transistors.
3. Simulate the circuit of Part 2 to verify its operation. Apply simultaneous active high inputs (S and R) and see the loss of memory.
4. Use an inverter to convert the SR latch of Part 2 to a clocked D-latch. Simulate this circuit to verify its operation.
5. Form an 8-bit register by wiring eight latches of Part 4.
6. Form an 8-bit shift register using the above latch. From left to right (*i* to 0), the output of latch *i* connects to the D input of latch *i-1*. The D input of latch *i* is the *sin* (serial input) of the shift register.
7. Simulate the circuit of Part 6 and explain why or why-not this circuit works as expected.
8. Use two D-latches of Part 4 to build a master-slave D-type flip-flop.
9. Create a synchronous reset (*rs*) for the flip-flop of Part 4 such that when this input becomes 1, the output becomes 0 with the clock.
10. Build an 8-bit register using the flip-flop of Part 8 in a **generate** statement. Simulate this register and verify its clocking and resetting operations.
11. Write a testbench for the circuit of Part 10 and test its resetting, and shifting operations. Explain why this circuit works and that of Part 6 does not.
12. Write an 8-bit register using an **always** statement.
13. Redo the fractional divider of CA 3 to use a single barrel-shifter instead of two. Recall that the fractional part required its own barrel-shifter. Use registers of Part 8 for completing this part. Note that the integer part and the fractional part become available at different clock times.